RH850/U2B Group

R01AN6609EJ0100
Rev.1.00

Fast Ethernet Application Note

Summary

This application note summarizes the operation example of FAST Ethernet communication with Ethernet TSN (ETN).

The operation example described in this application note have been confirmed to operate, be sure to confirm the operation before using it.

Summary

1. Introduction

This application describes the using method of Ethernet TSN (ETN) and the creation example of the software.

1.1 Use Function

The following shows the hardware functions of RH850/U2Bx used in this application note.

- TSNES
- Port (P10, P11)

1.1.1 System Configuration

Figure 1-1 shows the connection diagram with PHY.

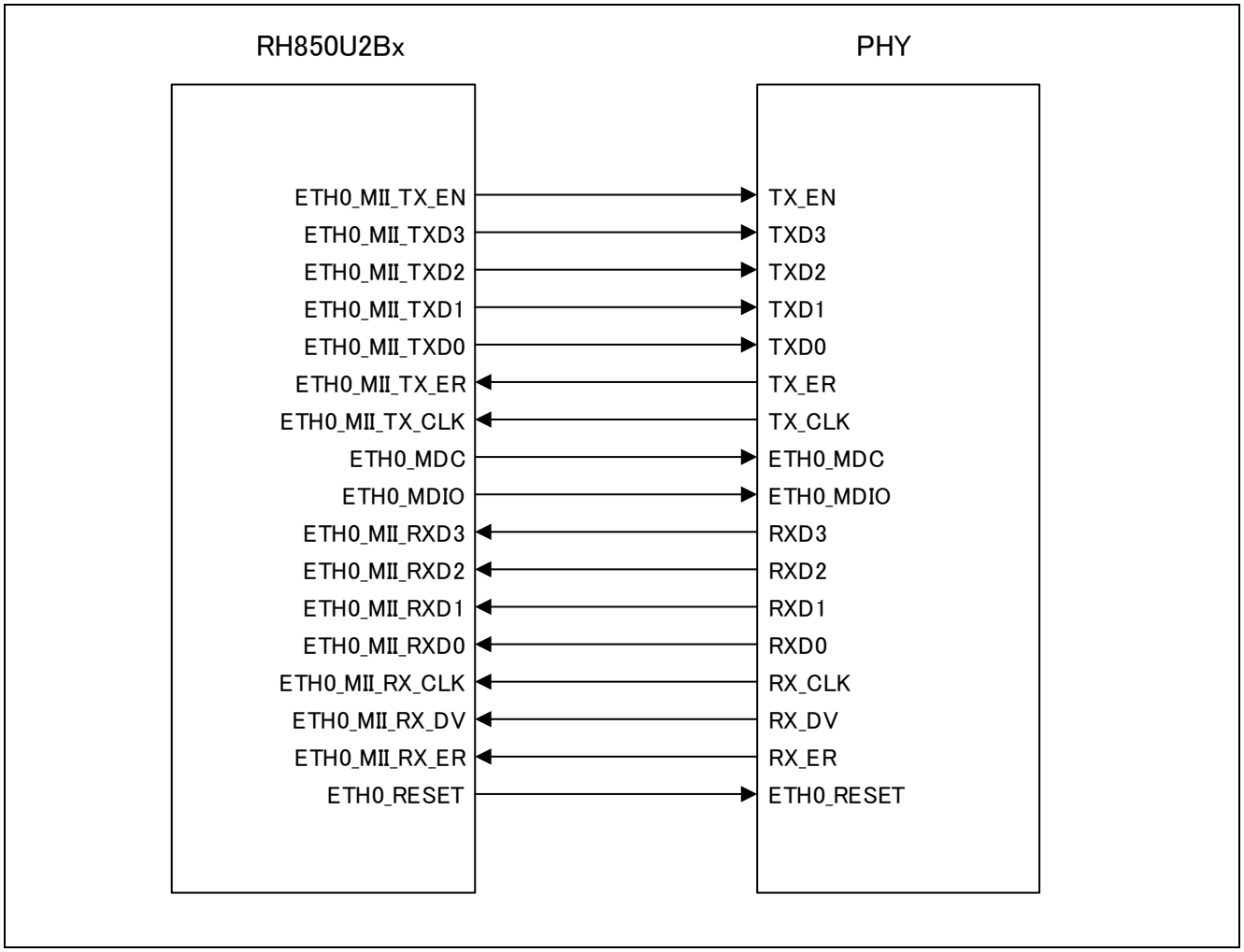

Figure 1-1 Connection Diagram of RH850/U2Bx and PHY

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1.2 TSN Overview

1.2.1 FAST Ethernet Communication

Figure 1-7 shows the block diagram of TSN module. In FAST Ethernet Communication, APB Slave I/F, AXI Master I/F, MHD (excluding TAS, CBS, and Counter), and RMAC System of TSNES.

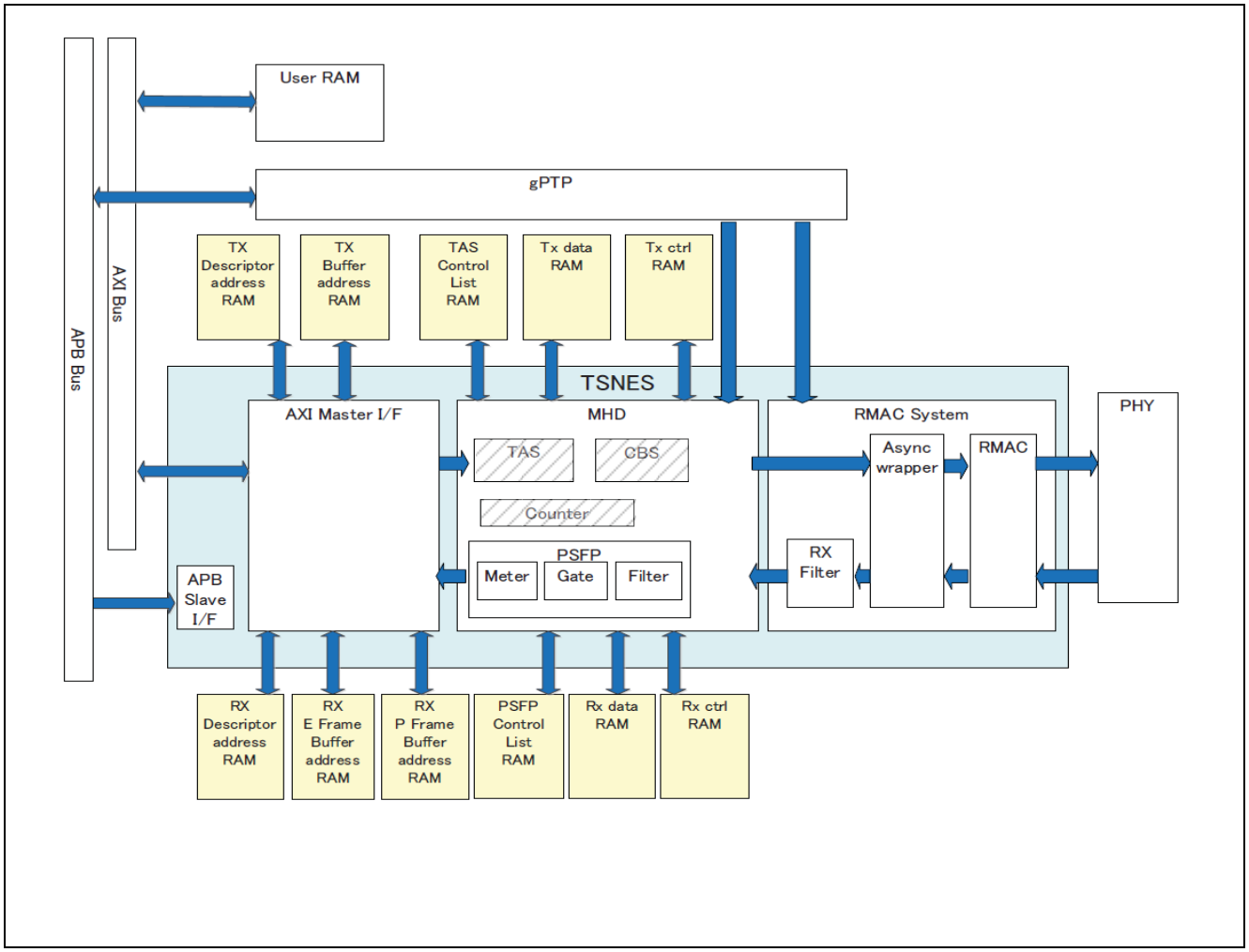

Figure 1-2 Block Diagram of TSN Module

1.2.2 Ethernet Frame Format

The frame format of Ethernet II/IEEE802.3 is supported.

1.2.3 Frame Format in Data Transmission/Reception

Figure1-3 shows the frame format of Ethernet II/IEEE802.3.

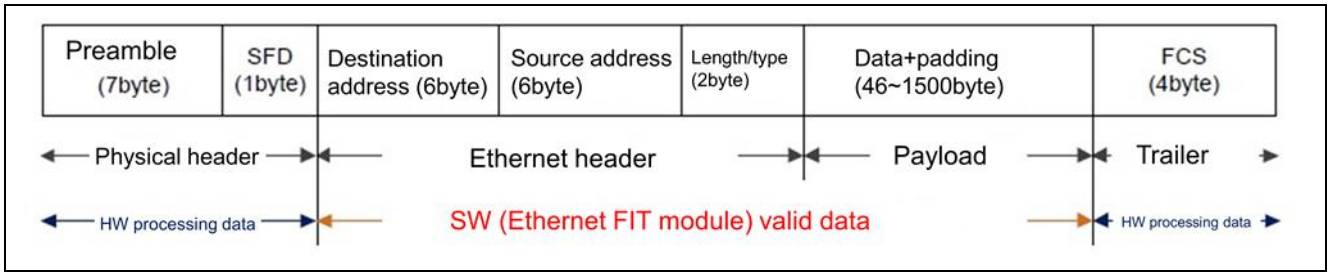

Figure1-3 Frame Format of Ethernet II /IEEE802.3

- Preamble and SFD is the signal for signing the start of Ethernet frame. Also, FCS stores the CRC value of the Ethernet frame calculated on the transmission side, and when the hardware receives the data, it also calculates the CRC value, and if it does not match, the Ethernet frame is discarded.
- When the hardware determines that the data is normal, the valid range of the received data is (destination address) + (source address) + (length / type) + (data).

1.2.4 Frame Format of PAUSE Frame

Figure1-4 shows the frame format of PAUSE frame.

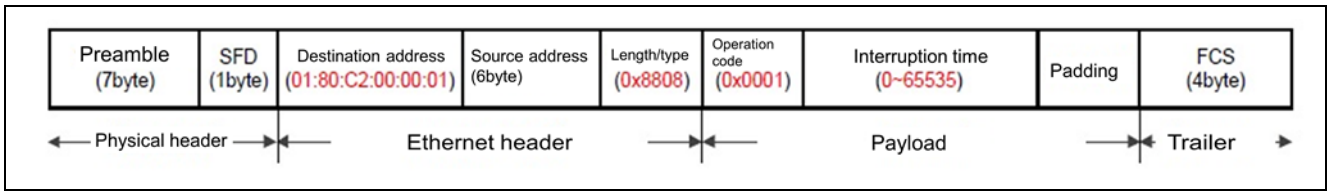

Figure1-4 Frame Format of PAUSE Frame

- "01: 80: C2: 00: 00: 01" (multicast address reserved for PAUSE frames) is specified as the destination address. In addition, "0x8808" is specified for the length / type, and "0x0001" is specified as the operation code at the beginning of the payload.
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1.2.5 Frame Format of Magic Packet

Figure1-5 shows the frame format of magic packet.

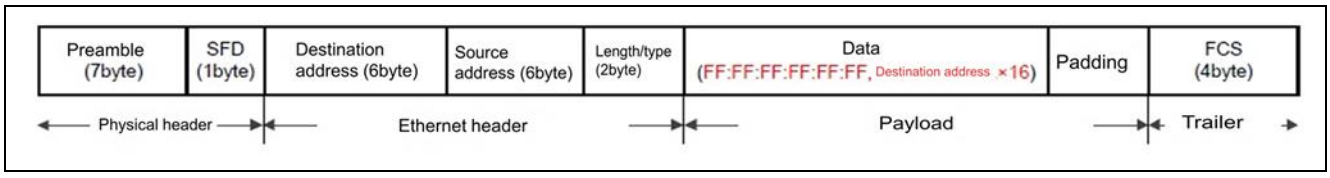

Figure1-5 Frame Format of Magic Packet

The magic packet inserts "the value obtained by repeating the destination address 16 times" after "FF: FF: FF: FF: FF: FF" somewhere in the Ethernet frame data.

1.2.6 TSNES Overview

In the data transmission, the frame data allocated to the user RAM is transmitted to xMII I/F via TX FIFO and outputted to PHY. In the data reception, the frame data inputted from PHY is received by xMII I/F, and transmitted to the user RAM via RX FIFO. Figure 1-6 shows the transmit/receive data processing.

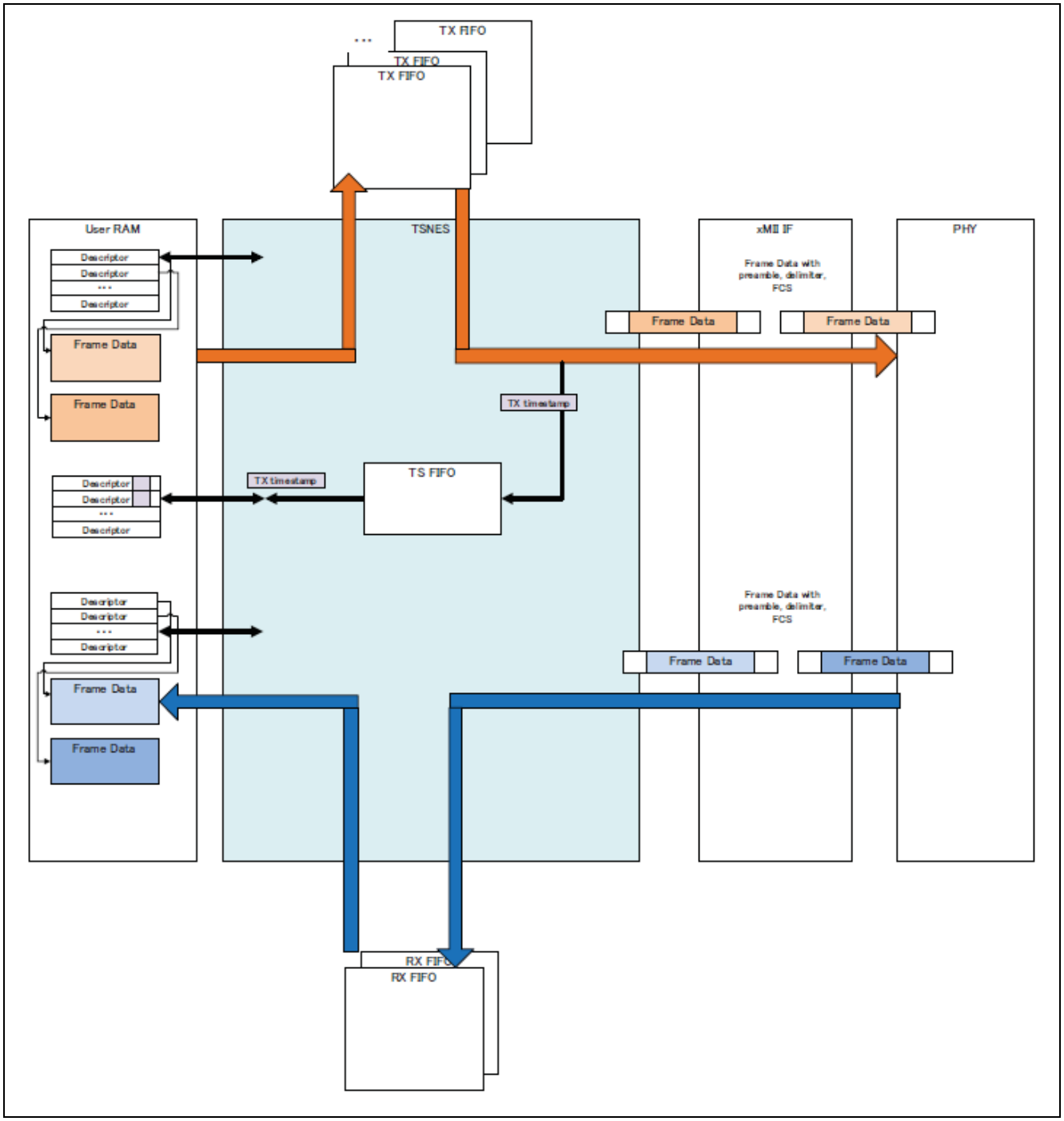

Figure 1-6 Transmit/Receive Data Processing

1.2.7 RMAC Overview

Figure 1-7 shows the block diagram of RMAC module. Perform the PHY management (reset and built-in register write/read) by using PHY MDIO interface function of RMAC.

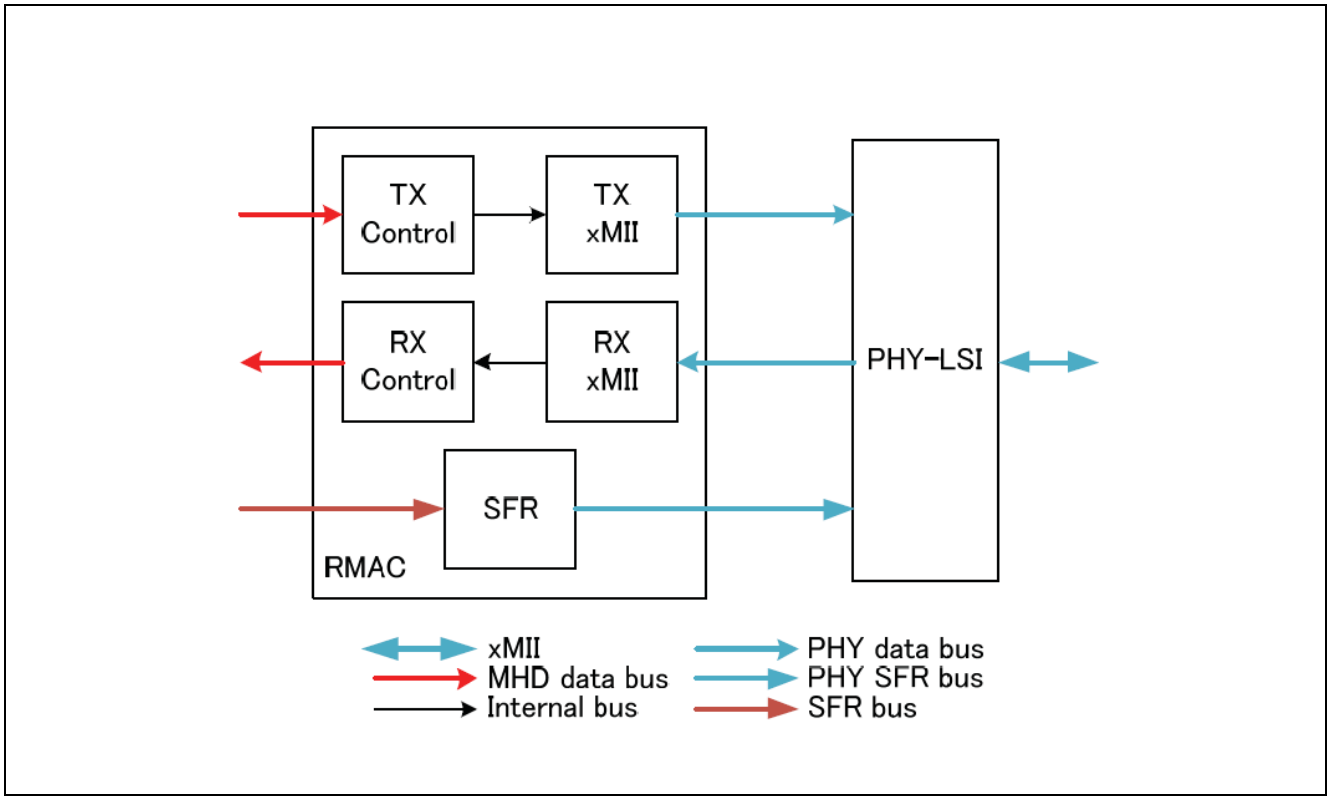

Figure 1-7 Block Diagram of RMAC

1.2.8 PHY Management and Linkup

This section describes PHY configuration by PHY MDIO interface function.

The following shows PHY specification in this operation example. エラー! 参照元が見つかりません。 shows the setting value of PHY register.

- PHY interface: MII
- Communication format: Full duplex
- Baud rate: 10/100base
- Management data lock: clk/66
- PHY address: 00000b

Table 1-1 PHY Register

Register Address	Setting Value	Function
0	0x8000 (in resetting)	PHY resetting
	0x3300 (in communicating)	100Mbps, Auto-negotiation, Restart, Full-duplex
4	0x0141	10Mbps full-duplex, 100Mbps full-duplex, IEEE 802.3

1.3 64 Bytes Transmission/Reception Operation Example (Loopback Mode)

This operation example describes the method that transmitting/receiving the 64 bytes normal frame by the loopback four times.

1.3.1 Communication Specification

Use channel: TSNES0

Frame: Normal frame

Number of data: 64 bytes

Transmission/Reception FIFO: 64 bytes

Number of descriptor: 4

1.3.2 System Configuration

Figure 1-8 shows the system configuration.

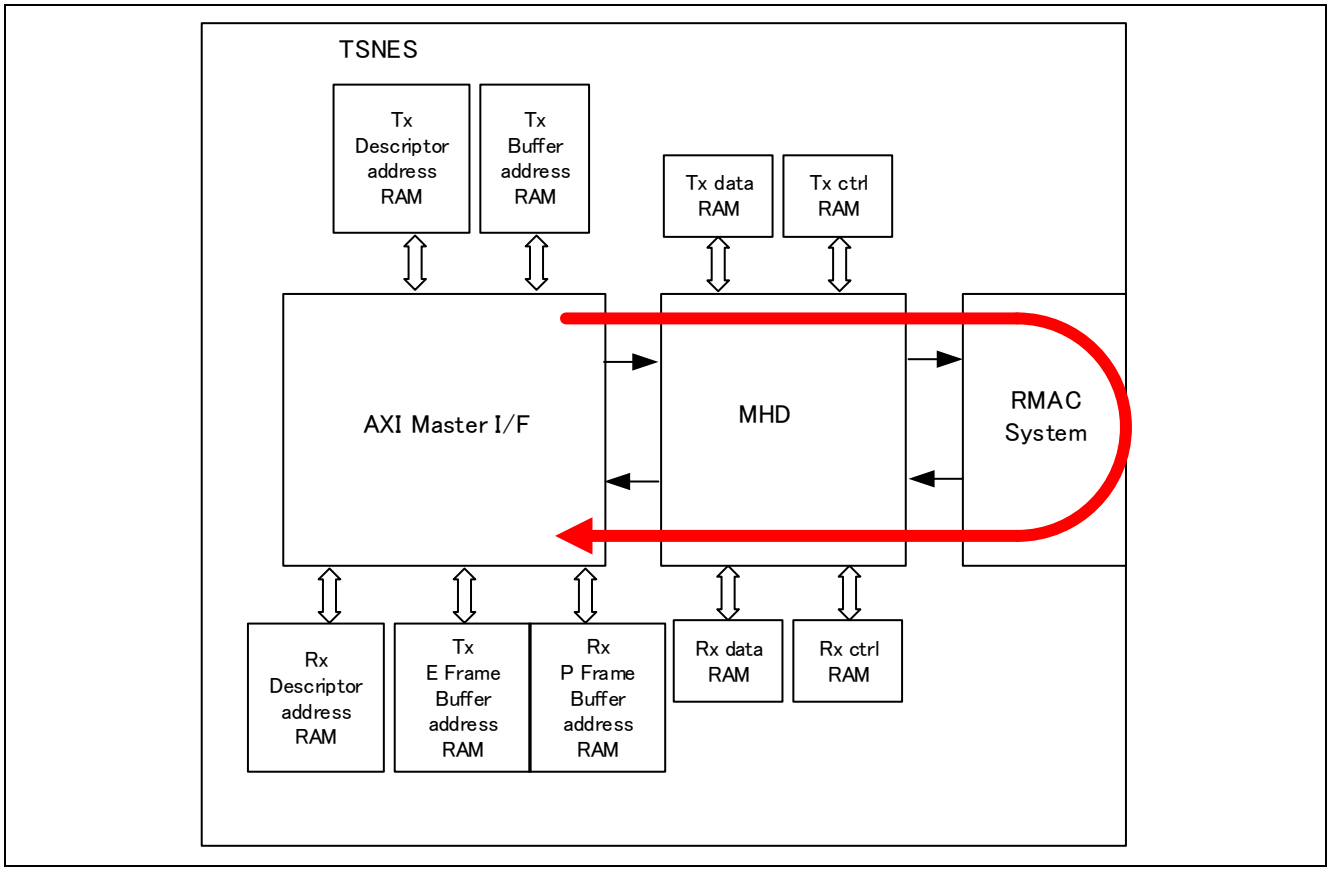

Figure 1-8 System Configuration

1.3.3 Descriptor Explanation

The storing destination of the transmit/receive (built-in RAM) data and the data delivering between FIFO in TSNES is performed by using the transfer data set to the descriptor. In this operation example, the format of the descriptor is the extended descriptor without timestamp (16 bytes). Table 1-2 shows the setting value of the descriptor.

Table 1-2 Setting Value of Descriptor

Classification	Number	Type	Data Storing Destination Address	Size
Reception	1	FEMPTY	0xFDC01000	64 bytes
	2	FEMPTY	0xFDC01040	64 bytes
	3	FEMPTY	0xFDC01080	64 bytes
	4	FEMPTY	0xFDC010C0	64 bytes
	5	EEMPTY	-	-
Transmission	1	FSINGLE	0xFDC01200	64 bytes
	2	FSINGLE	0xFDC01240	64 bytes
	3	FSINGLE	0xFDC01280	64 bytes
	4	FSINGLE	0xFDC012C0	64 bytes
	5	EEMPTY	-	-

1.3.4 MAC Address Filter

In the data reception, the filter processing of MAC address is performed. In this operation example, the unicast reception is enabled.

1.3.5 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 1-3 Module List

Module Name	Rabel Name	Function
Main routine	main_pe0	Performs each setting and the application startup.
Port initialization routine	port_init	Performs the initial setting of the port.
Ether communication start	eth_open	Performs the processing of Ether communication start.
Ether communication end	eth_close	Performs the processing of Ether communication end.
AXIBMI initial setting	axibmi	Performs the initial setting of AXIBMI.
RMACA initial setting	rmaca	Performs the initial setting of RMACA.
Descriptor initialization	init_ethram	Performs the initialization of the descriptor.
Data transmission	eth_write	Perform the transmit data setting and the transmit start processing.
Data reception	eth_read	Perform the reading of receive data and the storing processing.
Transmit data setting	write_ethram	Sets the transmit data to the local RAM.
Receive data setting	read_ethram	Sets the receive data to the local RAM.
PHY initialization	phy_init	Resets PHY.
Auto-negotiation	phy_start_autonegotiate	Performs communication format and baud rate setting and auto-negotiation enable/execution.
PHY register read	phy_read	Specify the address of PHY register, and read the built-in register.
PHY register write	phy_write	Specify the address of PHY register, and write the built-in register.

- Register Setting

The following shows the register setting of each function in this operation example.

Table 1-4 TSNES Register Setting

Register Name	Setting Value	Function
TSNES0OCR	0x00000000	Operation mode control: Disable mode
	0x00000001	Operation mode control: Config Mode
	0x00000002	Operation mode control: Operation mode
TSNES0TFS0	0x00020002	TX data FIFO size q+1: 256 bytes
		TX data FIFO size q: 256 bytes
TSNES0TGC1	0x00000101	Transmit mode: Store & Forward mode
		Transmit threshold value: 256 bytes
TSNES0RDFCR	0x00410041	pMAC receive FIFO waring level: 257 bytes
		eMAC receive FIFO warning level: 257 bytes
TSNES0SWR	0x00000001	Software reset

Table 1-5 AXIBMI Register Setting

Register Name	Setting Value	Function
AXIBMI0RR	0x00000003	TX descriptor address table RAM reset: Enable
		RX descriptor address table RAM reset: Enable
AXIBMI0AXIWC	0x00004411	Write RX P frame number: 4
		Write RX E frame number: 4
		Write TX P frame number: 1
		Write TX E frame number: 1
AXIBMI0AXIRC	0x00001122	Write RX P frame number: 1
		Write RX E frame number: 1
		Write TX P frame number: 2
		Write TX E frame number: 2
AXIBMI0TATLS0	0x00000002	Extended descriptor: Enable
		Normal mode: Transmit synchronization mode
AXIBMI0TATLS1	le0.txcurrent	TX descriptor address: le0.txcurrent
AXIBMI0TATLR	0x00000001	TX descriptor address learning: Enable
AXIBMI0RATLS0	0x00000028	RX descriptor wait: Enable
		RX frame size error: AXIBMI stop
		Extended descriptor: Enable
		Normal mode: Receive synchronization mode
AXIBMI0RATLS1	le0.rxcurrent	RX descriptor address: le0.rxcurrent
AXIBMI0RATLR	0x00000001	RX descriptor address learning: Enable
AXIBMI0TRCR0	0x00000001	Transmit start request: Enable
AXIBMI0TDIS0	0xFFFFFFFF	Transmit completion flag: Clear
AXIBMI0RDIS0	0xFFFFFFFF	Receive completion flag: Clear

Table 1-6 RMACA Register Setting

Register Name	Setting Value	Function
RMACA0MRMAC1	MAC_ADDR[1] MAC_ADDR[2]	MAC address low order: MAC_ADDR[1]、MAC_ADDR[2]
RMACA0MRMAC0	MAC_ADDR[0]	MAC address high order: MAC_ADDR[0]
RMACA0MRAFC	0x00010001	P frame unicast: Enable
		e frame unicast: Enable
RMACA0MPIC	0x77200004	Capture time correction: 7
		Hold time correction: 7
		Prinble prohibitation: Disable
		Clock collection: 0x20
		Link speed: 100Mbps
		PHY I/F：MII
RMACA0MLBC	0x00000001	Loopback mode: Enable
RMACA0MCC	0x00000000	TX enable: Disable
		RX enable: Disable

RMACA00MPSM (In reading)	0x0000XX00	PHY register write: 0
		PHY register address: XX(reg_addr)
		PHY device address: 0
		Access direction: Read
		Management: Disable
	↓	↓
	0x0000XX01	PHY register write: 0
		PHY register address: XX(reg_addr)
		PHY device address: 0
		Access direction: Read
		Management: Enable
RMACA00MPSM (In writing)	0xYY00XX02	PHY register write: YY(data)
		PHY register address: XX(reg_addr)
		PHY device address: 0
		Access direction: Write
		Management: Disable
	↓	↓
	0xYY00XX03	PHY register write: YY(data)
		PHY register address: XX(reg_addr) PHY device address: 0
		Access direction: Write
		Management: Enable

Table 1-7 Port Register Setting

Register Name	Setting Value	Function
PCR10_0	0x00000051	P10_0 : ETH0_MII_RXD3
PCR10_1	0x00000058	P10_1 : ETH0_MII_RX_CLK
PCR10_2	0x01000046	P10_2 : ETH0_MDC
PCR10_3	0x00000056	P10_3 : ETH0_MII_RXD2
PCR10_4	0x01000077	P10_4 : ETH0_MDIO
PCR10_5	0x00000051	P10_5 : ETH0_PHY_INT
PCR10_8	0x00001000	P10_8 : ETH0_RESET
PCR11_0	0x02000042	P11_0 : ETH0_MII_TX_EN
PCR11_1	0x02000043	P11_1 : ETH0_MII_TXD3
PCR11_2	0x00000053	P11_2 : ETH0_MII_RXD1
PCR11_3	0x00000053	P11_3 : ETH0_MII_RXD0
PCR11_4	0x00000054	P11_4 : ETH0_MII_TX_CLK
PCR11_5	0x02000042	P11_5 : ETH0_MII_TXD2
PCR11_7	0x00000054	P11_7 : ETH0_MII_RX_DV
PCR11_8	0x02000042	P11_8 : ETH0_MII_TXD0
PCR11_9	0x02000042	P11_9 : ETH0_MII_TXD1
PCR11_10	0x02000042	P11_10 : ETH0_MII_TX_ER

1.3.6 Flowchart

The following shows the flowchart in this operation example.

1.3.7 Main

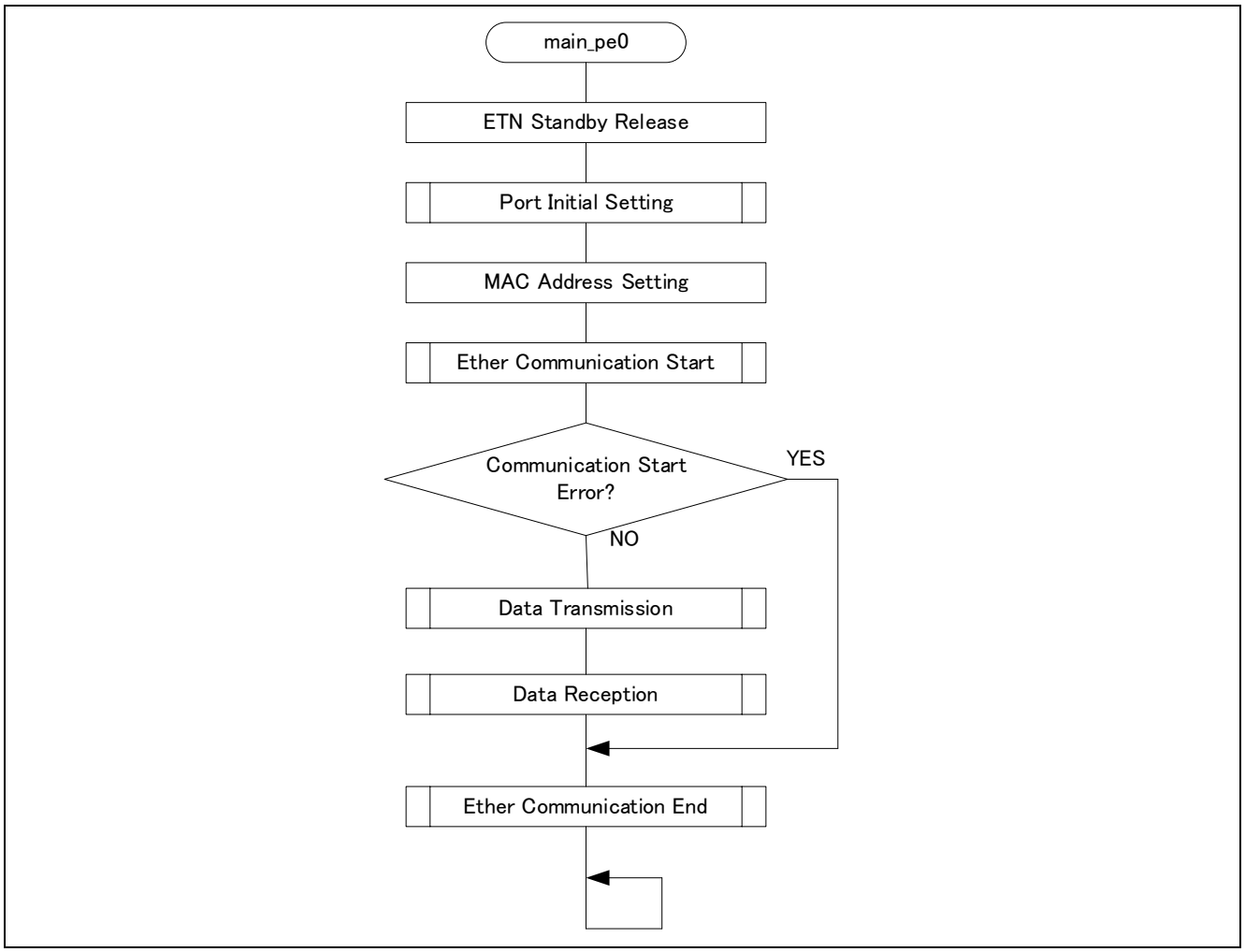

Figure 1-9 Main Module Flowchart

1.3.8 Ether Communication

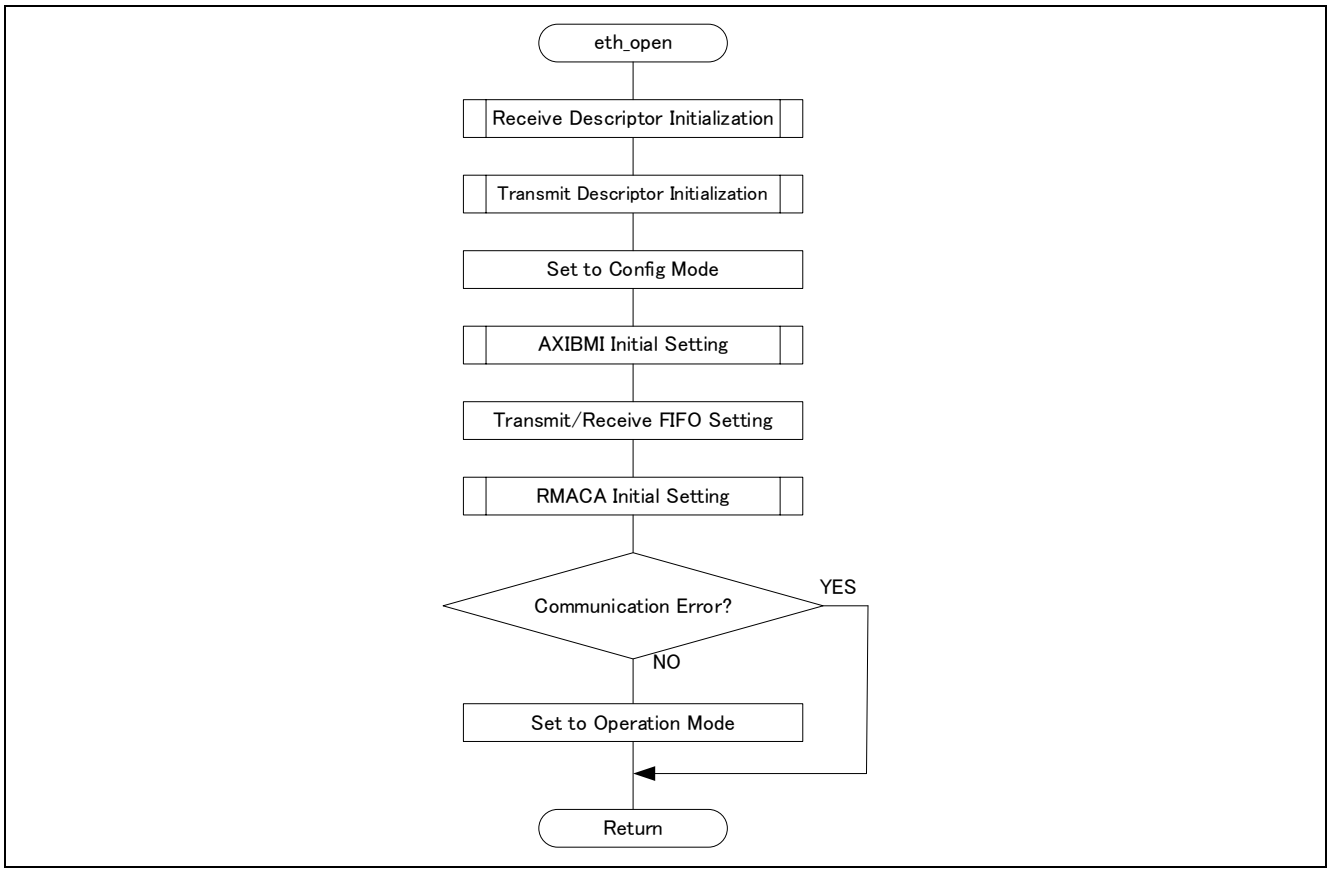

Figure 1-10 Ether Communication Start Module Flowchart

1.3.9 Ether Communication End

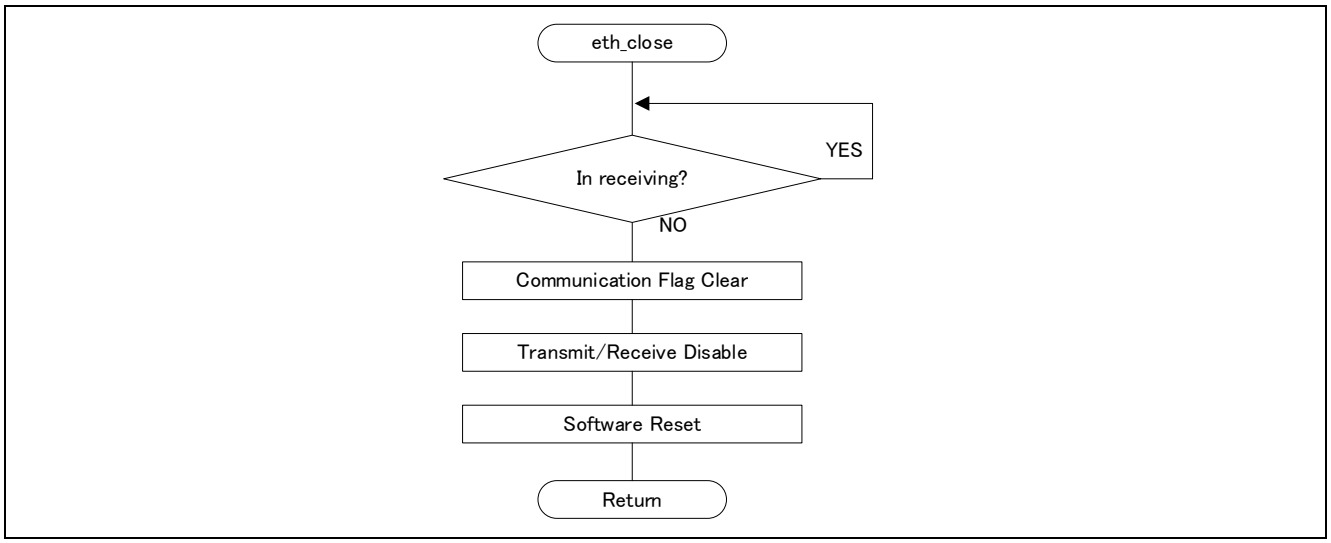

Figure 1-11 Ether Communication End Module Flowchart

1.3.10 AXIBMI Initial Setting

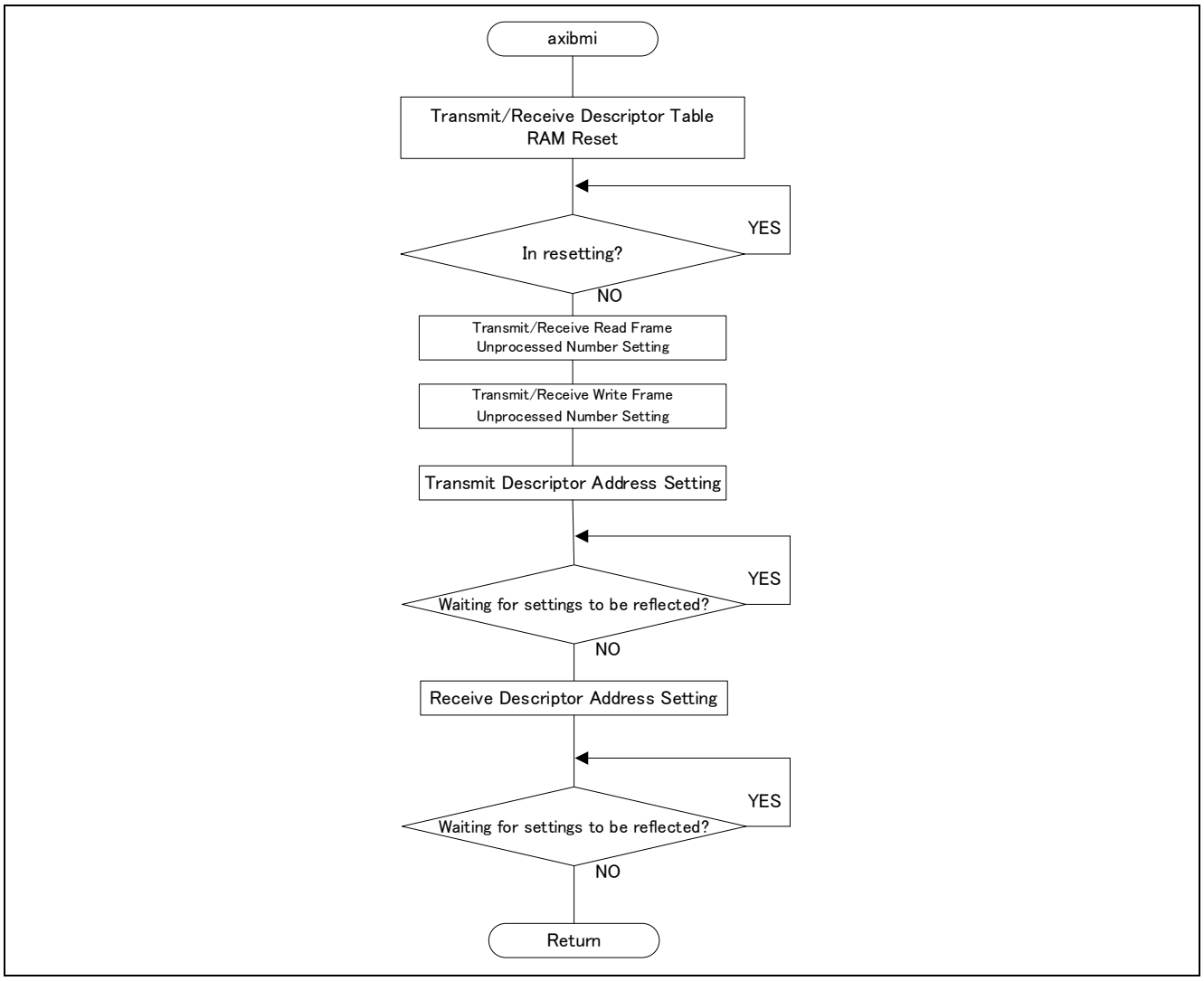

Figure 1-12 AXIBMI Initial Setting Module Flowchart

1.3.11 RMACA Initial Setting

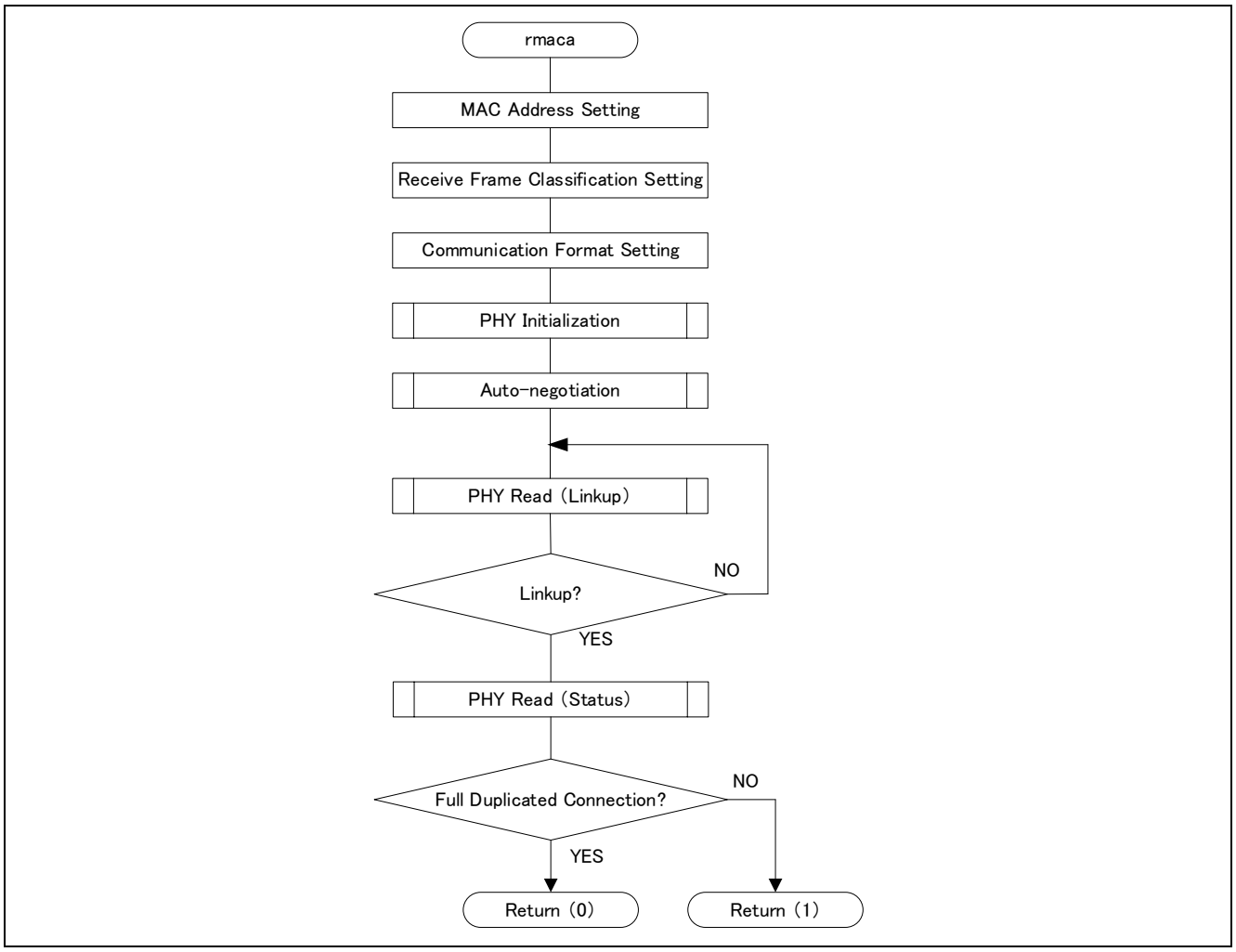

Figure 1-13 RMACA Initial Setting Module Flowchart

1.3.12 Transmit/Receive Descriptor Initialization

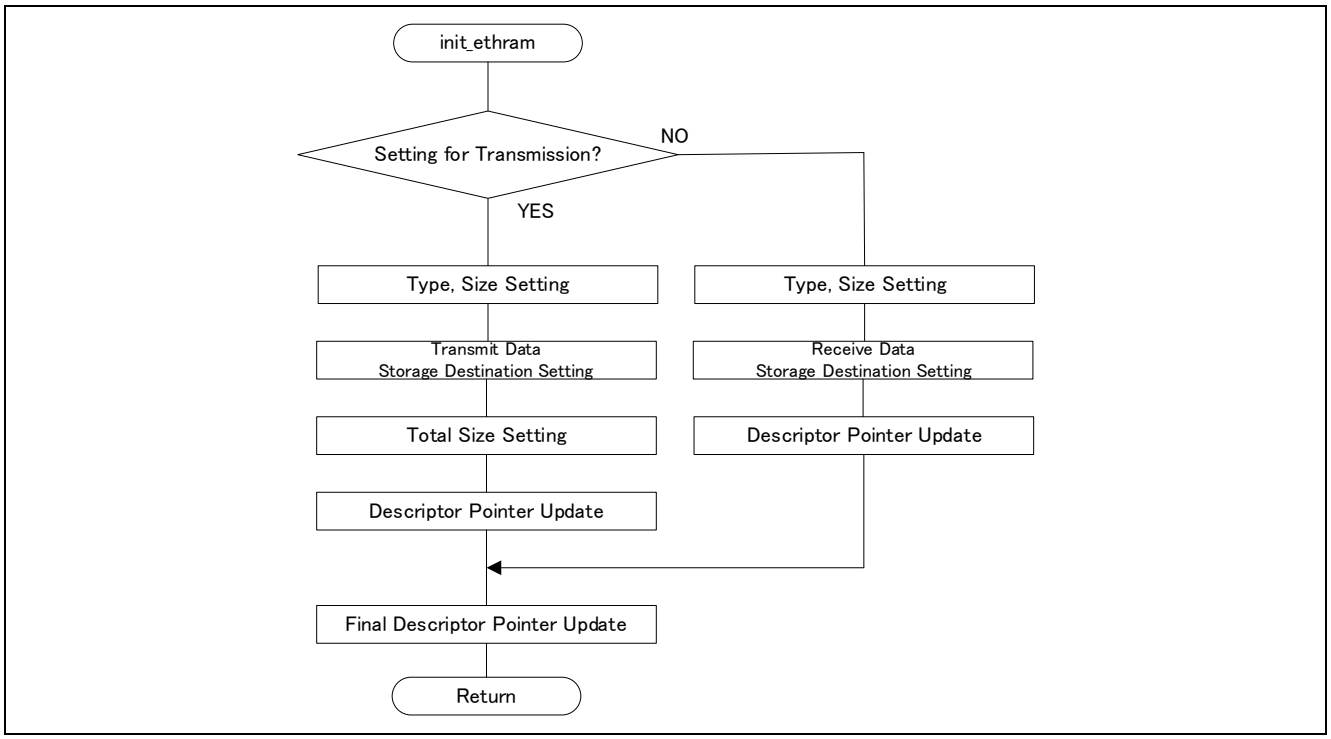

Figure 1-14 Transmit/Receive Descriptor Initialization Module Flowchart

1.3.13 Data Transmission

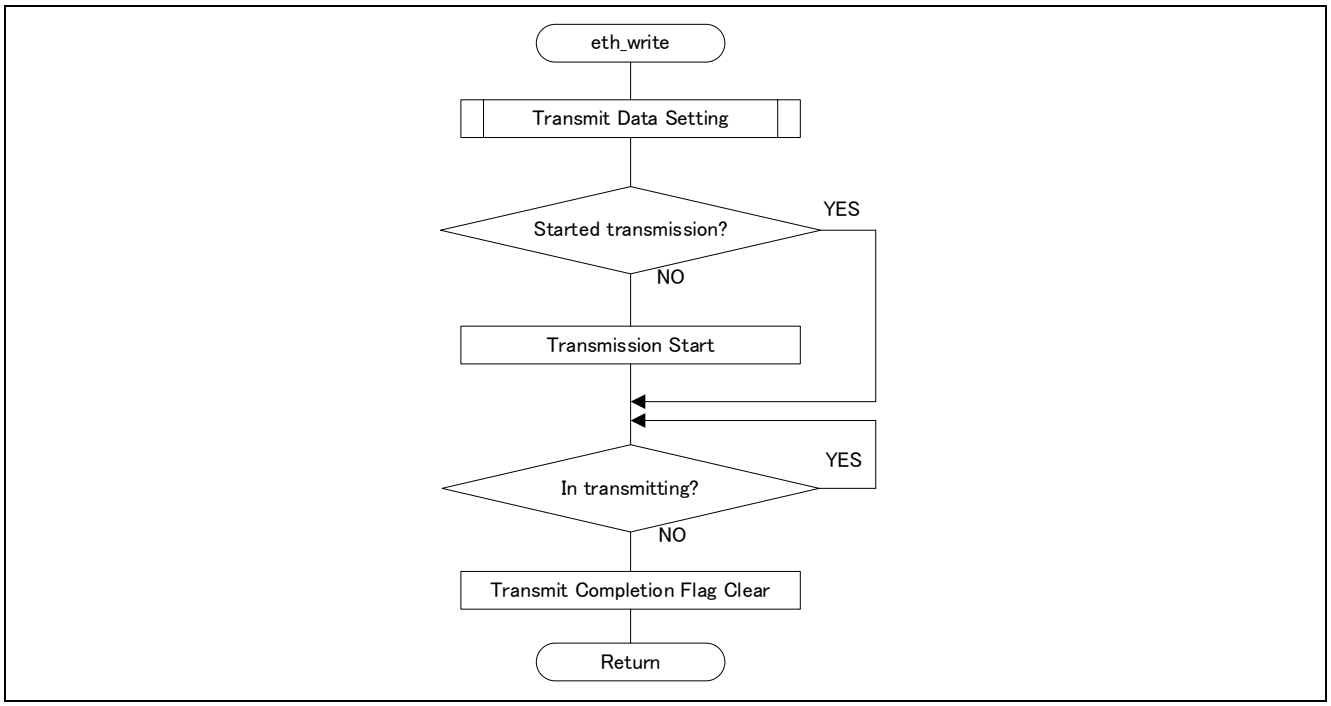

Figure 1-15 Data Transmission Module Flowchart

1.3.14 Data Reception

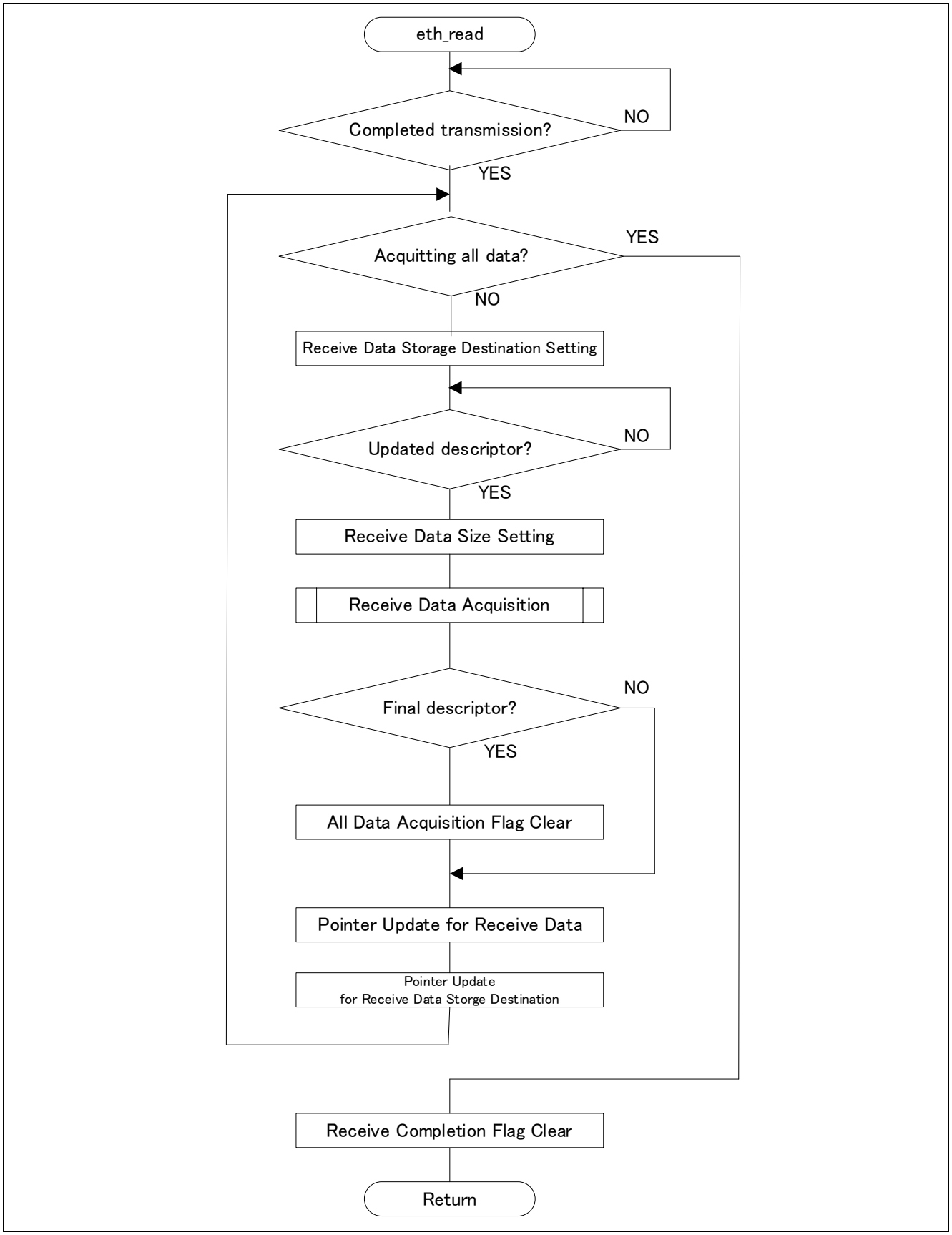

Figure 1-16 Data Receive Module Flowchart

1.3.15 Transmission Data Setting

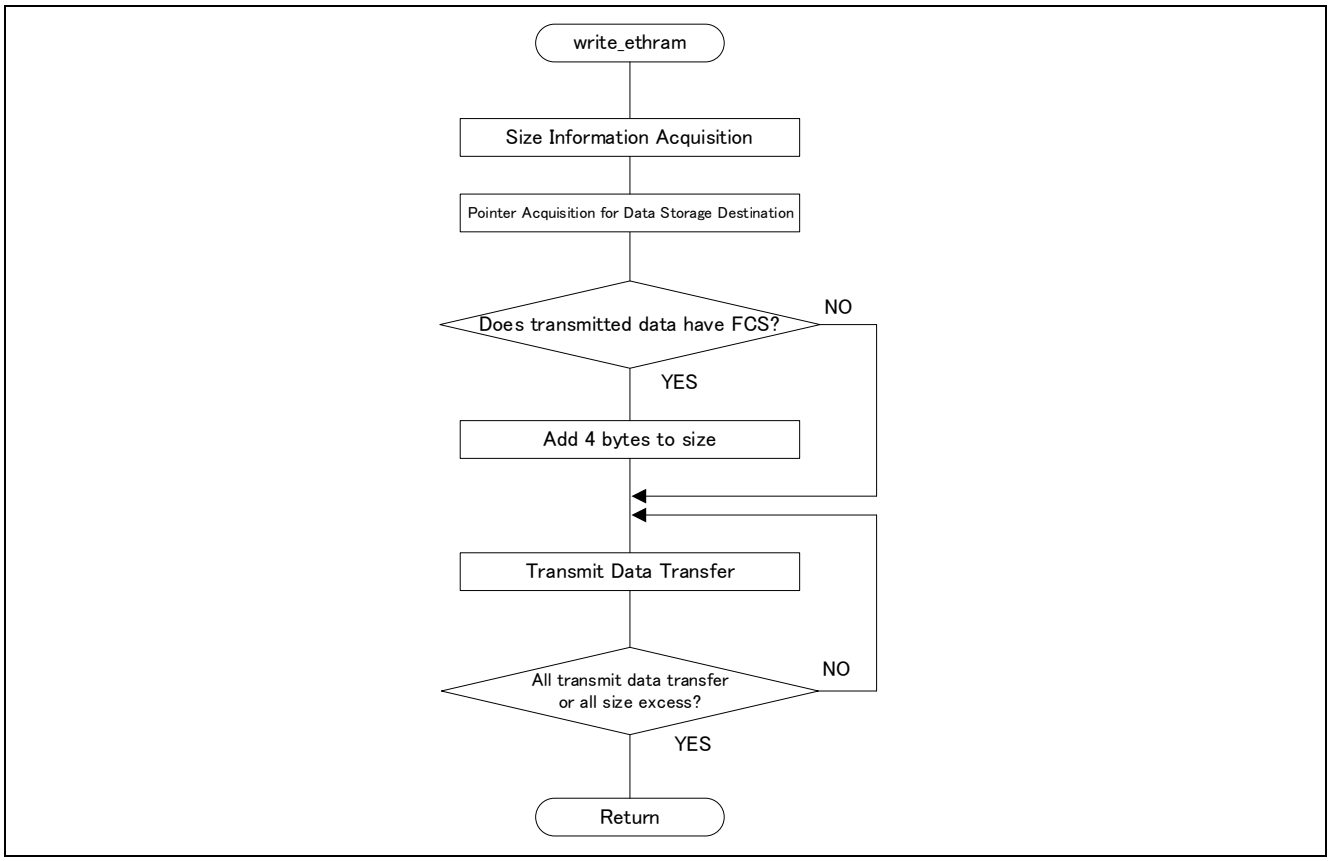

Figure 1-17 Transmit Data Setting Module Flowchart

1.3.16 Receive Data Acquisition

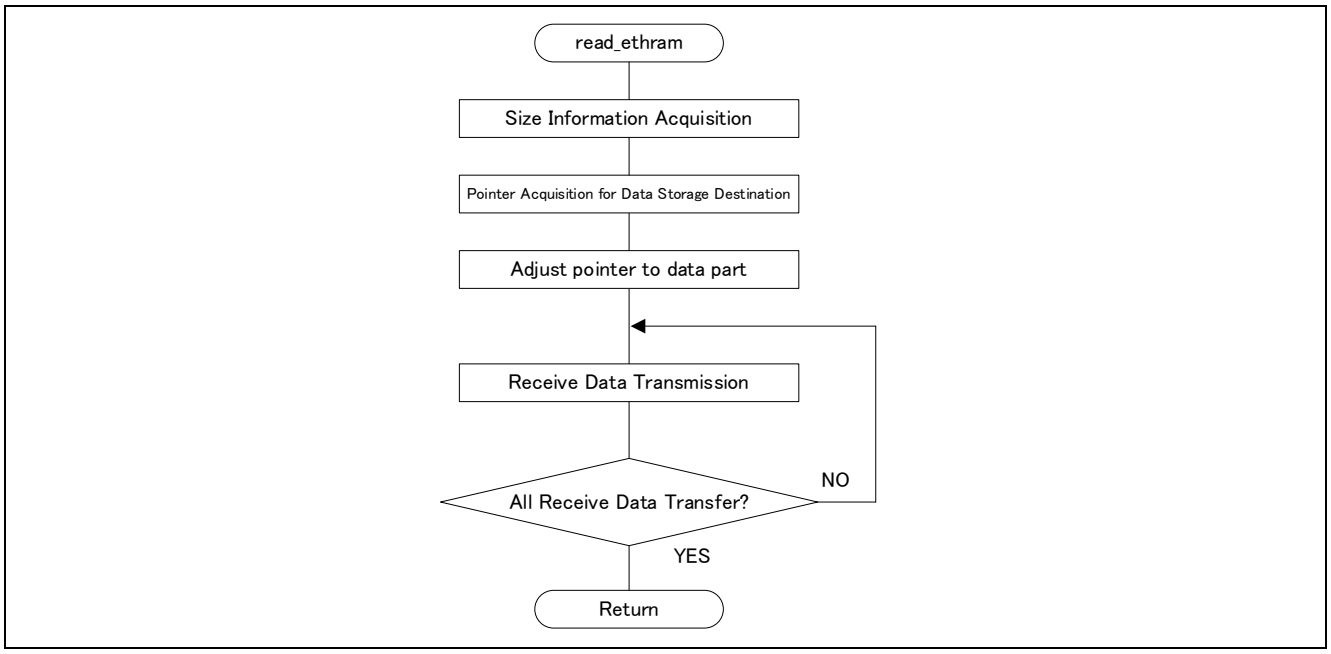

Figure 1-18 Receive Data Acquisition Module Flowchart

1.3.17 PHY Initialization

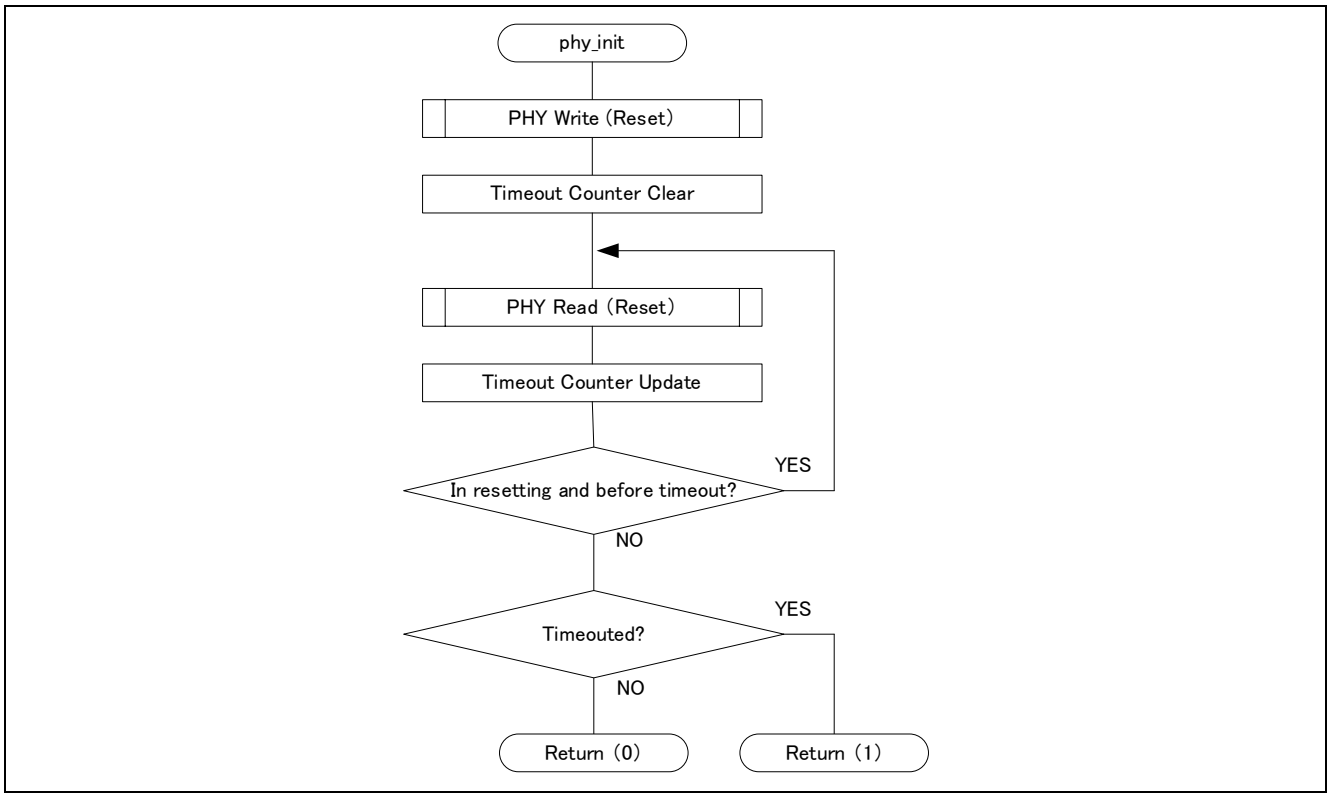

Figure 1-19 PHY Initialization Module Flowchart

1.3.18 Auto-negotiation

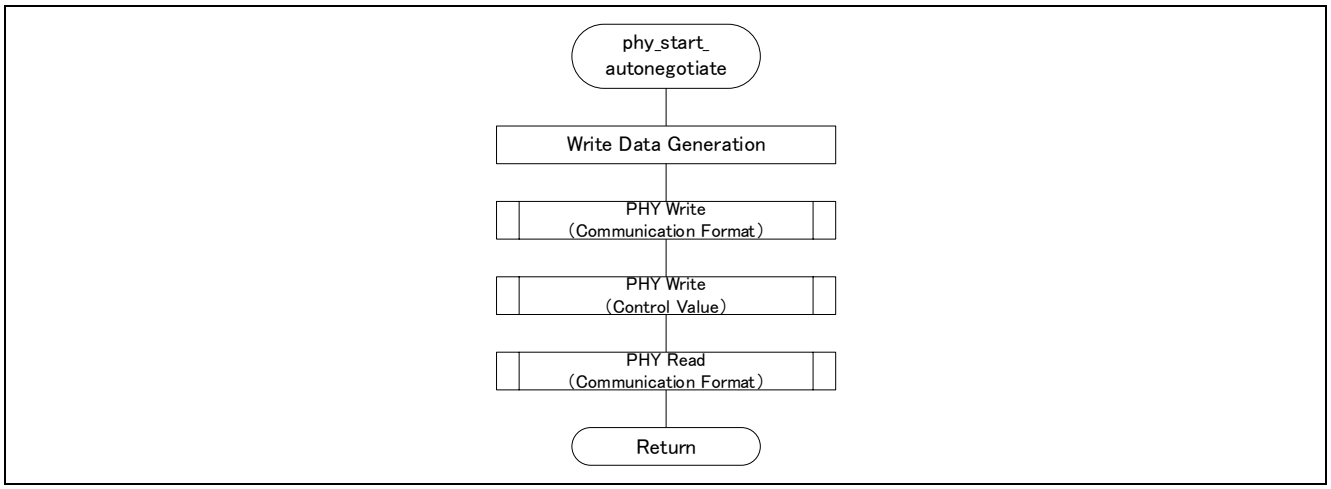

Figure 1-20 Auto-negotiation Module Flow Chart

1.3.19 PHY Write

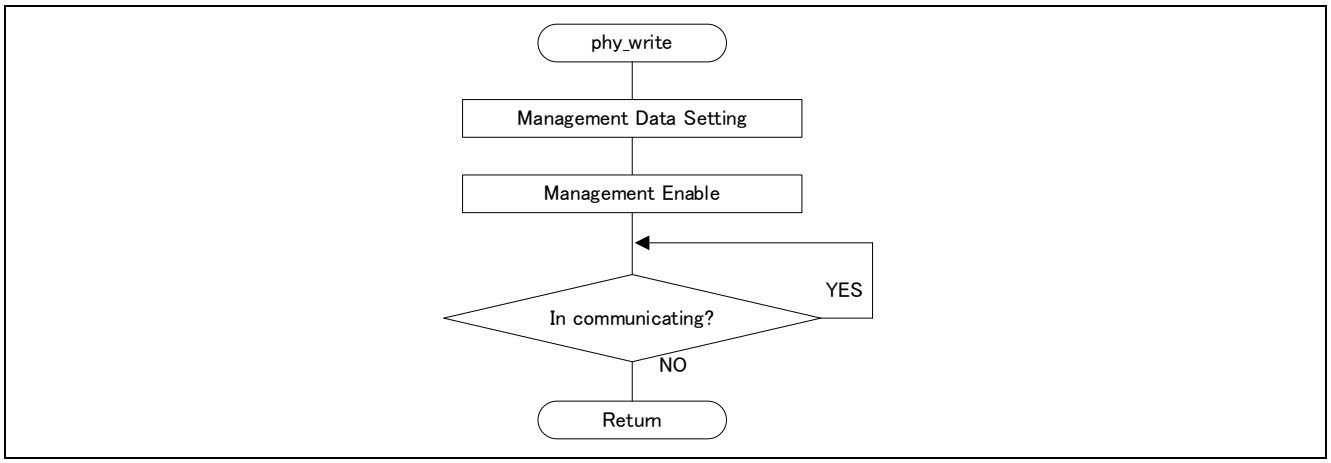

Figure 1-21 PHY Write Module Flowchart

1.3.20 PHY Read

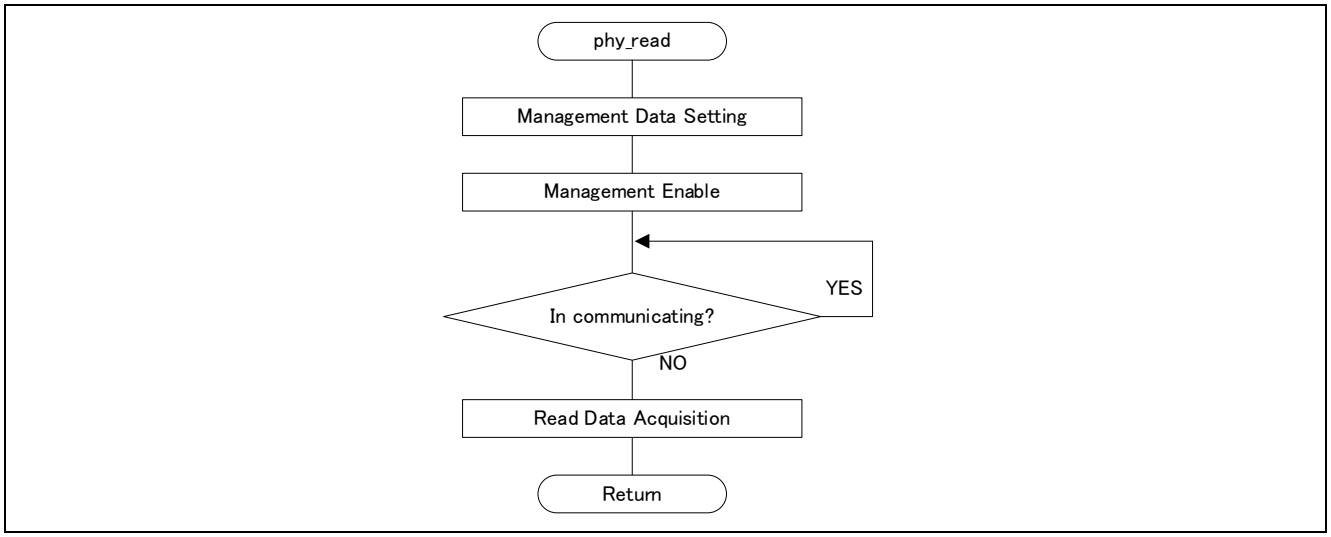

Figure 1-22 PHY Read Module Flowchart

1.4 256 Bytes Transmit/Receive Operation

In this operation example, the transmission/reception of 256 bytes normal frame and the reception of the magic packet are performed.

1.4.1 Communication Specification

Use Channel: TSNES0

Frame: Normal frame, Magic packet frame

Number of data: 256 bytes

Transmit/Receive FIFO: 256 bytes

Descriptor: 4

1.4.2 System Configuration

Figure 1-23 shows the system configuration.

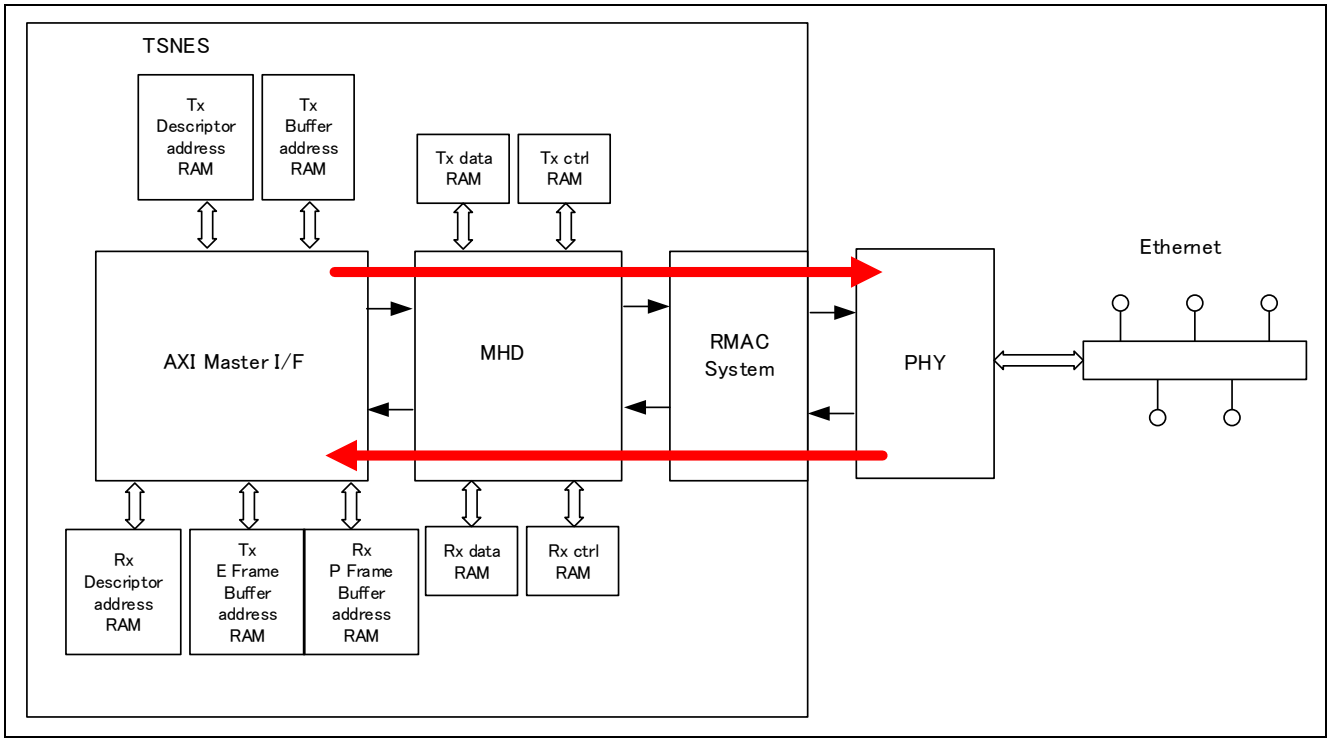

Figure 1-23 System Configuration

1.4.3 Descriptor Explanation

The storing destination of the transmit/receive (built-in RAM) data and the data delivering between FIFO in TSNES is performed by using the transfer data set to the descriptor. In this operation example, the format of the descriptor is the extended descriptor without timestamp (16 bytes). 256 bytes of data is divided into 64 bytes and transmitted/received. Figure 1-8 shows the setting value of the descriptor.

Table 1-8 Setting Value of Descriptor

Classification	Number	Type	Data Storing Destination Address	Size
Reception	1	FEMPTY	0xFDC01000	64 バイト
	2	FEMPTY	0xFDC01040	64 バイト
	3	FEMPTY	0xFDC01080	64 バイト
	4	FEMPTY	0xFDC010C0	64 バイト
	5	EEMPTY	-	-
Transmission	1	FSTART	0xFDC01200	64 バイト
	2	FMID	0xFDC01240	64 バイト
	3	FMID	0xFDC01280	64 バイト
	4	FEND	0xFDC012C0	64 バイト
	5	EEMPTY	-	-

1.4.4 Magic Packet Reception

In this operation example, the reception of the magic packet is performed. The data of received magic packet is following.

“0xFF,0xFF,0xFF,0xFF,0xFF,0xFF”, ”0x74,0x90,0x50,0x00,0x79,0x03” ×16

1.4.5 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 1-9 Module List

Module Name	Rabel Name	Function
Main routine	main_pe0	Performs each setting and the application startup.
Port initialization routine	port_init	Performs the initial setting of the port.
Ether communication start	eth_open	Performs the processing of Ether communication start.
Ether communication end	eth_close	Performs the processing of Ether communication end.
AXIBMI initial setting	axibmi	Performs the initial setting of AXIBMI.
RMACA initial setting	rmaca	Performs the initial setting of RMACA.
Descriptor initialization	init_ethram	Performs the initialization of the descriptor.
Data transmission	eth_write	Perform the transmit data setting and the transmit start processing.
Data reception	eth_read	Perform the reading of receive data and the storing processing.
Transmit data setting	write_ethram	Sets the transmit data to the local RAM.
Receive data setting	read_ethram	Sets the receive data to the local RAM.
PHY initialization	phy_init	Resets PHY.
Auto-negotiation	phy_start_autonegotiate	Performs communication format and baud rate setting and auto-negotiation enable/execution.
PHY register read	phy_read	Specify the address of PHY register, and read the built-in register.
PHY register write	phy_write	Specify the address of PHY register, and write the built-in register.

- Register Setting

The following shows the register setting of each function in this operation example.

Table 1-10 TSNES Register Setting

Register Name	Setting Value	Function
TSNES0OCR	0x00000000	Operation mode control: Disable mode
	0x00000001	Operation mode control: Config Mode
	0x00000002	Operation mode control: Operation mode
TSNES0TFS0	0x00020002	TX data FIFO size q+1: 256 bytes
		TX data FIFO size q: 256 bytes
TSNES0TGC1	0x00000101	Transmit mode: Store & Forward mode
		Transmit threshold value: 256 bytes
TSNES0RDFCR	0x00410041	pMAC receive FIFO waring level: 257 bytes
		eMAC receive FIFO warning level: 257 bytes
TSNES0SWR	0x00000001	Software reset

Table 1-11 AXIBMI Register Setting

Register Name	Setting Value	Function
AXIBMI0RR	0x00000003	TX descriptor address table RAM reset: Enable
		RX descriptor address table RAM reset: Enable
AXIBMI0AXIWC	0x00004411	Write RX P frame number: 4
		Write RX E frame number: 4
		Write TX P frame number: 1
		Write TX E frame number: 1
AXIBMI0AXIRC	0x00001122	Write RX P frame number: 1
		Write RX E frame number: 1
		Write TX P frame number: 2
		Write TX E frame number: 2
AXIBMI0TATLS0	0x00000002	Extended descriptor: Enable
		Normal mode: Transmit synchronization mode
AXIBMI0TATLS1	le0.txcurrent	TX descriptor address: le0.txcurrent
AXIBMI0TATLR	0x00000001	TX descriptor address learning: Enable
AXIBMI0RATLS0	0x00000028	RX descriptor wait: Enable
		RX frame size error: AXIBMI stop
		Extended descriptor: Enable
		Normal mode: Transmit synchronization mode
AXIBMI0RATLS1	le0.rxcurrent	RX descriptor address: le0.rxcurrent
AXIBMI0RATLR	0x00000001	RX descriptor address learning: Enable
AXIBMI0TRCR0	0x00000001	Transmit start request: Enable
AXIBMI0TDIS0	0xFFFFFFFF	Transmit completion flag: Clear
AXIBMI0RDIS0	0xFFFFFFFF	Receive completion flag: Clear

Table 1-12 RMACA Register Setting

Register Name	Setting Value	Function
RMACA0MRMAC1	MAC_ADDR[1]、MAC_ADDR[2]	MAC address low order: MAC_ADDR[1], MAC_ADDR[2]
RMACA0MRMAC0	MAC_ADDR[0]	MAC address high order: MAC_ADDR[0]
RMACA0MRGC	0x0000000F	Magic packet detection: Enable
		Pause frame receive frame: Enable
		Pause frame receive control: Enable
		Receive CRC passing: Passing
RMACA0MPIC	0x77200004	Capture time correction: 7
		Hold time correction: 7
		Prinble prohibitation: Disable
		Clock collection: 0x20
		Link speed: 100Mbps
		PHY I/F：MII
RMACA0MCC	0x00000000	Loopback mode: Enable
		TX enable: Disable

RMACA00MPSM (In reading)	0x0000XX00	PHY register write: 0
		PHY register address: XX(reg_addr)
		PHY device address: 0
		Access direction: Read
		Management: Disable
	↓	↓
	0x0000XX01	PHY register write: 0
		PHY register address: XX(reg_addr)
		PHY device address: 0
		Access direction: Read
		Management: Enable
RMACA00MPSM (In writing)	0xYY00XX02	PHY register write: YY(data)
		PHY register address: XX(reg_addr)
		PHY device address: 0
		Access direction: Write
		Management: Disable
	↓	↓
	0xYY00XX03	PHY register write: YY(data)
		PHY register address: XX(reg_addr) PHY device address: 0
		Access direction: Write
		Management: Enable

Table 1-13 Port Register Setting

Register Name	Setting Value	Function
PCR10_0	0x00000051	P10_0 : ETH0_MII_RXD3
PCR10_1	0x00000058	P10_1 : ETH0_MII_RX_CLK
PCR10_2	0x01000046	P10_2 : ETH0_MDC
PCR10_3	0x00000056	P10_3 : ETH0_MII_RXD2
PCR10_4	0x01000077	P10_4 : ETH0_MDIO
PCR10_5	0x00000051	P10_5 : ETH0_PHY_INT
PCR10_8	0x00001000	P10_8 : ETH0_RESET
PCR11_0	0x02000042	P11_0 : ETH0_MII_TX_EN
PCR11_1	0x02000043	P11_1 : ETH0_MII_TXD3
PCR11_2	0x00000053	P11_2 : ETH0_MII_RXD1
PCR11_3	0x00000053	P11_3 : ETH0_MII_RXD0
PCR11_4	0x00000054	P11_4 : ETH0_MII_TX_CLK
PCR11_5	0x02000042	P11_5 : ETH0_MII_TXD2
PCR11_7	0x00000054	P11_7 : ETH0_MII_RX_DV
PCR11_8	0x02000042	P11_8 : ETH0_MII_TXD0
PCR11_9	0x02000042	P11_9 : ETH0_MII_TXD1
PCR11_10	0x02000042	P11_10 : ETH0_MII_TX_ER

1.4.6 Flowchart

The following shows the flowchart in this operation example.

1.4.7 Main

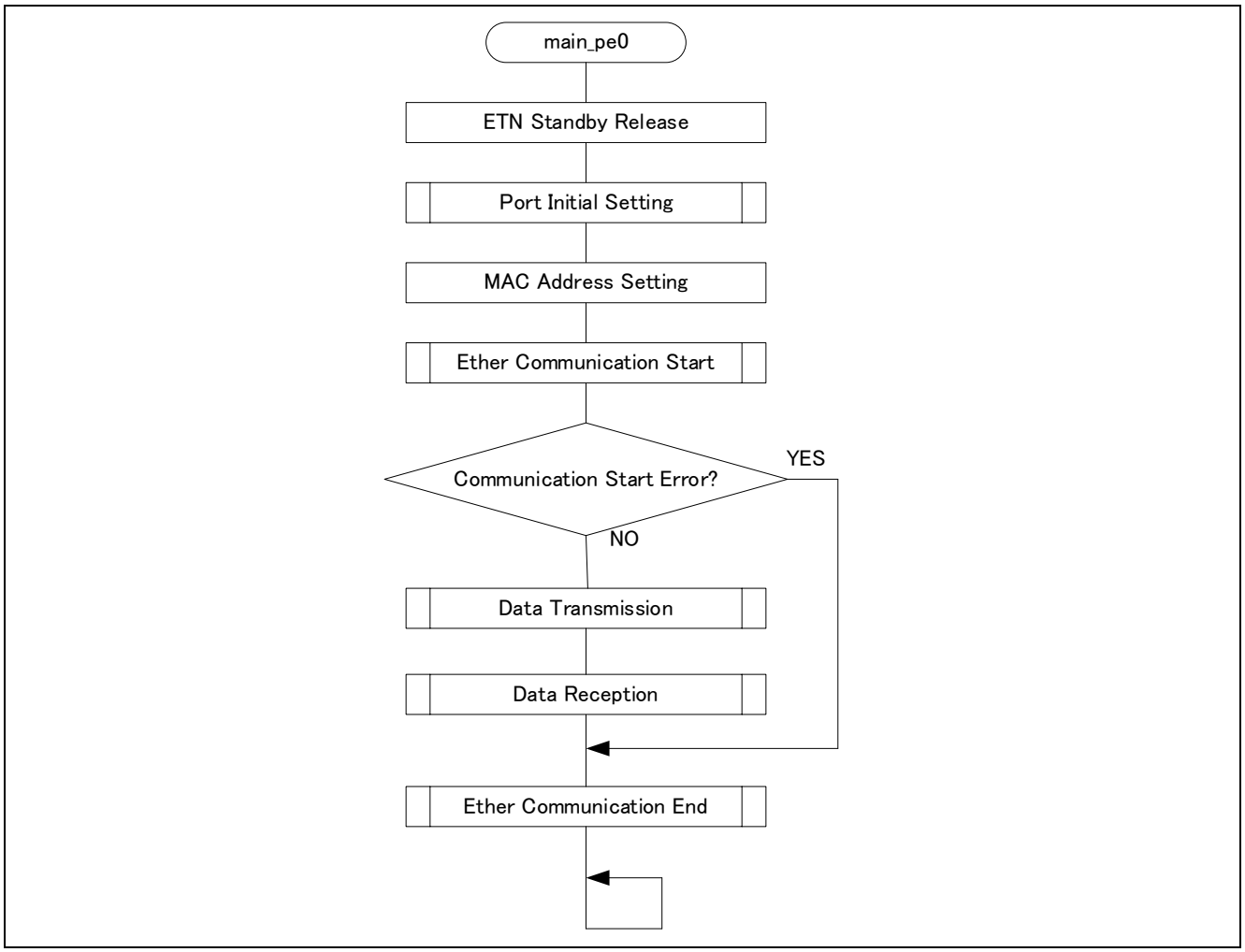

Figure 1-24 Main Module Flowchart

1.4.8 Ether Communication Start

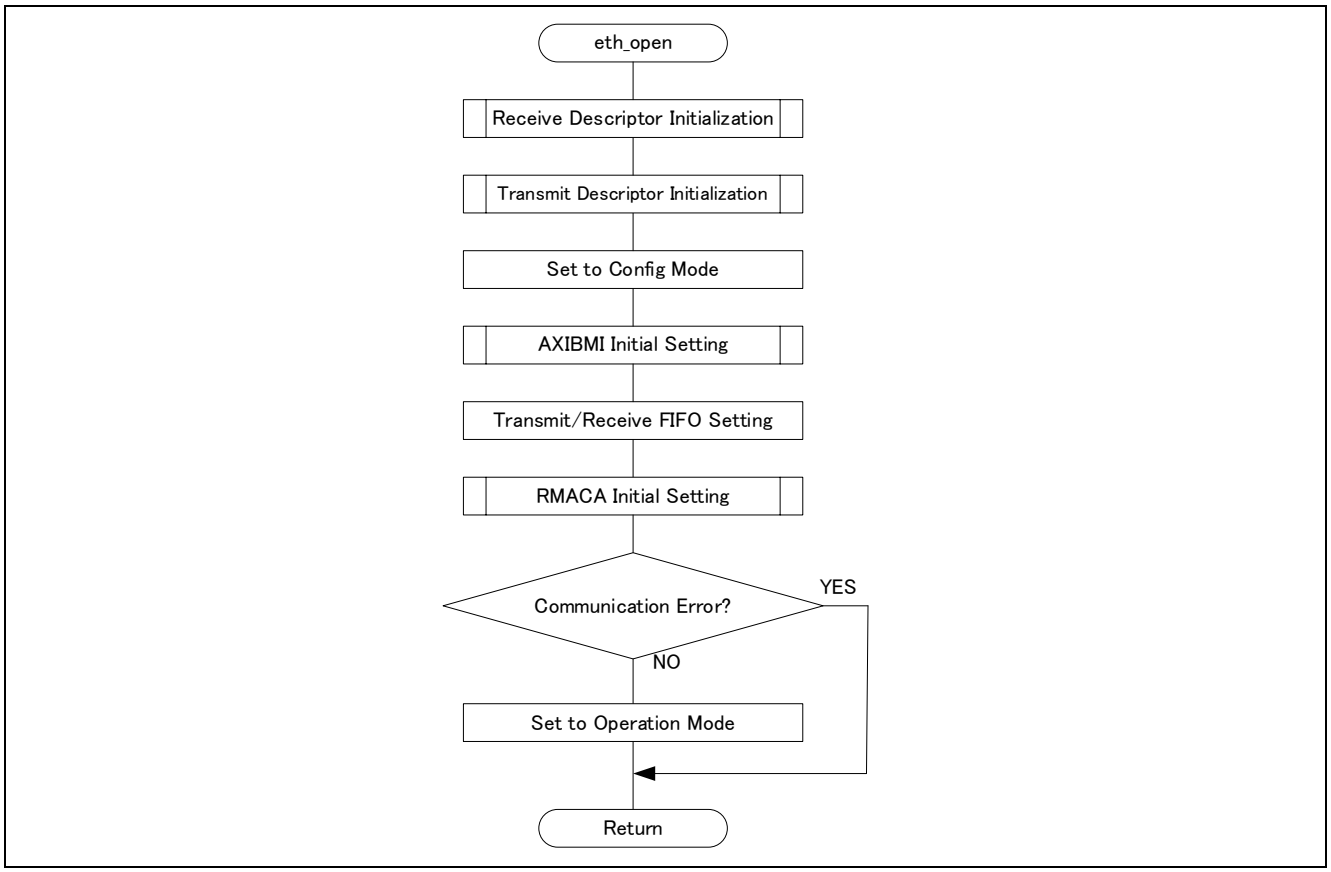

Figure 1-25 Ether Communication Start Module Flowchart

1.4.9 Ether Communication End

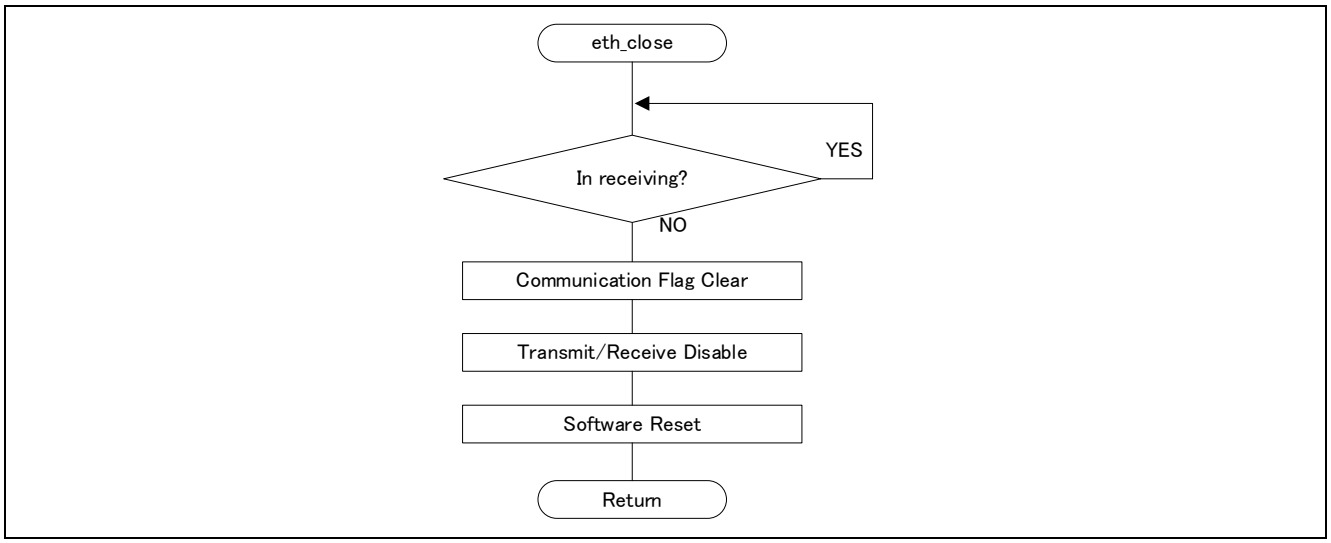

Figure 1-26 Ether Communication End Module Flowchart

1.4.10 AXIBMI Initial Setting

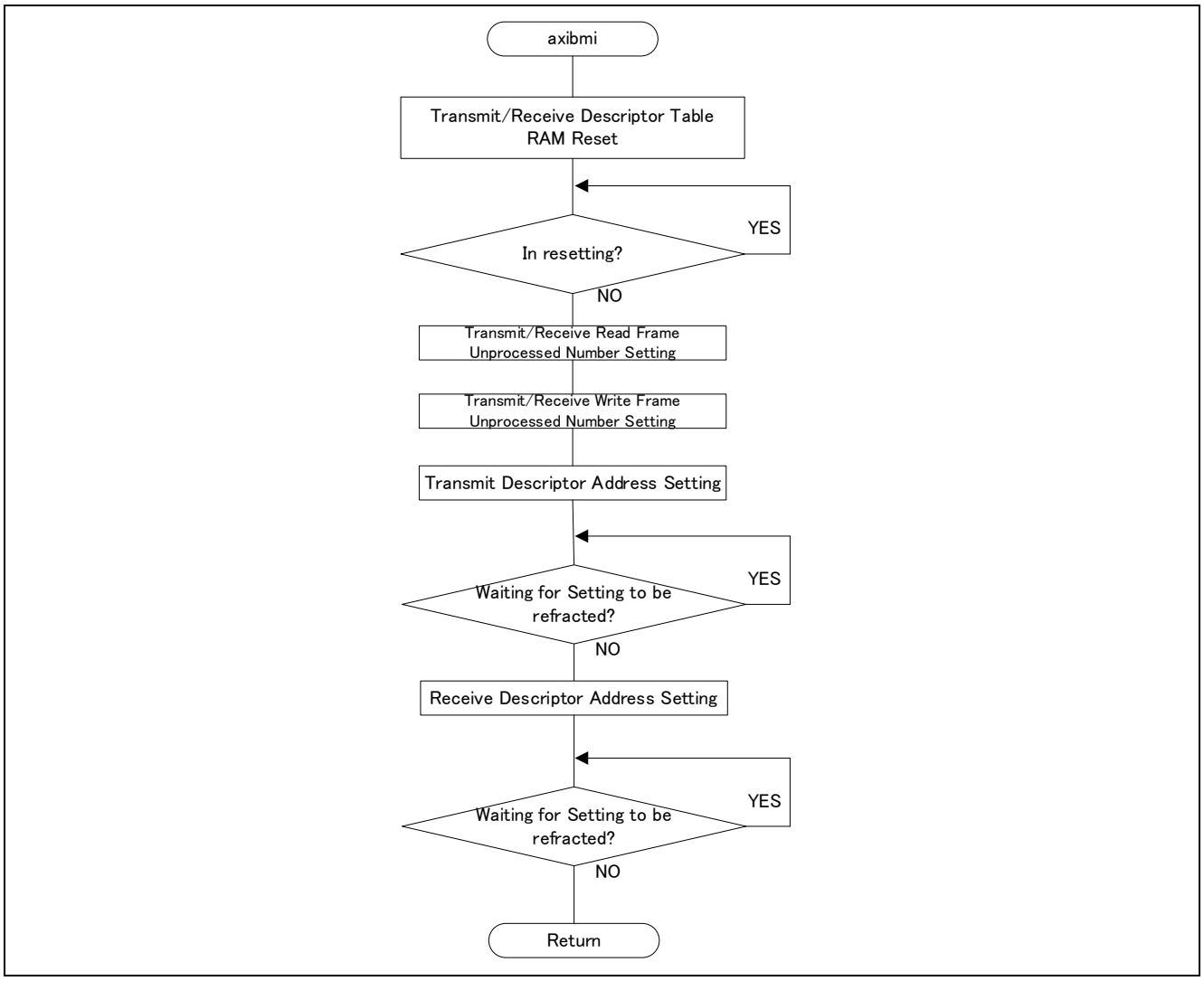

Figure 1-27 AXIBMI Initial Setting Module Flowchart

1.4.11 RMACA Initial Setting

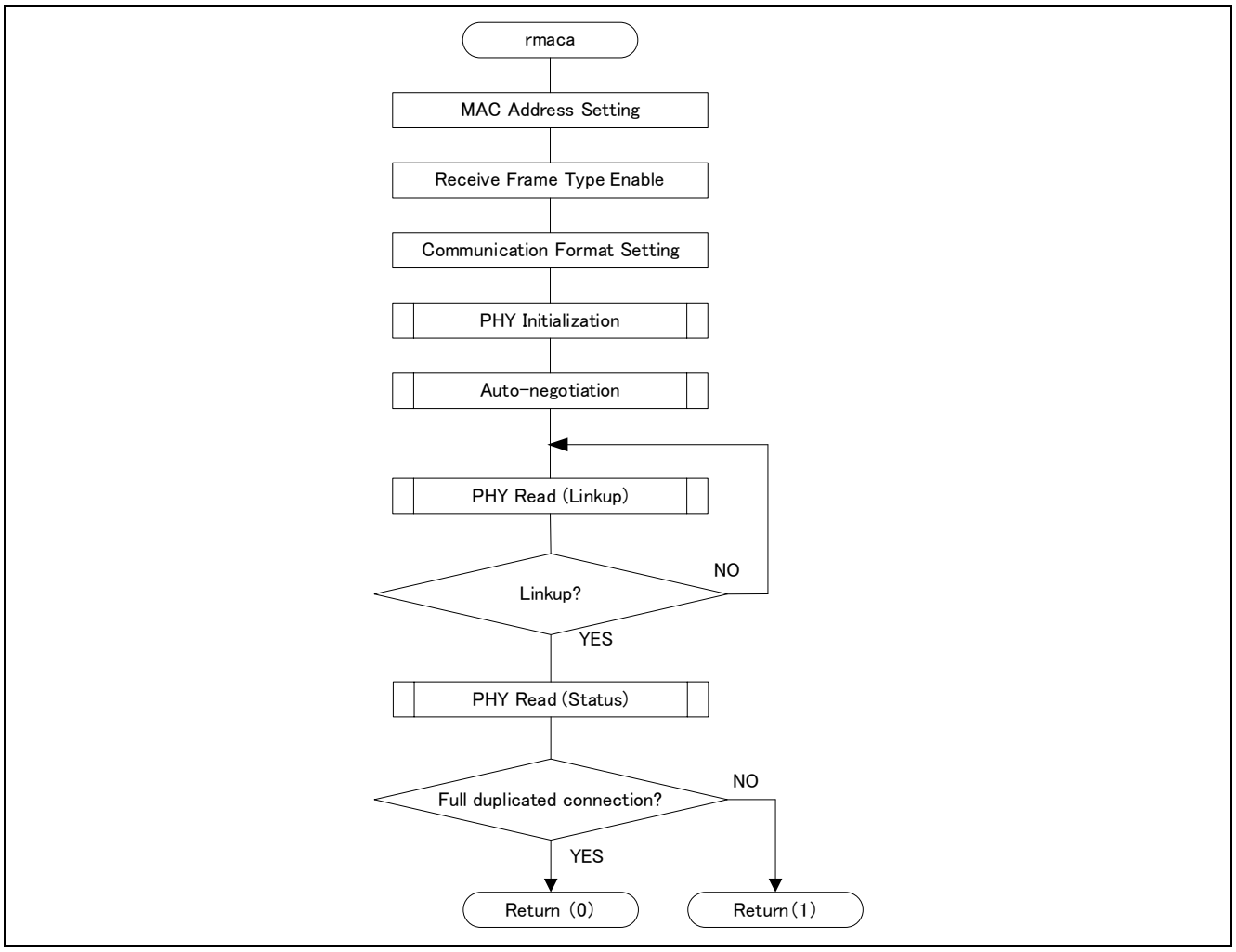

Figure 1-28 RMACA Initial Setting Module Flowchart

1.4.12 Transmit/Receive Descriptor Initialization

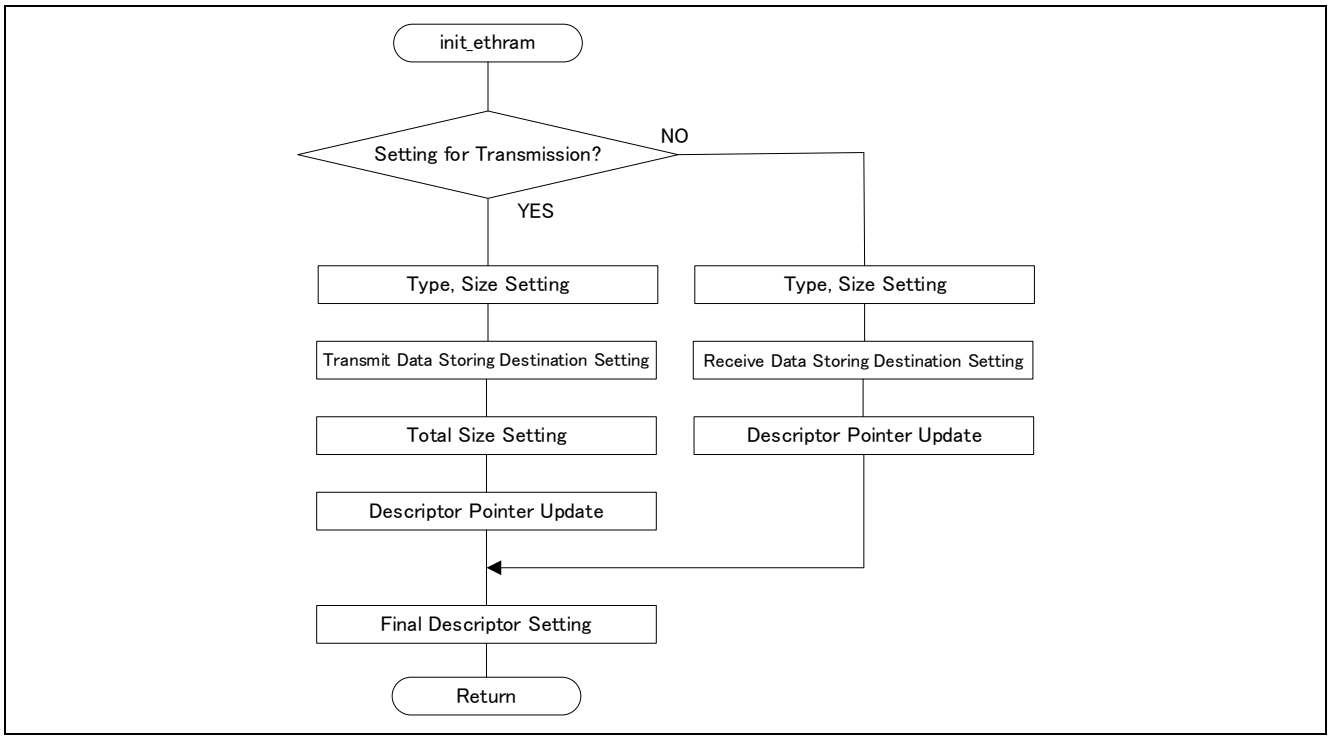

Figure 1-29 Transmit/Receive Descriptor Initialization Module Flowchart

1.4.13 Data Transmission

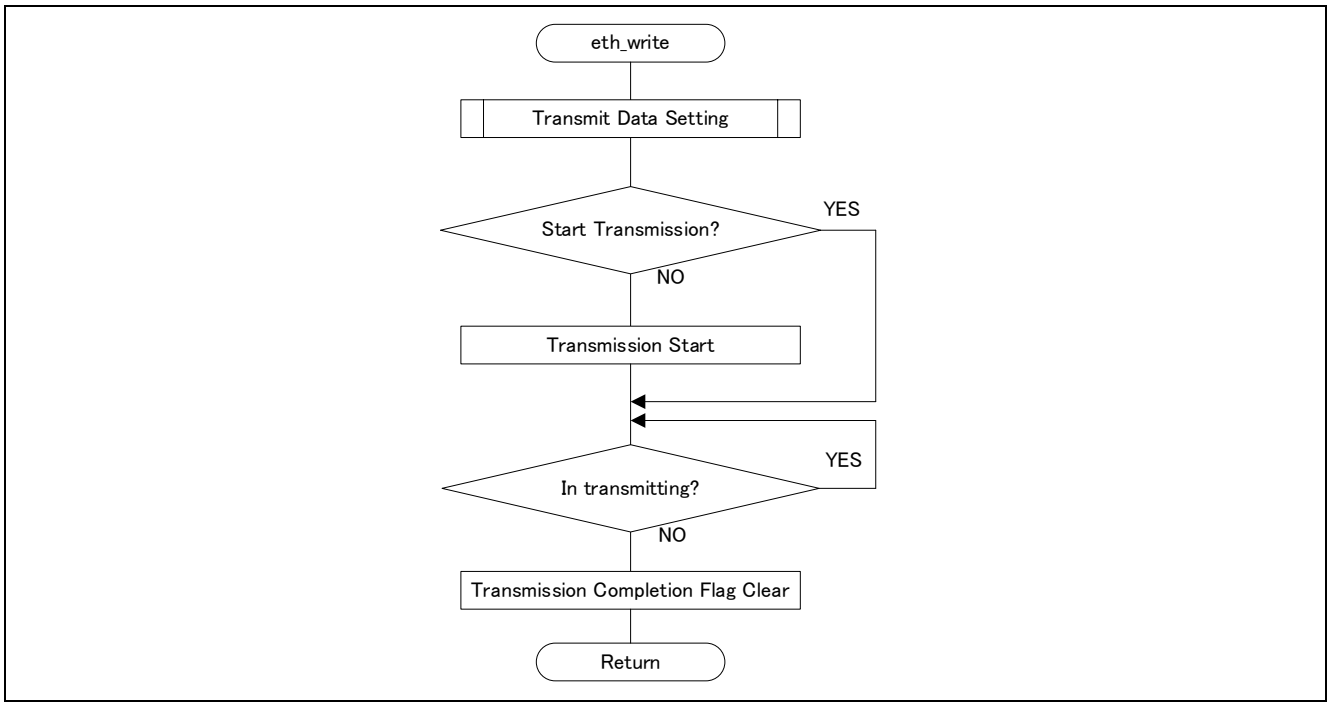

Figure 1-30 Data Transmit Module Flowchart

1.4.14 Data Transmission

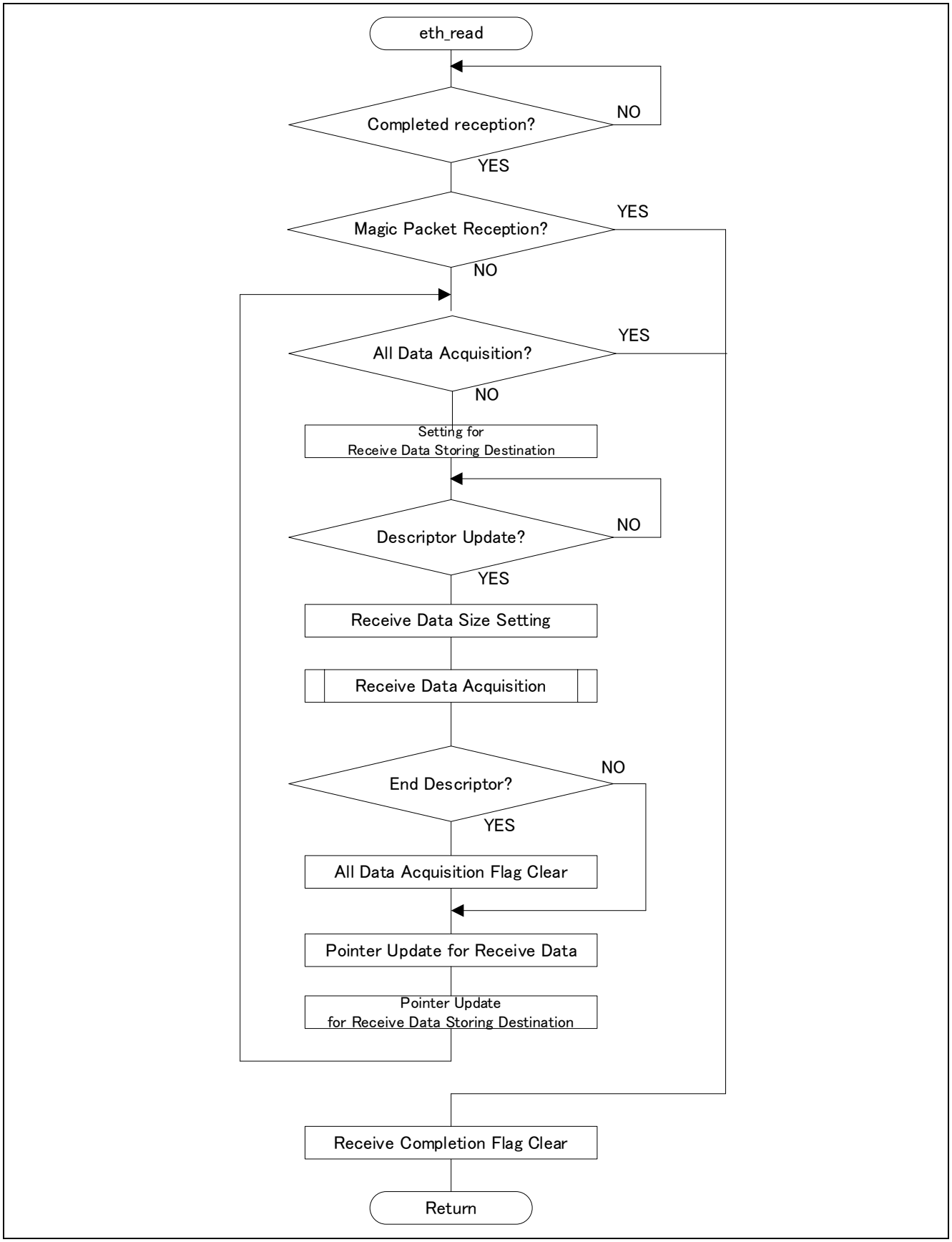

Figure 1-31 Data Receive Module Flowchart

1.4.15 Transmit Data Setting

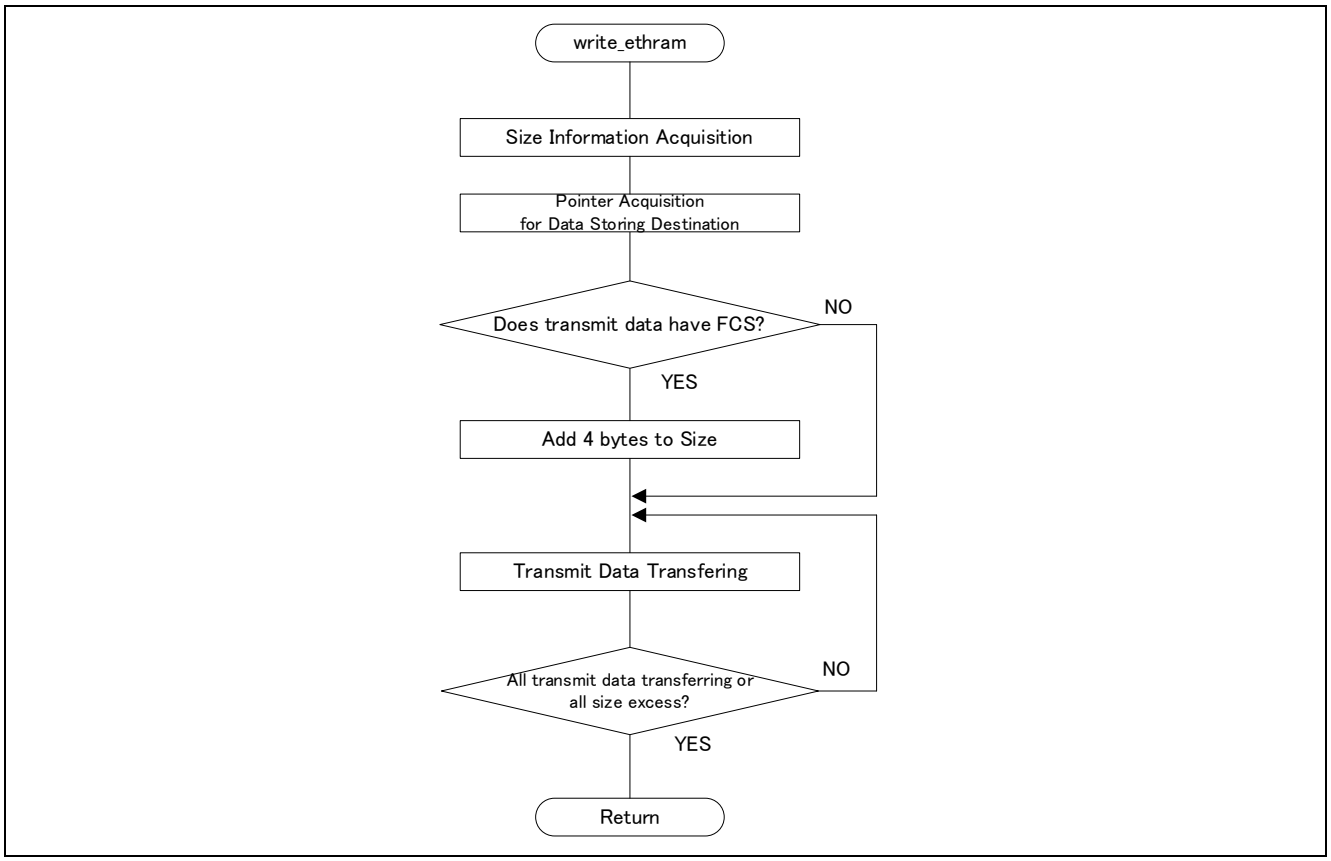

Figure 1-32 Transmit Data Setting Module Flowchart

1.4.16 Receive Data Acquisition

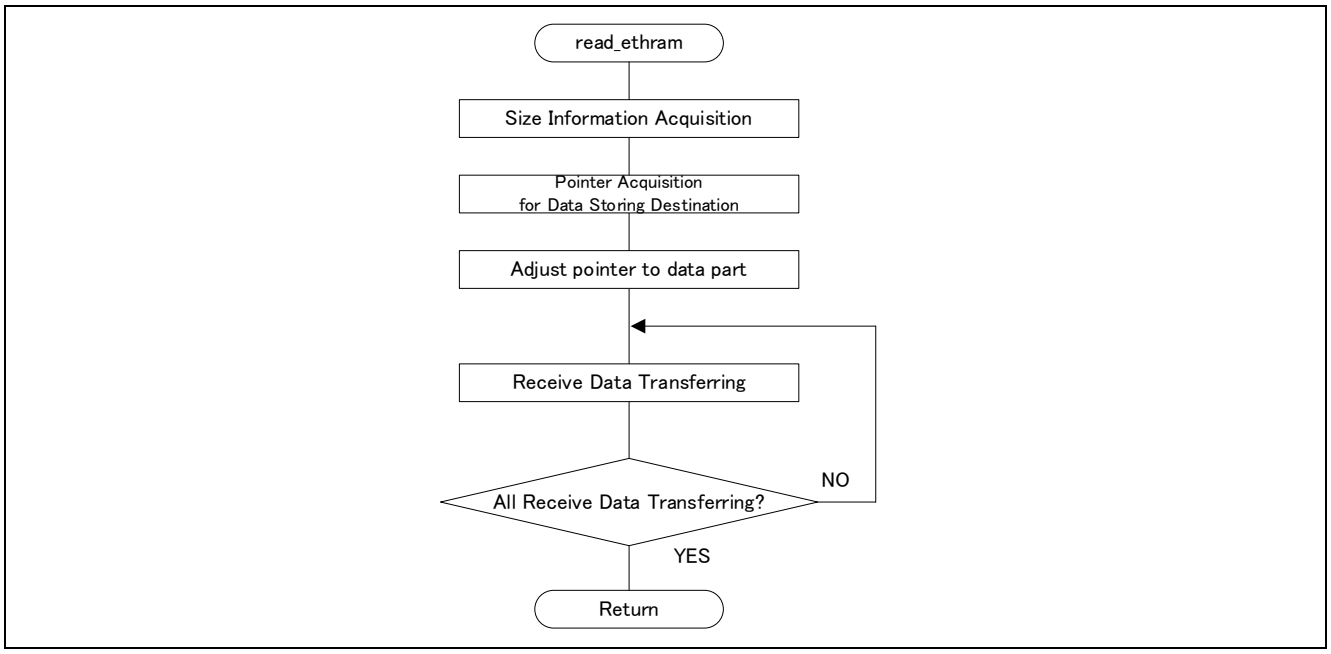

Figure 1-33 Receive Dara Acquisition Module Flowchart

1.4.17 PHY Initialization

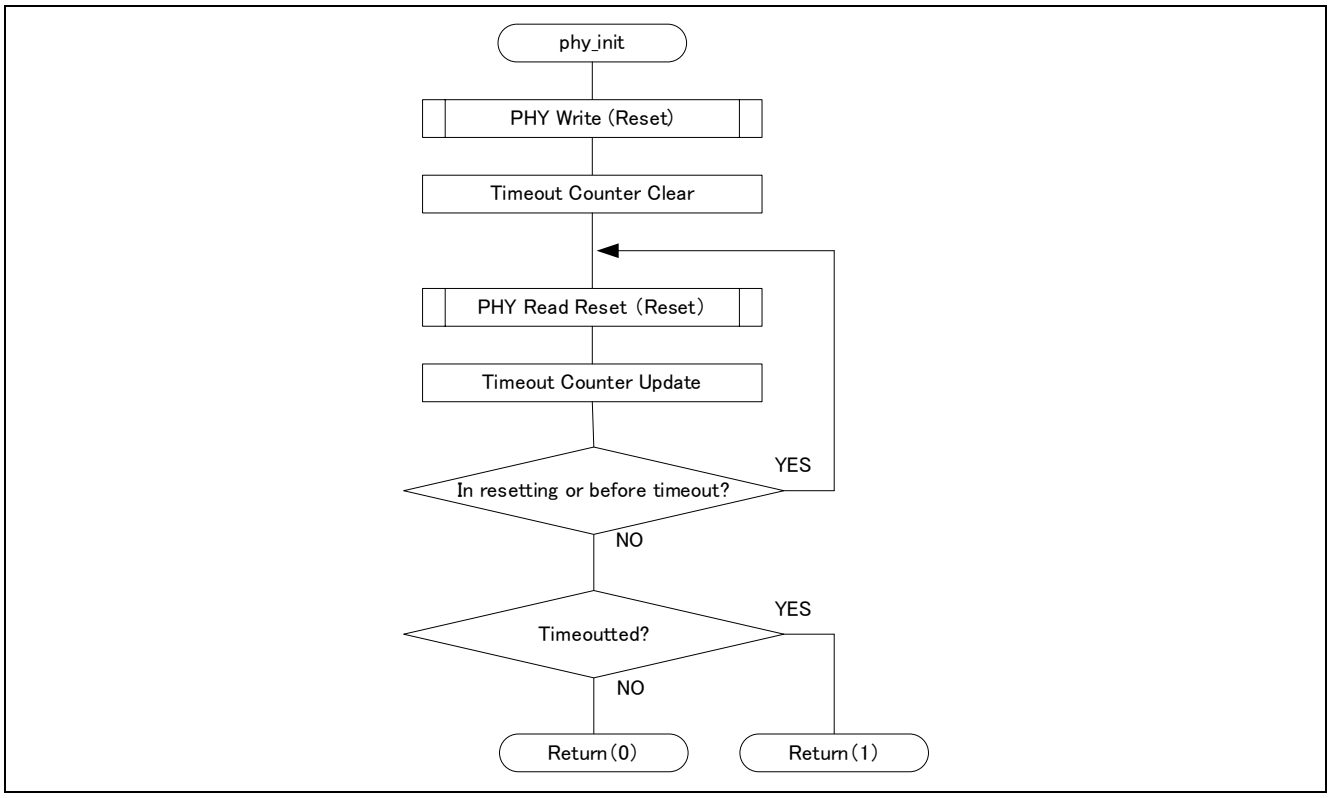

Figure 1-34 PHY Initialization Module Flowchart

1.4.18 Auto-negotiation

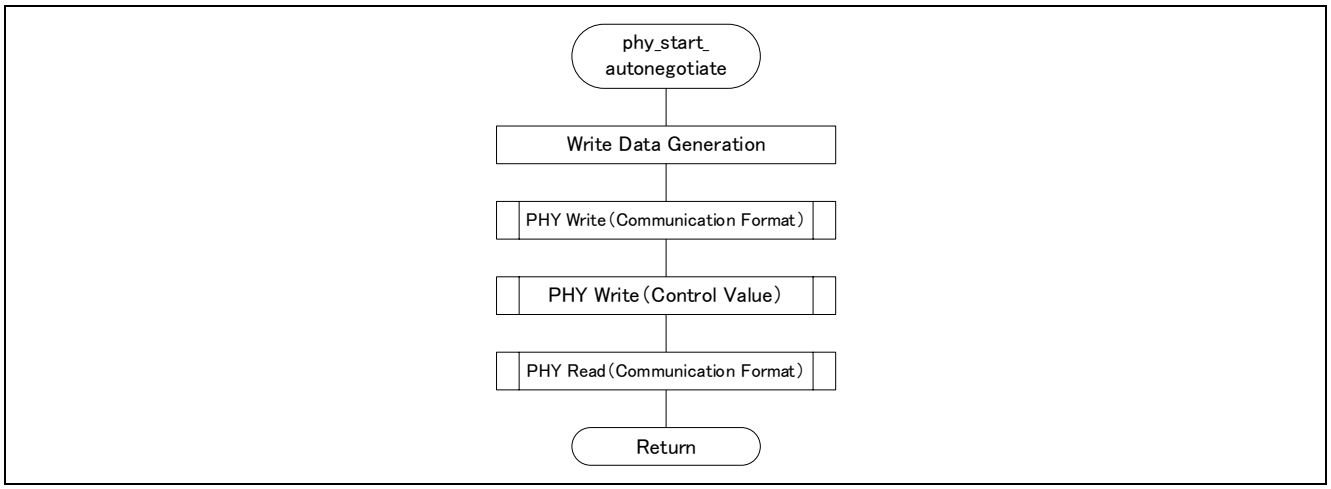

Figure 1-35 Auto-negotiation Module Flowchart

1.4.19 PHY Write

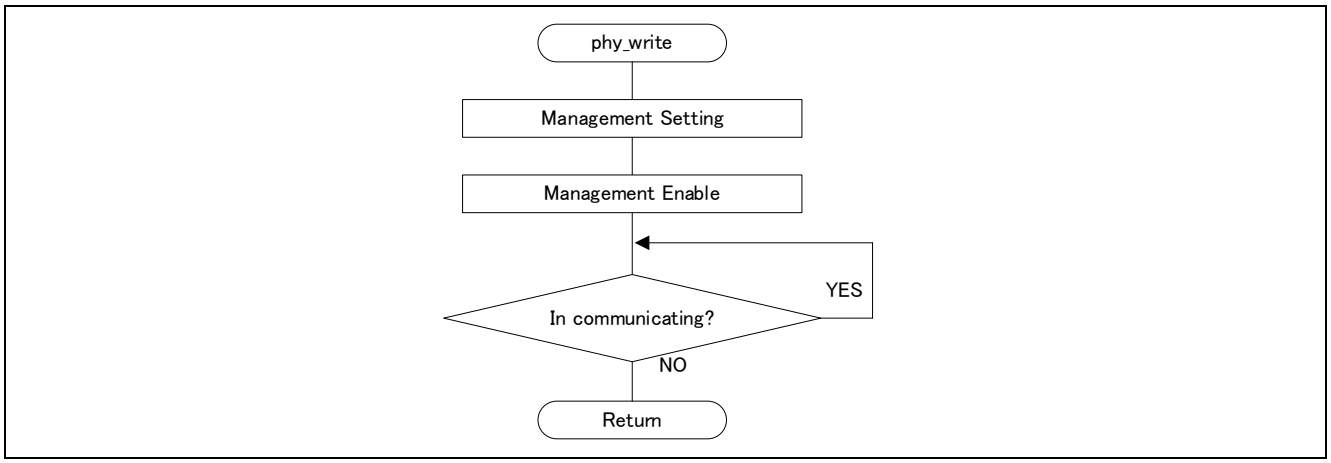

Figure 1-36 PHY Write Module Flowchart

1.4.20 PHY Read

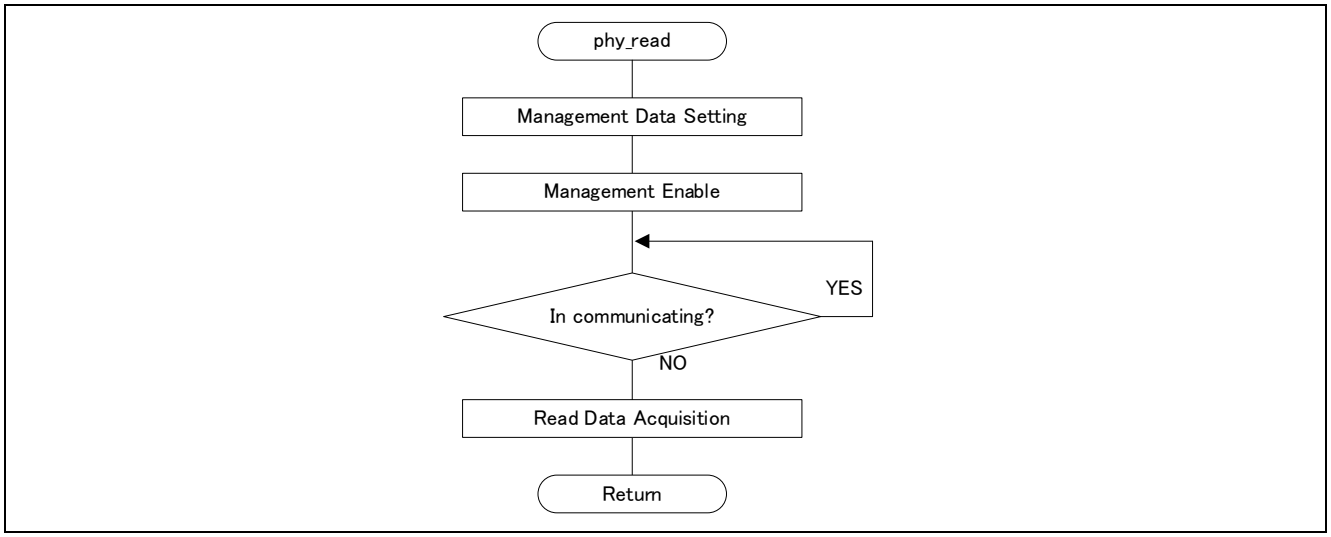

Figure 1-37 PHY Read Module Flowchart

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Website
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Revision History

Rev.	Data	Description	
		Page	Point
1.00	2023.10.10	-	Initial edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused terminals

   [Caution] Please dispose of unused terminals according to "Handling of unused terminals" in the text.

   The impedance of the input terminals of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

   [Caution] The state of the product is undefined when the power is turned on.

   When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.

   For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.

   Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of access to reserved addresses (reserved area)

   [Caution] Access to reserved addresses (reserved areas) is prohibited.

   The address area has a reserved address (reserved area) allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

   [Caution] When resetting, release the reset after the clock has stabilized.

   When switching the clock during program execution, switch the clock after the switching destination clock is stable.

   In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

   [Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.

   Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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