RH850/U2B Group

R01AN6436EJ0100
Rev.1.00

Data Flash Application Note

Summary

This application explains for the on-chipped RH850/U2Bx flash memory rewrite.

The contents of this application note are an example of a user program creation method related to the data flash rewrite. The adaption for the software configuration, the data format among, etc. are required according to the adaptive system.

Application

This document applicates to RH850/U2Bx.

Contents

1. Introduction

This application note explains the program for the data flash rewrite.

1.1 Functions

- Flash sequencer (Sequencer for flash memory)
- Data flash memory

1.2 Applicable Condition

- Self-programing condition enabling

In this application note, enable the following settings on “Cube Suite+” for rewriting the internal flash ROM.

(1) Select “***** (debugging tool)” from the Project Tree.

(2) Select the tab of “Setting for Connection”.

(3) Set “Flash” < “Perform flash self programing” < “Yes”.

2. Basic Operation of Data Flash Memory Rewriting

This section explains about the data flash rewriting of RH850/U2Bx and the basic operation used in this application note.

2.1 Flash Memory-Related Modules

Perform the flash memory erasing/rewriting to use the sequencer (flash sequencer) for the flash memory.

Figure 2-1 shows the configuration diagram of the flash memory-related sequencer. The flash sequencer is configured by FCU and FACI. FCU executes the basic control of the flash memory rewriting. FACI controls FCU according to the FACI command received via P-Bus. The product which mounts the data flash memory for ICUM FCU is mount another pair of sequencers. These sequencers individually control the data flash memory for ICUM. When operating the reset transmission, the FACI transmits the data to the IDCTRL/Option byte storing register from the flash memory.

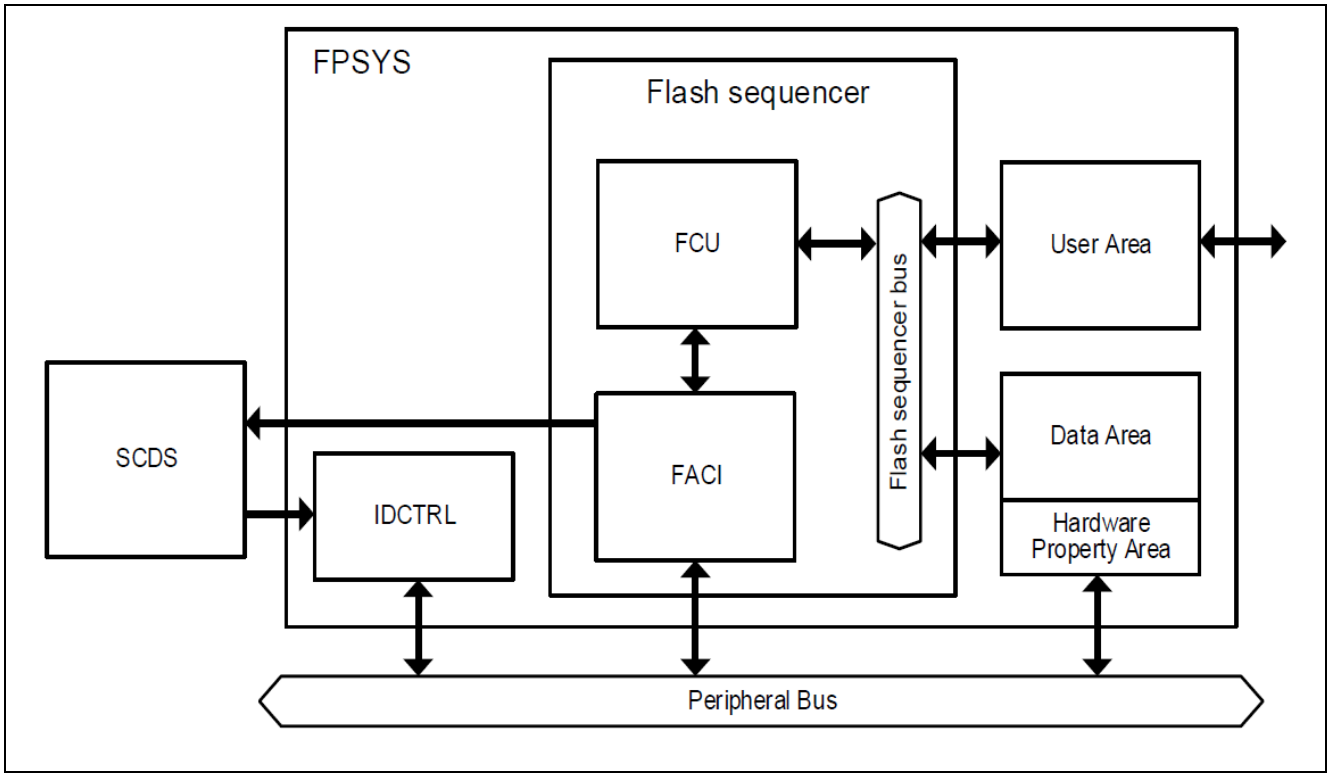


Figure 2-1 Configuration Diagram of Flash Memory-related Module

In this application note,

- Block erasing of data flash by FACI command
- 4 bytes data writing to data flash by FACI command
- Block (64 bytes) data writing by continuous execution of 4 bytes data writing

are as the basic operation of the data flash memory rewriting. For the other functions, refer to the related manuals,

2.2 Initial Setting for Flash Memory

In the user program example of this application note, **Table 2-1** shows the initial setting example of the flash memory-related module that required to execute the data flash memory rewriting (writing/erasing).

Table 2-1 Flash Memory-related Module Initial Setting Example for Data Flash Memory Rewriting

Register Name	Setting Value	Function
Flash access error interrupt enabling register (FAEINT_0)	0x00	・Disable code flash memory access violation interrupt ・Disable command lock interrupt ・Disable data flash memory access violation interrupt ・Disable error correction interrupt
Flash P/E mode entry register (FENTRYR_0)	0xAA00	Data flash memory is read mode
FHVE15 control register (FHVE15)	0x00000001	Flash memory writing/erasing
FHVE3 control register (FHVE3)	0x00000001	

Table 2-1 shows the function specification of the flash memory initial setting in this application note.

Table 2-2 Flash Memory Initial Setting Function Specification

Item	Description
Function name	ROM_INIT()
Function	Perform the initial setting of the flash-memory related module required to execute the data flash memory rewriting (writing/erasing) by the user program.
Implementation method	Function calling from the main routine

2.3 Block Erasing of Data Flash

The erasing of the data flash can execute in 4K bytes block unit. The data flash memory mounted in RH850/U2Bx is allocated from address area “H’FF200000”. Figure 2-2 shows the data flash memory map of RH850/U2Bx.

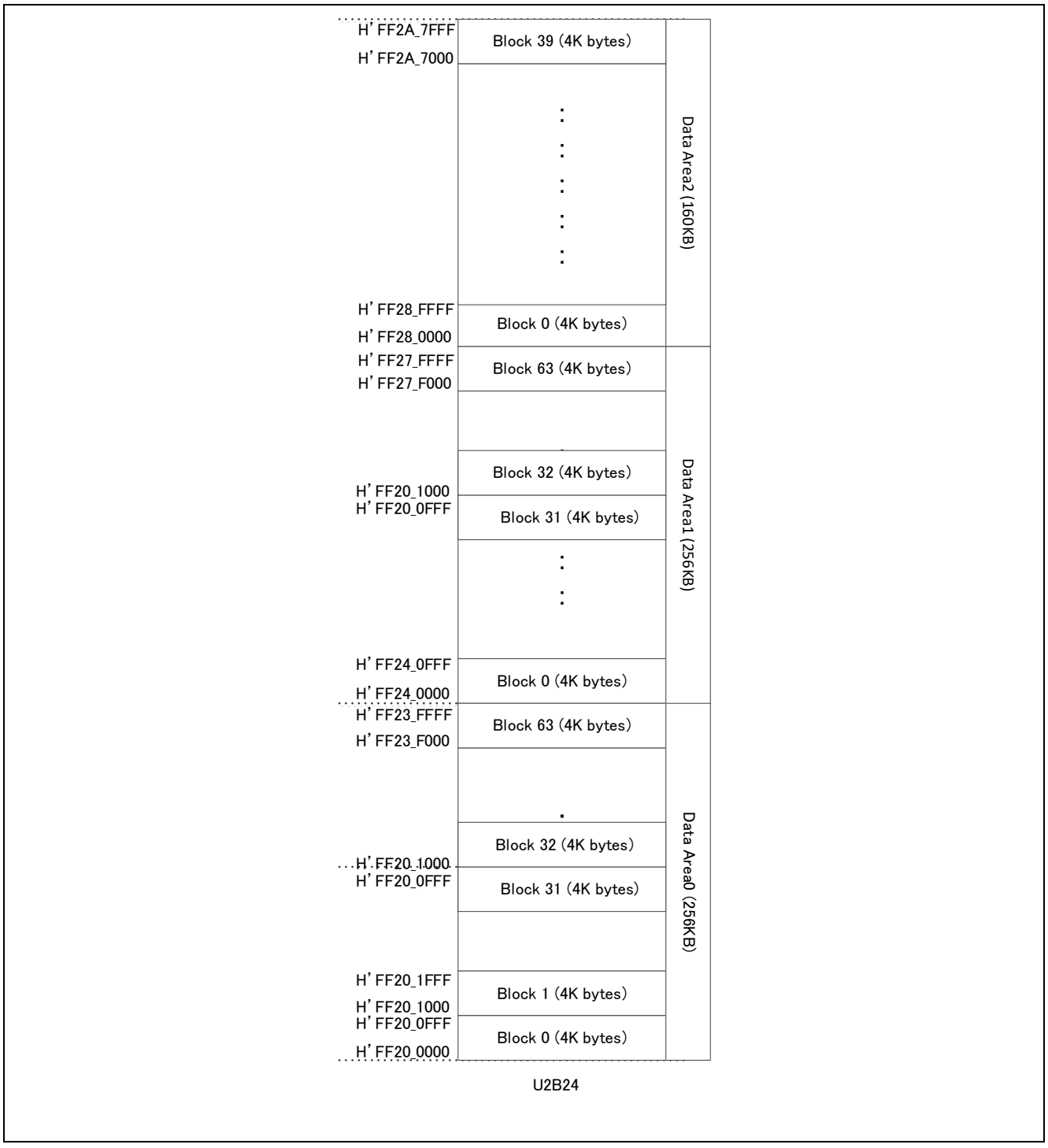


Figure 2-2 Data Flash Memory Mapping

For performing the block erasing of the data flash by the user program, use the block erase command of FACI command, and specify the lead address of the erase target block.

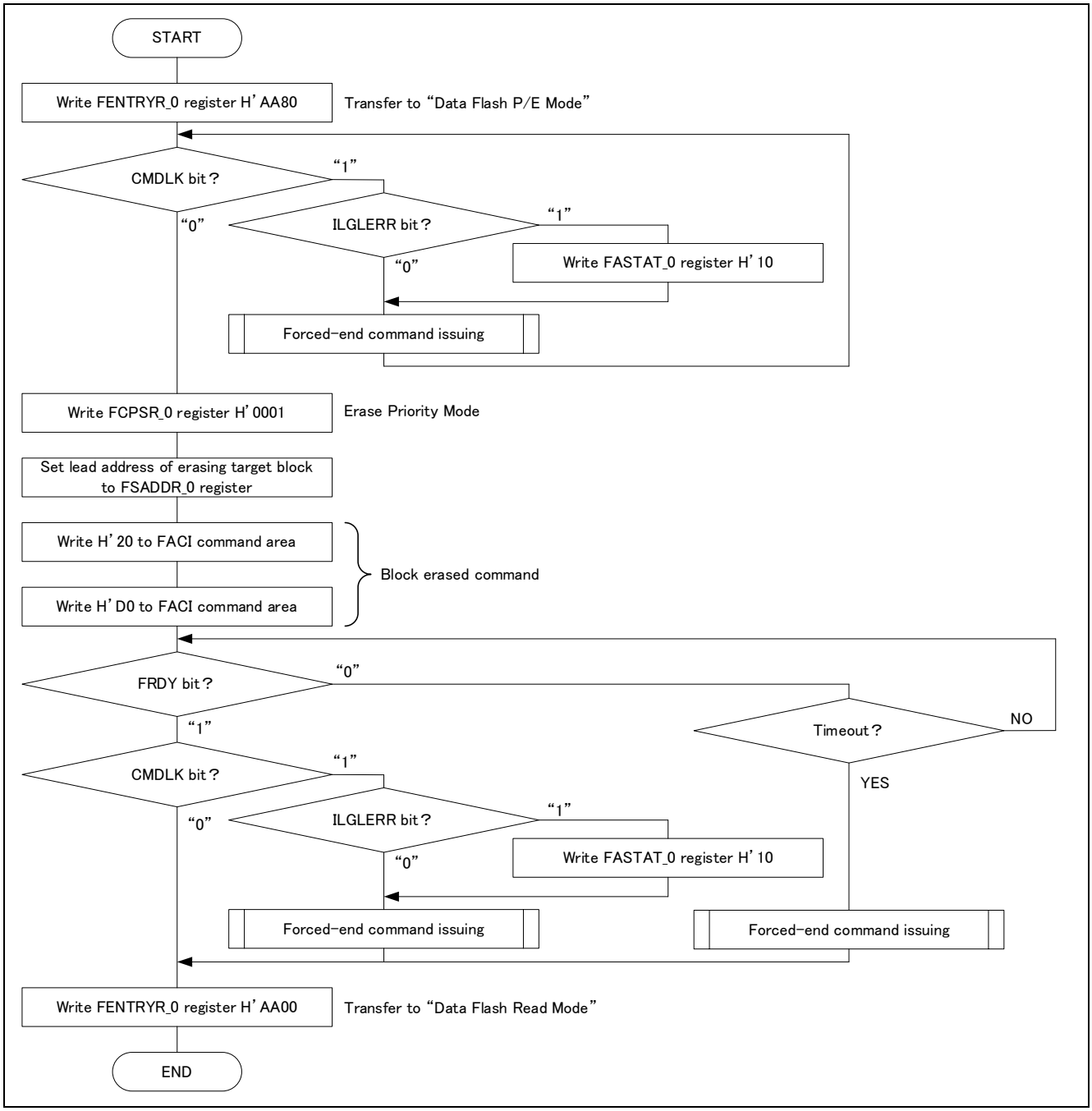
Before issuing the block erase command, set P/E mode to the data flash. Check the data flash which is not in the command lock status, and perform as required the setting for the protection releasing and the erase suspend processing command (Set erase priority mode in here.). After setting the lead address of the erase target block, issue the block erase command (Sequential command writing to the FACI command issuing area). After terminating the block erase command, return the data flash to the read mode.

エラー! 参照元が見つかりません。 shows the block erase flowchart of the data flash.

Table 2-3 shows the block erase function specification of the data flash in this application note.

Table 2-3 Block Erase Function Specification of Data Flash

Item	Description		
Function Name	ROM_ERASE()		
Function	Erase the specification block (Specify by lead address) contents of the data flash memory.		
Implementation Method	Function calling in the steps (several steps) that are required to data flash erasing in the user program.		
Argument Explanation	volatile unsigned long erase_addr		Lead address of erase target block
Return Value Explanation	unsigned long	Normal	Normal termination : Return 0.
		Error	Time out error : Return 0x80000000.
			Other errors : Return FSTATR_0 register contents.



【Note】"RH850/U2Bx Flash Memory User's Manual: Hardware Interface" for the timeout judgement time.

Figure 2-3 Block Erase Flowchart of Data Flash

2.4 4 Bytes Write to Data Flash

The data flash writing can be executed in units of 4 bytes to the erased area (blank).

The data flash writing by the user program is performed to use the program command of the FACI command and specify the write destination address and data.

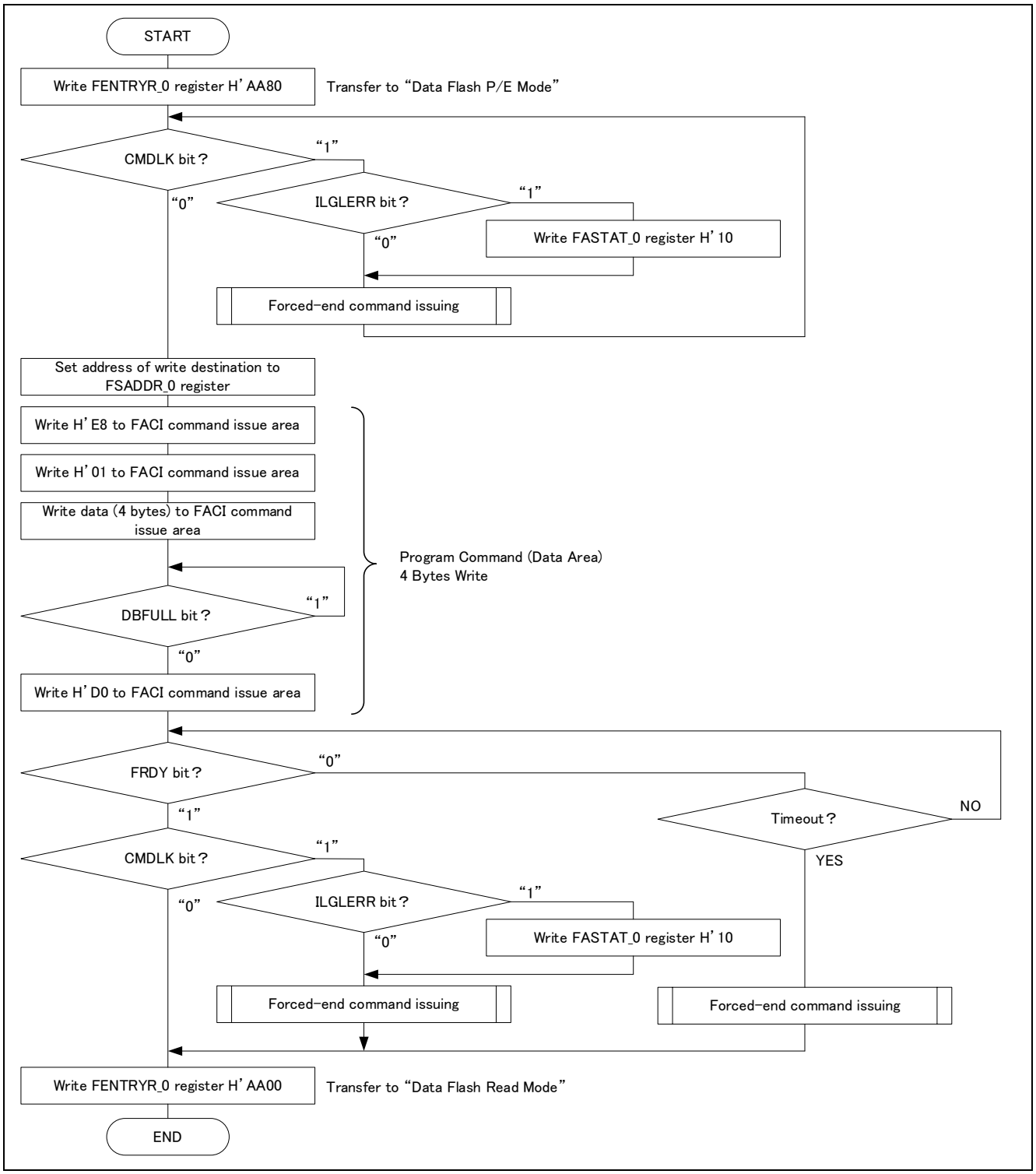
Before issuing the program command, set the data flash to P/E Mode. Check that data flash is not in command lock state, and release the protection as necessary. After setting the write address, issue the program command (Sequential command writing to FACI command issuing are). After completing the program code, return the data flash to Read Mode.

Figure 2-4 shows the 4 bytes write flowchart of the data flash.

Table 2-4 shows the 4 bytes write function specification of the data flash in this application note.

Table 2-4 4 Bytes Write Function Specification of Data Flash

Item	Description		
Function name	ROM_WRITE_4B()		
Function	Write 4 bytes to the specification address of the data flash memory.		
Implementation Method	Function calling in the steps (several steps) that write to the data flash in the user program.		
Argument Explanation	volatile unsigned long write_addr		Writing address
	unsigned long write_data		Writing data
Return Value Explanation	unsigned long	Normal	Normal termination : Return 0.
		Error	Time out error : Return 0x80000000.
			Other errors : Return FSTATR_0 register contents.



【Note】"RH850/U2Bx Flash Memory User's Manual: Hardware Interface" for the timeout judgement time.

Figure 2-4 4 Bytes Write Flowchart to Data Flash

2.5 Unit Block Wring of Data Flash

Applying program commands for data flash, this section explains the program example for writing the data by the unit block (4k bytes).

As the method that continuously writes 4 bytes or more of data for data flash (but multiples bytes of 4);

① The method that repeats the programming command (4 bytes writing) for data flash

② The method that uses DMA program command

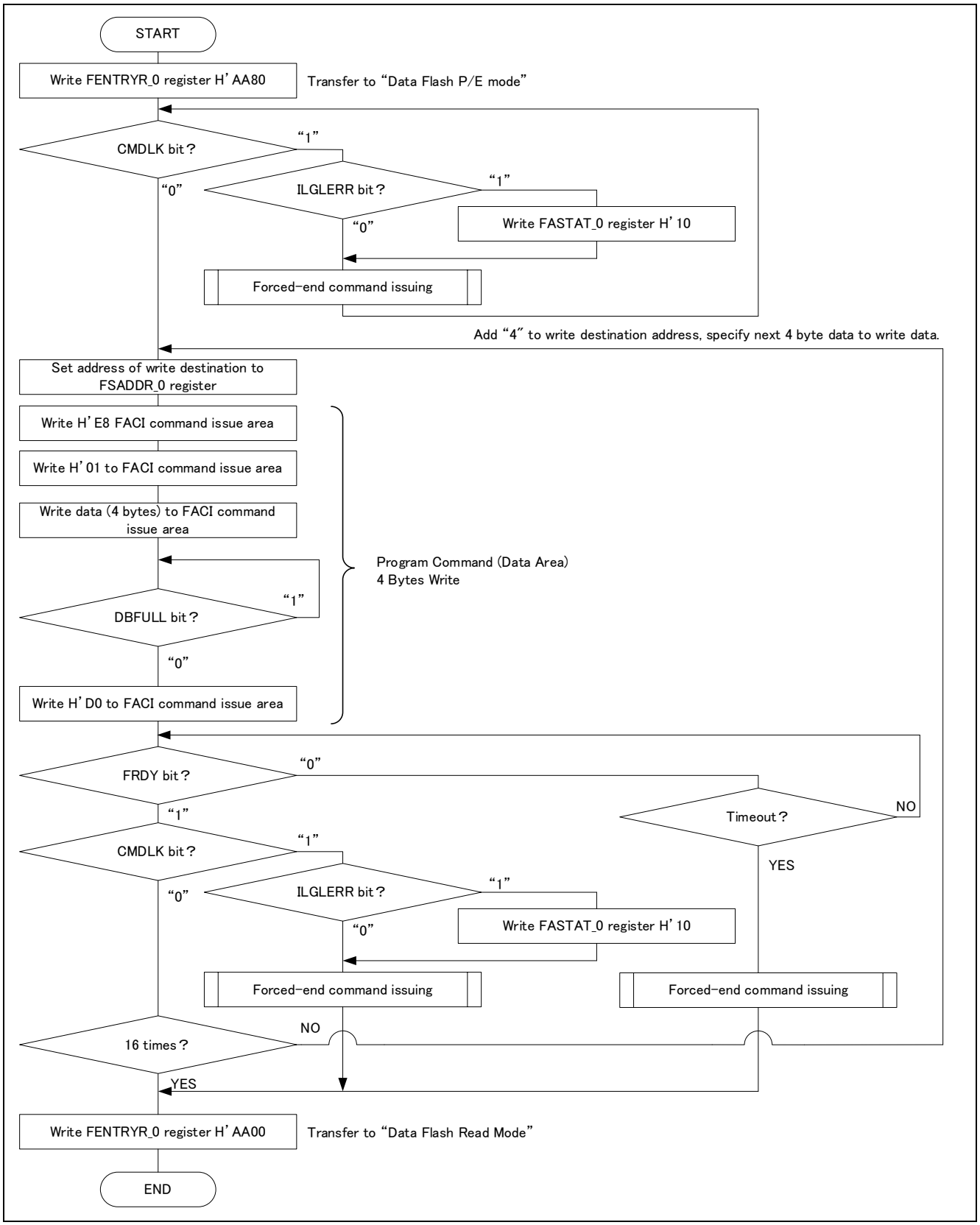
In this application note, "①The method that repeats the programming command (4 bytes writing) for data flash" is used. Write 64 bytes data to the block of the data flash memory by using the program command that writes the 4 bytes data for the data flash and using the program command to write 4 bytes data to the data flash.

Figure 2-5 shows the block write flowchart of the data flash.

Table 2-5 shows the block write function specification of the data flash in this application note.

Table 2-5 Block Write Function Specification of Data Flash

Item	Description		
Function name	ROM_WRITE_BLOCK()		
Function	Write 64 bytes to the block of the data flash memory.		
Implementation Method	Function calling in the steps (several steps) that write to the data flash in the user program.		
Argument Explanation	volatile unsigned long write_addr		Lead address of write destination.
	volatile unsigned long *write_data_ptr		Pointer to write data (lead address)
Return Value Explanation	unsigned long	Normal	Normal termination : Return 0.
		Error	Time out error : Return 0x80000000.
			Other errors : Return FSTATR_0 register contents.



【Note】"RH850/U2Bx Flash Memory User's Manual: Hardware Interface" for the timeout judgement time.

Figure 2-5 Block Write Flowchart to Data Flash

2.6 Forced-end Command

Forced-end command forcedly completes the command processing of the flash sequencer. When executing the command, entire FCU and the part of FACI are initialized.

Figure 2-6 shows the forced-end command issuing flowchart.

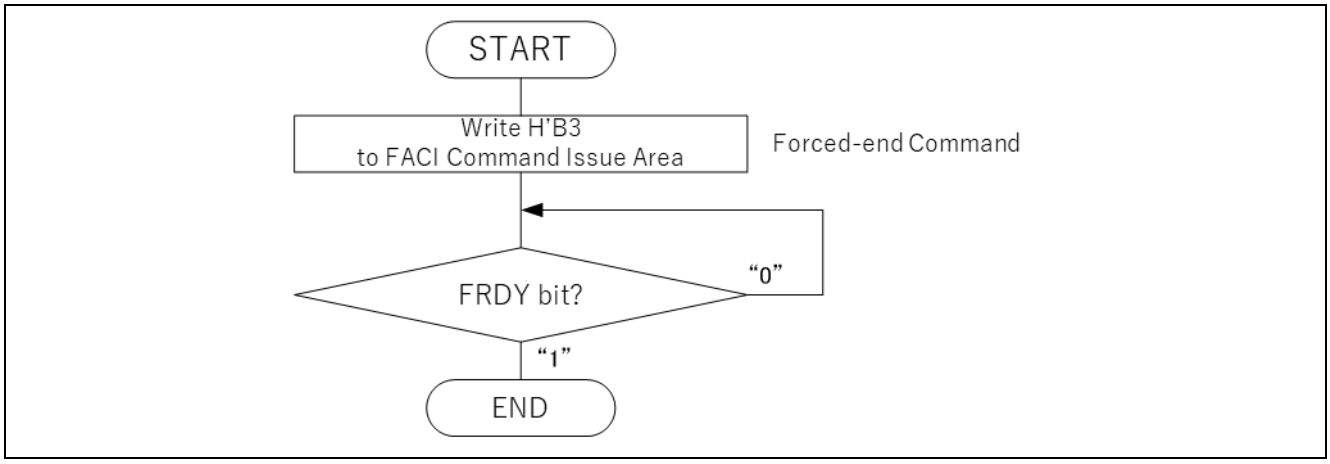


Figure 2-6 Forced-end Command Issuing Flowchart

In this application note, data flash erase and write are executed as error recovery processing at the start and end.

Figure 2-6 shows the function specification of the forced-end command issuing in this application note.

Table 2-6 Function Specification of Forced-end Command

Item	Description
Function name	COMM_END()
Function	Forcedly end the FACI command processing.
Implementation Method	Function calling in the steps (several steps) that required to recover from timeout error or command lock status after issuing the FACI command.

3. Detailed Specification

3.1 Address Map

Figure 3-1 shows the address allocation diagram.

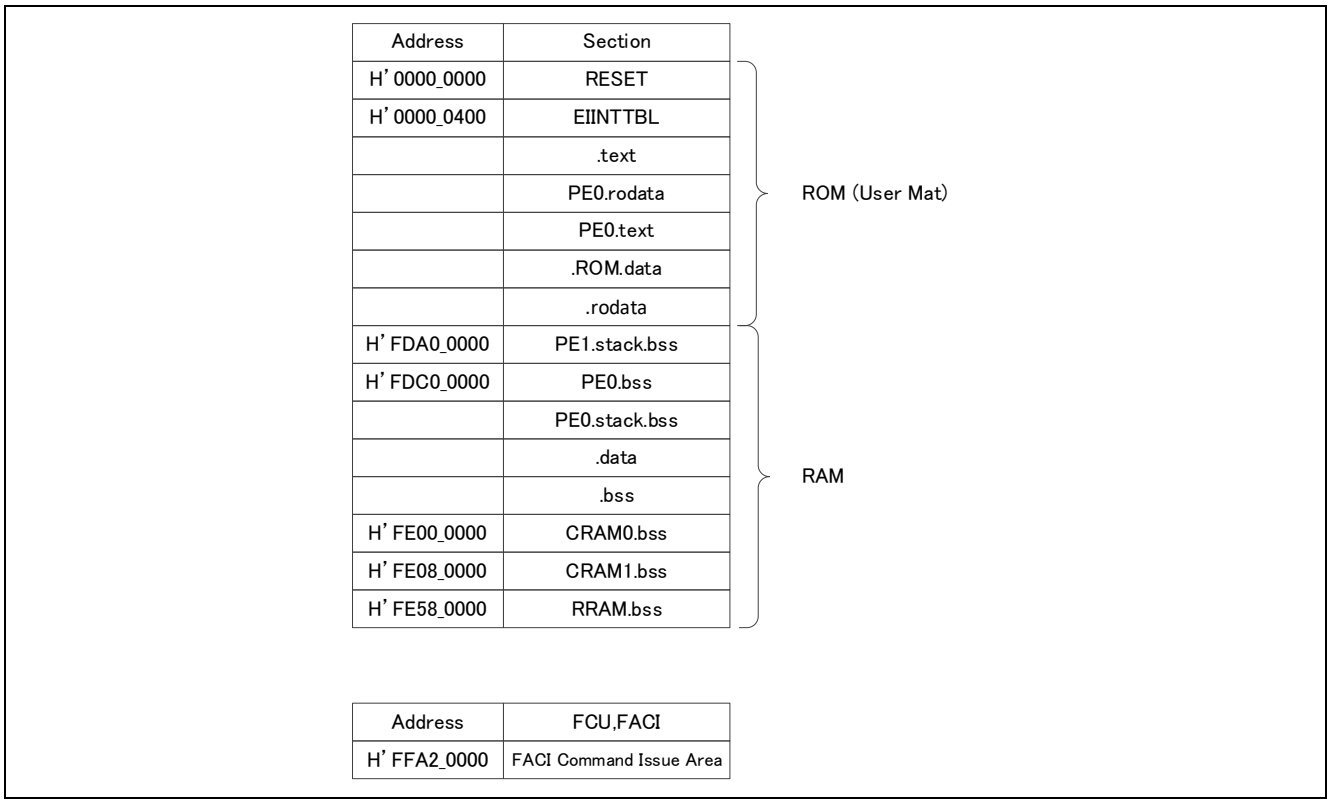


Figure 3-1 Address Allocation Diagram

Our Company's Website and Inquiry

- Website
  http://japan.renesas.com/
- Inquiry
  http://japan.renesas.com/inquiry

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- 1. Precaution against Electrostatic Discharge (ESD)

  A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

- 2. Processing at power-on

  The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

- 3. Input of signal during power-off state

  Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

- 4. Handling of unused pins

  Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

- 5. Clock signals

  After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

- 6. Voltage application waveform at input pin

  Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

- 7. Prohibition of access to reserved addresses

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