RH850/U2B Group
Cyclic ADC Application Note

Summary

This document describes precautions when using Cyclic ADC (CADC) of RH850 / U2B group products.

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1. Precautions for CADC Usage

1.1 Precautions for Board Design

When designing the board, lay out the digital and analog circuits as separately as possible. Also, avoid layouts that cross or approach the signal wiring of digital circuits and the signal wiring of analog circuits as much as possible. Induction causes malfunction of analog circuits and adversely affects the A/D conversion value. Be sure to separate the digital circuit from the analog input pin (CAN00*P, CAN00*N), analog reference voltage (ADSVREFH, ADSVREFL), and analog power supply (ADSVCC) with analog ground (ADSVSS). Connect ADSVSS and ADSVREFL as ADSVSS = ADSVREFL. In addition, connect ADSVSS to a stable digital ground (VSS) on the board at one point.

1.2 Recommended Example of Condenser Insertion

Figure 1 shows the example of condenser insertion.

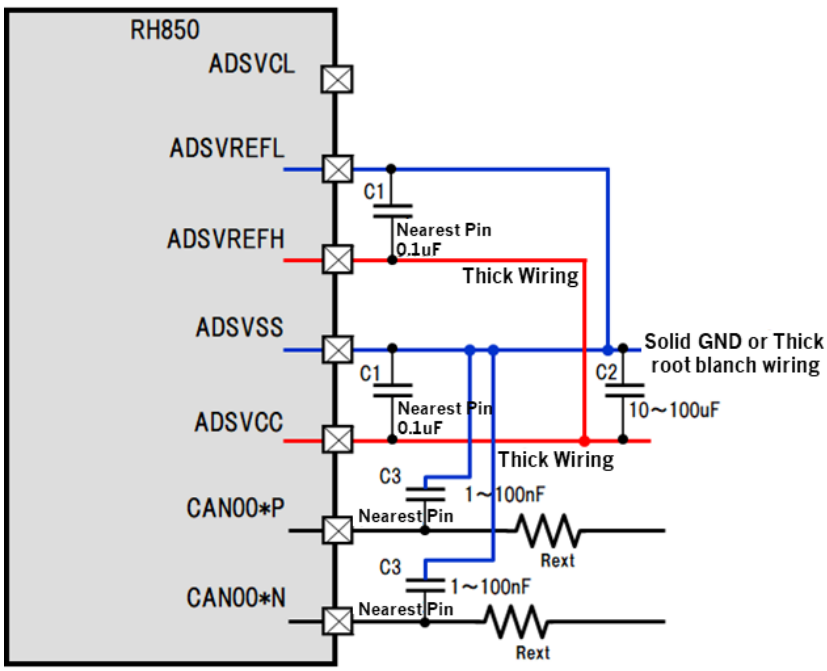

Figure 1 Condenser Insertion Example

*Not necessary to wire to ADVSL when DSADC is not used.

C1: Surge and Noise Countermeasures (0.1uF)

Connect the protection capacitance (C1) between ADSVCC-ADSVSS and ADSVREFH-ADSVSS to prevent device destruction due to abnormal voltage such as

excessive surge. For noise rejection, place C1 closest to the LSI

C2:Power Supply Stabilization Capacity and Measures against Mutual Interference (10uF～100uF)

Place the regulated power supply capacity (C2).

C3: Noise Countermeasure for Input Pin (1nF~100nF)

Refer to chapter 1.3 for CAN00*P, capacitors (C3) connected to CAN00*N, and external circuit resistors (Rext).

*Select a capacitor in consideration of voltage dependence and frequency characteristics.

・Full Scale Error Countermeasures

If the full-scale error worsens, it may be due to the instability of the ADS VREFH. To improve stability, reduce the wiring impedance of ADSVREFH or increase the capacitance value (C1) between ADSVREFH and ADSVREFL.

・Offset Error Countermeasures

For minimizing the potential difference between ADSVSS and ADSVREFL, which causes offset error, design the pattern so that the impedance of the wiring between ADSVSS, ADSVREFL and ADSVRES is small and equal.

1.3 Sampling Error due to External Circuit

Figure 2 shows the CADC input circuit. The analog input pin of the CADC has an input impedance Ri. When the resistance value Rext of the external circuit is large, the signal entering the CADC main unit is divided by Rext and Ri, so it becomes Ri / (Rext + Ri) times and a gain error occurs. Rext should be as small as possible to reduce the gain error. Since Rext and C3 configure an anti-aliasing filter for the CADC input, make sure that the cutoff frequency is Fc, which takes the signal frequency.

$$F_c = \frac{1}{2\pi R_{ext} C_3}$$

When Rext is 50 (Ω) and C3 is 4.7 (nF), the cutoff frequency is 677 (kHz)

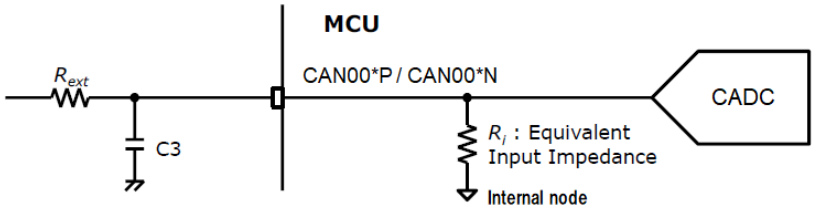

Figure 2 CADC Input Circuit

1.4 Precautions for Digital Dual-purpose Pin Usage

If A/D conversion is performed while the digital input/output is changing, the following noise may adversely affect the conversion accuracy.

(1) Power supply noise due to changes in the digital input of the general-purpose input pin of the same analog power supply as the analog input pin

(2) Coupling noise due to changes in digital input/output of neighboring pins

To reduce the influence of digital input/output on the A/D conversion result, there are the following precautions

For Analog Input Pin

(a) Place the RC," C" near the LSI terminal. By arranging C in the immediate vicinity of the terminal, deterioration of the conversion accuracy of the analog terminal is suppressed. Since the accuracy improvement level depends on the board conditions, evaluate it on the user side board.

For Digital Operating Pins near Analog Input Pin

(a) For pins that are not used as digital input, set digital input prohibition as a port function.

(b) Do not overshoot or undershoot the digital signal input to the digital input.

(c) Design the board so that the load capacity connected to the output pin is small in order to suppress the charge/discharge current.

(d) Use with reduced output drive capability of affected pins.

1.5 Configuration Example for Battery Input

If you want to input the battery voltage directly, follow the injection current limit value (Imax) and terminal voltage limit value (Vmax). The pin voltage may rise and occur destruction due to the influence of the injection current. As shown in Figure 3 configuration example when battery is input to the pin that directly inputs high voltage, perform voltage conversion by resistance voltage division so that the injection current and terminal voltage do not exceed the limit values.

For Imax and Vmax, refer to "RH850/U2B Group User's Manual: Hardware, 66.2.7 Injection Current Characteristics, Table 66.9 Injection Current Operating Conditions, IINJ_AIN" and Vin of NOTE.

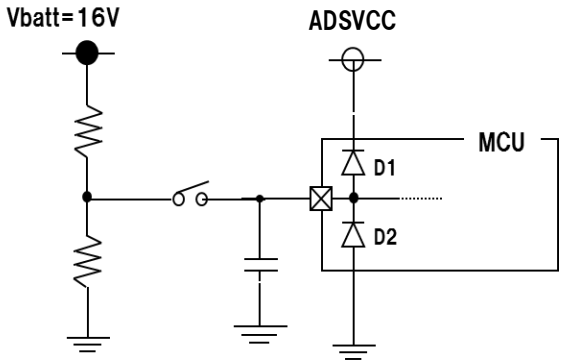

Figure 3 Configuration Example for Battery Input

Revision Record

Rev.	Issue date	Revised contents	
		Page	Points
0.50	2021.9.30	-	First edition
1.00	2023.4.7	-	Official version
1.10	2025.7.5	1	Correction of Typo

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

- 1. Precaution against Electrostatic Discharge (ESD)

  A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

- 2. Processing at power-on

  The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

- 3. Input of signal during power-off state

  Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

- 4. Handling of unused pins

  Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

- 5. Clock signals

  After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

- 6. Voltage application waveform at input pin

  Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

- 7. Prohibition of access to reserved addresses

  Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

- 8. Differences between products

  Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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