RH850/U2B Group

R01AN6618EJ0100
Rev.1.00

Current Feedback Control using Generic Timer Module (GTM)

Summary

This application note explains about Generic Timer Module (GTM) function in the RH850/U2A series of single-chip microcomputers for automobiles from Renesas Electronics (hereafter referred to as U2A).

Aim of this document and software is to provide supplemental information for the function on RH850/U2B. It is not intended to implement in the design for mass production.

There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update, and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update, and development environment.

Target Device

RH850/U2B Group

Target Integrated Development Environment

CS+(from RENESUS Electronics)

Device file : DR7F702Z21*.DVF

DR7F702Z22*.DVF

Reference Document

RH850/U2B User's Manual: Hardware

For function details and electrical characteristics, prese refer to "User's Manual Chapter: Hardware".

This application note is made to refer to the following manual.

- RH850/U2B User's Manual (Rev.1.00): R01UH0923EJ0100

Items

1. Current Feedback Control Overview

1.1 Operation Overview

In this operation example, the current feedback control of solenoid is performed by GTM. ABFG generates the border flag from the upper/lower limit judgement error, and input it to GTM via the virtual port.

GTM judges the current value form the border flag inputted to TIM or AD conversion value, and outputs the pulse ATOM0_o pin by ATOM.

Figure 1-1 shows the current feedback control example in this operation example.

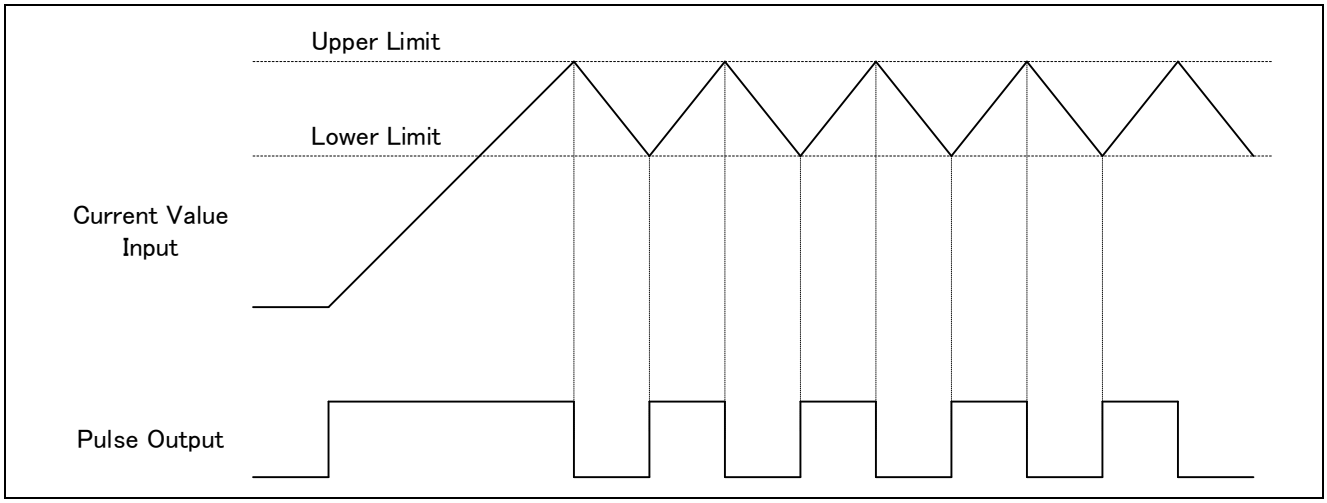

Figure 1-1 Current Feedback Control Example

1.2 System Configuration Diagram

Figure 1-2 shows the system configuration diagram in this operation example.

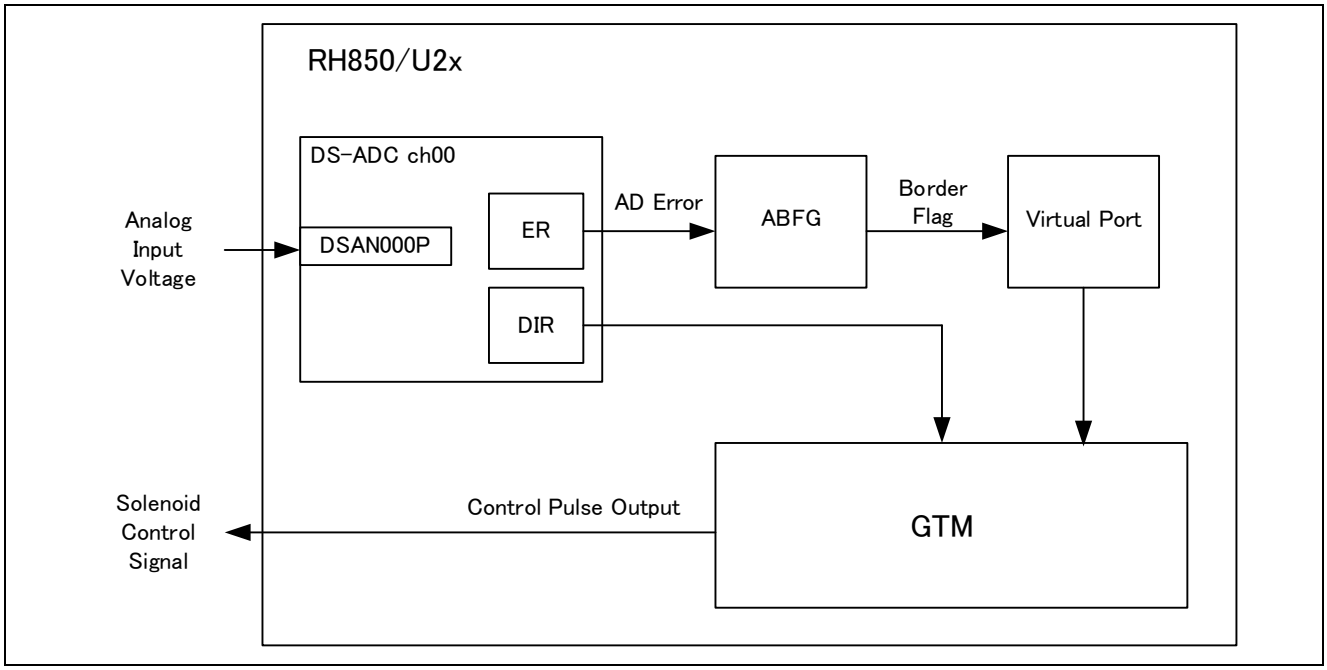

Figure 1-2 System Configuration

1.3 Pin Function

Table 1-1 shows the pin functions used in this operation example.

Table 1-1 Pin Function List

Pin Name	Function
DSAN000P（AN003）	Analog input pin
ATOM0_0（P00_2）	Pulse output
TIM0_0（P37_0）	Border flag input

1.4 Peripheral Function

Table 1-2 shows the peripheral function list used in this operation example.

Table 1-2 Peripheral Function List

Peripheral Function	Purpose
GTM Multi Channel Sequencer (MCS)	・Upper/Lower limit decision for current value, and pulse output instruction
GTM Timer Input Module（TIM）	・Border flag input
GTM ARU-connected Timer Output Module（ATOM）	・Pulse output
Δ Σ A/D Convertor（DS-ADC）	・Digital conversion for current value
ABFG	・ADC border flag generation

1.4.1 GTM Multi Channel Sequencer (MCS)

Acquire the border flag level detected by TIM using ARU and AEI bus ,and determine the upper/lower limt for the current value. Controls the level of pulses output from ATOM according to the upper/lower limit judgments.

1.4.2 GTM Timer Input Module（TIM）

Input the border flag.

1.4.3 GTM ARU-connected Timer Output Module（ATOM）

Perform the pulse output.

・Set to SOMI mode and High/Low level output.

1.4.4 Δ Σ A/D Convertor (DS-ADC)

Digital-convert the current value.

- DS-ADC (DSADC00) continuously performs A/D conversion for the analog input voltage in no gain (x1), single-end input, and common voltage ADSVREFL.
- A/D conversion value of DS-ADC (DSADC00) is entered to ABFG after determining the upper/lower limit.
- DS-ADC start trigger : Software trigger
- DS-ADC Sampling plate : 200ksps
- Input voltage area:
  Ste the following in this operation example.
  - AnVCC = ADSVCC = AFCVCC = 5V
  - ADSVREFH = 5V
  - ADSVSS = 0V
  - ADSVREFL = 0V
  - ADSVCL=10nF
  - Analog input (DSAN000P) = 0～3.5V

  Please refer to "*RH850/U2B User's Manual Section 66 Electrical Characteristics"* for the details of each function.

1.4.5 ADC Border Flag Generation (ABFG)

Generates the border flag by the upper/lower determination of ADC conversion value.

2. Operation Example

When using the border flag for determining the current value upper/lower limit, MCS acquires the border flag form TIM via ARU or AEI bus. Furthermore, MCS set the output level to ATOM via ARU for outputting the control pule from ATOM. The following explains the details of the operation example 1 to 3.

- Operation Example 1 (ARU Access)
- Operation Example 2 (AEI Access)
- Operation Example 3 (AD Data Register Access)

2.1 Operation Example 1 (ARU Access)

2.1.1 Overview

Figure 2-1 shows the overview diagram in this operation example. Input the border flag from virtual port into TIM. Detect the input pulse edge by TIM, and MCS acquires the edge detection result via ARU (Advanced Routing Unit). Depending on the edge direction, High/Low output is set to ATOM via ARU, and pulses are output.

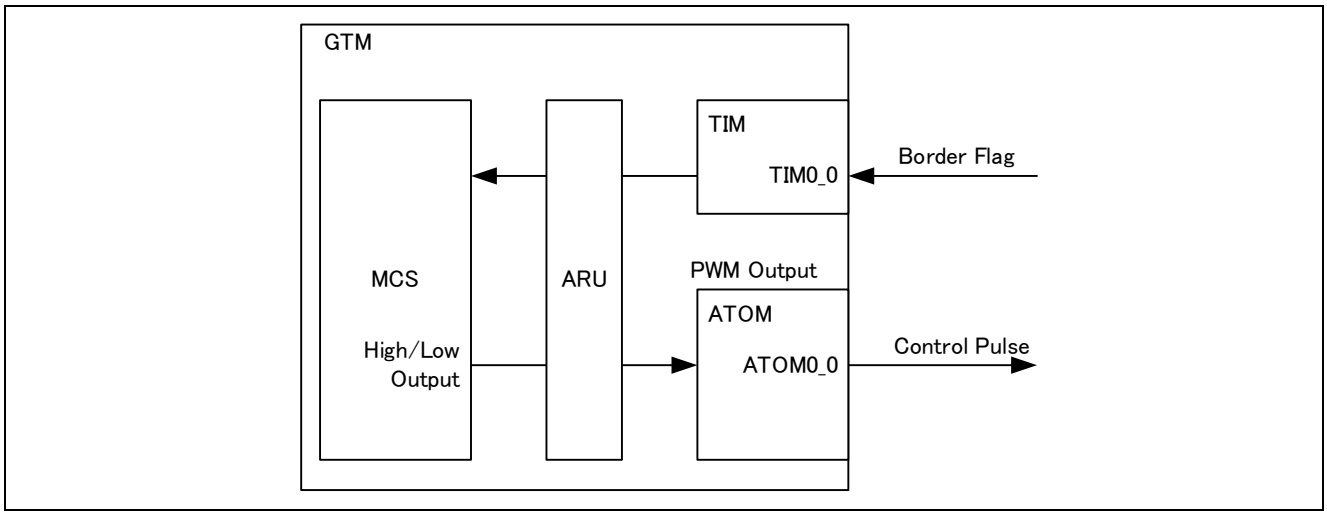

Figure 2-1 Overview Diagram

The following shows the overview of ARU access.

Table 2-1 shows the ARU address used in this operation example. (Please refer to GTM specification for the details of other ARU addresses.)

Table 2-1 ARU Address

Name	Address
TIM0_WRADDR0	0x1B7
TIM0_WRADDR1	0x1B8
MCS0_ WRADDR0	0x04F

2.1.2 TIM Edge Detection Result Acquisition by MCS

Set ARU_EN=’1’ in TIM0_ch0 to 1 control registers (ARU routing enable setting). The measurement result is written to TIM0_WRADDRx(x=0,1) by the setting. The measurement result by TIM can be acquired by reading the data from TIM0_WRADDRx(x=0,1) in ARU read Direction (ARD) of MCS. (ARU read direction starts the read operation when the data is written to the specified address.)

The following shows the data flow of ARU read direction.

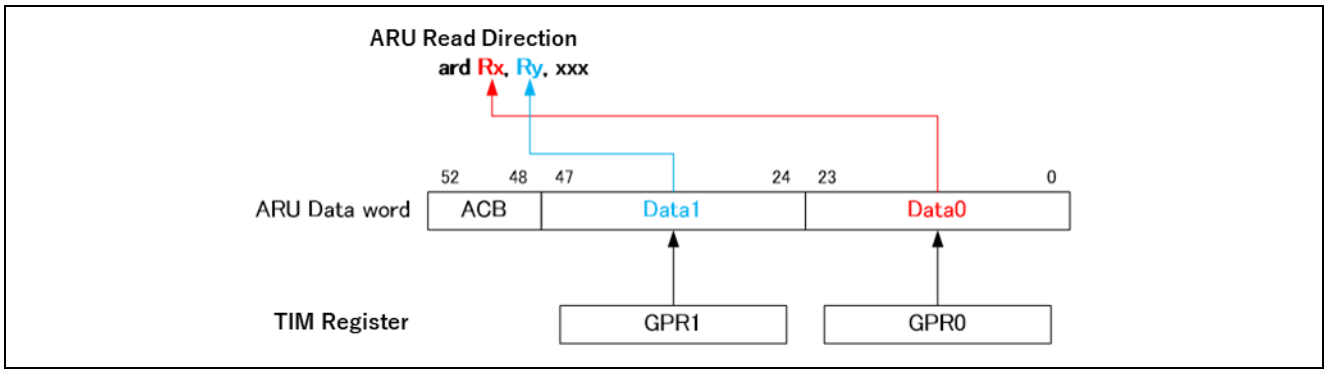

Figure 2-2 ARU Read Direction (ARD)

2.1.3 Pulse Output by MCS

Figure 2-3 shows the overview diagram in this operation example. Use ATOM in SOMI mode (Signal Output Mode Immediate). Control High/Low output in ACB (ARU Control Bit Register) of MCS.

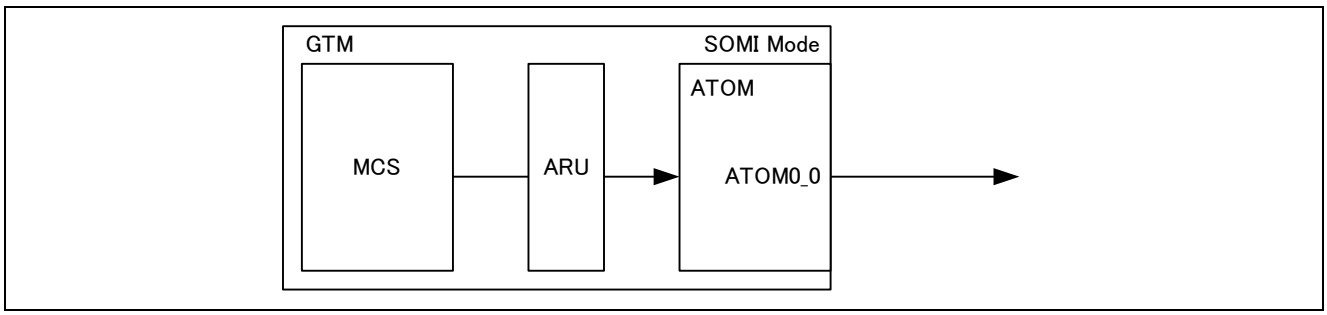

Figure 2-3 Overview Diagram

The following shows the overview of ACB (ARU Control Bit Register).

When using ATOM in SOMI mode (Signal Output Mode Immediate), the setting value of ACB (ARU Control Bit Register) is transferred to ACB bit in ATOM control register when executing ARU write direction.

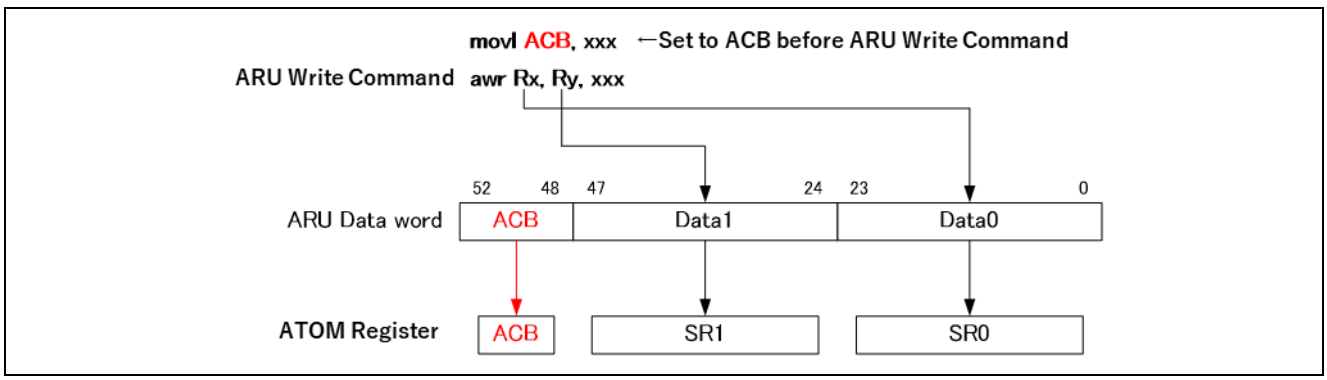

Figure 2-4 ACB (ARU Control Bit Register)

2.1.4 Operation Condition of Use Function

The following shows the operation condition of use function in this operation example.

Table 2-2 Port Setting

Items	Contents
Use Pin (Input)	P37_0 : TIM0_0
Use Pin (Output)	P00_2 : ATOM0_0

Table 2-3 TIM0 Setting

Items	Contents
TIM0 Operation Clock	100MHz
Use Channel	TIM0 ch0 to 1
Operation Mode	TIM Input Event Mode (TIEM)
Signal Level	ch0 : Falling edge detection, ch1 : Rising edge detection
ARU Routing	Enable

Table 2-4 ATOM0 Setting

Items	Contents
ATOM0 Operation Clock	100MHz
Use Channel	ATOM0 ch0
Operation Mode	Signal Output Mode Immediate (SOMI)
Signal Level	High/Low level output
ARU Input Stream	Enable
ARU Read Address	ATOM0 ch0 : 0x04F (MCS0_WRADDR0)

Table 2-5 MCS0 Setting

Items	Contents
MCS0 Operation Clock	100MHz
Use Channel	MCS0 ch0 to 1
Scheduling Mode	Multiple Priority Scheduling

2.1.5 Software Explanation

The following shows the setting example of each register used in this operation example. Set OPBT8.CKSEL_GTM=0 (CLK_GTM=200MHz) for operating in this operation example.

Table 2-6 STBC Register Setting Example

Register Name	Setting Value	Function
Module Standby Register for GTM (MSR_GTM)	0x0000 0000	Clock-supply to MS_GTM_0 0 : GTM
Module Standby Register for DS-ADC and Cyclic-ADC (MSR_DSADC_CADC)	0x0000 0000	Clock-supply to MS_DSADC_CADC_0 0 : DS-ADC & CADC COMMON
		Clock supply to MS_DSADC_CADC_2 0 : DS-ADC00,10
Module Standby Register for SAR-ADC (MSR_ADCK_ISO)	0x0000 00BF	Clock supply to MS_ADCK_ISO_6 0 : ABFG

Table 2-7 GTM Register Setting Example

Register Name	Setting Value	Function
GTM-IP Global control register (GTM_CTRL)	0x0000 0000	RF_PROT 0 : SW RST Function Enable (Protection release of GTM_RST register)
GTM-IP Global reset register (GTM_RST)	0x00000001	RST 1 : Initialization reset of all sub module

Table 2-8 MCS Register Setting Example

Register Name	Setting Value	Function
MCS0 Control and Status register (MCS0_CTRL_STAT)	0x0200 0003	SCD_MODE 0x3 : Multiple Priority Scheduling
MCS0 Channel x control register (MCS0_CH[x]_CTRL, x=0,1)	0x0000 0001	EN 1:MCS0_ch[x] enable

Table 2-9 TIM Register Setting Example

Register Name	Setting Value	Function
TIM0 Channel 0 control register (TIM0_CH0_CTRL)	0x0000 0C24 ↓ 0x0000 0C25	DSL 0 : Falling edge measurement
		GPR1_SEL 0x3 : CNT
		CICTRL 0 : Channel input is TIM_IN0
		ARU_EN 1 : Registers content routed
		TIM_MODE 0x2 : Input event mode (TIEM)
		TIM_EN 0 : Channel disable 1 : Channel enable
TIM0 Channel 1 control register (TIM0_CH1_CTRL)	0x0000 2C64 ↓ 0x0000 2C65	DSL 1 : Rising edge measurement
		GPR1_SEL 0x3 : Input is CNT
		CICTRL 1: Channel input is TIM_IN0
		ARU_EN 1 : Registers content routed
		TIM_MODE 0x2 : Input event mode (TIEM)
		TIM_EN 0 : Channel disable 1 : Channel enable

Table 2-10 ATOM Register Setting Example

Register Name	Setting Value	Function
ATOM Channel 0 control register (ATOM0_CH0_CTRL)	0x0000 0808	MODE[1:0] 0x0 : Signal Output Mode Immediate (SOMI)
		ARU_EN 1 : ARU Input stream enable
		SL 1 : High level output
ATOM Channel 0 ARU read address register (ATOM0_CH0_RDADDR)	0x01FE 004F	RDADDR0 0x04F : ARU read address is MCS0_WRADDR0
AGC Output enable status register (ATOM0_AGC_OUTEN_STAT)	0x0000 0002	OUTEN_STAT0 0x02 : CH0 output enable
AGC Enable/disable status register (ATOM0_AGC_ENDIS_STAT)	0x0000 0002	ENDIS_STAT0 0x02 : CH0

Table 2-11 CMU Register Setting Example

Register Name	Setting Value	Function
CMU Clock enable register (CMU_CLK_EN)	0x0000 0002	EN_CLK0 0x2 : CMU_CLK_RES0 enable

Table 2-12 DS-ADC Register Setting Example

Register Name	Setting Value	Function
AD Global Control Register (DSADCADGCR)	0x01	When UNSND 1 : UNSND=1 or CNVCLS=0, AD conversion result is unsigned. In other cases, with sign.
Unit Control Register (DSADC00UCR)	0x0400 0400	RESO0 1 : High impedance mode
		DFMT[3:0] 0x4 : Lower 4 bits mask of AD conversion result
		VCEP[2:0] 0x0 : End virtual channel is virtual channel 0.
Virtual Channel Register 0 (DSADC00VCR0)	0x0C10 4000	FSELEXTE=0, DSDFTYP[3:0]=0, ORT=0, TPVSL[2:0]=0x1 : Filter type is 2nd Stage Used Case 2 (F1b)
		GAIN[1:0] 0x0 : Input gain is x1
		VCULME 1 : AD conversion result upper limit exceeded notification enable
		VCLLME 1 : AD conversion result lower limit under notification enable
		VCULLMTBS[1:0] Upper/Lower limit check by 0x0:DSADCnULTBR0
		CNVCLS[1:0] 0x0 : Sigle-end input and Common voltage is =ADSVREFL
		GCTRL[3:0] 0 : Analog input channel is DSAN000P
Upper-Limit/Lower-Limit Table Register 0 (DSADC00ULTBR0)	0xA8E0 0A30	ULMTB[15:4] 0xA8E : AD conversion result upper limit 3.3V (=0xFFF/5*3.3V)
		LLMTB[15:4] 0xA3 : AD conversion result lower limit 0.2V (0xA3=0xFFF/5*0.2V)
Virtual Channel Pointer Control Register (DSADC00VCPTRR)	0x00	VCPTR[2:0] 0 : Start virtual channel is virtual channel 0

Table 2-13 ABFG Register Setting Example

Register Name	Setting Value	Function
Boundary Flag Control Register 0 (ABFGBFGCR0)	0x0100 00A0	ABFGBTGC 1 : When upper limit error, border flag is low. When lower limit error, border frag is high.
		ABFGCHS 0xA0 : Channel used for border fag generation is virtual channel of DS-ADC00.
Filter Counter Control Register 0 (ABFGCNTCR0)	0x1000 0101	ABFGENB 1 : Border flag enable
		ABFGNRMCNT 1 : If the signal is within the boundary for 1 count, it is determined as recovery.
		ABFGERRCNT 1 : If the signal is outside the boundary for 1 count, it is determined as recovery.

Table 2-14 Port Register Setting Example

Register Name	Setting Value	Function
Port Control Register (PCR37_0)	0x0000 0055	P37_0 Dual Use Mode 6 Input :TIM0_0
Port Control Register (PCR00_2)	0x0000 004D	P00_2 Dual Use Mode 14 Output : ATOM0_0

Table 2-15 shows the function list used in this operation example.

Table 2-15 Function List

Function Name	Overview
current_control_main	Main processing in this operation example. Perform calling of each function.
cmu_init	Perform initial setting of clock.
gtm_init	Perform GTM initial setting.
mcs0_init	Perform MCS0 initial setting.
atom0_init	Perform ATOM0 initial setting.
tim0_init	Perform TIM0 initial setting.
port_init	Perform port initial setting.
ds_adc_init	Perform DS-ADC initial setting.
abfg_init	Perform ABFG initial setting.

2.1.6 Operation Flow

Figure 2-5 shows the operation flow in this operation example.

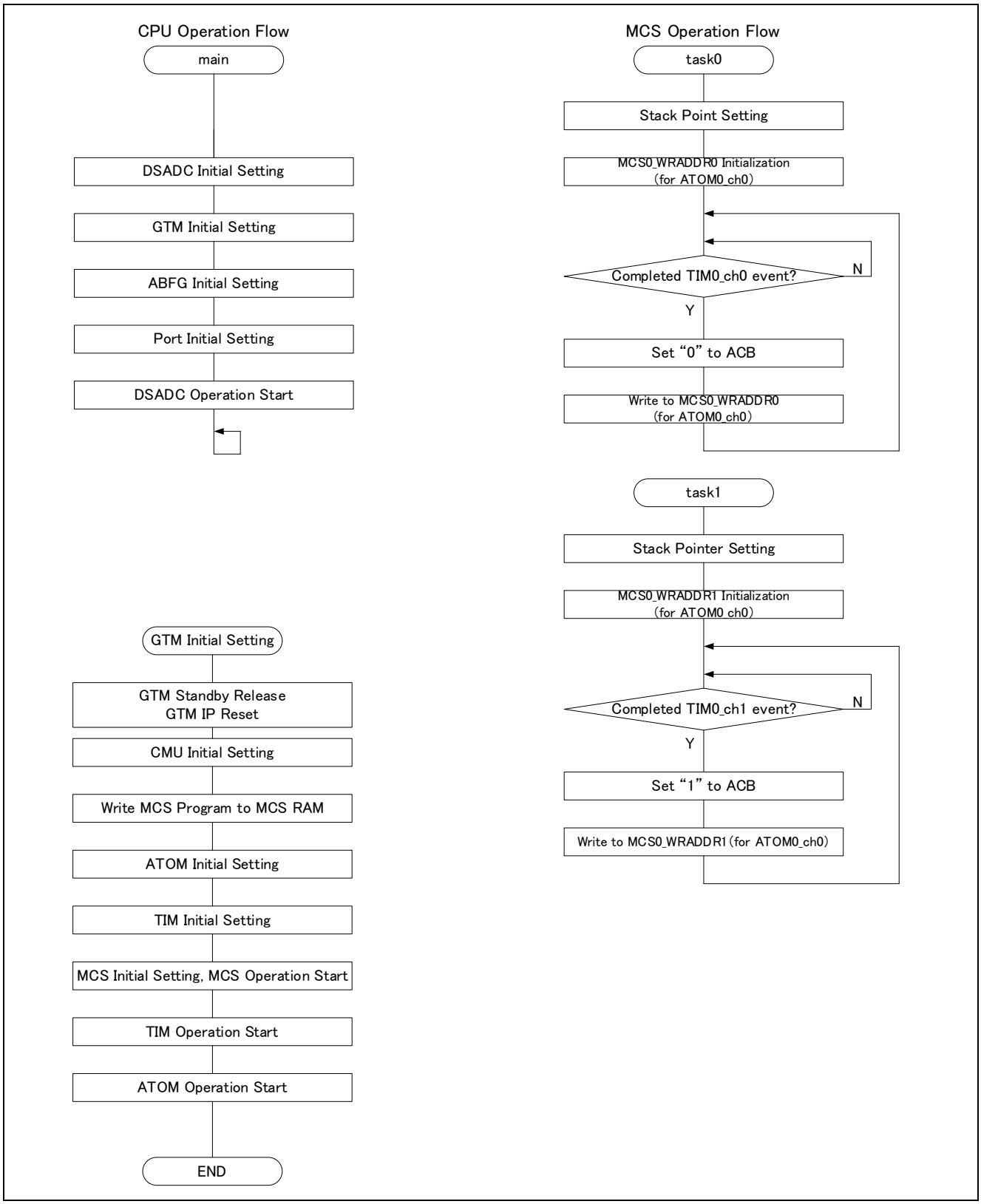

Figure 2-5 Operation Flow

2.2 Operation Example 2 (AEI Access)

2.2.1 Overview

Figure 2-6 shows the overview diagram in this operation example. In this operation example, the operation of “2.1 Operation Example 1 (ARU Access)” is changed to AEI access. AEI is the general purpose bus interface.

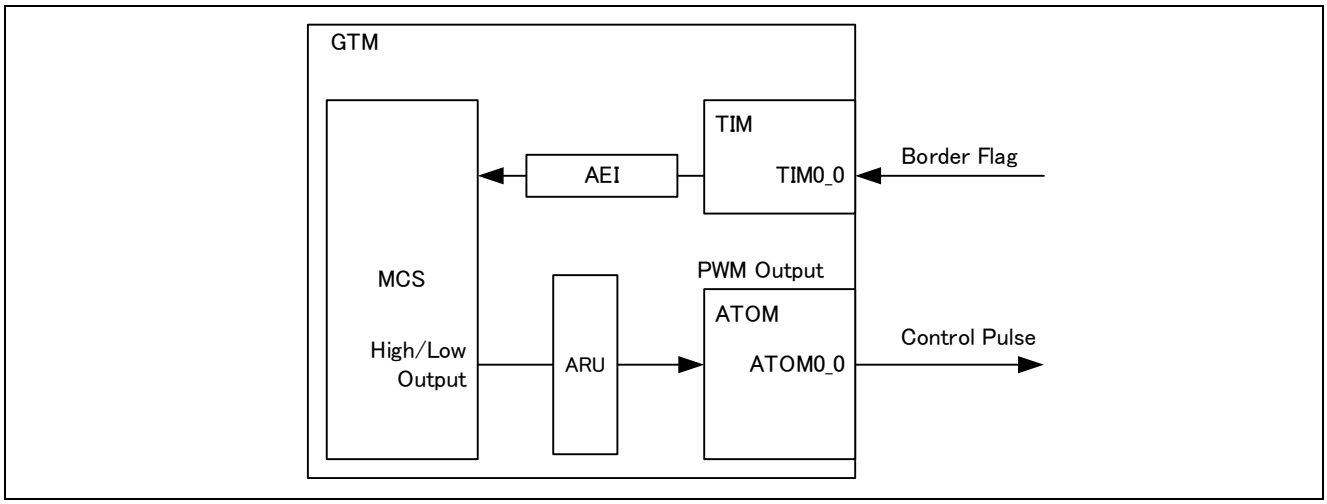

Figure 2-6 Overview Diagram

2.2.2 Acquire TIM Input Level by MCS

The following shows the overview of AEI access. (Please refer to GTM specification for the details of each direction.)

(1) Read of Register in GTM

TIM status register value (TIM0_INP_VAL) can be read by bus read direction (BRD).

TIM0 CH0 input level is TIM_IN0 bit value in TIM0_INP_VAL register.

2.2.3 Pulse Output by MCS

Same with Operation Example 1 (ARU Access).

2.2.4 Operation Condition of Use Function

The following shows the operation condition of use function in this operation example.

Table 2-16 Port Setting

Items	Contents
Use Pin (Input)	P37_0 : TIM0_0
Use Pin (Output)	P00_2 : ATOM0_0

Table 2-17 ATOM0 Setting

Items	Contents
TIM0 Operation Clock	100MHz
Use Channel	ATOM0 ch0
Operation Mode	Signal Output Mode Immediate (SOMI)
Signal Level	High/Low level output
ARU Input Stream	Enable
ARU Read Address	ATOM0 ch0 : 0x04F (MCS0_WRADDR0)

Table 2-18 MCS0 Setting

Items	Contents
MCS0Operation Clock	100MHz
Use Channel	MCS0 ch0
Scheduling Mode	Accelerated Scheduling

2.2.5 Software Explanation

The following shows the setting example of each register used in this operation example. Set OPBT8. CKSEL_GTM=0 (CLK_GTM=200MHz) for operating in this operation example

Table 2-19 STBC Register Setting Example

Register Name	Setting Value	Function
Module Standby Register for GTM (MSR_GTM)	0x0000 0000	Clock-supply to MS_GTM_0 0 : GTM
Module Standby Register for DS-ADC and Cyclic-ADC (MSR_DSADC_CADC)	0x0000 0000	Clock-supply to MS_DSADC_CADC_0 0 : DS-ADC & CADC COMMON
		Clock supply to MS_DSADC_CADC_2 0 : DS-ADC00,10
Module Standby Register for SAR-ADC (MSR_ADCK_ISO)	0x0000 00BF	Clock supply to MS_ADCK_ISO_6 0 : ABFG

Table 2-20 GTM Register Setting Example

Register Name	Setting Value	Function
GTM-IP Global control register (GTM_CTRL)	0x0000 0000	RF_PROT 0 : SW RST Function Enable (Protection release of GTM_RST register)
GTM-IP Global reset register (GTM_RST)	0x00000001	RST 1 : Initialization reset of all sub module

Table 2-21 MCS Register Setting Example

Register Name	Setting Value	Function
MCS0 Control and Status register (MCS0_CTRL_STAT)	0x0200 0000	SCD_MODE 0x0 : Accelerated Scheduling
MCS0 Channel 0 control register (MCS0_CH0_CTRL)	0x0000 0001	EN 1 : MCS0_ch0 enable

Table 2-22 ATOM Register Setting Example

Register Name	Setting Value	Function
ATOM Channel 0 control register (ATOM0_CH0_CTRL)	0x0000 0808	MODE[1 : 0] 0x0 : Signal Output Mode Immediate (SOMI)
		ARU_EN 1 : ARU Input stream enable
		SL 1 : High level output
ATOM Channel 0 ARU read address register (ATOM0_CH0_RDADDR)	0x01FE 004F	RDADDR0 0x04F : ARU read address is MCS0_WRADDR0
AGC Output enable status register (ATOM0_AGC_OUTEN_STAT)	0x0000 0002	OUTEN_STAT0 0x02 : CH0 output enable
AGC Enable/disable status Register (ATOM0_AGC_ENDIS_STAT)	0x0000 0002	ENDIS_STAT0 0x02 : CH0

Table 2-23 CMU Register Setting

Register Name	Setting Value	Function
CMU Clock enable Register (CMU_CLK_EN)	0x0000 0002	EN_CLK0 0x2 : CMU_CLK_RES0 enable

Table 2-24 DS-ADC Register Setting Example

Register Name	Setting Value	Function
AD Global Control Register (DSADCADGCR)	0x01	When UNSND 1 : UNSND=1 or CNVCLS=0, AD conversion result is unsigned. In other cases, with sign.
Unit Control Register (DSADC00UCR)	0x0400 0400	RESO0 1 : High impedance mode
		DFMT[3:0] 0x4 : Lower 4 bits mask of AD conversion result
		VCEP[2:0] 0x0 : End virtual channel is virtual channel 0.
Virtual Channel Register 0 (DSADC00VCR0)	0x0C10 4000	FSELEXTE=0, DSDFTYP[3:0]=0, ORT=0, TPVSL[2:0]=0x1 : Filter type is 2nd Stage Used Case 2 (F1b)
		GAIN[1:0] 0x0 : Input gain is x1
		VCULME 1 : AD conversion result upper limit exceeded notification enable
		VCLLME 1 : AD conversion result lower limit under notification enable
		VCULLMTBS[1:0] Upper/Lower limit check by 0x0:DSADCnULTBR0
		CNVCLS[1:0] 0x0 : Sigle-end input and Common voltage is =ADSVREFL
		GCTRL[3:0] 0 : Analog input channel is DSAN000P
Upper-Limit/Lower-Limit Table Register 0 (DSADC00ULTBR0)	0xA8E0 0A30	ULMTB[15:4] 0xA8E : AD conversion result upper limit 3.3V (=0xFFF/5*3.3V)
		LLMTB[15:4] 0xA3 : AD conversion result lower limit 0.2V (0xA3=0xFFF/5*0.2V)
Virtual Channel Pointer Control Register (DSADC00VCPTRR)	0x00	VCPTR[2:0] 0 : Start virtual channel is virtual channel 0

Table 2-25 ABFG Register Setting Example

Register Name	Setting Value	Function
Boundary Flag Control Register 0 (ABFGBFGCR0)	0x0100 00A0	ABFGBTGC 1 : When upper limit error, border flag is low. When lower limit error, border frag is high.
		ABFGCHS 0xA0 : Channel used for border fag generation is virtual channel of DS-ADC00.
Filter Counter Control Register 0 (ABFGCNTCR0)	0x1000 0101	ABFGENB 1 : Border flag enable
		ABFGNRMCNT 1 : If the signal is within the boundary for 1 count, it is determined as recovery.
		ABFGERRCNT 1 : If the signal is outside the boundary for 1 count, it is determined as recovery.

Table 2-26 Port Register Setting Example

Register Name	Setting Value	Function
Port Control Register (PCR37_0)	0x0000 0055	P37_0 Dual Use Mode 6 Input :TIM0_0
Port Control Register (PCR00_2)	0x0000 004D	P00_2 Dual Use Mode 14 Output : ATOM0_0

Table 2-27 shows the function list used in this operation example.

Table 2-27 Function List

Function Name	Overview
current_control_main	Main processing in this operation example. Perform calling of each function.
cmu_init	Perform initial setting of clock.
gtm_init	Perform GTM initial setting.
mcs0_init	Perform MCS0 initial setting.
atom0_init	Perform ATOM0 initial setting.
port_init	Perform port initial setting.
ds_adc_init	Perform DS-ADC initial setting.
abfg_init	Perform ABFG initial setting.

2.2.6 Operation Flow

Figure 2-7 shows the operation flow in this operation example.

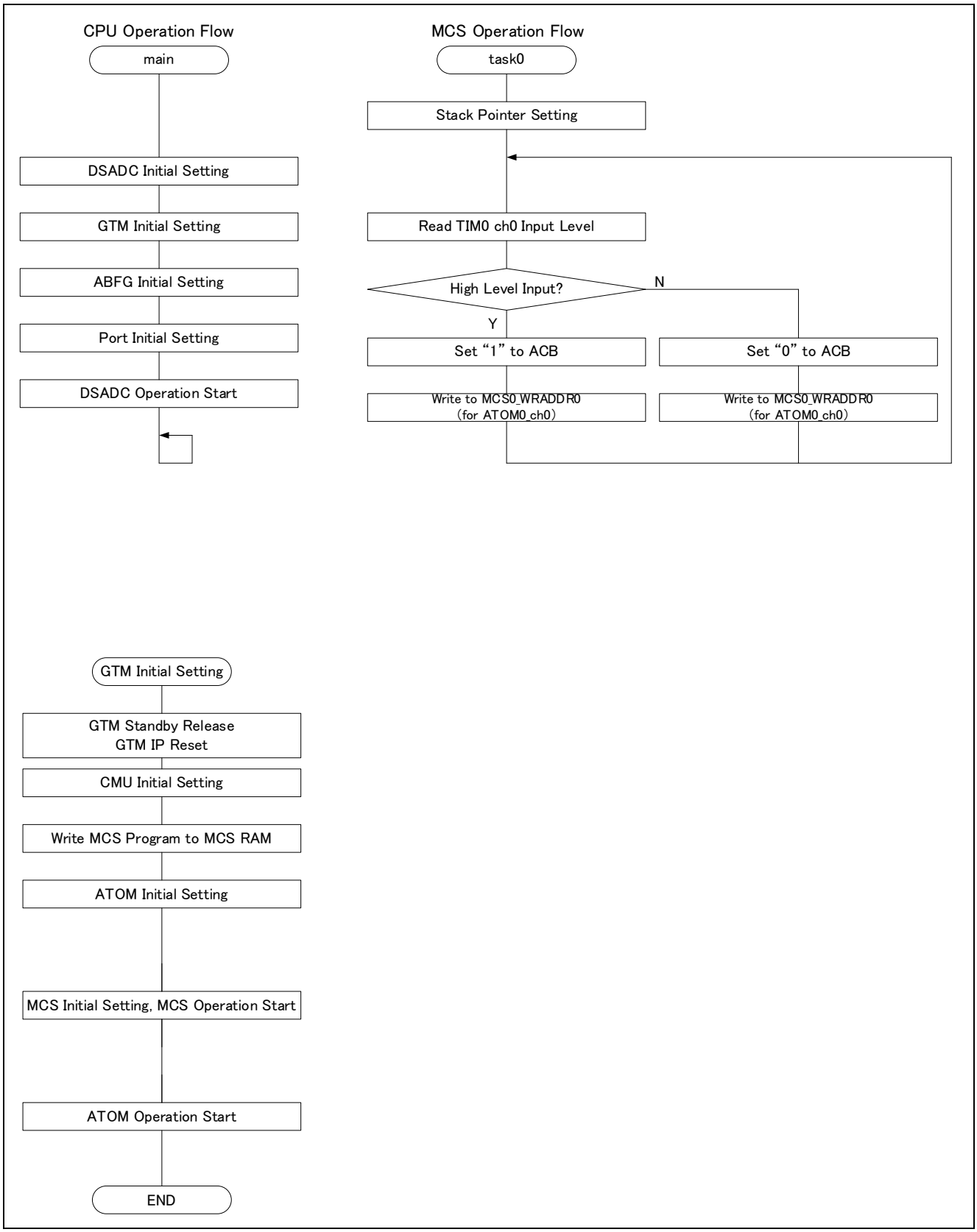

Figure 2-7 Operation Flow

2.3 Operation Example 3 (AD Data Register Access)

2.3.1 Overview

Figure 2-8 shows the overview diagram in this operation example. MCS acquires AD conversion result of DS-ADC by reading ADC_CH0_DATA register in GTM by AEI bus. Set High/Low output to ATOM via ARU by comparing AD conversion result of the acquired DS-ADC with the threshold, and output the pulse.

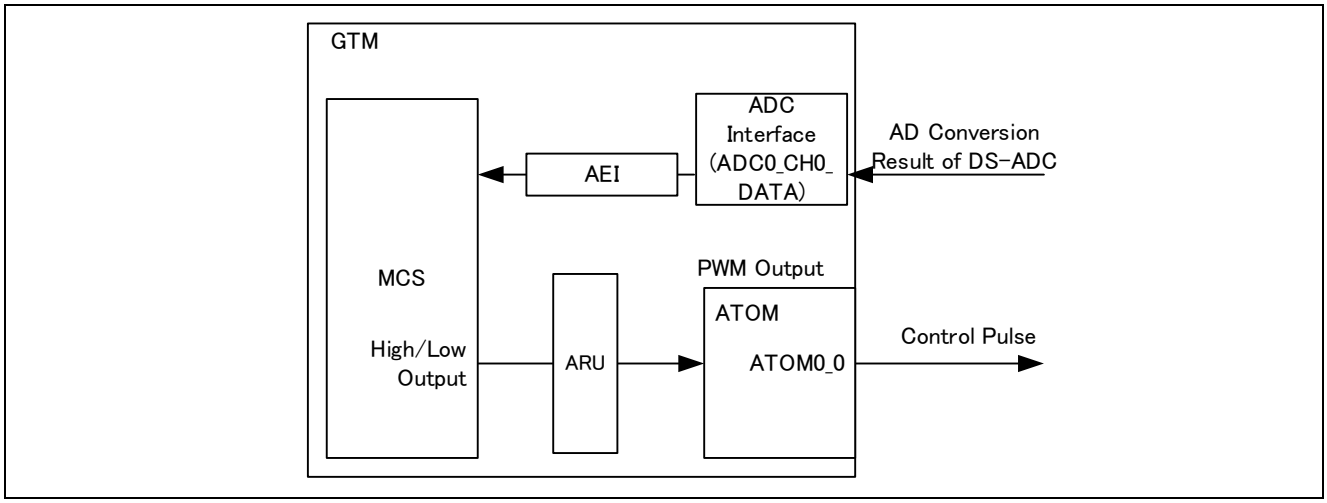

Figure 2-8 Overview Diagram

2.3.2 Acquire AD Conversion Result by MCS

The following shows the overview of AEI access. (Please refer to GTM specification for the details of each direction.)

(1) Read of Register outside GTM (DS-ADC)

ADC_CH0_DATA register value can be read by the bus read direction (BRD).

DS-ADC stores ADC_CH0_DATA register to AD conversion result.

2.3.3 Pulse Output by MCS

Same with Operation Example 1 (ARU Access).

2.3.4 Operation Condition of Use Function

The following shows the operation condition of use function in this operation example.

Table 2-28 Port Setting

Item	Contents
Use Pin (Output)	P00_2 ：ATOM0_0

Table 2-29 ATOM0 Setting

Items	Contents
ATOM0 Operation Clock	100MHz
Use Channel	ATOM0 ch0
Operation Mode	Signal Output Mode Immediate (SOMI)
Signal Mode	High/Low level output
ARU Input Stream	Enable
ARU Read Address	ATOM0 ch0：0x04F (MCS0_WRADDR0)

Table 2-30 MCS0 Setting

Items	Contents
MCS0Operation Clock	100MHz
Use Channel	MCS0 ch0
Scheduling Mode	Accelerated Scheduling

2.3.5 Software Explanation

The following shows the setting example of each register used in this operation example.

Set OPBT8. CKSEL_GTM=0 (CLK_GTM=200MHz) for operating in this operation example.

Table 2-31 STBC Register Setting Example

Register Name	Setting Value	Function
Module Standby Register for GTM (MSR_GTM)	0x0000 0000	Clock-supply to MS_GTM_0 0 : GTM
Module Standby Register for DS-ADC and Cyclic-ADC (MSR_DSADC_CADC)	0x0000 0000	Clock-supply to MS_DSADC_CADC_0 0 : DS-ADC & CADC COMMON
		Clock supply to MS_DSADC_CADC_2 0 : DS-ADC00,10

Table 2-32 GTM Register Setting Example

Register Name	Setting Value	Function
GTM-IP Global control register (GTM_CTRL)	0x0000 0000	RF_PROT 0 : SW RST Function Enable (Protection release of GTM_RST register)
GTM-IP Global reset register (GTM_RST)	0x00000001	RST 1 : Initialization reset of all sub module
GTM_ADCI_STRSEL	0x0000 0000	DFE0_CH00_SEL 0 : Store AD conversion result of ADCK, DSADC, CADC ADC_CH0_DATA to register.
GTM_ADCI_STRSEL1	0x0000 0000	emu30_tstwdcmp0 0 : Store selected data by DFE0_CH00_SEL to ADC_CH0_DATA register

Table 2-33 MCS Register Setting Example

Register Name	Setting Value	Function
MCS0 Control and Status register (MCS0_CTRL_STAT)	0x0200 0000	SCD_MODE 0x0 : Accelerated Scheduling
MCS0 Channel 0 control register (MCS0_CH0_CTRL)	0x0000 0001	EN 1 : MCS0_ch0 enable

Table 2-34 ATOM Register Setting Example

Register Name	Setting Value	Function
ATOM Channel 0 control register (ATOM0_CH0_CTRL)	0x0000 0808	MODE[1:0] 0x0 : Signal Output Mode Immediate (SOMI)
		ARU_EN 1 : ARU Input stream enable
		SL 1 : High level output
ATOM Channel 0 ARU read address register (ATOM0_CH0_RDADDR)	0x01FE 004F	RDADDR0 0x04F : ARU read address is MCS0_WRADDR0
AGC Output enable status register (ATOM0_AGC_OUTEN_STAT)	0x0000 0002	OUTEN_STAT0 0x02 : CH0 output enable
AGC Enable/disable status register (ATOM0_AGC_ENDIS_STAT)	0x0000 0002	ENDIS_STAT0 0x02 : CH0

Table 2-35 CMU Register Setting Example

Register Name	Setting Value	Function
CMU Clock enable register (CMU_CLK_EN)	0x0000 0002	EN_CLK0 0x2 : CMU_CLK_RES0 enable

Table 2-36 DS-ADC Register Setting Example

Register Name	Setting Value	Function
AD Global Control Register (DSADCADGCR)	0x00	UNSND 0 : AD conversion result is signed.
Unit Control Register (DSADC00UCR)	0x0400 0400	RESO0 1 : High impedance mode
		DFES 0 : When DFENT=1 and DFTAG=0, transfer AD conversion result to ADC_CH0_DATA of GTM
		DFMT[3:0] 0x4 : Lower 4 bits mask of AD conversion result
		VCEP[2:0] 0x0 : End virtual channel is virtual channel 0.
Virtual Channel Register 0 (DSADC00VCR0)	0x0010 5000	FSELEXTE=0, DSDFTYP[3:0]=0, ORT=0, TPVSL[2:0]=0x1 : Filter type is 2nd Stage Used Case 2 (F1b)
		GAIN[1:0] 0x0 : Input gain is x1
		VCULME 0 : AD conversion result upper limit exceeded notification enable
		VCLLME 0 : AD conversion result lower limit under notification enable
		DFENT 1 : Enable AD conversion result transfer to GTM
		DFTAG 0 :When DFENT=1 and DFES=0, transfer AD conversion result to ADC_CH0_DATA of GTM
		CNVCLS[1:0] 0x0 : Sigle-end input and Common voltage is =ADSVREFL
		GCTRL[3:0] 0 : Analog input channel is DSAN000P
Virtual Channel Pointer Control Register (DSADC00VCPTRR)	0x00	VCPTR[2:0] 0 : Start virtual channel is virtual channel 0

Table 2-37 Port Register Setting Value

Register Name	Setting Value	Function
Port Control Register (PCR00_2)	0x0000 004D	P00_2 Dual Use Mode 14 Output : ATOM0_0

Table 2-38 shows the function list used in this operation example.

Table 2-38 Function List

Function Name	Overview
current_control_main	Main processing in this operation example. Perform calling of each function.
cmu_init	Perform initial setting of clock.
gtm_init	Perform GTM initial setting.
mcs0_init	Perform MCS0 initial setting.
atom0_init	Perform ATOM0 initial setting.
port_init	Perform port initial setting.
ds_adc_init	Perform DS-ADC initial setting.

2.3.6 Operation Flow

Figure 2-9 shows the operation flow in this operation example.

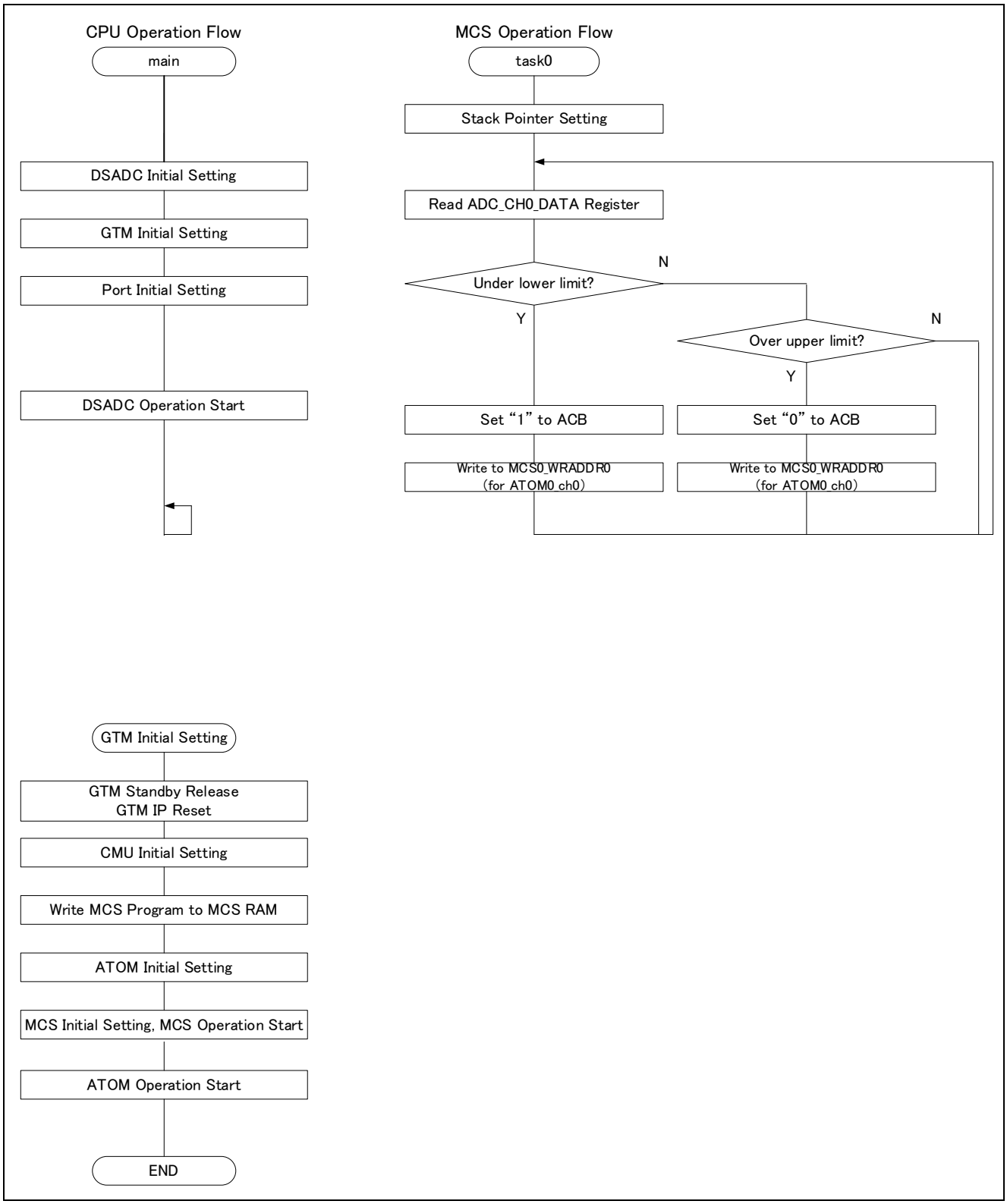

Figure 2-9 Operation Flow

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	2024.5.7	-	Initial edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.