RH850/U2B Group

R01AN6914EJ0100
Rev.1.00

Clock Monitor Application Note

Summary

This application note describes the basic clock monitor usage of RH850/U2Bx.

Aim of this document and software is to provide supplemental information for the function on RH850/U2B. It is not intended to implement in the design for mass production. There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Operation Confirmation Target Device

- RH850/U2B Group

Target Integrated Development Environment

CS+(from RENESAS Electronics)

Version : E8.07.00g6

Device file : DR7F702Z21EDBA.DVF

Reference Document

RH850/U2B User's Manual : Hardware

For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

・ RH850/U2B User's Manual (Rev.0.80): R01UH0923EJ0080

Items

1. Introduction

This application note describes the clock monitor usage and software creation example for RH850/U2Bx

1.1 Use Function

The following shows the hardware function of RH850/U2Bx used in this application note.

- Clock monitor (CLMA)
- Error control module (ECM)

1.2 Function Overview of Clock Monitor

The clock monitor detects the abnormal frequency of the monitoring target clock. When detection the abnormal frequency of the clock, it notifies the error to the error control module (ECM).

Table 1-1 shows the monitor clock and sampling clock list.

Table 1-1 Monitor Clock and Sampling Clock List

Unit Name	CLMATMON (Monitor Clock)	CLMATSMP (sampling Clock)
CLMA0	CLK_MOSC	CLK_HSIOSC / 400
CLMA1	CLK_WDT（CLMA1SEL=1）	CLK_LSIOSC / 2
	CLK_HSIOSC / 20（CLMA1SEL=0）	CLK_MOSC /32
CLMA2	CLK_LSIOSC	CLK_HSIOSC / 1600
CLMA3	CLK_LSB	CLK_MOSC /32
CLMA4	CLK_LSB	CLK_HSIOSC / 20
CLMA5	CLKC_SBUS / 2 (CLEAN) (CKSEL_GTM=0)	CLKC_LSB / 8 (CLEAN)
	CLKC_UHSB / 2 (CLEAN) (CKSEL_GTM=1)	
CLMA6	CLK_CPU (PE0) / 4	CLKC_LSB / 8 (CLEAN)
CLMA7	CLK_CPU (PE1) / 4	CLKC_LSB / 8 (CLEAN)
CLMA8	CLK_CPU (PE2) / 4	CLKC_LSB / 8 (CLEAN)
CLMA12	CLK_DFP / 4(DFP_DISABLE=0)	CLKC_LSB / 8 (CLEAN)
CLMA15	CLKC_LSB(CLEAN)	CLK_MOSC / 32

2. Clock Mpniotr Operation Example

2.1 Specification Overview

This section explains the usage of the clock monitor.

(1) CLMAn counts the rising of the clock (CLMATMON) monitored within 16 cycles of sampling clock (CLMATSMP), and compares with the threshold set the count value.

- CLMAnCMPL.CLMAnCMPL[11:0] Definition of lower limit value
- CLMAnCMPH.CLMAnCMPH[11:0] Definition of upper limit value

(2) When the frequency of CLMATMON is too low[*1], the counting is less than CLMAnCMPL.CLMAnCMPL.

(3) When the frequency of CLMATMON is too high[*1], the counting is more than CLMAnCMPL.CLMAnCMPL.

(4) In case (2) or (3), it will be frequency error, and the error is notified to ECM.

[Note 1] When the monitored clock is stopped, the error may not be detected.

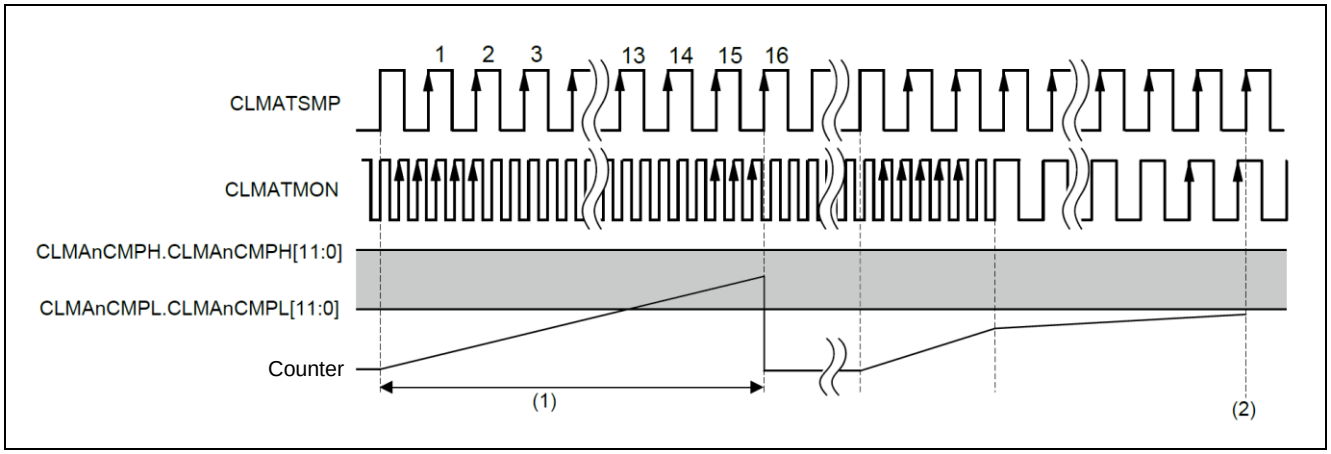

Figure 2-1 Example : fCLMATMON is lower than lower limit

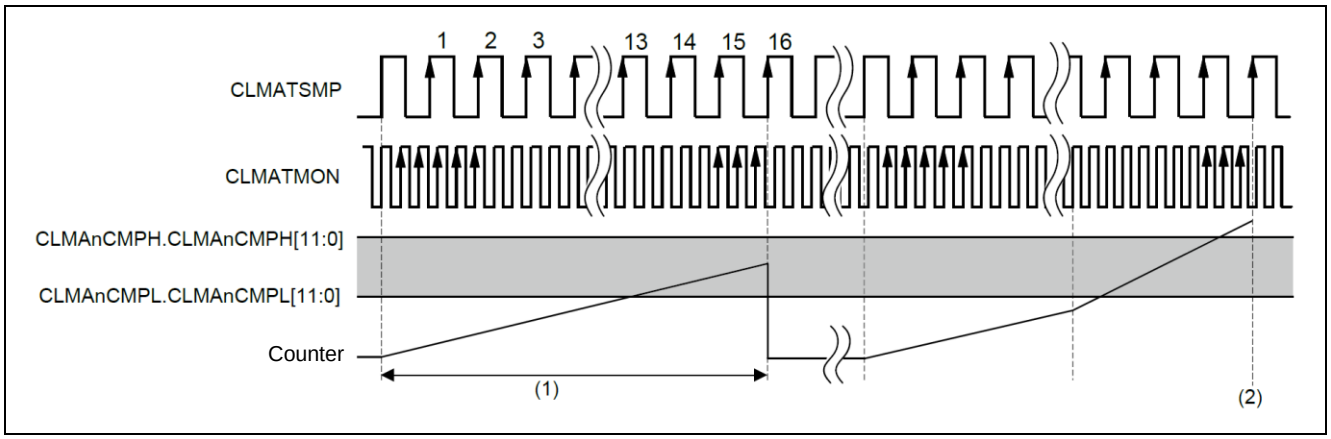

Figure 2-2 Example : fCLMATMON is higher than higher limit

2.2 Use Function

The following shows the hardware function used in this operation example.

- Clock monitor (CLMA0 to 3, CLMA5, CLMA6, CLMA12, CLMA15)
- Error control module (ECM)

2.3 Explanation for Operation Example

When occurring the CLMA abnormal frequency, the ECM error interrupt is issued. Table 2-1 shows the monitor clock and sampling clock list in this operation example.

Table 2-1 Monitor Clock and Sampling Clock List (in this operation example)

	CLMATMON			CLMATSMP		
	Clock	Frequency	Error	Clock	Frequency	Error
CLMA0	CLK_MOSC	20MHz	±0.1%	CLK_HSIOSC / 400	0.5 MHz	±5%
CLMA1	CLK_WDT HS IntOSC /640	0.3125 MHz	±5%	CLK_LSIOSC / 2	0.12 MHz	±10%
CLMA2	CLK_LSIOSC	0.24 MHz	±10%	CLK_HSIOSC / 1600	0.125 MHz	±0.1%
CLMA3	CLK_LSB	40 MHz	±0.1%	CLK_MOSC / 32	0.625 MHz	±5%
CLMA5	CLKC_SBUS/2	100 MHz	±0.1%	CLKC_LSB / 8	5 MHz	±0%
CLMA6	CLK_CPU/4	100 MHz	±0.1%	CLKC_LSB / 8	5 MHz	±0.1%
CLMA12	CLK_DFP / 4	100 MHz	±0.1%	CLKC_LSB / 8	5 MHz	±0.1%
CLMA15	CLKC_LSB (CLEAN)	40 MHz	±0.1%	CLK_MOSC / 32	0.625 MHz	±0.1%

2.3.1 Threshold Calculation

For the compare register CLMAnCMPL and CLMAnCMPH, specify the minimum/maximum value of CLMATMON clock cycle that that occur within 16 cycles of the sampling clock CLMATSMP that sets the normal range for CLMATMON. The number of CLMATMON clock cycle that occur within 16 cycles of CLMATSMP is indicated as N.

$$N = (f\ CLMATMON / f\ CLMATSMP) \times 16$$

Considering the allowable frequency deviation of CLMATMON and CLMATSMP, the threshold is calculated by the following formulas.

Note that the lower threshold value is rounded down to the decimal point, and the upper threshold value is rounded up.

$$\text{Lower limit threshold (Nmin)} = (f\ CLMATMON(min) / f\ CLMATSMP(max)) \times 16 - 1$$

$$\text{Highr limit threshold (Nmax)} = (f\ CLMATMON(max) / f\ CLMATSMP(min)) \times 16 + 1$$

2.3.2 Option Byte Setting

Table 2-2 to Table 2-4 show the selected option byte setting in this operation example.

Table 2-2 Contents of Option Byte (OPBT8)

Bit Position	Bit Name	Function
24	ATU_GTM_SEL	ATU, GTM selection 0 : ATU disable, GTM enable
22	CLMA1SEL	CLMA1 clock monitor target selection 1 : CLK_WDT
3	CKSEL_SSCG1	DFP clock source selection 1 : SSCG1

Table 2-3 Contents of Option Byte (OPBT36)

Bit Position	Bit Name	Function
23	SSCG1_DIS	SSCG1 disable signal 0 : SSCG1 enable

Table 2-4 Contents of Option Byte (OPBT37)

Bit Position	Bit Name	Function
31	DFP_DCLS_DIS_SYS	SYS disable 0 : Enable
30	DFP_DCLS_DIS_VLM	VLM disable 0 : Enable
29	DFP_DCLS_DIS_VPU	VPU disable 0 : Enable
28	DFP_DCLS_DIS_ROC	ROC disable 0 : Enable
27	DFP_DCLS_DIS_SPU	SPU disable 0 : Enable
26	DFP_DCLS_DIS_CCU	CCU disable 0 : Enable

2.4 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-5 Module List

Module Name	Label Name	Function
Main routine	main_pe0	Perform various setting and application startup.
ECM initialization routine	ecm_init	Perform initial setting for error control module.
Interrupt initialization routine	intc_init	Perform initial setting for interrupt function.
Clock monitor initialization routine	clk_mon_init	Perform initial setting of clock monitor.
Clock monitor operation enable	clk_mon_start	Set clock monitor to operation enable.
Interrupt processing routine	ecm_int	Interrupt function. When error is issued, the error status is stored to variable.

- Register Setting

The following shows the register setting for each function in this operation example.

Table 2-6 Register Setting of Clock Monitor

Register Name	Setting Value	Function
CLMAKCPROT	0xA5A5A501	Enable writing access to protected register.
	0xA5A5A500	Disable writing access to protected register.
CLMA0CMPL	0x025F	CLMA0 lower limit threshold
CLMA0CMPH	0x02A4	CLMA0 upper limit threshold
CLMA1CMPL	0x0022	CLMA1 lower limit threshold
CLMA1CMPH	0x0032	CLMA1 upper limit threshold
CLMA2CMPL	0x001A	CLMA2 lower limit threshold
CLMA2CMPH	0x0023	CLMA2 upper limit threshold
CLMA3CMPL	0x03CD	CLMA3 lower limit threshold
CLMA3CMPH	0x0438	CLMA3 upper limit threshold
CLMA5CMPL	0x013E	CLMA5 lower limit threshold
CLMA5CMPH	0x0142	CLMA5 upper limit threshold
CLMA6CMPL	0x013E	CLMA6 lower limit threshold
CLMA6CMPH	0x0142	CLMA6 upper limit threshold
CLMA12CMPL	0x013E	CLMA12 lower limit threshold
CLMA12CMPH	0x0142	CLMA12 upper limit threshold
CLMA15CMPL	0x03FC	CLMA15 lower limit threshold
CLMA15CMPH	0x0404	CLMA15 upper limit threshold

Register Name	Setting Value	Function
CLMABCE	0x00	Backup clock function disable
CLMA0CTL	0x01	CLMA0 operation enabla
CLMA1CTL	0x01	CLMA1 operation enabla
CLMA2CTL	0x01	CLMA2 operation enabla
CLMA3CTL	0x01	CLMA3 operation enabla
CLMA5CTL	0x01	CLMA5 operation enabla
CLMA6CTL	0x01	CLMA6 operation enabla
CLMA12CTL	0x01	CLMA12 operation enabla
CLMA15CTL	0x01	CLMA15 operation enabla

Table 2-7 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD8	0x00000000	Bind interrupt to PE0 (CPU0).
EIC8	0x0040	Table reference/Priority level 0

Table 2-8 ECM Register Setting

Register Name	Setting Value	Function
ECMKCPROT	0xA5A5A501	Enable writing access to protected register.
	0xA5A5A500	Disable writing access to protected register.
ECMMECLR	0x00000001	Set ERROROUT pin to high level output.
ECMCECLR	0x00000001	Set ERROROUT pin to high level output.
ECMINCFG0_2	0x00002F80	Enable CLMA0 to CLMA5 and CLMA15 error interrupt generation.
ECMINCFG0_6	0x00400000	Enable CLMA 12 error interrupt generation.
ECMINCFG0_7	0x00000020	Enable CLMA 6 error interrupt generation.

- Operation Flow

The following shows the flowchart in this operation example.

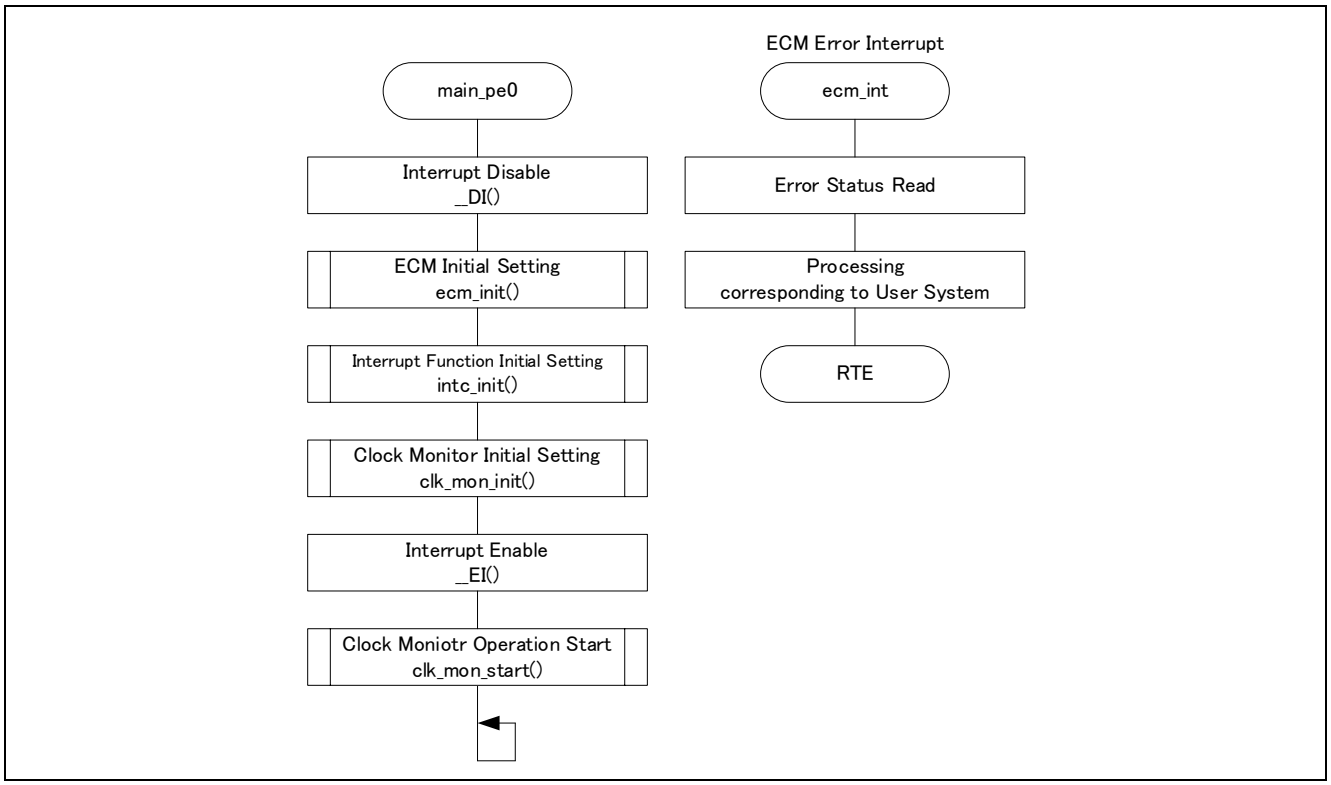

Figure 2-3 Flowchart

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024.03.27	-	Initial edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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