RH850/U2B Group

R01AN6328EJ0100
Rev.1.00

CAN Receive Procedure Application Note

Summary

This document applies to the RH850 series. This document and the program are intended to promote understanding of the installed functions in the RH850/U2B, and it is not intended for mass production. design. It also does not reflect the latest manuals, errata, technical updates, and development environment updates. When using the corresponding function, please treat this program as a reference, and use the latest documents and development environment at your own risk. RSCFDnCFD is omitted from the register name in the text.

Target Device

- • RH850/U2Bx
-

Contents

1. Receive Function

The functions that can be used when receiving CAN messages are shown below. For details on each process, refer to the following chapters.

- ・Receive using the receive buffer
- ・Receive using the receive FIFO buffer
- ・Receive using the transmit / receive FIFO buffer

2. Receive Using Receive Buffers

Receive buffer q shared by all channels is available. Since the message stored in the receive buffer with the same number is overwritten, the latest received data can be read.

If it is received in the receive buffer, no interrupt is generated.

When the process of storing the received message in the receive buffer starts, the receive buffer q becomes "new message" (the RMNSq flag in the RMNDt register becomes "1"). Received data information can be read from the RMIDq register, RMPTRq register, and RMDFbq register (b = 0 to 15).

For the configuration settings for using the receive buffer, refer to "CAN Configuration Application Note".

Figure 2-1 shows the operation of the receive buffer.

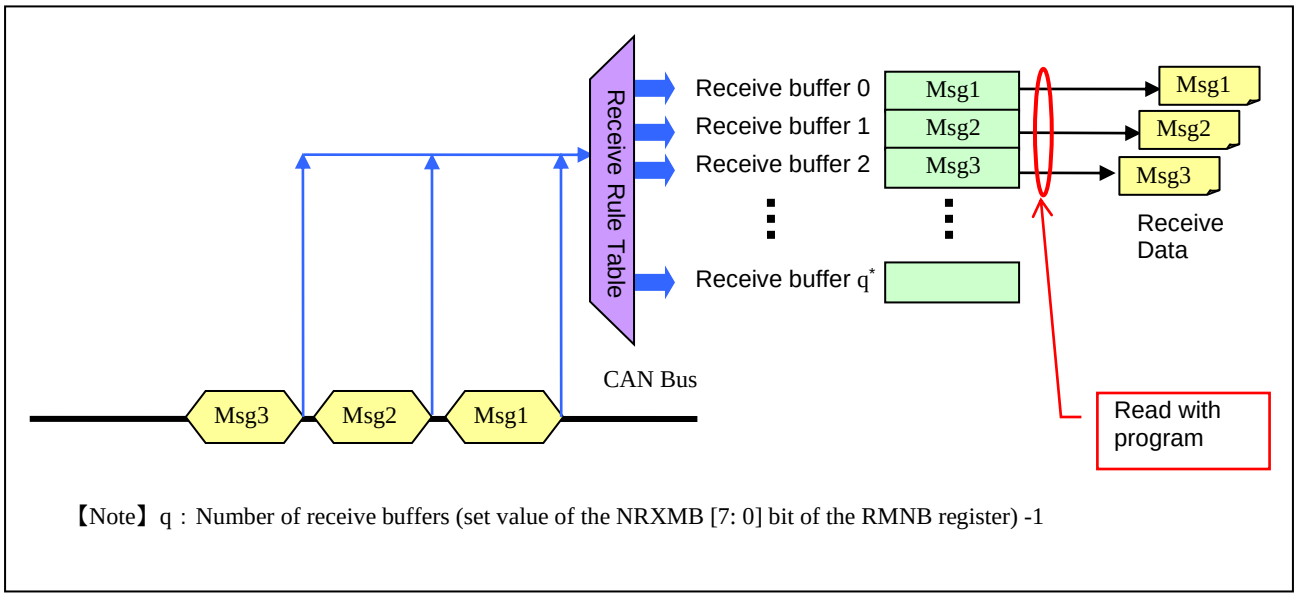
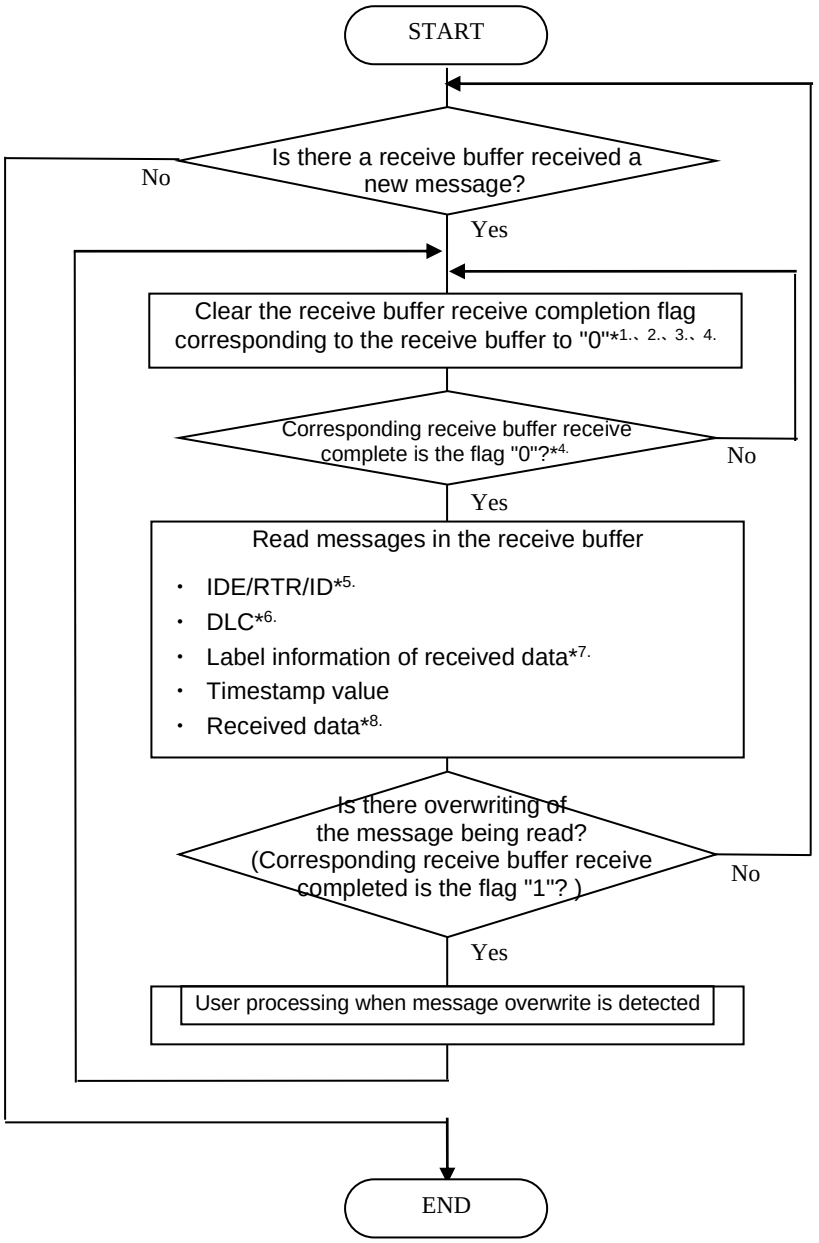


Figure 2-1 Receive Buffer Operation

2.1 Receive Buffer Read Procedure

Figure 2-2 shows the procedure for reading the receive buffer.



【Note】 1. Write “0” for the RMNSu flag in the RMNDt register in global operation mode or global test mode.

2. To set the RMNSu flag to “0”, write “0” with the program.
3. To write "0" in the RMNSu flag, use the store instruction to write "0" in the bit you want to set to "0" and "1" in the other bits.
4. The RMNSu flag cannot be set to “0” while the message is being stored. The time to store a message depends on the size of the payload stored in the receive buffer.
5. For a standard ID, read b10 to b0 of the ID (the RMID [15: 0] bit of the RMIDL register). “0” can be read for b15 to b11.

6. If DLC replacement is enabled after filtering by the reception rule (the DCE bit of the GCFGL register is “1”, DRE bit is “1”), the received message matches the DLC set value in the reception rule table (t:he GAFLDLC[3:0] bit of the GAFLPHj register) that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
7. After filtering by the receive rule, the set value of the label of the receive rule table (the GAFLPTR [15: 0] bit of the GAFLPHj register) that matches the received message is stored.
8. If the DLC of the received message (the value of the RMDLC [3: 0] bit of the RMPTR register) is less than the payload storage size of the receive buffer, “H'00” can be read for the data byte (RMDFq register) for which no data is set.
9. CANグローバルRAMウィンドウ1（GRWCRレジスタのRPAGEビットが"1"）の場合、受信バッファ（RMIDLn,Hnレジスタ、RMTSnレジスタ、RMPTRnレジスタ、RMDF0nレジスタ~RMDF3nレジスタ）を読めます。

Figure 2-2 Receive Buffer Read Procedure

3. Receive Using Receive FIFO Buffers

There are two receive FIFO buffers shared by all channels. Messages can be stored in each receive FIFO buffer for the number of buffers.

When a received message is stored in the receive FIFO buffer, the value of the corresponding message count display counter (the RFMC [7: 0] bit of the RFSTS register) is incremented.

Received messages can be read from the RFIDLm,Hx register, RFTSm register, RFPTR register, RFFDSTS register, and RFDFp register. The receive FIFO buffer can be read from the oldest message.

When the value of the message count display counter matches the buffer value of the FIFO buffer (the value set by the RFCCx register RFDC [2: 0] bit), the receive FIFO buffer becomes full (the RFFLL flag in the RFSTSx register is “1”). When all messages are read from the receive FIFO buffer, the receive FIFO buffer becomes empty (the RFEMP flag in the RFSTSx register is “1”).

Refer to the CAN Configuration Application Note for configuration settings to use the receive FIFO buffer.

Figure 3-1 shows the operation of the receive FIFO buffer.

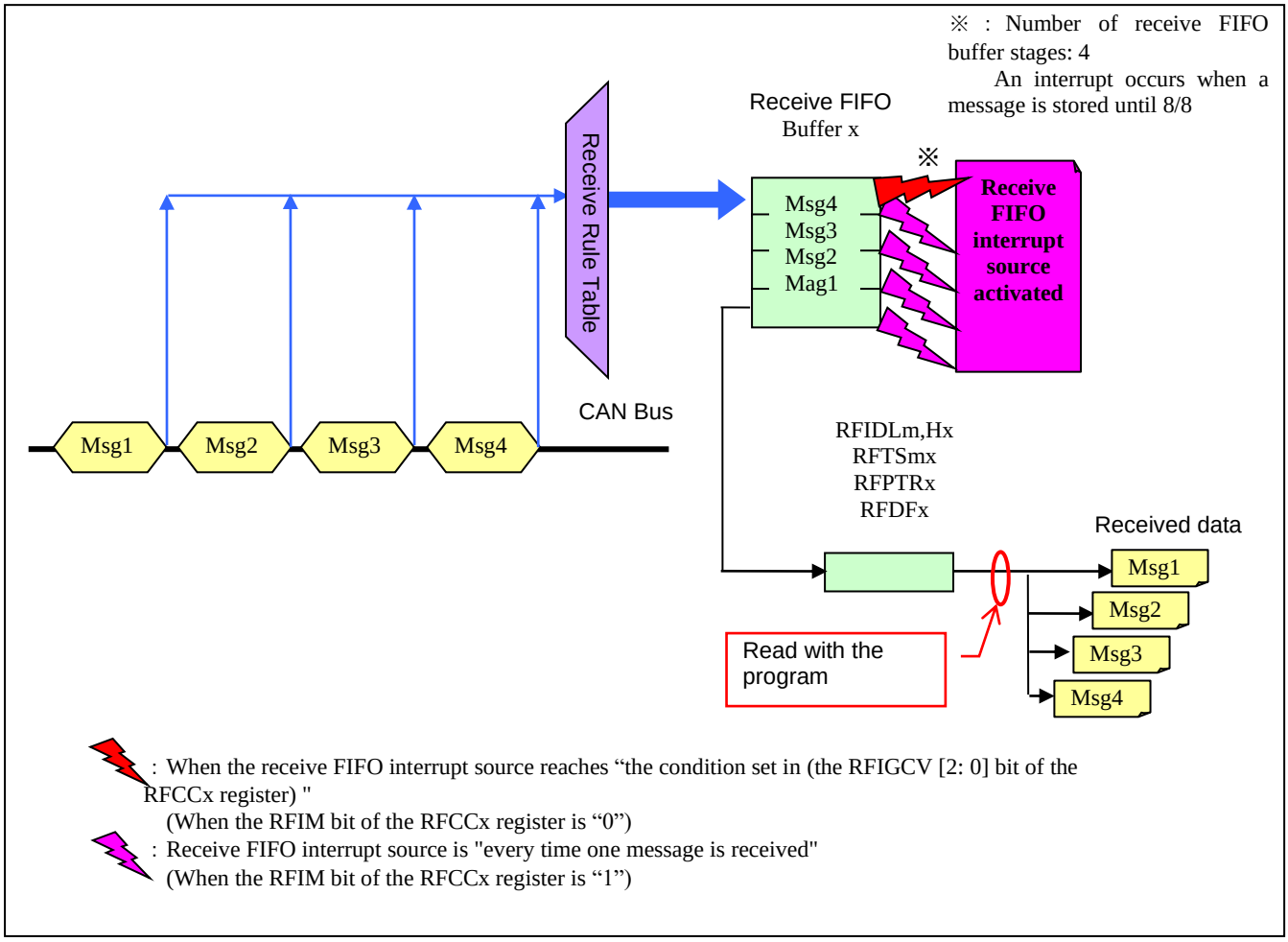
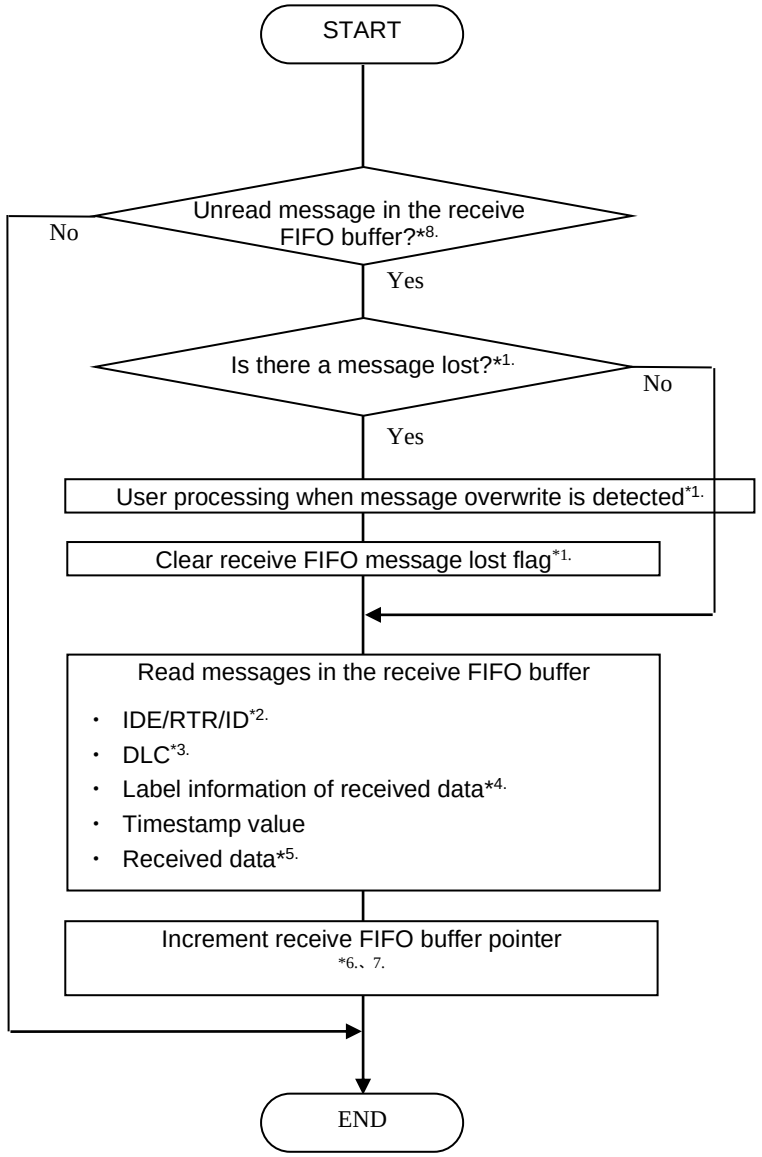


図 3-1 Receive FIFO Buffer Operation

3.1 Receive FIFO Buffer Read Procedure

Figure 3-2 shows the procedure for reading the receive FIFO buffer, and Figure 3-3 and Figure 3-4 show the procedure for enabling and prohibiting the use of the receive FIFO buffer.

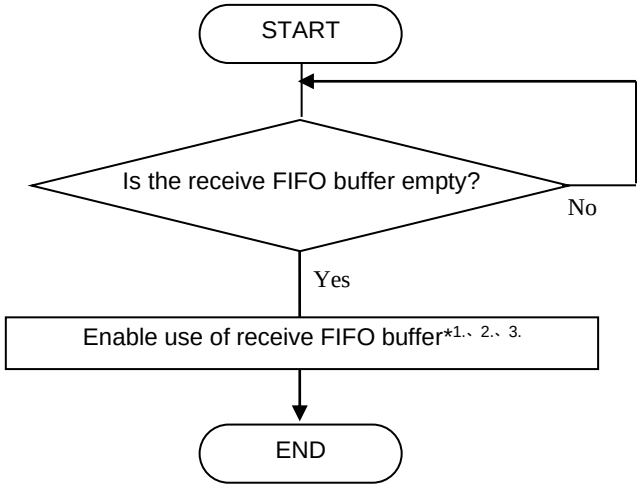


【Note】 1. If the FIFO message lost interrupt is enabled, execute it in the global error interrupt processing.

2. For standard ID, read b10-b0 of ID (the RFID [28: 0] bit of the RFIDL register). “0” can be read for b15-b11 and RFID [12:0] of the RFIDHm register.
3. If DLC replacement is enabled after filtering by the reception rule (the DCE bit of the GCFGL register is “1”, DRE bit is “1”), the DLC set value in the reception rule table (the GAFLDLC[3:0] bit of the GAFLPHj register) that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
4. After filtering by the reception rule, the set value of the receive rule table label (the GAFLPTR [11: 0] bit of GAFLPHj) that matches the received message is stored.

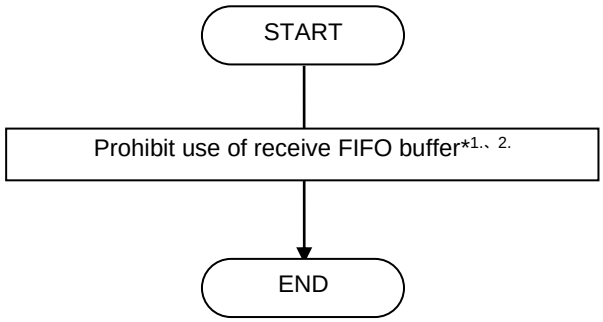
5. If the DLC of the received message (value of the RFDLC [3: 0] bit of the RFPTR register) is less than the payload storage size of the receive FIFO buffer, "H'00" can be read for the data byte (RFDFp register) for which no data is set.
6. After reading the messages in the receive FIFO buffer (RFIDLm,H register, RFTSm register, RFPTR register, RFDFp register), increment the pointer (write "H'FF" to the RFPC [7: 0] bit of the RFPCTRx register).
7. Increment the pointer when the receive FIFO buffer is used (the RFE bit of the RFCCx register is “1”) and there are unread messages in the receive FIFO buffer (the RFEMP flag in the RFSTSx register is “0”).
8. When reading all the unread messages in the receive FIFO buffer, use a loop statement or the like to read until the buffer is empty.
9. CANグローバルRAMウィンドウ1（GRWCRレジスタのRPAGEビットが"1"）の場合、受信バッファ（RFIDLm,Hmレジスタ、RFTSmレジスタ、RFPTRmレジスタ、RFDF0mレジスタ~RFDF3mレジスタ）を読めます。

Figure 3-2 Receive FIFO Buffer Read Procedure (no interrupt used)



【Note】 1. Rewrite to enable/disable the receive FIFO buffer (the RFE bit of the RFCCx register) in the global operation mode or global test mode.
2. Make the configuration settings for using the receive FIFO buffer, and then enable the use of the receive FIFO buffer (the RFE bit is "1").
3. If the number of receive FIFO buffers is set to “0” (“B’000” in the RFDC [2: 0] bit of the RFCCx register), do not allow the receive FIFO buffer to be used.

Figure 3-3 Procedure to Enable Receive FIFO Buffer Use



【Note】 1. Rewrite to enable/disable the receive FIFO buffer (the RFE bit of the RFCCx register) in the global operation mode or global test mode.
2. Even if the use of the receive FIFO buffer is prohibited (the RFE bit is “0”) while an interrupt request is generated (the RFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Figure 3-4 Procedure to Prohibit Receive FIFO Buffer Use

3.2 Receive FIFO Interrupt Processing

3.2.1 Receive FIFO Interrupt Processing

If the receive FIFO interrupt is enabled, the receive FIFO interrupt is generated when the condition selected in the RFIM bit setting of the RFCCx register is satisfied.

Even if the use of the receive FIFO buffer is prohibited (RFE bit is “0”) while an interrupt request is generated (the RFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Whether to enable or disable receive FIFO interrupts can be set for each receive FIFO buffer using the RFIE bit of the RFCCx register. The sources of receive FIFO interrupts are shown below.

A receive FIFO interrupt request is generated when the condition set by the RFIGCV [2: 0] bit of the RFCCx register is reached (the RFIM bit of the RFCCx register is "0").

RFIGCV[2:0] bit settings

- When a message is stored up to 1/8 in the receive FIFO buffer*1
- When a message is stored up to 2/8 in the receive FIFO buffer
- When a message is stored up to 3/8 in the receive FIFO buffer*1
- When a message is stored up to 4/8 in the receive FIFO buffer
- When a message is stored up to 5/8 in the receive FIFO buffer*1
- When a message is stored up to 6/8 in the receive FIFO buffer
- When a message is stored up to 7/8 in the receive FIFO buffer*1
- When the receive FIFO buffer is full

— Receive FIFO interrupt request occurs every time message reception is completed (the RFIM bit of RFCCx register is “1”)

【Note】 1. Do not set if the number of receive FIFO buffers is set to 4 messages (the RFDC [2: 0] bit of the RFCCx register is set to "B'001").

3.2.2 Receive FIFO Full Interrupt Processing

If the FIFO full interrupt is enabled (RFFIE bit of RFCCx register is “1”), the receive full interrupt is occurred when the receive FIFO buffer is full.

Even if the use of the receive FIFO buffer is prohibited (RFE bit is “0”) while an interrupt request is generated (the RFFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFFIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

3.2.3 Global Error Interrupt Processing

If the FIFO message lost interrupt is enabled, a global error interrupt is generated when a message lost in the receive FIFO buffer is detected. Whether to enable or disable the interrupt can be set in common for the entire module with the MEIE bit of the GCTR register.

4. Receive Using Transmit/Receive FIFO Buffer

The transmit/receive FIFO buffer can be used in receive mode or transmit mode (only receive mode is described in this chapter).

There is a transmit/receive FIFO buffers per channel dedicated to each channel. The transmit/receive FIFO buffer set to receive mode can store as many messages as the number of buffers, just like the receive FIFO buffer.

When a received message is stored in the transmit/receive FIFO buffer set to receive mode, the value of the corresponding message count display counter (the CFMC [7: 0] bit of the CFSTSk register) is incremented.

Received messages can be read from the CFIDLk,H register, CFTSk register, CFPTR register, CFFDCTST register, and CFDFp register. The transmit/receive FIFO buffer can be read from the oldest message.

When the value of the message count display counter matches the buffer value of the transmit/receive FIFO buffer (the value set by the CFDC [2: 0] bit of the CFCCk register), the transmit/receive FIFO buffer becomes full (the CFFLL flag in the CFSTsk register is “1”).

When all messages are read from the transmit/receive FIFO buffer, the transmit/receive FIFO buffer becomes empty (the CFEMP flag in the CFSTSk register is “1”).

For the configuration settings for using the transmit/receive FIFO buffer, refer to "CAN Configuration Application Note".

Figure 4-1 shows the receive operation of the transmit/receive FIFO buffer.

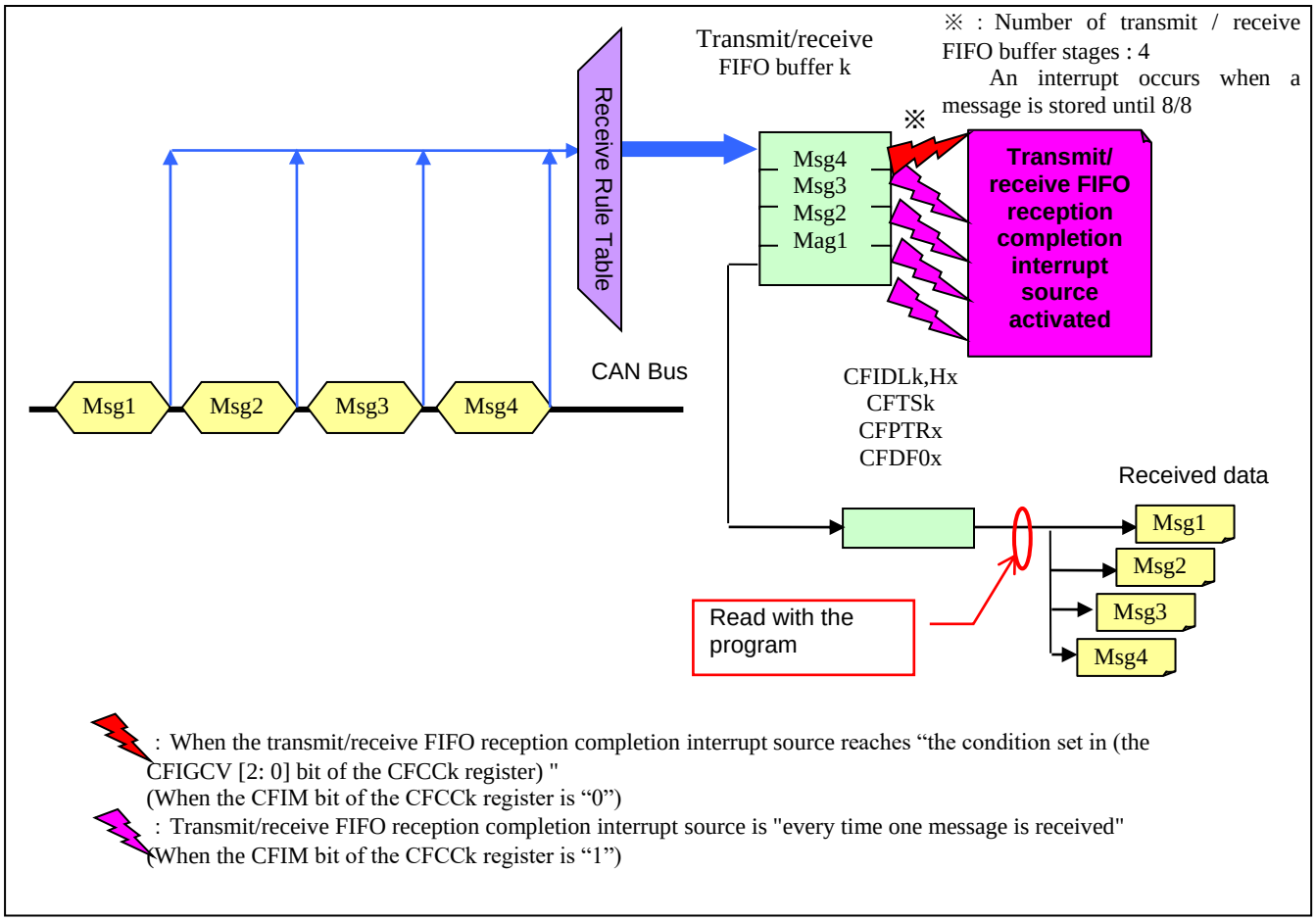
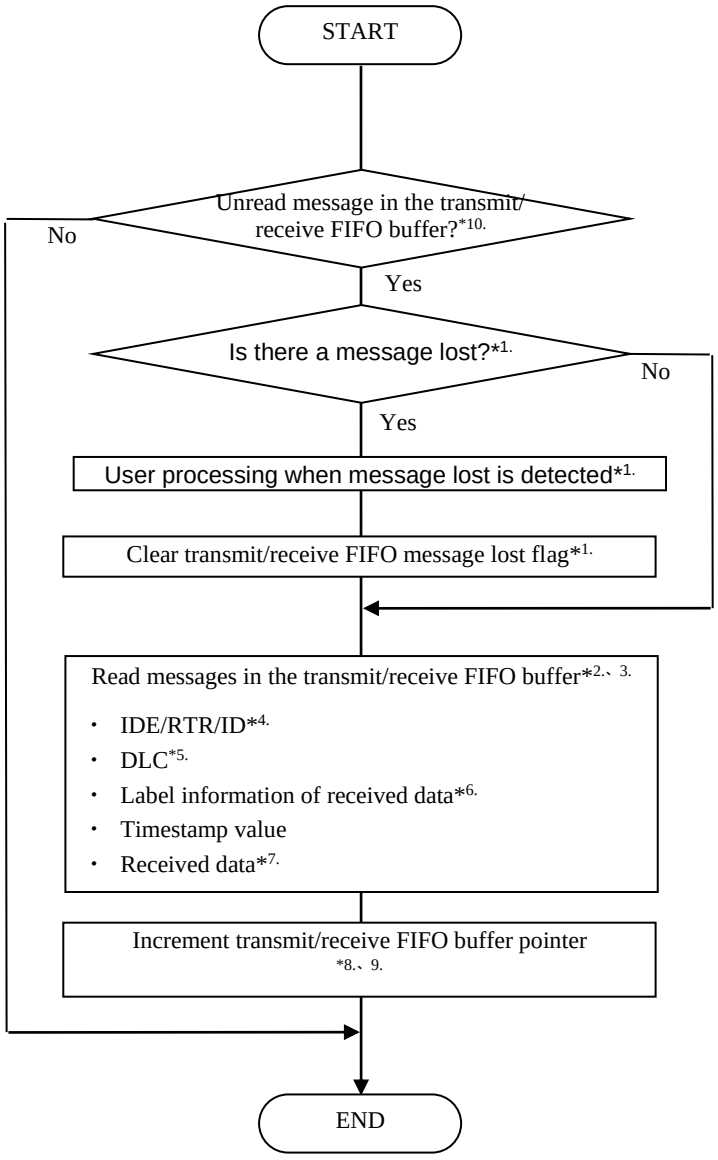


Figure 4-1 Transmit/receive FIFO Buffer Operation (Receive mode)

4.1 Transmit/receive FIFO Buffer Read Procedure

Figure 4-2 shows the procedure for reading the transmit/receive FIFO buffer, and Figure 4-3 and Figure 4-4 show the procedure for enabling and prohibiting the use of the transmit/receive FIFO buffer.

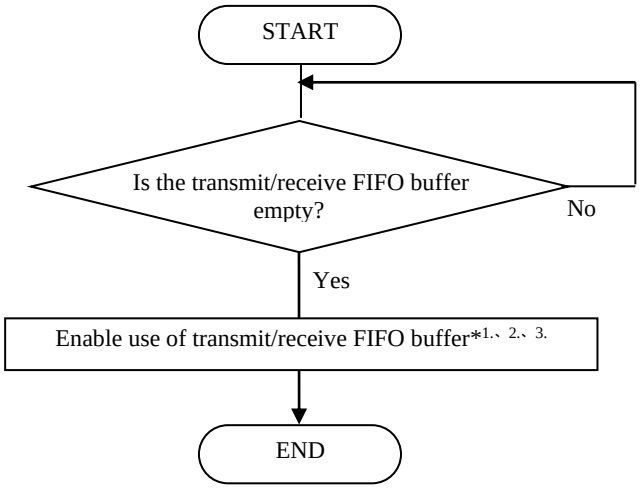


【Note】 1. If the FIFO message lost interrupt is enabled, execute it in the global error interrupt processing.

2. The transmit/receive FIFO buffer (CFIDLk,H register, CFTSk register, CFPTR register, CFDF to CFDF3k register) can be read only in the receive mode (CFM [1:0] bis of the CFCCHk register is “B’00”) and the CAN global RAM window 1 (RPAGE bit of the GRWCR register is “1”).
3. In the receive mode, enabling or prohibiting the storage of transmission history data (the THLEN bit of CFIDHk register) is invalid.
4. For standard ID, read b10 to b0 of ID (the CFID [15:0] bit of the CFIDLk register). “0” can be read for b15 to b11 and the CFID[12:0] of the CFIDHk register.

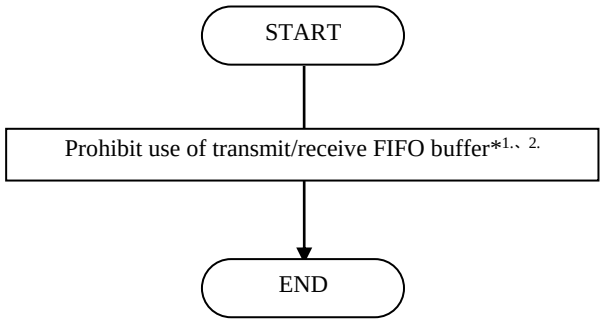
5. If DLC replacement is enabled after filtering by the reception rule (the DCE bit of the GCFGL register is “1”, DRE bit is “1”), the DLC set value in the reception rule table (the GAFLDLC bit of the GAFLPHj register) that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
6. After filtering by the reception rule, the set value of the reception rule table label (GAFLPTR [15:0] bit of GAFLPHj register) that matches the received message is stored.
7. If the DLC of the received message (value of the CFDLC [3: 0] bit of the CFPTRk register) is less than the payload storage size of the transmit/receive FIFO buffer, "H'00" can be read for the data byte (the CFDFp register) for which no data is set.
8. After reading the messages in the transmit/receive FIFO buffer (the CFIDLk,H register, CFTSk register, CFPTR register, CFDFp register), increment the pointer (write "H'FF" to the CFPC [7: 0] bit of the CFPCTRk register).
9. Increment the pointer when the transmit/receive FIFO buffer is used (the CFE bit of the CFCCLk register is “1”) and there are unread messages in the transmit/receive FIFO buffer (the CFEMP flag in the CFSTSk register is “0”).
10. When reading all the unread messages in the transmit/receive FIFO buffer, use a loop statement or the like to read until the buffer is empty.

Figure 4-2 Read Procedure (Receive mode) of Transmit/receive FIFO Buffer (no interrupt used)



【Note】 1. Rewrite to enable/disable the transmit/receive FIFO buffer (the CFE bit of the CFCCLk register) in the global operation mode or global test mode.
2. Make the configuration settings for using the transmit/receive FIFO buffer, and then enable the use of the transmit/receive FIFO buffer (CFE bit is "1").
3. If the number of transmit/receive FIFO buffers is set to “0” (“B’000” in the CFDC [2: 0] bit of the CFCCLk register), do not allow the transmit/receive FIFO buffer to be used.

Figure 4-3 Procedure to Enable Transmit/receive FIFO Buffer Use



【Note】 1. Rewrite to enable/disable the transmit/receive FIFO buffer (the CFE bit of the CFCCLk register) in the global operation mode or global test mode.
2. Even if the use of the transmit/receive FIFO buffer is prohibited (the CFE bit is “0”) while an interrupt request is generated (the CFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFRXIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Figure 4-4 Procedure to Prohibit Transmit/receive FIFO Buffer Use

4.2 Transmit/Receive FIFO Buffer (Receive Mode) Interrupt Processing

4.2.1 Transmit/receive FIFO Reception Completion Interrupt Processing

If the transmit/receive FIFO interrupt is enabled, the transmit/receive FIFO interrupt is generated when the condition selected in the CFIM bit setting of the CFCCLk register is satisfied.

Even if the use of the transmit/receive FIFO buffer is prohibited (CFE bit is “0”) while an interrupt request is generated (the CFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFRXIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Whether to enable or disable transmit/receive FIFO interrupts can be set for each transmit/receive FIFO buffer using the CFRXIE bit of the CFCCLk register.

The sources of transmit/receive FIFO interrupts in receive mode are shown below.

A transmit/receive FIFO interrupt request is generated when the condition set by the CFIGCV [2: 0] bit of the CFCCLk register is reached (the CFIM bit of the CFCCLk register is "0").

RFIGCV[2:0] bit settings

- When a message is stored up to 1/8 in the transmit/receive FIFO buffer*1
- When a message is stored up to 2/8 in the transmit/receive FIFO buffer
- When a message is stored up to 3/8 in the transmit/receive FIFO buffer*1
- When a message is stored up to 4/8 in the transmit/receive FIFO buffer
- When a message is stored up to 5/8 in the transmit/receive FIFO buffer*1
- When a message is stored up to 6/8 in the transmit/receive FIFO buffer
- When a message is stored up to 7/8 in the transmit/receive FIFO buffer*1
- When the transmit/receive FIFO buffer is full

— Transmit/receive FIFO interrupt request occurs every time message reception is completed (the CFIM bit of CFCCLk register is “1”)

【Note】 1. Do not set if the number of transmit/receive FIFO buffers is set to 4 messages (the CFDC [2: 0] bit of the CFCCLk register is set to "B'001").

4.2.2 FIFO Full Interrupt Processing

If the FIFO full interrupt is enabled (CFFIE bit of CFCCEx register), the transmit/receive full interrupt is occurred when the transmit/receive FIFO buffer is full.

Even if the use of the transmit/receive FIFO buffer is prohibited (CFE bit is “0”) while an interrupt request is generated (the CFFIF flag in the CFSTSx register is “1”), the interrupt request flag (CFFIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

4.2.3 Transmit/ Receive FIFO One-Frame Reception Interrupt Processing

If the transmit/receive FIFO one-frame reception interrupt is enabled (CFOFRXIE bit of CFFCCEk register), transmit/receive FIFO one-frame reception interrupt is occurred when the transmit/receive FIFO buffer received the message by one-frame reception.

Even if the use of the transmit/receive FIFO buffer is prohibited (CFE bit is “0”) while an interrupt request is generated (the CFOFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFOFRXIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

4.2.4 Global Error Interrupt Processing

If the FIFO message lost interrupt is enabled, a global error interrupt is generated when a message lost in the transmit/receive FIFO buffer is detected. Whether to enable or disable the FIFO message lost interrupt can be set in common for the entire module with the MEIE bit of the GCTRH register.

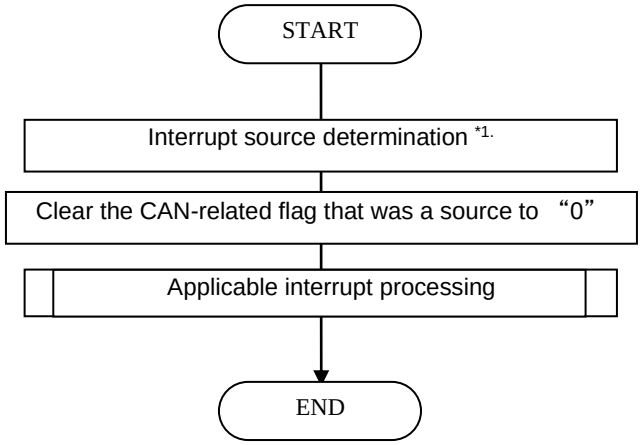
If the FIFO message overwrite interrupt is enabled, the global error interrupt is occurred when the message overwrite of the transmit/receive FIFO buffer is detected.

Whether to enable or disable the FIFO message lost interrupt can be set in common for the entire module with the MEIE bit of the GCTR register. Also, whether to enable or disable the FIFO message overwrite interrupt can be set in common for the entire module with the GCTR register.

5. CAN-related Interrupt Processing

When using interrupts, the interrupt source flag must be cleared to “0”. For CAN-related flags related to each interrupt source flag on the interrupt control side, refer to "CAN Configuration Application Note".

Figure 5-1 shows how to clear the interrupt source flag in interrupt processing.



【Note】 1. End the interrupt processing after making sure that all the interrupt request flags of the CAN module corresponding to the interrupt source are set to “0”. However, there is no interrupt request flag on the CAN module side because the CAN wakeup interrupt is controlled only by the interrupt function.

Figure 5-1 CAN-related Interrupt Processing Procedure

6. Precautions for Processing Flow

6.1 About Functions

In this application note, there is a part that is functionalized even in the processing of single line, but this is only described as a function to clarify the processing for each function. When you actually create a program, it is not necessary to make it functional.

6.2 Settings for Each Channel, FIFO, and Buffer

In this application note, even if processing is required for each channel, FIFO, or buffer, only one processing is described. When actually creating a program, perform multiple processes as necessary.

6.3 Infinite Loop

To simplify the notation, there are some infinite loops in the processing flow. When actually creating a program, give each loop a time limit so that it can be exited during overtime. Figure 6-1 shows an example of processing with a loop time limit.

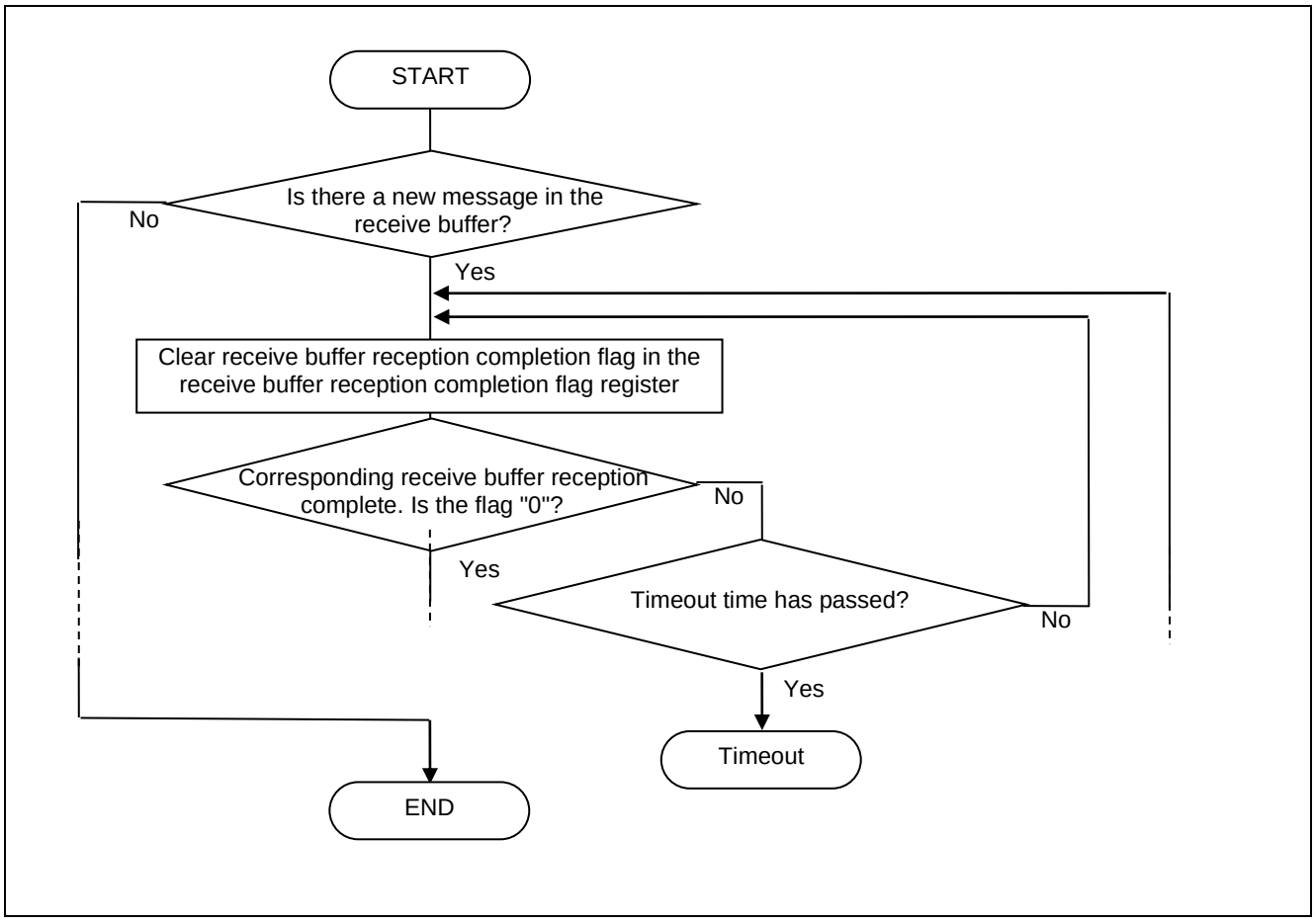


Figure 6-1 Example of Processing with Loop Time Limit

7. Appendix

7.1 Operation when Receive Buffer is Completed and Receive (Transmit/receive) FIFO Buffer is Full

Table 7-1 shows the operation when a message to be stored is received when the reception buffer reception is completed, and the reception FIFO buffer, the transmit/receive FIFO buffer (reception mode) are full.

Table 7-1 Operation when Receive Buffer is Completed and Receive (Transmit/receive) FIFO Buffer is Full

FIFO/Buffer	When the next message is received*1	Occurred Interrupt request
Receive Buffer	Overwrite	Global Error Interrupt (CAN-FD message payload overwrite Interrupt)
Receive FIFO Buffer	Discard	Global error interrupt (Message lost in receive FIFO buffer)
Transmit/Receive FIFO Buffer (receive mode)	Overwrite to oldest buffer, and increment pointer. When CFCCEk.CFMOWM=1 is set.	Global Error Interrupt (Transmit/Receive FIFO message overwrite)
	Discard When CFCCEk.CFMOWM=0 is set.	Global Error Interrupt (Message lost in transmit/receive FIFO buffer)

【Note】 1. Overwrite : The next message is overwritten in the receive buffer
Discard : The next message is discarded (not stored in FIFO) and the message is lost.

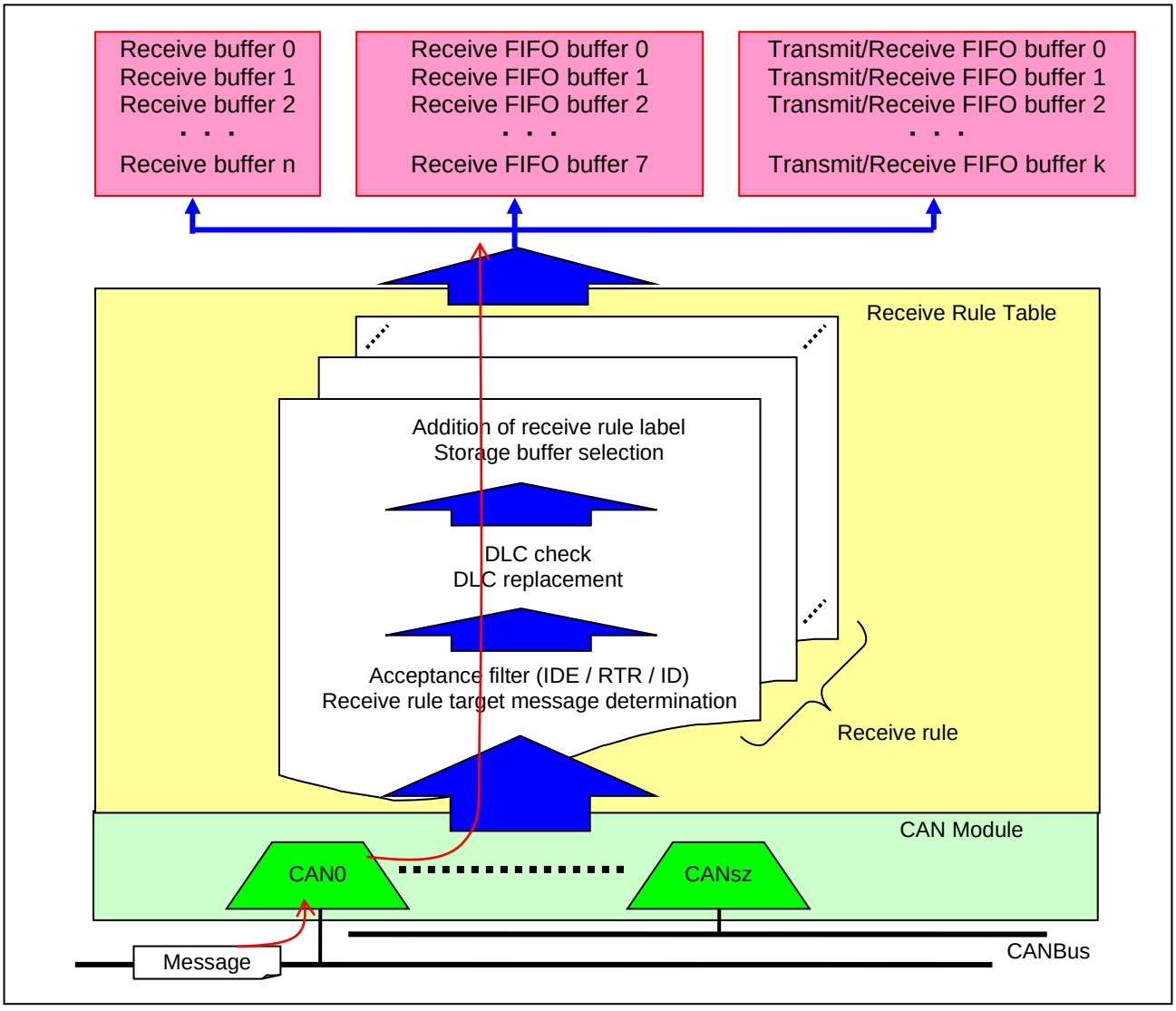
7.2 About Receive Rule Table

The receive rule table is a table with rules for filtering received messages.

The selected messages are stored in the specified buffer by data processing using the receive rule table. Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function. For details on how to set the receive rule table, refer to "CAN Configuration Application Note".

The functions performed during data processing of received message according to the receive rule are shown below.

- Comparison of IDE / RTR / ID by IDE mask / RTR mask / ID mask
- Determination of receive rule target message (message sent by other node / own node) (when mirror function is enabled)
- DLC check (when DLC check is enabled)
- DLC replacement (when DLC check and DCL replacement are enabled)
- Storage FIFO / buffer selection
- Addition of receive rule label



7-1 Filtering Image by receive rule table

Our Company's Website and Inquiry

Website
http://japan.renesas.com/

Inquiry
http://japan.renesas.com/contact/

Revision History

Rev.	Issue	Description	
		Page	Summary
1.0	2023.10.5	—	Initial edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused pins

[Caution] Please dispose of unused pins according to "Handling of unused pins" in the text.

The impedance of the input pins of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

[Caution] The state of the product is undefined when the power is turned on.

When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.

For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.

Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of Access to Reserved Addresses

[Caution] Access to reserved addresses is prohibited.

The address area has a reserved address allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

[Caution] When resetting, release the reset after the clock has stabilized.

When switching the clock during program execution, switch the clock after the switching destination clock is stable.

In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

[Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.

Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

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