RH850/U2B Group

R01AN6583EJ0100
Rev.1.00

CADC Application Note

Summary

This application note describes Cyclic A/D Converter (CADC) in RENESAS Electronics single-chip microcomputer RH850/U2B series for automobile (Hereafter referred to as U2B).

Aim of this document and software is to provide supplemental information for the function on RH850/U2B. It is not intended to implement in the design for mass production.

There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2B Group

Target Integrated Development Environment

CS+(from Renesas Electronics)

Device file : DR7F702Z21*.DVF

Reference Document

RH850/U2B User's Manual : Hardware
For function details and electrical characteristics, please refer to "User's Manual: Hardware".
This application note is based on the following manual.

- RH850/U2B User's Manual (Rev.1.00): R01UH0923EJ0100

Summary

1. Introduction

This application note describes the usage and software creation example of cyclic conversion method 16bits A/D converter in RH850/U2Bx.

1.1 Use Function

The following shows the hardware functions in RH850/U2Bx used in this application note.

- 16 bits A/D Convertor with Cyclic Conversion Method (CADC)
- DMA (sDMAC)
- OS Timer (OSTM0)

2. CADC Overview

2.1 Operation of CADC

2.1.1 Virtual Channel

16 bits A/D convertor with cyclic conversion method (CADC) is mounted on RH850/U2Bx. It possible to totally convert 8 channels when using in the single-end input, and totally 4 channels when using in the differential input. There are the virtual channels for 8 channels in CADC. It sets the accompanying information; analog channel, conversion mode, and interrupt that are A/D converted to each virtual channel.

The scan operation is executed sequentially from virtual channel 0 to the end virtual channel pointer for each A/D conversion start trigger (hardware or software) input.

The following shows the interrupt example of the input pin and virtual channel.

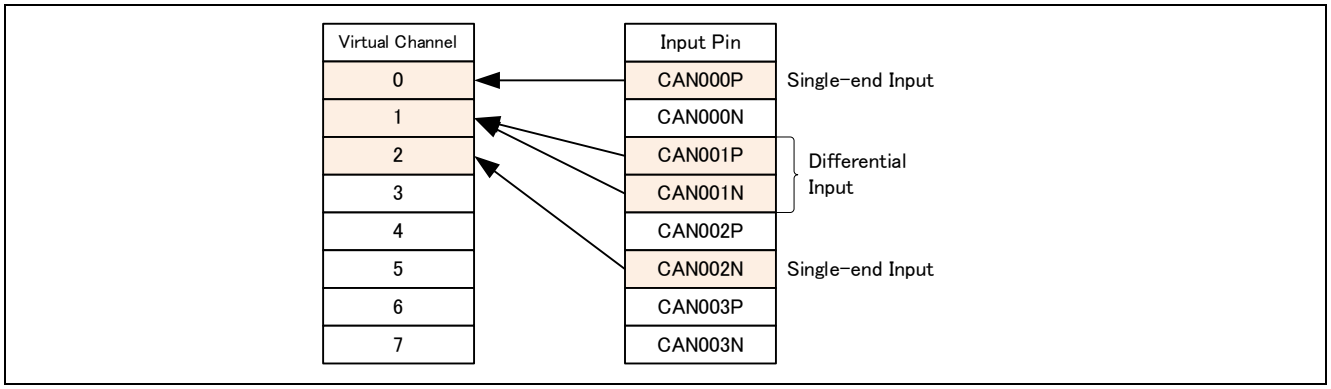

Figure 2-1 Interrupt Example of Virtual Channel

2.1.2 Conversion Completion Interrupt

Conversion completion interrupt (CADIn) is used as the start trigger for DMA conversion. The setting for the conversion completion interrupt enable/disable is performed by ADIE of CADCnVCRj (0 = disable, 1= enable).

The following shows the conversion completion interrupt occurrence timing in the scan executing.

Ex.1) When only using the virtual channel 0

Set ADIE (1 = enable) of CADC0VCR0.

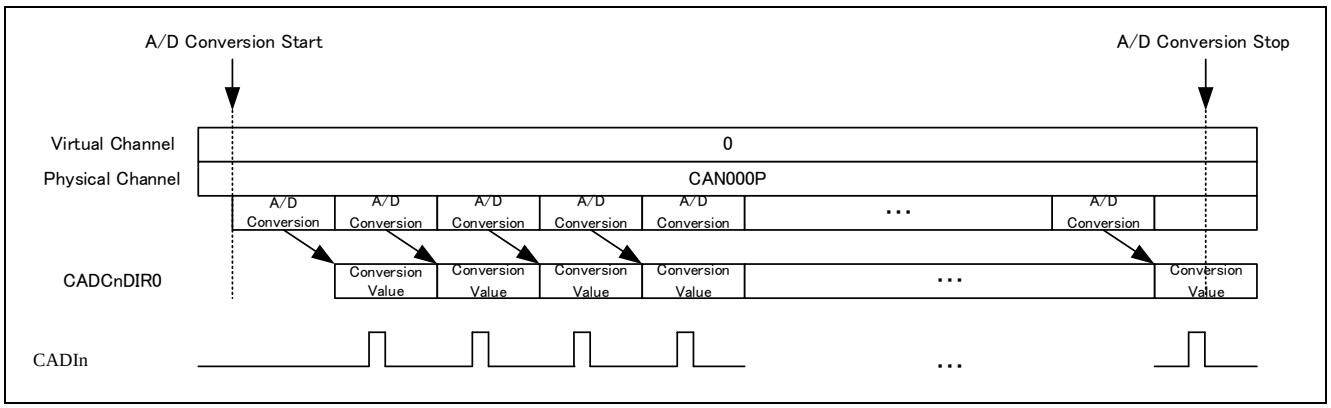

Figure 2-2 Scan End Interrupt Occurrence Timing 1

Ex.2) When multiply using virtual channel 1

Set to ADIE (1 = Enable) in CADC0VCR0.

Set to ADIE (1 = Enable) in CADC0VCR1.

Set to ADIE (1 = Enable) in CADC0VCR2.

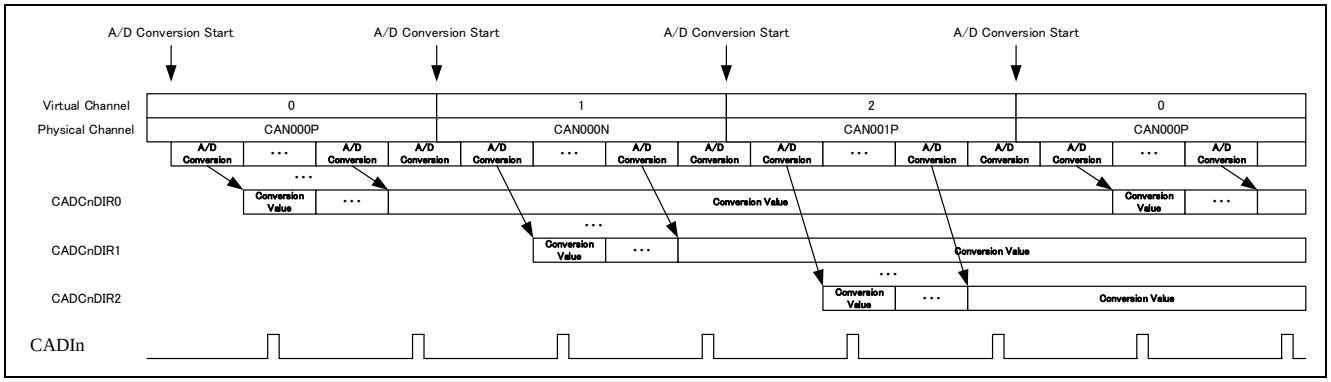

Figure 2-3 Scan End Interrupt Occurrence Timing 2

Ex.3) When multiply using virtual channel 2

Set to ADIE (1 = Disable) in CADC0VCR0

Set to ADIE (1 = Disable) in CADC0VCR1

Set to ADIE (1 = Enable) in CADC0VCR2

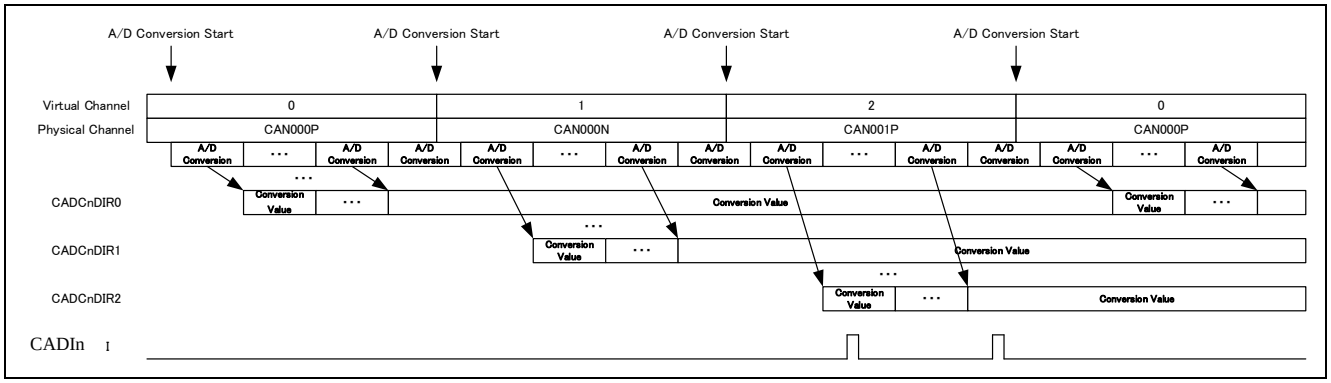

Figure 2-4 Scan End Interrupt Occurrence Timing 3

3. Operation Overview

3.1 Conversion Operation Only Using Virtual Channel 0

3.1.1 Specification Overview

This section explains the method for performing the A/D conversion only used the virtual channel 0.

Allocate the analog input pin (CAN000P) to the virtual channel 0, set “enable” to the conversion completion interrupt, and start scanning (soft trigger). Boot DMA and store the variable in the variable completion interrupt. Furthermore, in this operation example, the operation is ended when overtrained 150 conversion value.

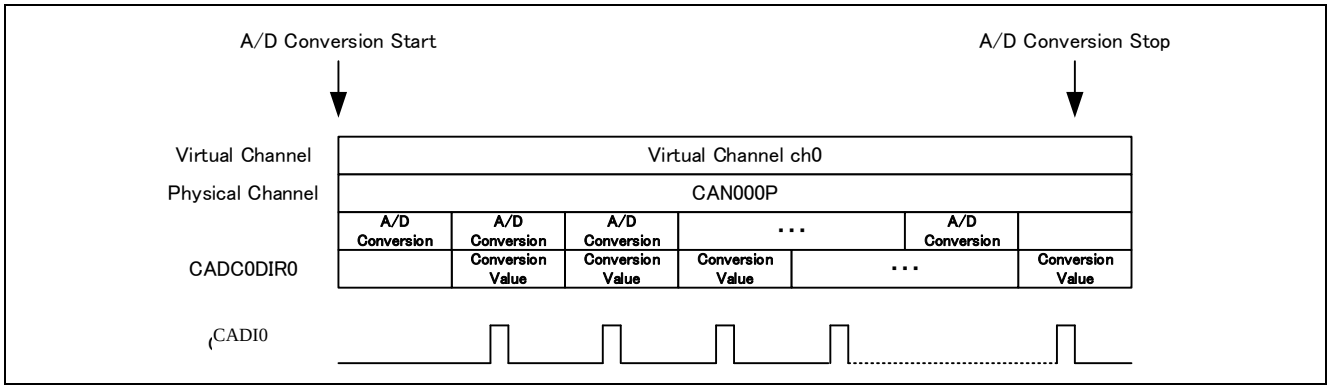

Figure 3-1 A/D Conversion Operation

3.1.2 Use Function

The following shows the hardware functions used in this operation example.

- A/D Convertor (CADC0)
- DMA (sDMAC)

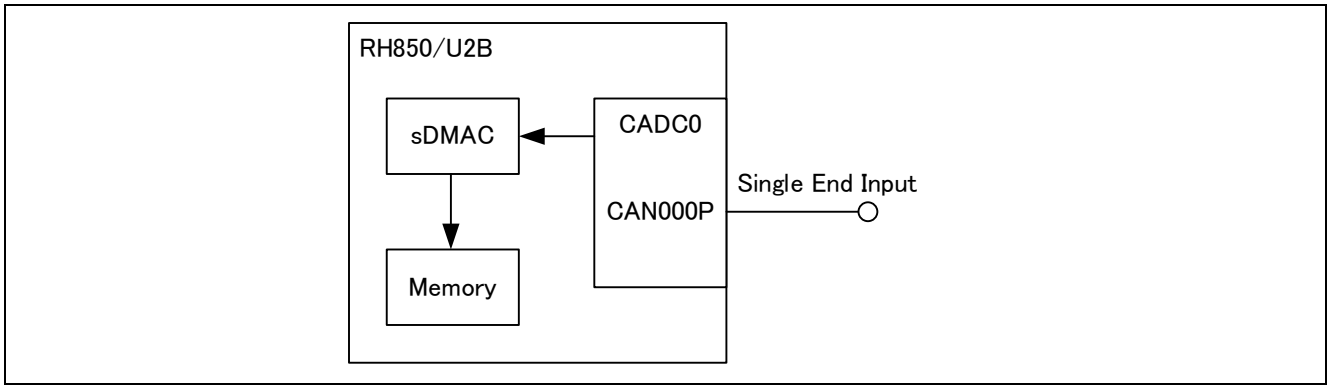

Figure 3-2 System Configuration

3.1.3 Explanation for Operation Example

In this operation example, the A/D conversion only used the virtual channel 0 of CADC0 module is performed.

Allocate the analog input pin CAN000P to the virtual channel 0, and set “Enable” to the conversion completion interrupt (CADI0).

Input a sine wave to the analog input pin CAN000P.

Start the soft trigger CADC0ADST and perform A/D conversion of CAN000P.

Boot DMA in the conversion completion interrupt (CADI0) and store the variable value to the variable. Furthermore, in this operation example, A/D conversion is stopped, and the operation is ended by the transferring completion interrupt of DMA (completed 150 conversion value transferring).

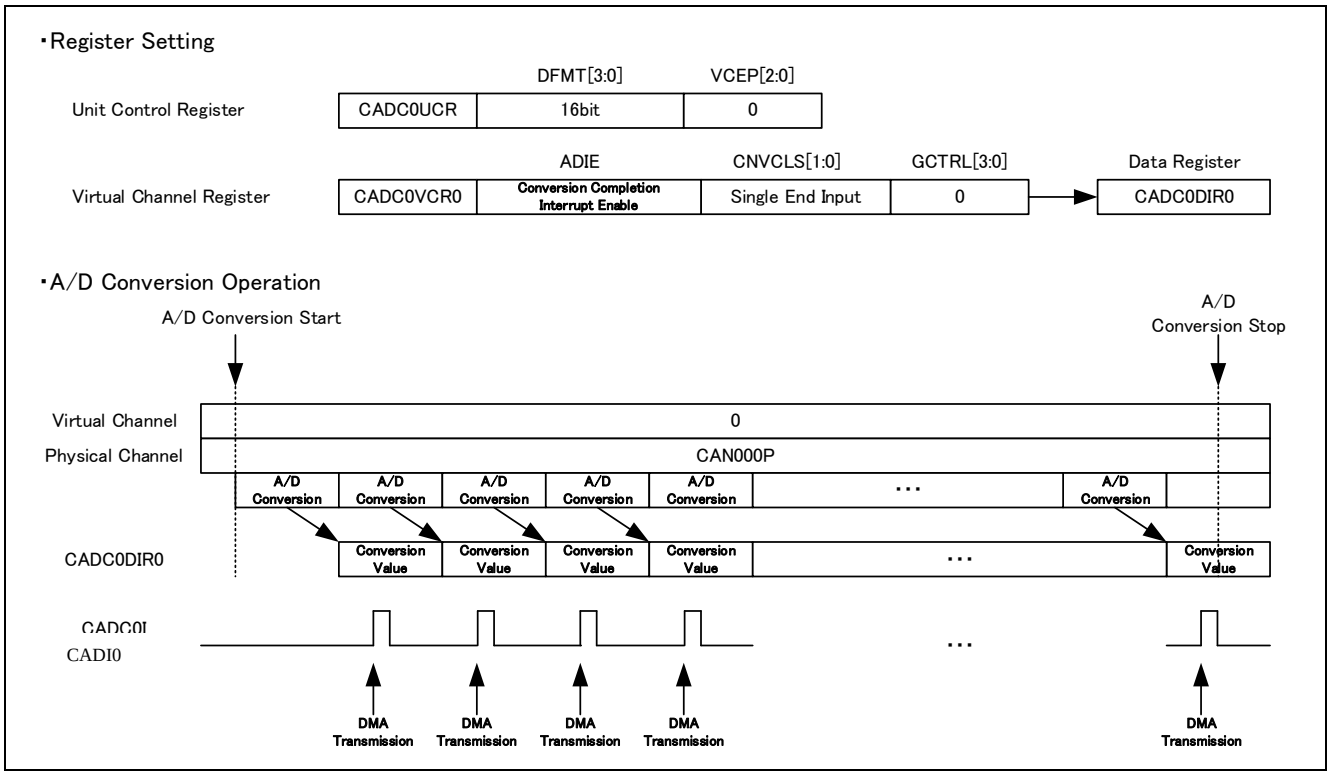

Figure 3-3 A/D Conversion Operation Example

3.1.4 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 3-1 Module List

Module Name	Rable Name	Function
Main routine	cadc_main	Perform various setting and application startup.
CADC initialization routine	cadc_init	Perform CADC initial setting.
sDMAC initialization routine	sdmac_init	Perform sDMAC initial setting.
Interrupt initialization routine	intc_init	Perform sDMAC interrupt initial setting.
Transfer completion interrupt processing routine	IRQ_INTSDMAC0CH0	Stop A/D conversion in transfer completion interrupt processing.

- Register Setting

The following shows the register setting of the various functions in this operation example.

Table 3-2 CADC Register Setting

Register Name	Setting Value	Function
MSR_DSADC_CADC	0x00000000	Module standby release ・DS-ADC&CADC common ・CADC0
CADCADGCR	0x01	Self-diagnosis of disconnection detection function is enabled.
		Disconnection detection disable
		A/D conversion result is unsigned.
CADCTDCR	0x00	Not performed pin-level self-diagnosis.
CADC0UCR	0x20000000	Clear virtual channel pointer when ended A/D conversion.
		Data format : 16 bits
		End virtual channel : 0
CADC0VCR0	0x00008000	Output conversion completion interrupt.
		Single-end input
		Analog input pin : CAN000P
CADC0SFTCR	0x00	Read & clear disable
		Error interrupt disable
CADC0ADSTCR	0x01	A/D conversion start
CADC0ADENDCR	0x01	A/D conversion stop

Table 3-3 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD70	0x00000000	Bind interrupt to PE0 (CPU0).
EIC70	0x8040	Level detection / Priority level 0

Table 3-4 sDMAC Register Setting

Register Name	Setting Value	Function
MSR_ADCK_ISO	0x0000007F	AIR standby release
AIRDSELR1	0x00000000	INTAIRDMAREQ38: CADI0
DMATRGS ELDMACSEL0_2	0x00002000	DMA transfer source 38 : Group2 (INTAIRDMAREQ38)
SDMAC0DMA0CM_0	0x00001C00	SPID : 0x1C
		Supervisor mode
SDMAC0DMA0SAR_0	CADC0DIR0 address	Transfer source : CADC0DIR0
SDMAC0DMA0DAR_0	smp_data[0] address	Transfer destination : smp_data[0]
SDMAC0DMA0TSR_0	0x00000258	Transfer size : 4byte×150 times＝600 bytes
SDMAC0DMA0TMR_0	0x00001422	DMA transfer request : Hardware
		Destination address : Increment
		Source address : Fixed
		Transfer size : 4 bytes
SDMAC0DMA0RS_0	0x00010026	Startup trigger : DMA transfer source 38
SDMAC0DMA0CHFCR_0	0x0000320F	All flag clear
SDMAC0DMA0OR	0x0001	All channel DMA transfer enable
SDMAC0DMA0CHCR_0	0x0003	Transfer completion interrupt enable
		Transfer enable

- Operation Flow

The following shows the flowchart in this operation example.

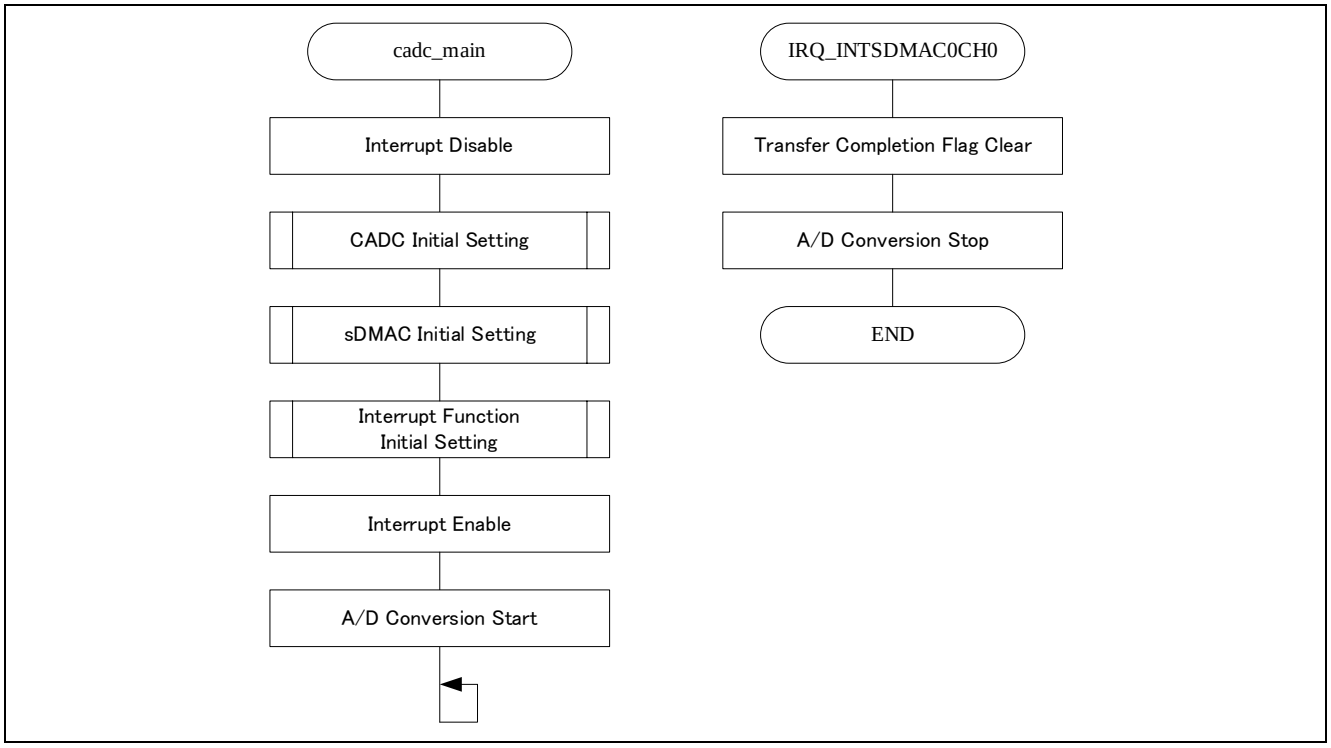

Figure 3-4 Flowchart

3.2 A/D Conversion Operation Multiply Used Virtual Channels

3.2.1 Specification Overview

This section explains the method for performing the A/D conversion multiply used the virtual channels (In this operation example, 3 virtual channels are used).

Allocate the analog input pin (CAN000P) to the virtual channel 0, the analog input pin (CAN000N) to the virtual channel 1, the analog input pin (CAN001P) to the virtual channel 2, and set “Enable” to the conversion completion interrupt of each channel. Furthermore, Set “2” to the end virtual channel pointer.

After started A/D conversion, the virtual channel pointer is incremented every A/D conversion start trigger (soft trigger) inputting, and A/D conversion of each analog input pin is performed.

Conversion value starts DMA by the conversion completion interrupt of each virtual channel and stores to the variable. Furthermore, in this operation example, the operation is ended by obtaining the variable value of each 150 virtual channels.

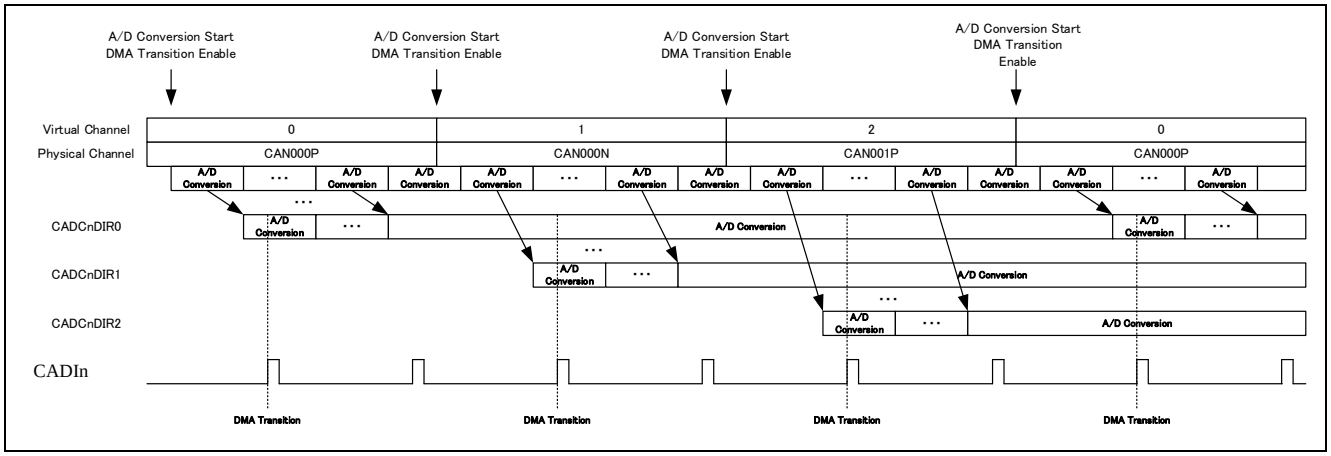

Figure 3-5 A/D Conversion Operation

3.2.2 Use Function

The following shows the hardware function used in this operation example.

- A/D Convertor (CADC0)
- DMA (sDMAC)
- OS Timer (OSTM0)

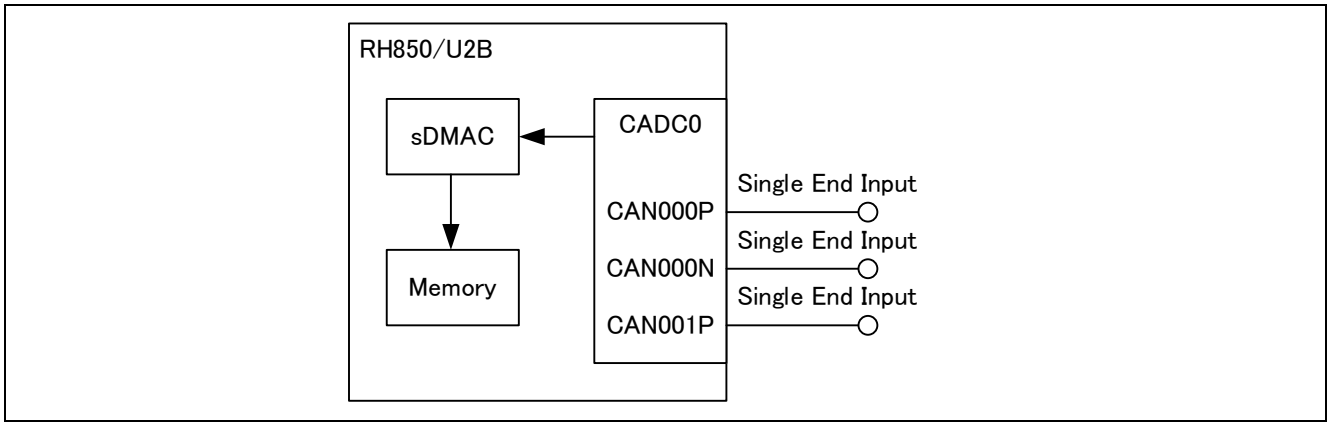

Figure 3-6 System Configuration

3.2.3 Explanation for Operation Example

In this operation example, the A/D conversion used 3 virtual channels of CADC0 module is performed.

Allocate the analog input pin (CAN000P) to the virtual channel 0, the analog input pin (CAN000N) to the virtual channel 1, the analog input pin (CAN001P) to the virtual channel 2, and set “Enable” to the conversion completion interrupt of each channel. Furthermore, Set “2” to the end virtual channel pointer.

Input a 0V to 5V sine wave to the analog input pin CAN000P, CAN000N, and CAN001P.

Start by the soft trigger CADC0ADST and perform A/D conversion of CAN000P. Aftar this, input A/D conversion start trigger by the soft trigger CADC0ADST at 1ms intervals.

The virtual channel pointer is incremented every A/D conversion start trigger (soft trigger) inputting, and A/D conversion of each analog input pin is performed.

The conversion value starts DMA by the conversion completion interrupt of each virtual channel and stores to the variable. Furthermore, in this operation example, the operation is ended by obtaining the variable value of each 150 virtual channels.

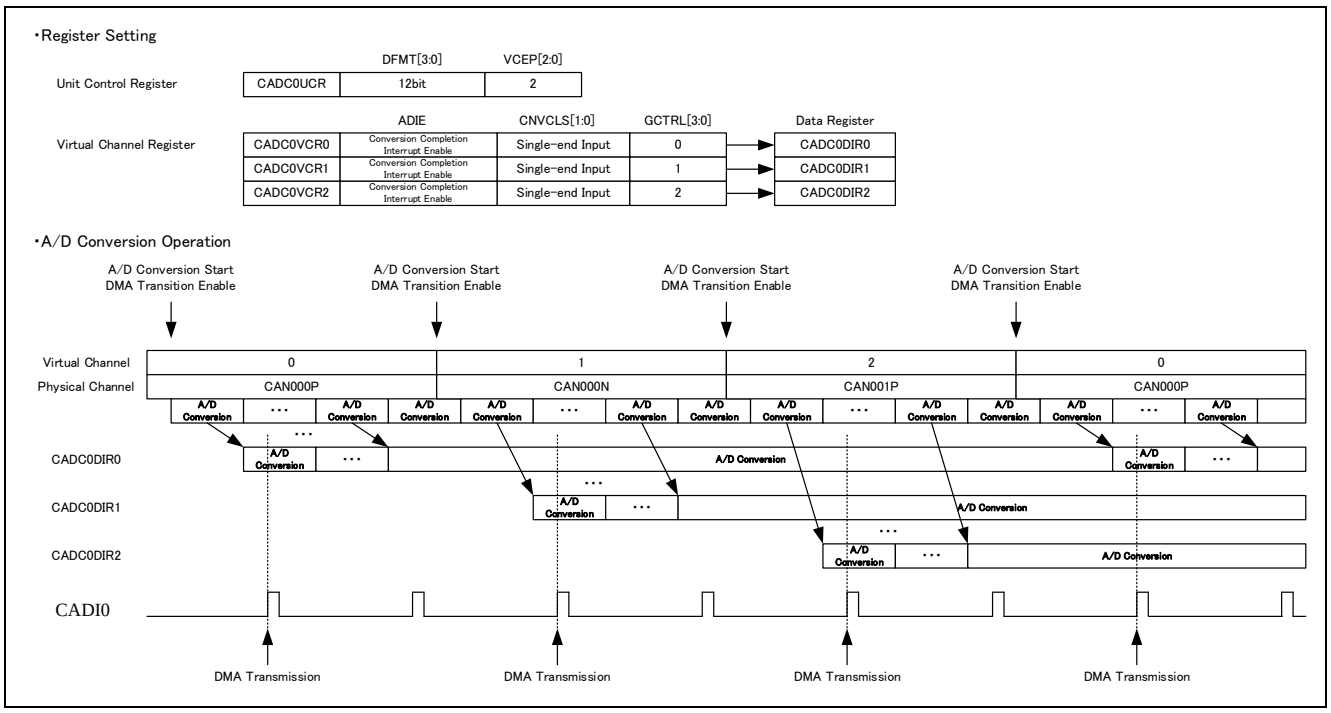

Figure 3-7 A/D Conversion Operation Example

3.2.4 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 3-5 Module List

Module Name	Rable Name	Function
Main routine	cadc_main	Perform various setting and application startup.
CADC initialization routine	cadc_init	Perform CADC initial setting.
sDMAC initialization routine	sdmac_init	Perform sDMAC initial setting.
Interrupt initialization routine	intc_init	Perform sDMAC interrupt initial setting.
Software Timer	wait	Wait 1ms.
Transfer completion interrupt processing routine	IRQ_INTSDMAC0CH0	Perform transfer completion flag clear, sDMAC reset, A/D conversion stop processing.

- Register Setting

The following shows the register setting of the various functions in this operation example.

Table 3-6 CADC Register

Register Name	Setting Value	Function
MSR_DSADC_CADC	0x00000000	Module standby release ・DS-ADC&CADC common ・CADC0
CADCADGCR	0x01	Self-diagnosis of disconnection detection function is enabled.
		Disconnection detection disable
		A/D conversion result is unsigned.
CADCTDCR	0x00	Not performed pin-level self-diagnosis.
CADC0UCR	0x20000402	Clear virtual channel pointer when ended A/D conversion.
		Data format : 12 bits
		End virtual channel : 2
CADC0VCR0	0x00008000	Output conversion completion interrupt.
		Single-end input
		Analog input pin : CAN000P
CADC0VCR1	0x00008001	Output conversion completion interrupt.
		Single-end input
		Analog input pin : CAN000N
CADC0VCR2	0x00008002	Output conversion completion interrupt.
		Single-end input
		Analog input pin : CAN001N
CADC0SFTCR	0x00	Read & clear disable
		Error interrupt disable
CADC0ADSTCR	0x01	A/D conversion start
CADC0ADENDCR	0x01	A/D conversion stop

Table 3-7 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD70	0x00000000	Bind interrupt to PE0 (CPU0).
EIC70	0x8040	Level detection / Priority level 0

Table 3-8 sDMAC Register Setting

Register Name	Setting Value	Function
MSR_ADCK_ISO	0x0000007F	AIR standby release
AIRDSELR1	0x00000000	INTAIRDMAREQ38: CADI0
DMATRGS ELDMACSEL0_2	0x00002000	DMA transfer source 38 : Group2 (INTAIRDMAREQ38)
SDMAC0DMA0CM_0	0x00001C00	SPID：0x1C
		Supervisor mode
SDMAC0DMA0SAR_0	CADC0DIR0 address	Transfer source : CADC0DIR0
SDMAC0DMA0DAR_0	smp_data[0] address	Transfer destination : smp_data[0]
SDMAC0DMA0TSR_0	0x00000258	Transfer size : 4byte×150 times＝600 bytes
SDMAC0DMA0TMR_0	0x00001422	DMA transfer request : Hardware
		Destination address : Increment
		Source address : Fixed
		Transfer size : 4 bytes
SDMAC0DMA0RS_0	0x00010026	Startup trigger : DMA transfer source 38
SDMAC0DMA0CHFCR_0	0x0000320F	All flag clear
SDMAC0DMA0OR	0x0001	All channel DMA transfer enable
SDMAC0DMA0CHCR_0	0x0003	Transfer completion interrupt enable
		Transfer enable

Table 3-9 OSTM Register Setting

Register Name	Setting Value	Function
MSR_OSTM	0x000003FE	OSTM0 module standby release
OSTM0CMP	80000 - 1	Counter value = 1ms * OSTM count clock (80MHz)
OSTM0CTL	0x82	OSTM interrupt enable
		Free run compare mode
		Load 0x0000 0000 to OSTMnCNT[31:0] when starting counter mode of free run compare mode.
		Interrupt disable when starting count.
OSTM0TS	0x01	Count start
OSTM0TT	0x01	Count stop

- Operation Flow

The following shows the flow chart in this operation example.

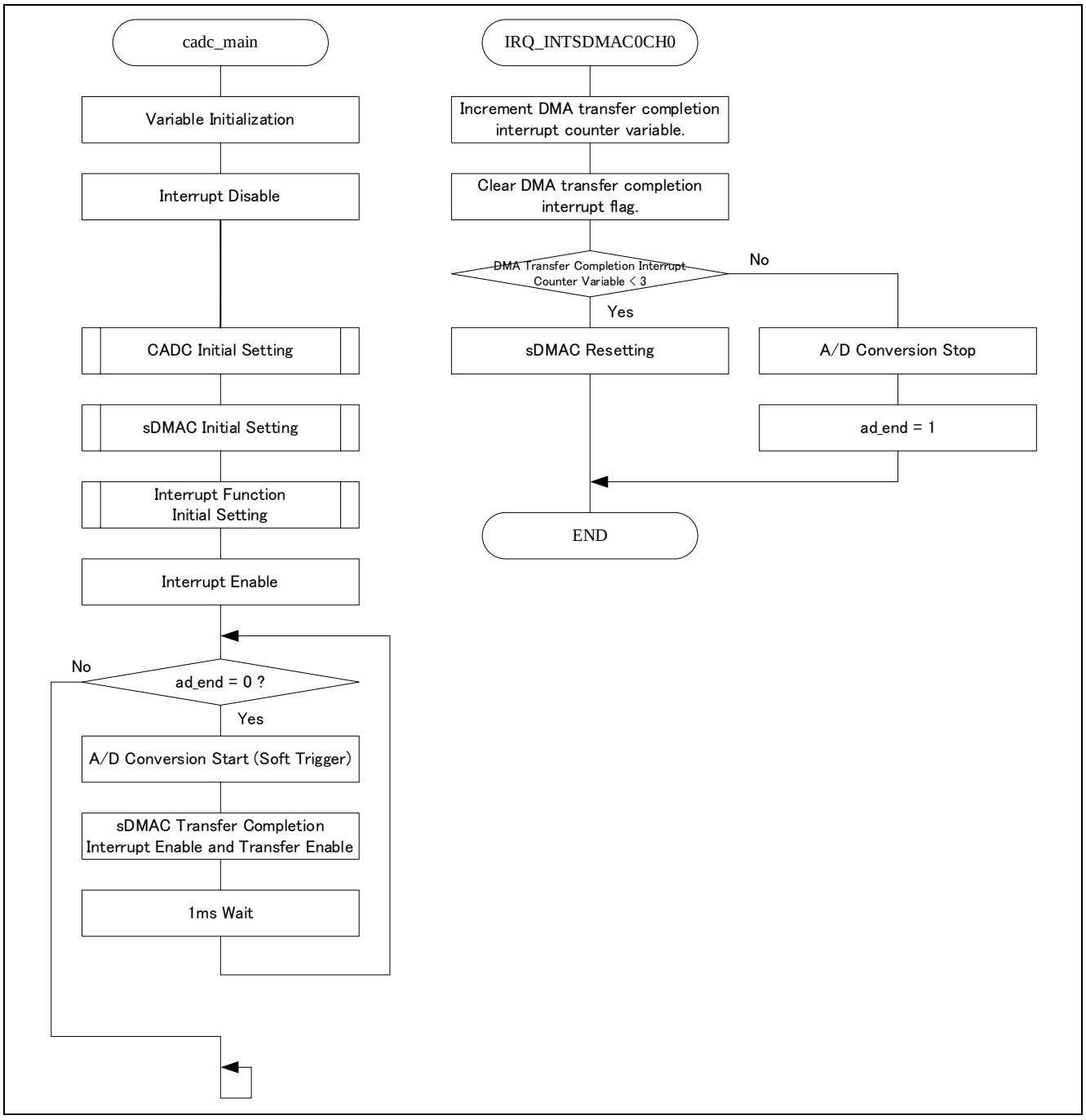

Figure 3-8 Flowchart

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024.5.7	-	Initial edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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