RH850/U2B Group

ATU-VI Application Note

R01AN6568EJ0100
Rev.1.00

Summary

This application note summarizes the example of the timer operation using the advanced timer unit-VI (ATU-VI).

Each timer block of ATU-VI has different functions and can operate independently of each other. It is also possible to operate multiple timers in conjunction with each other via the clock bus. A timer block is configured one or more timer subblocks with the same function, and each subblock has one or more channels.

The operation examples described in this application note have been confirmed to operate, but be sure to confirm the operation before using them.

Contents

1. Specification

This application not describes the usage of RH850/U2Bx advanced timer unit-VI (ATU-VI) and the farmwear creation example

1.1 Use Hardware Functions

Hardware functions of RH850/U2Bx used in this application note are shown below.

- Advanced Timer Unit-V (ATU-VI)
- Port
- Interrupt Controller (INTC)
- Direct Memory Access Controller (sDMAC)
- A/D Convertor (ADCK)
- Trigger Select Function (PIC2)

2. Explanation for Application Example

This application example summarizes the operation examples of various functions of timers A to G of ATU-VI. It is necessary to arbitrarily generate the external input signal required for the input capture function.

2.1 ATU-Ⅵ Operation Overview

ATU-VI is configured by the seven types of timer blocks, timers A to G, the prescaler, and the common control part. Each timer block has different functions and can operate independently of each other. It is also possible to operate multiple timers in conjunction with each other via the clock bus. A timer block is configured one or more timer subblocks with the same function, and each subblock has one or more channels.

2.2 Operation Ex.1 Pulse Period Measurement [Timer A]

2.2.1 Overview

1) Measure the period of the input pulse and save the result in RAM as shown in Figure 2.1.

2) The pulse period can be calculated by the following equation.

[Pulse period (ns)=Timer value × Low speed peripheral clock period (25ns when operating at 40MHz) × 2 (Prescaler division ratio)]

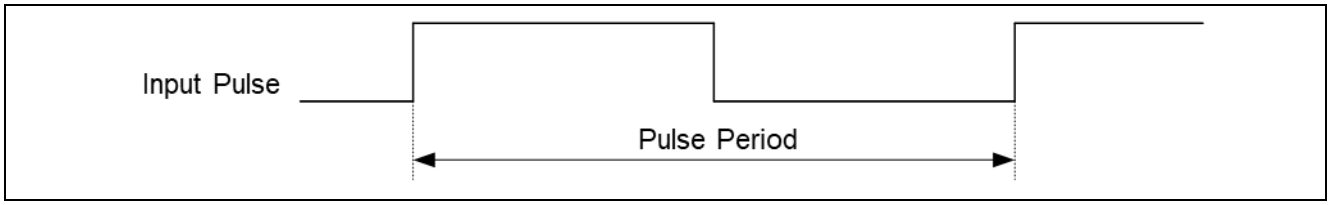


Figure 2.1 Pulse Period Measurement Timing

2.2.2 Explanation for Use Function

Table 2.1 shows the functions allocations of the ports used and related registers.

Table 2.1 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Inputs the pulse to be measured to this port.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer A register	TIOR1A	Sets the edge to capture the external input.
	TCNTA	Performs the timer count by the selected clock bus.
	ICRA0	The TCNTA value in input capture generation is stored.
	TSRA	The flag is set when the input capture is generated.
	TSCRA	Clears the flag of input capture generation.
	TIERA	Performs the setting of the input capture interrupt.
PORT register	PCR23_0	Sets the port function.
INTC register	EIBD86	Specifies the bind destination of TIA00 input capture interrupt.
	EIC86	Set the interrupt vector method and the interrupt priority.

2.2.3 Operation Explanation

Figure 2.2 shows the operation principle. According to this, the pulse period measurement is performed by the hardware and software processing of RH850/U2Bx. The timer count by the input capture interrupt is started and the current capture value is saved according to the rising edge of the external input pulse. At the next rising edge, the input capture interrupts again. Also, the counter value of the pulse cycle is acquired by acquiring the difference between the previous capture value and the current capture value.

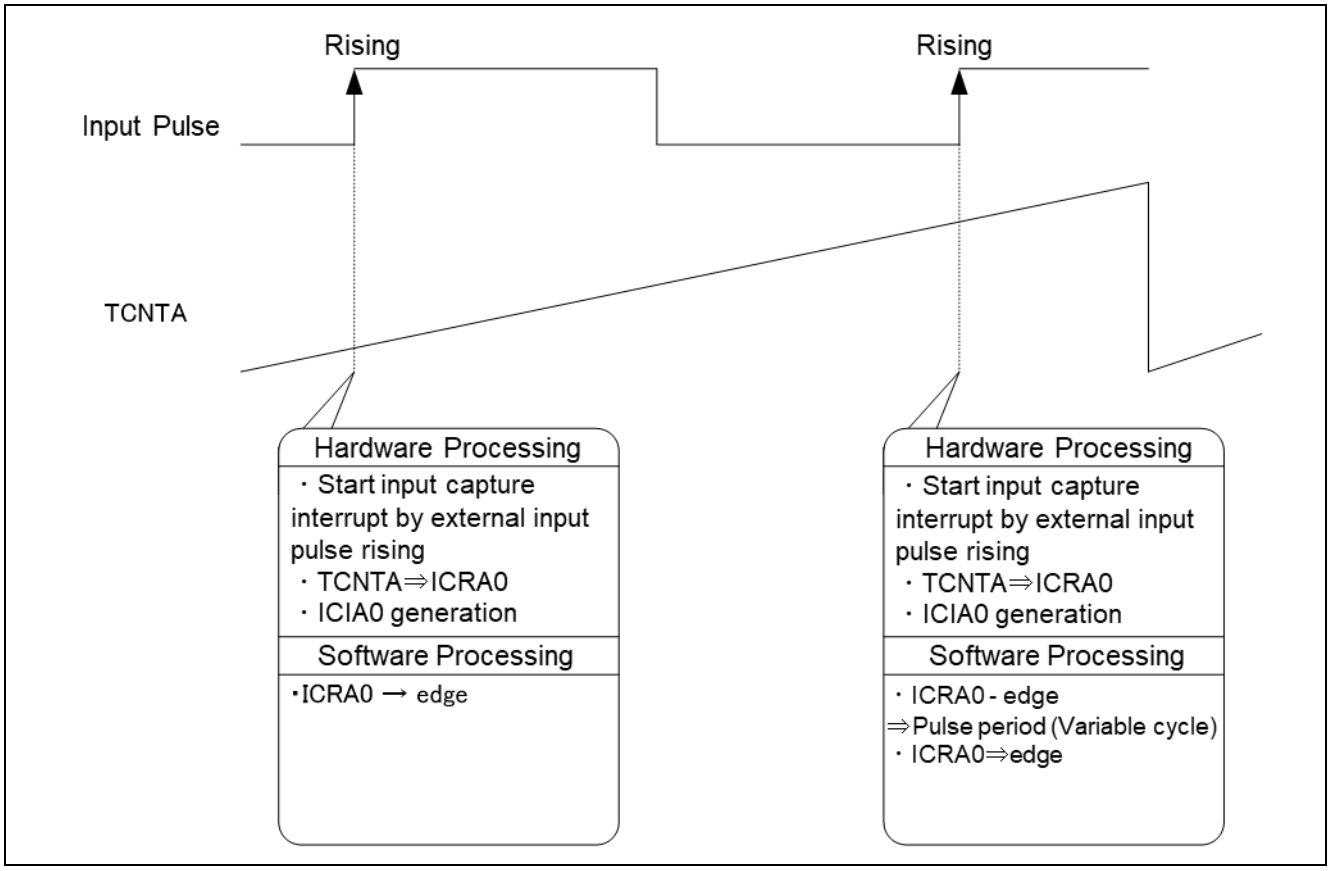


Figure 2.2 Operation Principle of Pulse Period Measurement

2.2.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Main routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Sets the port (P23_0) to the TIA00 input.
ATU setting	atu_init	Performs the initial setting of timer A
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Pulse period Measurement	eiint86	Starting by ICIA0. Measuring the pulse period by the ICRA0 value.

Explanation for Use Variable

Label Name	Function	Data Length	Use module
cycle	Stores timer count value corresponding to the pulse cycle. The pulse period can be calculated by the following equation. Pulse period (ns)=cycle value × Unmodulated slow clock period (25ns when operating at 40MHz) × 2 (Prescaler division ratio)	unsigned long	Pulse period measurement
edge	Saves the value of TCNT0 when the input capture is generated.		

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of the timer A and the prescaler.	0x03	
PCR23_0	Sets the port P23_0 to the input port TIA00.	0x00000058	Port setting
PSCR0	Sets the “2” to the division ration of the prescaler 0.	0x0001	ATU setting
TIOR1A	Sets to capture the input at the rising edge of the input signal from TIA00.	0x0001	
TSCRA	Clears the flag of Timer A.	0x80FF	
TIERA	Sets the TIA00 input capture interrupt enable.	0x0001	
EIBD86	Binds the TIA00 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC86	Set the interrupt vector method and the interrupt priority.	0x0040	
TSCRA	Clears the input capture flag of Timer A.	0x01	Pulse period measurement
ICRA0	Stores the value of TCNTA when the input capture signal is detected.	-	

2.3 Operation Ex. 2 High Width Measurement of Pulse [Timer A]

2.3.1 Overview

1) Measures the high width of the input pulse and saves the result in RAM as shown in Figure 2.3.

2) The high width can be calculated by the following equation.

[Pulse high width(ns)=Timer value × Low speed peripheral clock period (25ns when operating at 40MHz) × 2 (Prescaler division ratio)]

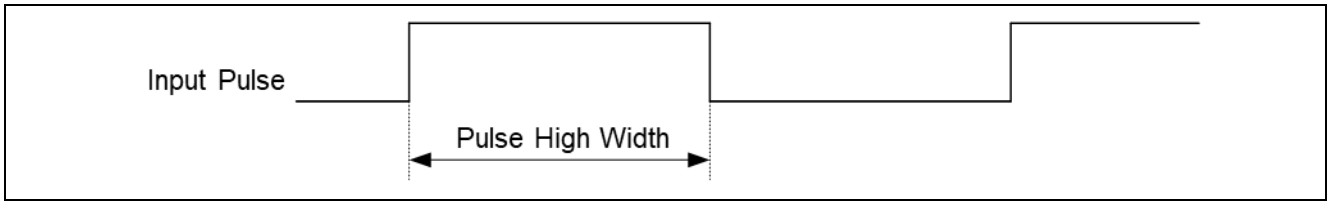


Figure 2.3 High Width Measurement of Pulse

2.3.2 Explanation for Use Function

Table 2.2 shows the functions allocations of the ports used and related registers.

Table 2.2 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Inputs the pulse to be measured to this port.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer A register	TIOR1A	Sets the edge to capture the external input.
	TCNTA	Performs the timer count by the selected clock bus.
	ICRA0	The TCNTA value in input capture generation is stored.
	TSRA	The flag is set when the input capture is generated.
	TSCRA	Clears the flag of input capture generation.
	TIERA	Performs the setting of the input capture interrupt.
PORT register	PCR23_0	Sets the port function.
INTC register	EIBD86	Specifies the bind destination of TIA00 input capture interrupt.
	EIC86	Set the interrupt vector method and the interrupt priority.

2.3.3 Operation Explanation

Figure 2.4 shows the operation principle. According to this, the pulse high width measurement is performed by the hardware and software processing of RH850/U2Bx. The timer count by the input capture interrupt is started and the current capture value is saved according to the rising edge of the external input pulse. At the next rising edge, the input capture interrupts again. Also, the counter value of the pulse high width is acquired by acquiring the difference between the previous capture value and the current capture value.

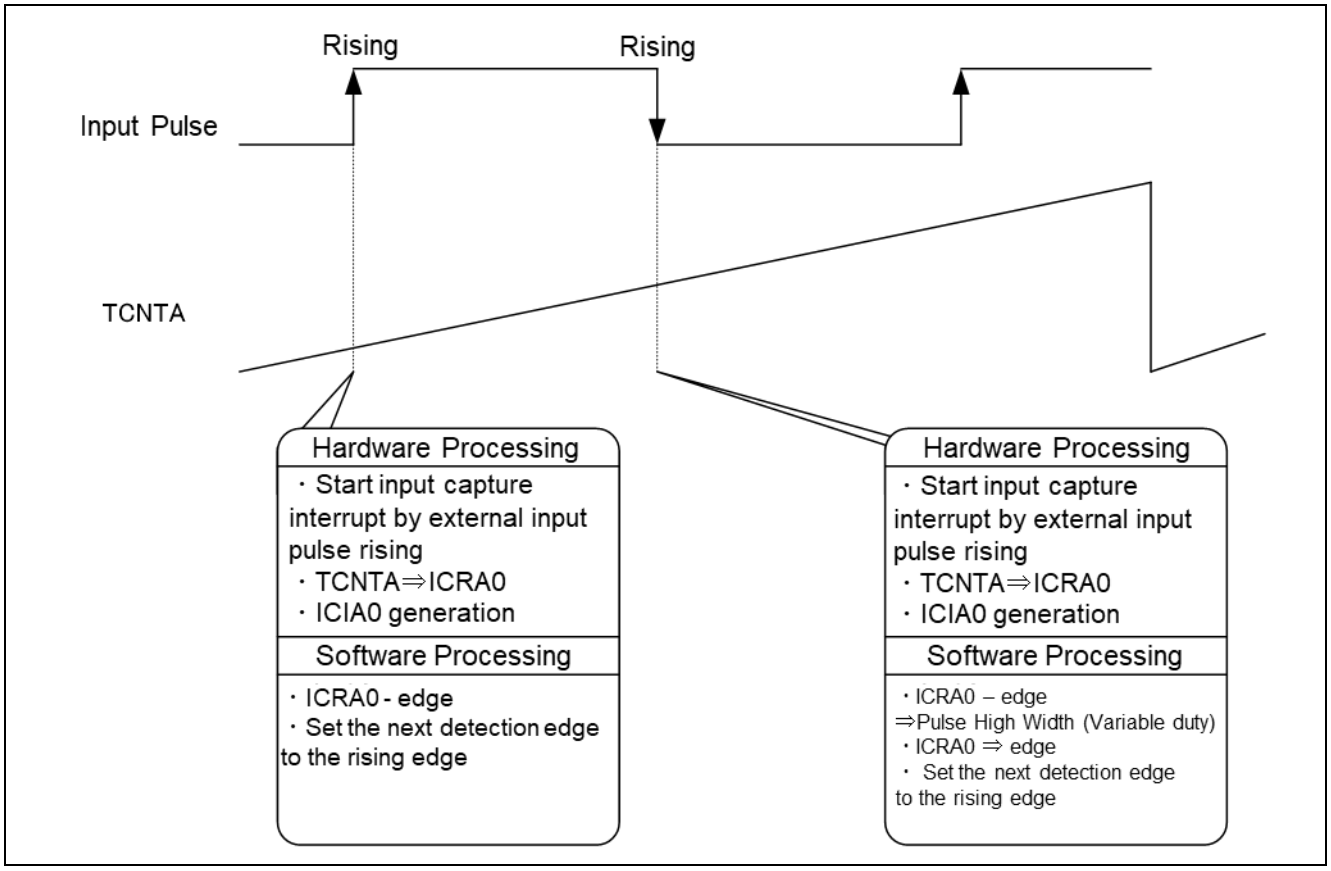


Figure 2.4 Operation Principle of Pulse High Width Measurement

2.3.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Sets the port (P23_0) to the TIA00 input.
ATU setting	atu_init	Performs the initial setting of timer A
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Pule high width measurement	eiint86	Starting by ICIA0. Measuring the pulse width by the ICRA0 value.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module
duty	Stores timer count value corresponding to the pulse high width. The pulse high width can be calculated by the following equation. Pulse high width(ns)=duty value×Slow clock period (25ns when operating at 40MHz)×2 (Prescaler division ratio)	unsigned long	Pulse period measurement
edge	Saves the input capture value.		

Explanation of Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enables the count operation of the timer A and the prescaler.	0x03	
PCR23_0	Sets the port P23_0 to the input port TIA00.	0x00000058	Port setting
PSCR0	Sets the “2” to the division ration of the prescaler 0.	0x0001	ATU setting
TIOR1A	Sets to capture the input at the rising edge of the input signal from TIA00.	0x0001	
TSCRA	Clears the flag of Timer A.	0x80FF	
TIERA	Sets the TIA00 input capture interrupt enable.	0x0001	
EIBD86	Binds the TIA00 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC86	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRA	Clears the input capture flag of Timer A.	0x0001	Pulse high width measurement
ICRA0	TCNTA value is stored when the input capture signal is detected.	-	
TIOR1A	Sets to perform input capture in the input signal rising/falling form TIA00. It changes with the previous TIOR1A value.	0x0001 0x0002	

2.4 Operation Ex. 3 Noise Cancel (Subsequent Edge Cancel) [Timer A]

2.4.1 Overview

As shown in Figure 2.5, the subsequent edge cancel function ignores the level change within a certain period from the input to remove the noise mixed with the input signal. The noise cancellation period is controlled by the compare match with the timer.

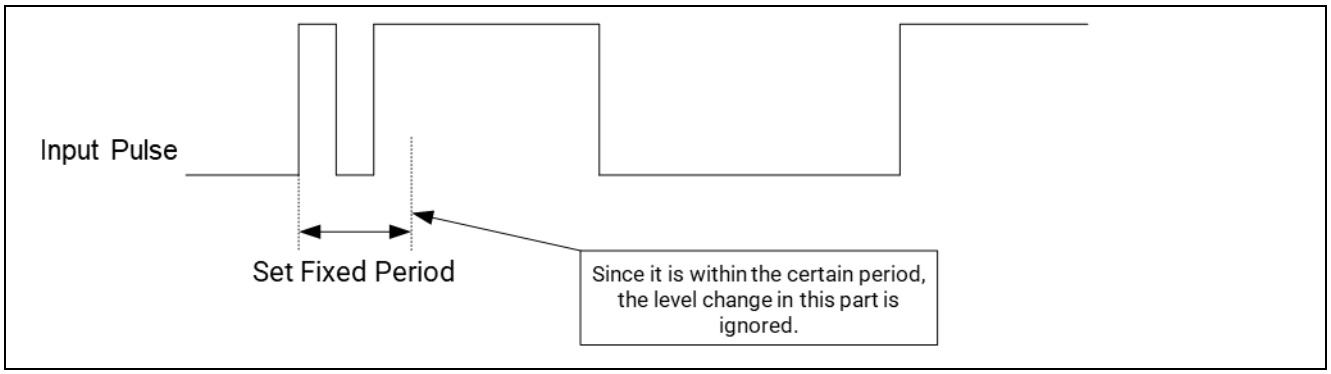


Figure 2.5 Conceptual Diagram of Subsequent Noise Cancellation

2.4.2 Explanation for Use Function

Table 2.3 shows the functions allocations of the ports used and related registers.

Table 2.3 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Inputs the pulse to be measured to this port.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	NCMR	Sets the noise canceling operation mode and counts clock for each timer.
Timer A register	TIOR1A	Sets the edge to capture the external input.
	TIOR2A	Set the noise cancel function enbale/disbale and the clock for noise cancel.
	NCMCR1A	Sets the noise cancel operation mode.
	TSRA	The flag is set when the input capture is generated.
	TSCRA	Clears the flag of input capture generation.
	NCNTA0	The counting is stared at the same time as the edge input, and the noise cancellation period is measured.
	NCRA0	Sets the noise cancellation period.
PORT register	PCR23_0	Sets the port function.

2.4.3 Operation Example

Figure 2.6 shows the operation principle. According to this, the subsequent noise cancel is performed by the processing of RH850/U2Bx hardware and software. The signal after noise cancel is not updated after the timer count starts until a compare match generates. (The figure shows an example of detecting a rising edge.)

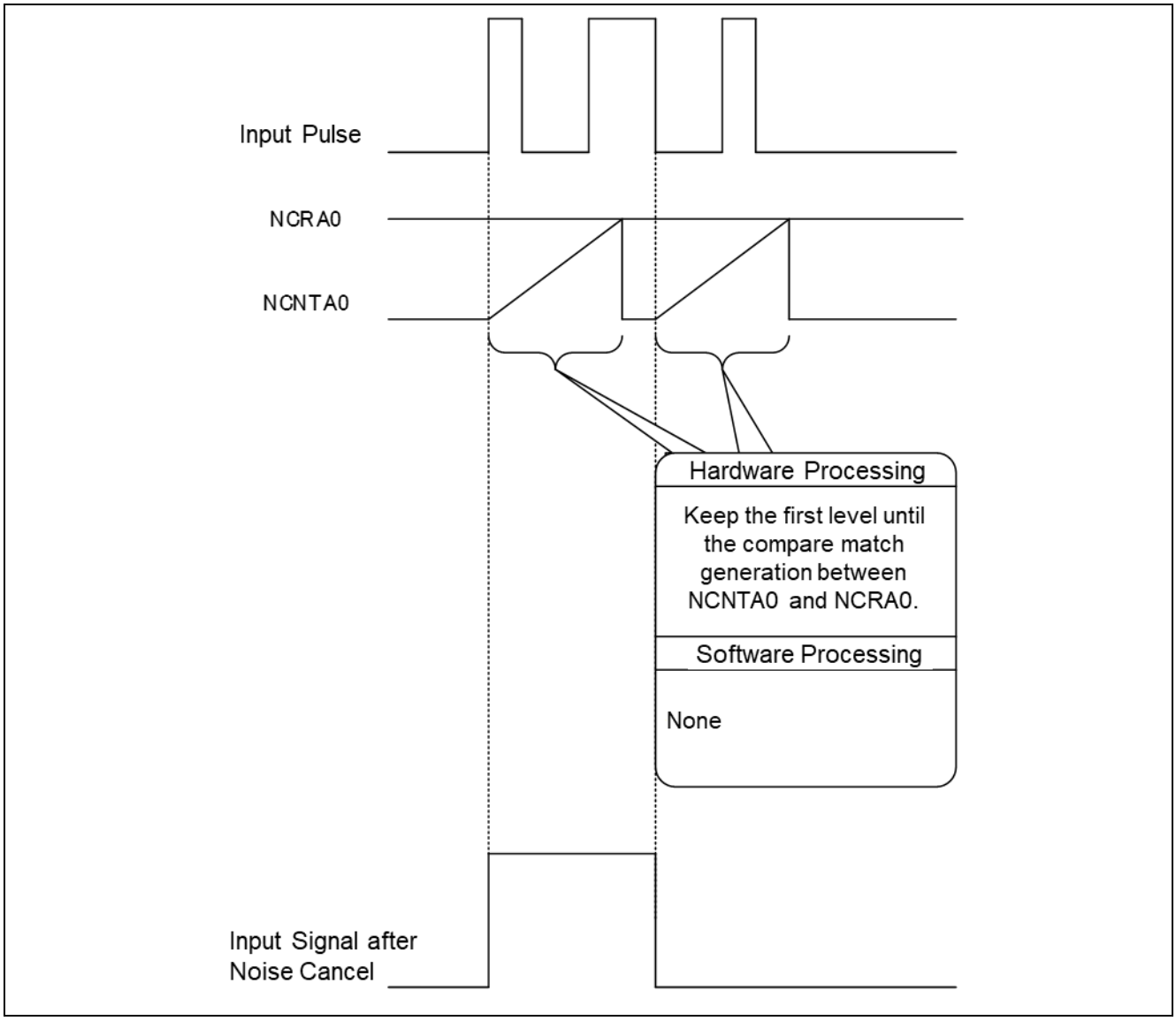


Figure 2.6 Operation Principle of Subsequent Noise Cancel

2.4.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Sets the port (P23_0) to the TIA00 input.
ATU setting	atu_init	Performs the initial setting of timer A

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enables the count operation of the timer A and the prescaler.	0x03	
PCR23_0	Sets the port P23_0 to the input port TIA00.	0x00000058	Port setting
PSCR0	Sets the “2” to the division ration of the prescaler 0.	0x0001	ATU setting
NCMR	Sets the noise cancel function of timer A to the subsequent noise cancel.	0x00	
TIOR1A	Sets to capture the input at the rising/falling edge of the input signal from TIA00.	0x0003	
TSCRA	Clears the input capture flag of Timer A.	0x80FF	
NCMCR1A	Sets the noise cancel function of timer A of channel 0 to the subsequent noise cancel.	0x00	
TIOR2A	Enables the clock bus and operation of the noise cancel counter.	0x00000001	
NCRA0	Sets 0x0012 to the upper limit of noise cancellation counter.	0x0012	

2.5 Operation Ex. 4 Noise Cancel (Leading Edge Cancel) [Timer A]

2.5.1 Overview

As shown in Figure 2.7, the leading edge cancel function ignores level changes with a period less than a certain period to remove noise mixed with the input signal.

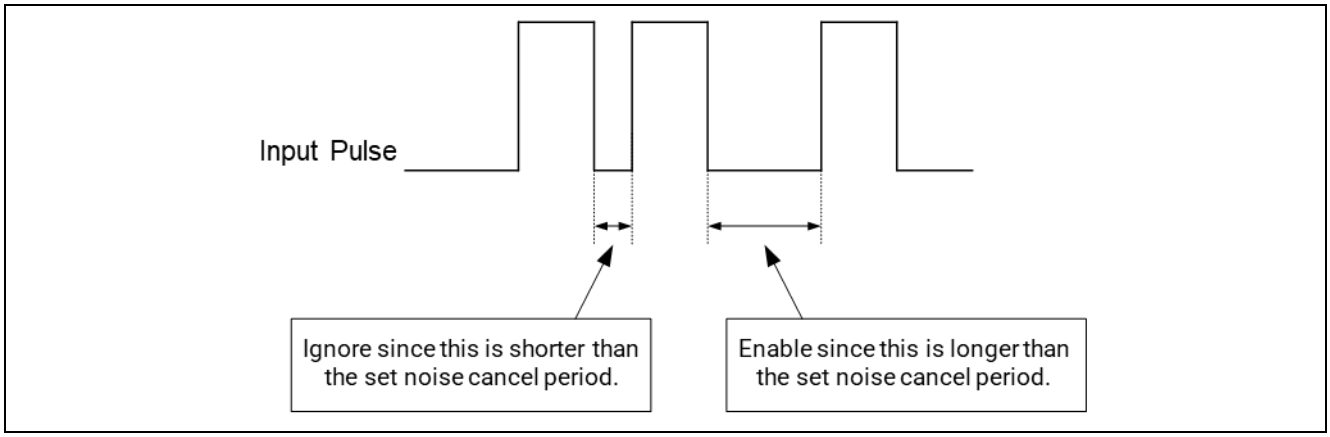


Figure 2.7 Conceptual Diagram of Subsequent Noise Cancellation

2.5.2 Explanation for Use Function

Table 2.4 shows the functions allocations of the ports used and related registers.

Table 2.4 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Inputs the pulse to be measured to this port.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	NCMR	Set the noise cancel operation mode and counter clock of each timer.
Timer A register	TIOR1A	Sets the edge to capture the external input.
	TIOR2A	Set the noise cancel enable/disbale and the clock of noise cancel.
	TSRA	The flag is set when the input capture is generated.
	TSCRA	Clears the flag of input capture generation.
	NCMCR1A	Sets the noise cancel opearion mode.
	NCMCR2A	Sets the noise cancel opearion mode.
	NCNTA0	The counting is stared at the same time as the edge input, and the noise cancellation period is measured.
	NCRA0	Sets the noise cancellation period.
PORT register	PCR23_0	Sets the port function.

2.5.3 Operation Example

Figure 2.6 shows the operation principle. In order to ignore the signal whose signal level is not high for the specified period or longer, capture the input signal after the compare match as a noise-canceled signal.

According to this, the subsequent noise cancel is performed by the processing of RH850/U2Bx hardware and software. (The figure shows an example of detecting a rising edge.)

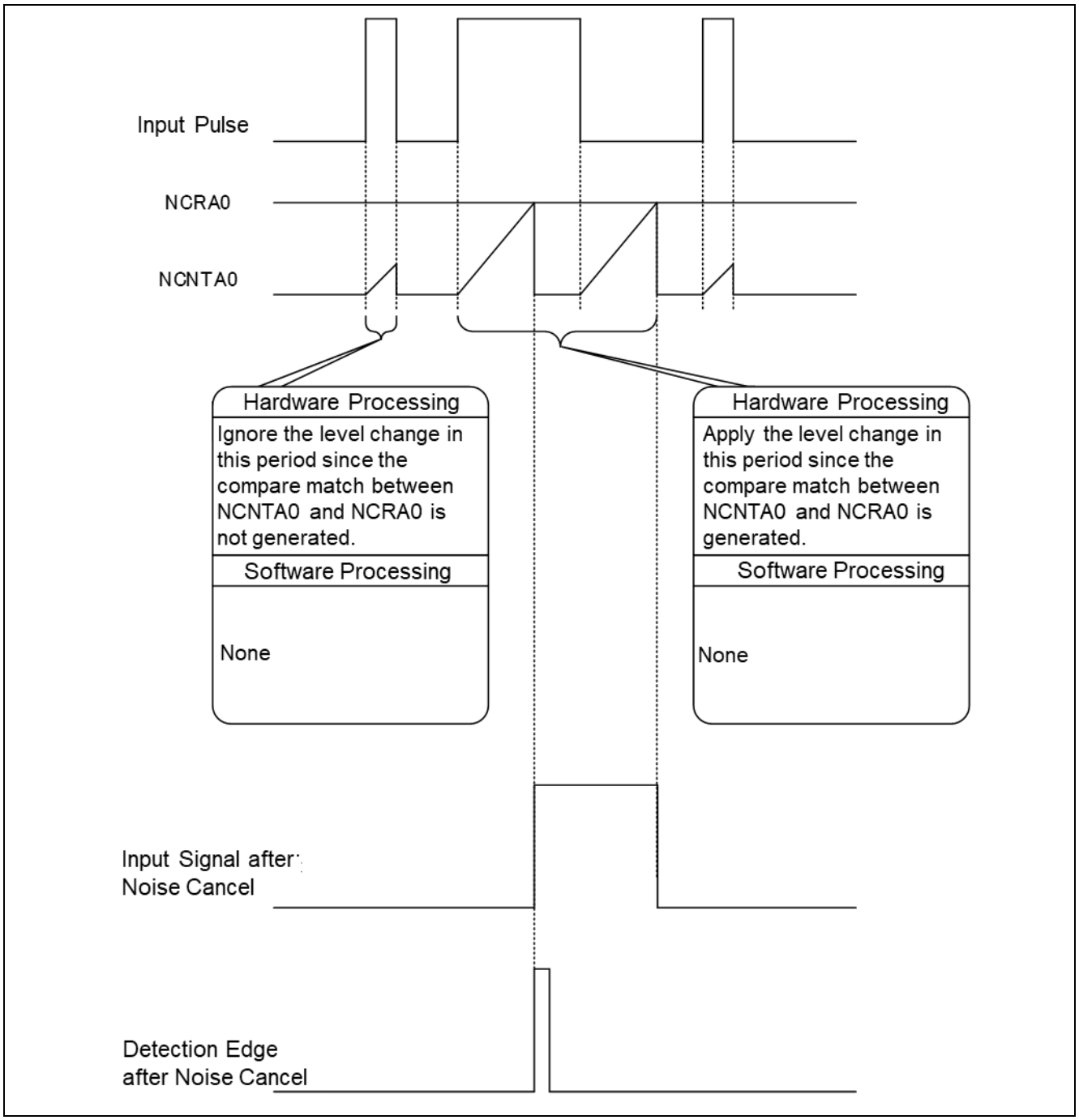


Figure 2.8 Operation Principle of Leading Noise Cancel

2.5.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Sets the port (P23_0) to the TIA00 input.
ATU setting	atu_init	Performs the initial setting of timer A

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of the timer A and the prescaler.	0x03	
PCR23_0	Sets the port P23_0 to the input port TIA00.	0x00000058	Port setting
PSCR0	Sets the “2” to the division ration of the prescaler 0.	0x0001	ATU setting
NCMR	Sets the noise cancel function of timer A to the leading noise cancel.	0x01	
TIOR1A	Set to capture the input at the rising edge of the input signal from TIA00.*	0x0001	
TSCRA	Clears the input capture flag of Timer A.	0x80FF	
NCMCR1A	Sets the noise cancel function of channel 0 to the leading noise cancel.	0x01	
NCMCR2A	Sets the noise cancel function of channel 0 to the leading noise cancel.	0x00	
TIOR2A	Enable the clock bus and operation of the noise cancel counter.	0x00000001	
NCRA0	Sets 0x0012 to the upper limit of noise cancellation counter.	0x0012	

*Since the level fluctuation after capture is monitored, set the level to be noise canceled in this register.

2.6 Operation Ex. 5 Noise Cancel (Level Accumulation Cancel) [Timer A]

2.6.1 Overview

Figure 2.9 shows the operation principle.

In the level accumulation cancel mode, the noise cancellation counter performs up-count or down-count operation according to the level of the input signal. The high level is output when the counter reaches the upper limit by the up count, and the low level is output when the counter reaches 0 by the down count. By this operation, the change of the input signal while the counter is up-counting or down-counting is regarded as noise and is eliminated.

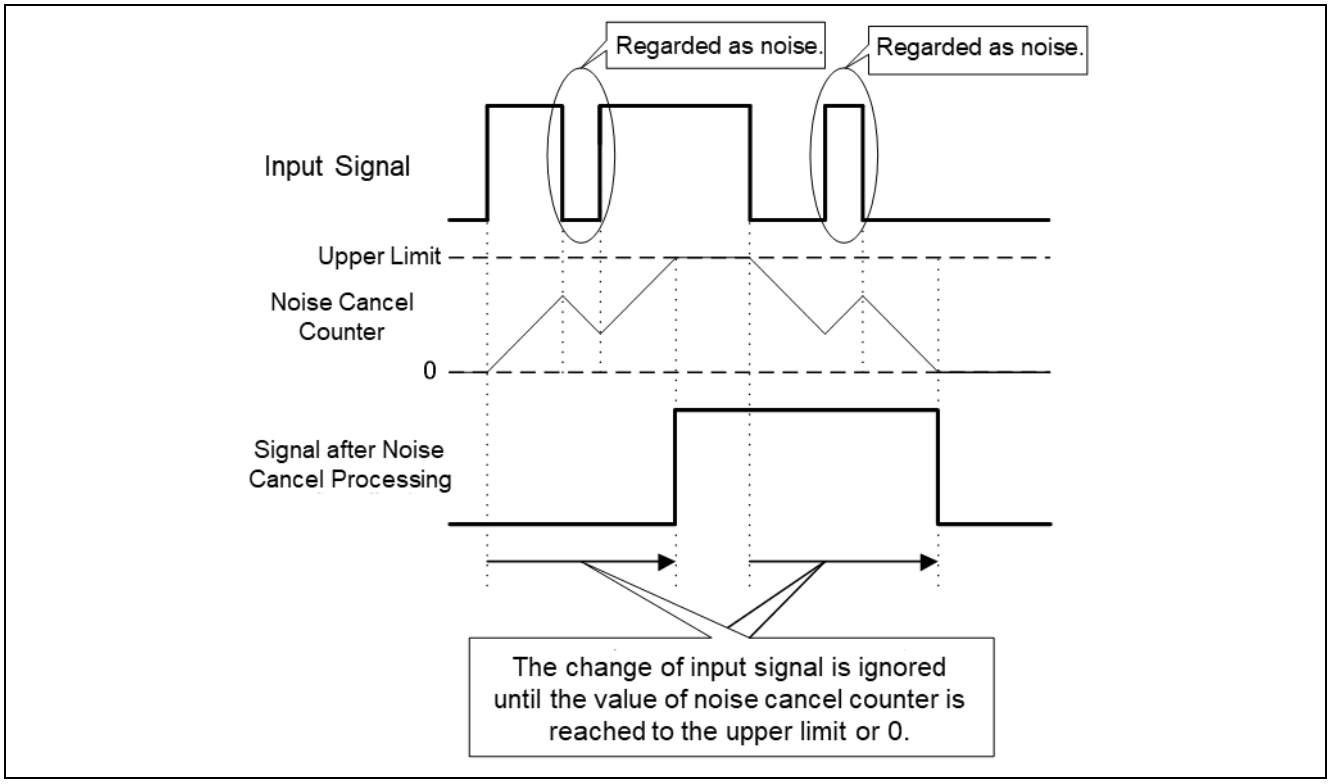


Figure 2.9 Operation Principle of Noise Cancel

2.6.2 Explanation for Use Function

Table 2.5 shows the functions allocations of the ports used and related registers.

Table 2.5 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Inputs the pulse to be measured to this port.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	NCMR	Set the noise canceling operation mode and count clock for each timer.
Timer A register	TIOR1A	Sets the edge to capture the external input.
	TIOR2A	Set the noise cancel function enbale/disbale and the clock for noise cancel.
	TSRA	The flag is set when the input capture is generated.
	TSCRA	Clears the flag of input capture generation.
	NCMCR1A	Sets the noise cancel operation mode.
	NCMCR2A	Sets the noise cancel operation mode.。
	NCNTA0	The counting is stared at the same time as the edge input, and the noise cancellation period is measured.
	NCRA0	Sets the noise cancellation period.
PORT register	PCR23_0	Sets the port function.

2.6.3 Operation Explanation

Figure 2.10 shows the operation principle. In the level accumulation cancel mode, the noise cancellation counter performs up-count or down-count operation according to the level of the input signal. If the counter counts up and matches the setting value of the noise cancel register NCRA0, the High level is outputted. If the counter counts down and matches with 0000H, the Low level is outputted.

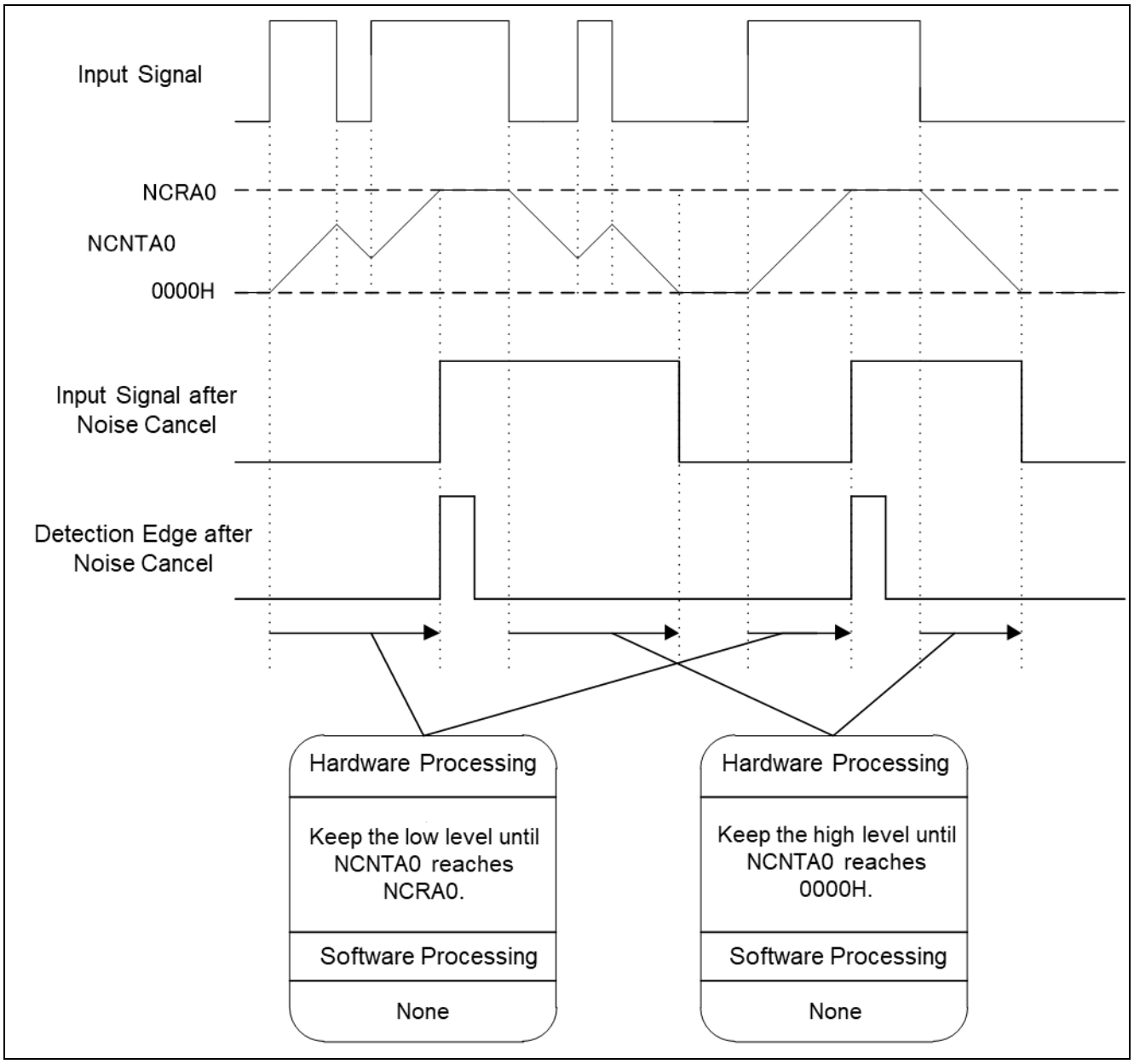


Figure 2.10 Operation Principle of Level Accumulation cancellation

2.6.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Sets the port (P23_0) to the TIA00 input.
ATU setting	atu_init	Performs the initial setting of timer A

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of the timer A and the prescaler.	0x03	
PCR23_0	Sets the port P23_0 to the input port TIA00.	0x00000058	Port setting
PSCR0	Sets the “1” to the division ration of the prescaler 0.	0x0000	ATU Setting
NCMR	The noise cancellation mode of timer A can be set for each channel.	0x00	
TIOR1A	Set to capture the input at the rising/falling edge of the input signal from TIA00.	0x0003	
TSCRA	Clears the input capture flag of Timer A.	0x80FF	
NCMCR1A	Sets the level accumulation cancel mode to the noise cancel mode of channel 0.	0x01	
NCMCR2A	Sets the level accumulation cancel mode to the noise cancel mode of channel 0.	0x01	
TIOR2A	Selects the noise cancel clock (128 division of internal peripheral clock) as the clock of noise cancel counter. Enables the noise cancel function of channel 0.	0x00000001	
NCRA0	Sets 0x927C to the upper limit of the noise cancellation counter.	0x927C	

2.7 Operation Ex. 6 Event Cycle Measurement [Timer C]

2.7.1 Overview

As shown in Figure 2.11, measure the event cycle and store the result to RAM. The cycle between events is measured to receive the event trigger from the outside n-times and divide the counter value between events by n.

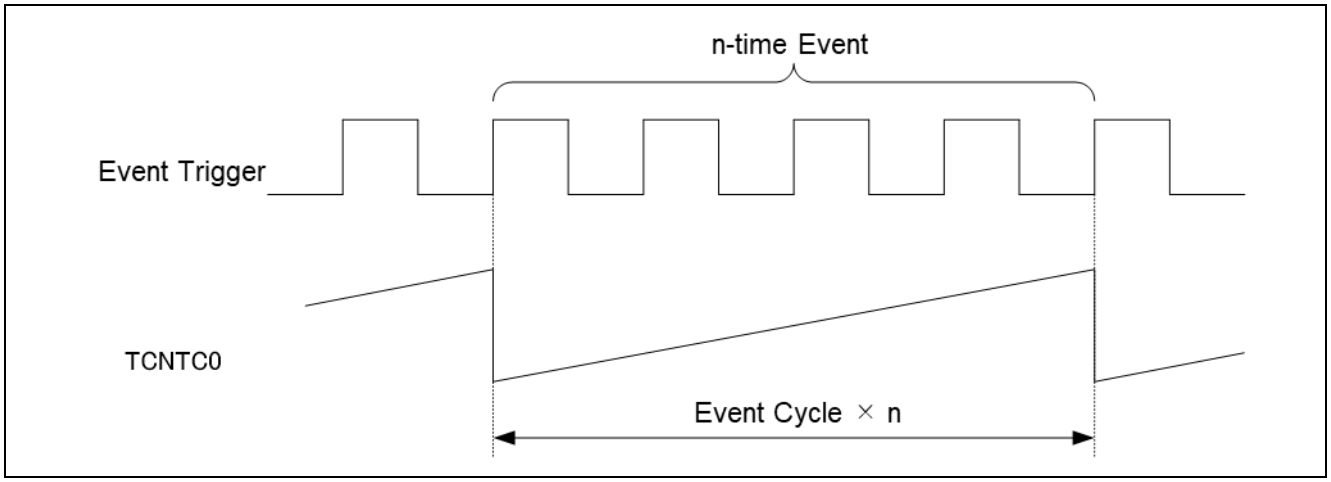


Figure 2.11 Event Cycle Measurement Timing

2.7.2 Explanation for Use Function

Table 2.6 shows the functions allocations of the ports used and related registers.

Table 2.6 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TCLKA	Inputs the pulse to be measured to this port.
	TIOC10	Uses as the output conpare outputport.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	CBCNT	Sets the external input signal provide to the clock bus 4 and 5.
Timer C register	TIORC1	Sets I/O control of Timer C.
	TIERC1	Sets enable/disable for the conpare match interrupt by GRC10.
	TSRC1	The flag is set in the conpare match generation by GRC10.
	TSCRC1	Clears the flag of the conpare match generation by GRC10.
	GRC10	Sets the conpare match value with TCNTC1.
	TSTRC	Enables/suspends the count operation of Timer C.
	TCNTC0	This is the counter for the period caliculation of Timer C.
	TIERC1	Performs the setting of the compare match interrupt.
	TCRC1	Sets Timer C operation.
PORT register	PCR32_5	Sets the port function.
	PCR34_0	Sets the port function.
INTC register	EIBD108	Specifies the binding destination of the compare match interrupt by GRC10.
	EIC108	Sets the interrupt vector method and the interrupt priority.

2.7.3 Operation Explanation

Figure 2.12 shows the operation principle. Perform the event period measurement by hardware and software processing of RH850/U2Bx. TIOC10 toggles output by compare match with GRC10 register.

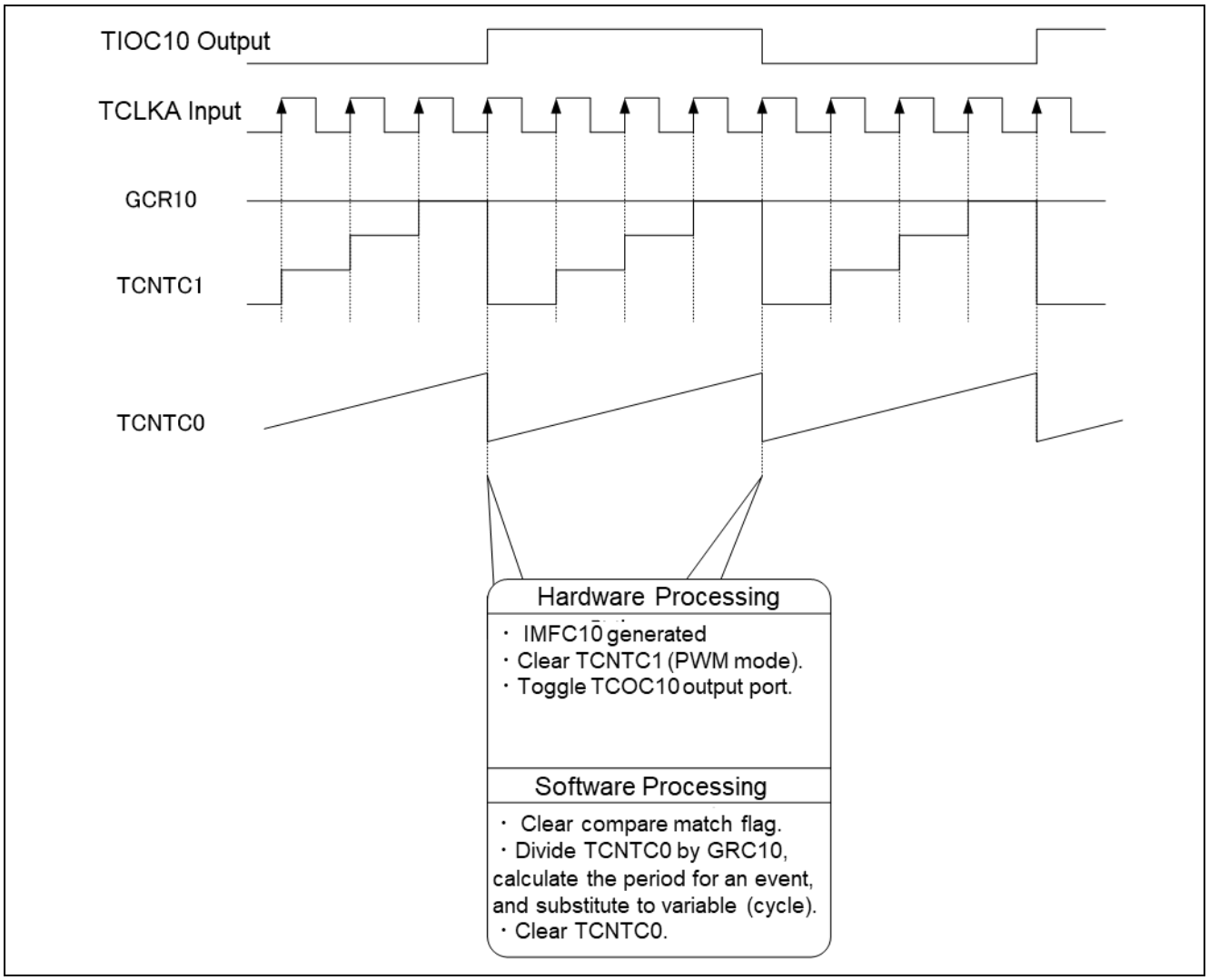


Figure 2.12 Operation Principle of Event Period Measurement

2.7.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Sets TCLKA input to port (P32_5), and TIOC10 output to port (P34_0).
ATU setting	atu_init	Performs the initial setting of Timer C.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Event period measurement	eiint108	Starting by IMFC10. Measuring the pulse period by the TCNTC0 value.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module
cycle	Stores the timer value corresponding to the event cycle. The event cycle can be calculated by the following equation. Event cycle (ns)=Timer value × Unmodulated slow clock period (25ns when operating at 40MHz) × 10 (Prescaler division ratio)	unsigned long	Pulse cycle mesurement

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer C and prescaler.	0x09	
PCR32_5	Sets the port P32_5 pin to TCLKA function (external input for clock bus 4).	0x00000058	Port setting
PCR34_0	Sets the port P34_0 pin to TIOC10 output.	0x00000049	
CBCNT	Specifies the edge of the external clock (TCLKA) to be output to clock bus 4 as the rising edge.	0x10	ATU setting
PSCR0	Sets the “10” to the division ration of the prescaler 0.	0x0009	
TCRC1	Operates subblock 1 in PWM mode and select TCLKA (clock bus 4) as the count clock.	0x000C	
TIERC1	Enables the compare match interrupt by GRC10.	0x0001	
TIORC1	Set to toggle output by compare match by GRC10 register.	0x0003	
GRC10	Sets the compare match value corresponding to TCNTC1.	0x0000500	
TSTRC	Enable the sub block 0 and 1 count operation of Timer C.	0x03	
EIBD108	Binds the compare match interrupt to PE0 (CPU0) by GRC10.	0x00000000	Interrupt setting
EIC108	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRC1	Clears the flag of the conpare match generation	0x0001	Event cycle measurement
TCNTC0	Clears the timer counter.	0x00000000	

2.8 Operation Ex. 7 Pulse Output (Toggled-output, Timer Count Clear) [Timer C]

2.8.1 Overview

As shown in Figure 2.13, generate the pulse by the toggle output in a constant period. For realizing this function, set PMW mode to the timer operation mode.

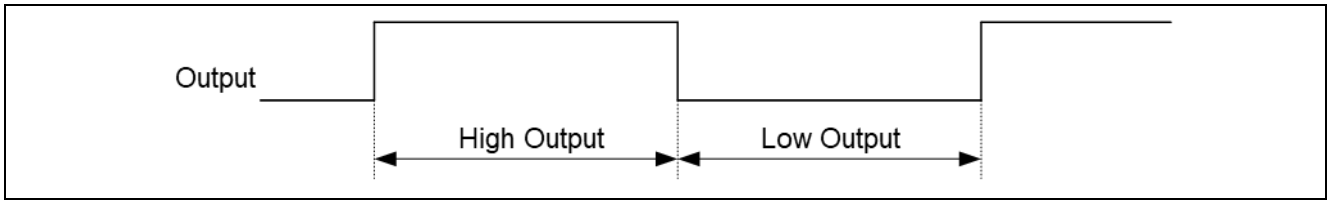


Figure 2.13 Toggled-output

2.8.2 Explanation for Use Function

Table 2.7 shows the functions allocations of the ports used and related registers.

Table 2.7 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIOC00	Output the pulse.
Related register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Set the division ration of the prescaler 0.
Timer C register	TIORC0	Set the Timer C function.
	TCRC0	Set the operation mode and clock bus of Timer C.
	GRC00	Set the cycle of toggle output.
	TSTRC	Set the counter operation of the each sub block of the Timer C.
PORT register	PCR00_4	Set the port function.

2.8.3 Operation Explanation

Figure 2.14 shows the operation principle. According to this, the pulse output is performed by the processing of RH850/U2Bx hardware and software. In PMW mode, TCNTC0 value is cleared as 0 when the compare match between TCNTC0 and GCR00 is generated, and TCNTC0 starts counter operation from 0 again.

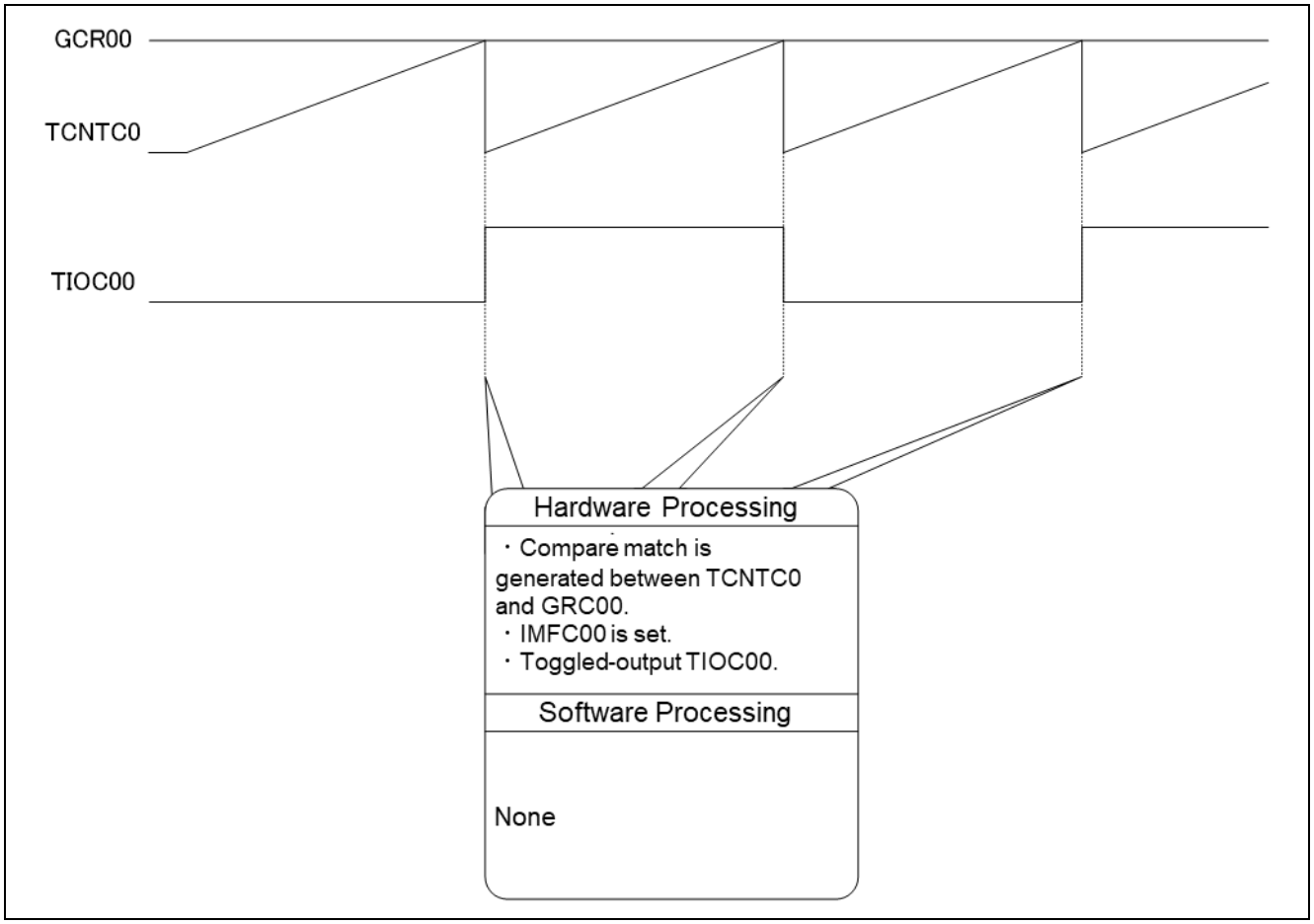


Figure 2.14 Operation Principle of Pulse Output

2.8.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Set the port (P00_4) to the TIOC00 input.
ATU setting	atu_init	Perform the initial setting of Timer C

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Release the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer C and prescaler.	0x09	
PCR00_4	Set the port P00_4 pin to TIOC00 output.	0x00000049	Port setting
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TCRC0	Perform the clock selection of Timer C sub block 0, the operation mode setting, and the forced compare match setting.	0x0008	
TIORC0	Set to toggle output by compare match by GRC00 register.	0x0003	
GRC00	Set the compare match value corresponding to TCNTC0.	0x00000050	
TSTRC	Enable to operate the count of sub block 0.	0x0001	

2.9 Operation Ex. 8 Pulse Output (Toggled-output, Compare Value Addition) [Timer C]

2.9.1 Overview

As shown in Figure 2.15, the pulse is generated by the toggle output with a constant cycle. In this operation example, pulse output is generated to update the switching timing between High and Low by adding the compare match value.

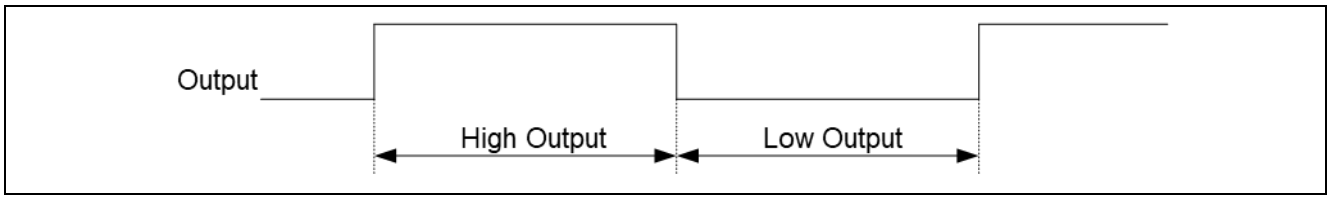


Figure 2.15 Toggled-output

2.9.2 Explanation for Use Function

Table 2.8 shows the functions allocations of the ports used and related registers.

Table 2.8 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIOC00	Output the pulse.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Set the division ration of the prescaler 0.
Timer C register	TIORC0	Set Timer C function.
	TIERC0	Set enable/disable for the input capture and conpare match interrupt
	TSRC0	Set the flag in the inputcapture and conpare match generation.
	TSCRC0	Clear the flag of the input capture and conpare match.
	GRC00	Set the cycle of toggle out put.
	TSTRC	Set the counter operation of the each sub block of the Timer C.
PORT register	PCR00_4	Set the port function.
INTC register	EIBD104	Specify the binding destination of the compare match interrupt by IMIC00.
	EIC104	Set the interrupt vector method and the interrupt priority.

2.9.3 Operation Explanation

Figure 2.16 shows the operation principle. According to this, the pulse output is performed by the processing of RH850/U2Bx hardware and software. When a compare match is generated between the timer counter TCNTC0 and the compare match register GRC00, it adds itself to GRC00.

In this operation example, the GRC00 value always increases constantly, so a pulse with a constant High / Low width is output.

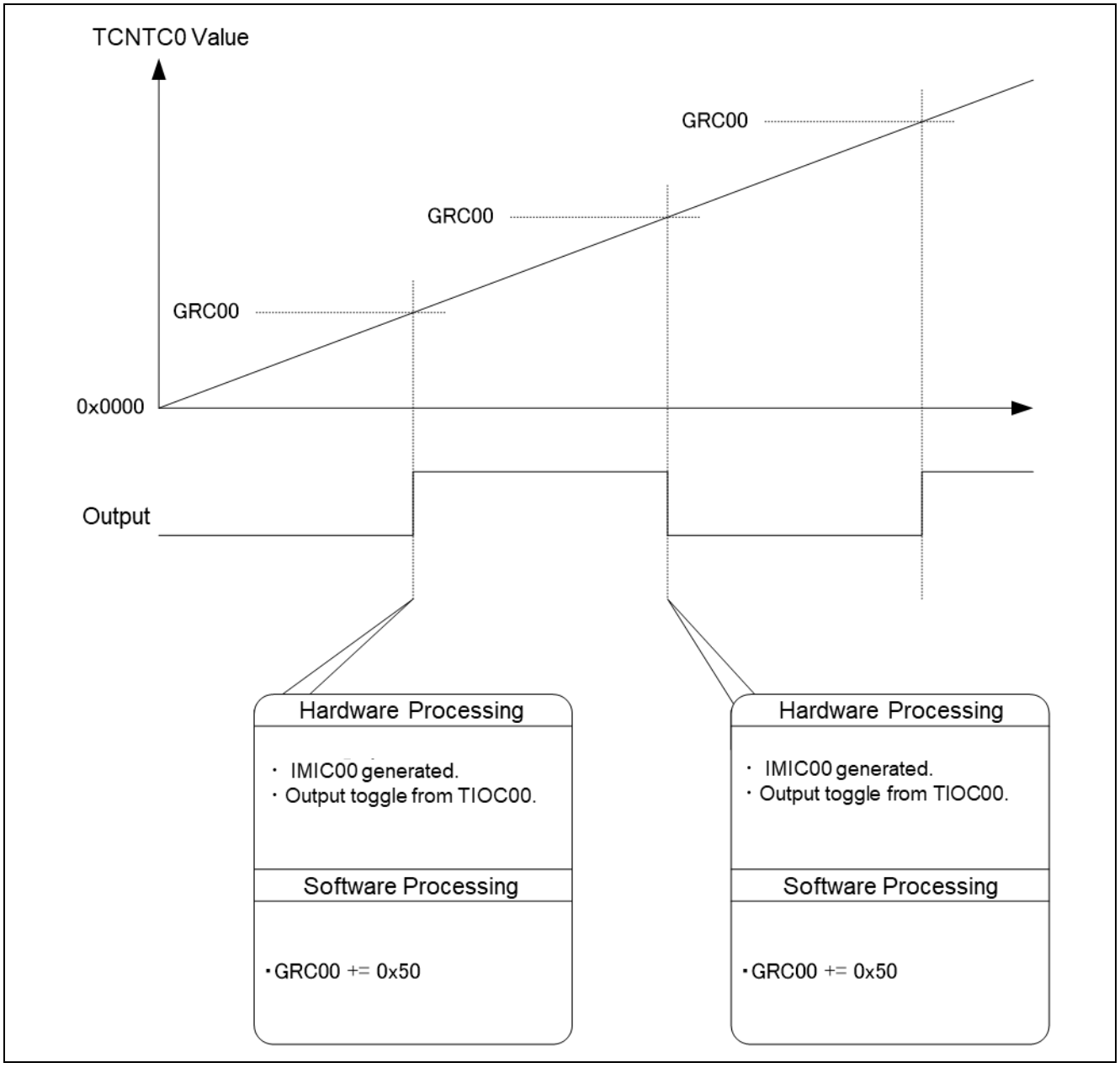


Figure 2.16 Operation Principle of Pulse Output

2.9.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Set the port (P00_4) to the TIOC00 input.
ATU setting	atu_init	Perform the initial setting of Timer C
Interrupt setting	intc_init	Perform the initial setting of interrupt function.
Re-compare match routine	eiint104	Enable to generate the compare match again to start by IMF, clear TSRC0, and add to the value of the general-purpose register GRC00.

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Release the ATU module standby.	0x00000000	Main routine
ATUENR	Enable the count operation of Timer C and prescaler.	0x09	
PCR00_4	Set the port P00_4 pin to TIOC00 output.	0x00000042	Port setting
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TIORC0	Set to toggle output by compare match by GRC00 register.	0x0003	
TIERC0	Enable the compare match interrupt corresponding to GRC00.	0x0001	
GRC00	Set the compare match value corresponding to TCNTC0.	0x00000050	
TSTRC	Enable to operate the count of sub block 0.	0x0001	
EIBD104	Bind the compare match interrupt to PE0 (CPU0) by GRC00.	0x00000000	Interrupt setting
EIC104	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRC0	Clear the compare match flag by GRC00.	0x0001	Re-compare match routine
GRC00	Set the compare match value corresponding to TCNTC0.	+= 0x00000050	

2.10 Operation Ex. 9 Pulse Output (High/Low Switching Output, Compare Value Addition) [Timer C]

2.10.1 Overview

As shown in Figure 2.17, the pulse is generated by the toggle output with a constant cycle.

In this operation example, the high and low switching timing of the port output is updated by the compare match value addition of the timer.

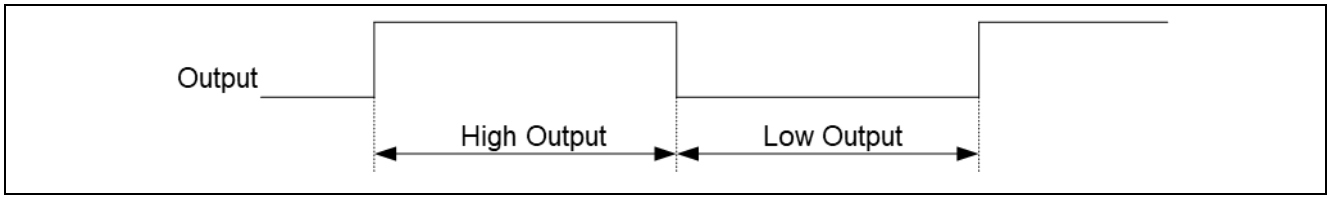


Figure 2.17 Toggled-output

2.10.2 Explanation for Use Function

Table 2.9 shows the functions allocations of the ports used and related registers.

Table 2.9 ATU-VI Function Allocation

Use Port		Function
Port	P30_0	Output the pulse of the set level.
Related Register		Function
ATU-VI common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Set the division ration of the prescaler 0.
Timer C register	TIORC0	Set Timer C function.
	TIERC0	Set enable/disable for the input capture and conpare match interrupt
	TSRC0	Set the flag in the inputcapture and conpare match generation.
	TSCRC0	Clear the flag of the input capture and conpare match.
	GRC00	Set the compare match cycle.
	TSTRC	Set the counter operation of the each sub block of the Timer C.
PORT register	PCR11_0	Set the Input/output direction of P11_0 port and output level.
INTC register	EIBD104	Specify the bind destination of IMIC00 input capture interrupt.
	EIC104	Set the interrupt vector method and the interrupt priority.

2.10.3 Operation Explanation

Figure 2.2 shows the operation principle. According to this, the pulse period measurement is performed by the hardware and software processing of RH850/U2Bx. When a compare match is generated between the timer counter TCNTC0 and the compare match register GRC00, it adds itself to GRC00.

In this operation example, the GRC00 value always increases constantly, so a pulse with a constant High / Low width is output.

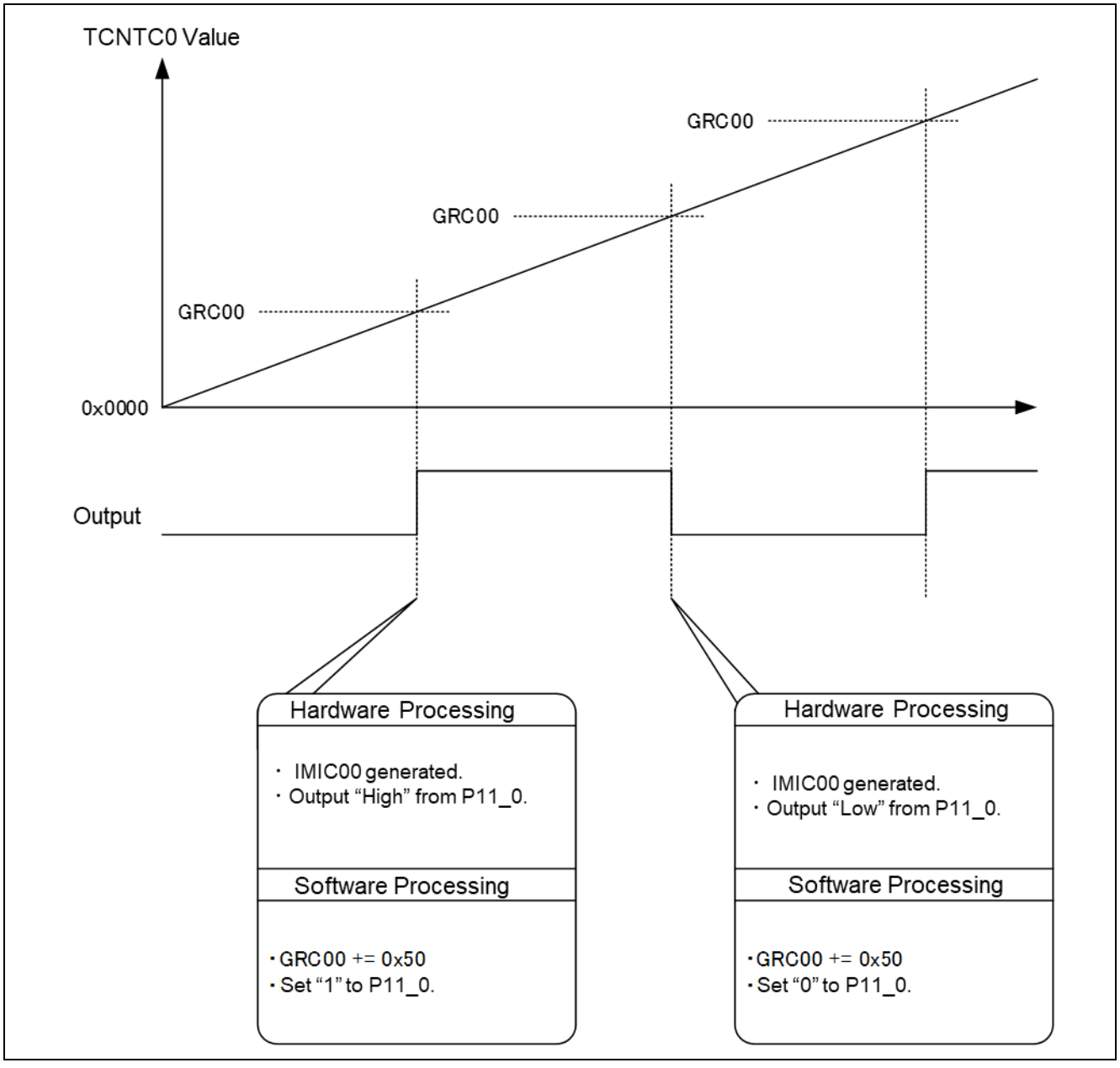


Figure 2.18 Operation Principle of Pulse Output

2.10.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Set the port (P30_0) to the output port.
ATU setting	atu_init	Perform the initial setting of Timer C
Interrupt setting	intc_init	Perform the initial setting of interrupt function.
Output switching routine	eiint104	Start by IMFC00, switch the output level of P30_0, and perform the processing for re-compare match.

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Release the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer C and prescaler.	0x09	
PCR11_0	Set the port P11_0 pin to general purpose output and set “Low” to the output initial value.	0x00000000	Port setting
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TIORC0	Set the compare match by GRC00, and the operation in the compare match generation.	0x0003	
TIERC0	Enable the compare match interrupt corresponding to GRC00.	0x0001	
GRC00	Set the compare match value corresponding to TCNTC0.	0x00000050	
TSTRC	Enable to operate the count of sub block 0.	0x01	
EIBD104	Bind the compare match interrupt to PE0 (CPU0) by GRC00.	0x00000000	Interrupt setting
EIC104	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRC0	Clear the compare match value by GRC00.	0x0001	Output switching routine
GRC00	Update the compare match value corresponding to TCNTC0.	+=0x00000050	
P11	Set the output value of Port11_0.	Low output：0x00000000 High output：0x00000001	

2.11 Operation Ex.10 One-shot Pulse Output (with Offset) [Timer C]

2.11.1 Overview

As shown in Figure 2.19, a one-shot pulse with offset is outputted in synchronization with the rising edge of the external signal. In this operation example, the offset time and pulse width can be changed within the range shown below.

3.3 μs(Pulse setting routine execution time) ＜ Offset time
＜ 100ns (Prescaler output cycle setting value) × 0xFFFFFFFF (Timer C counter maximum value)

100ns (Prescaler output cycle setting value) <= Pulse width
< 100ns (Prescaler output cycle setting value) × 0xFFFFFFFF (Timer C counter maximum value)

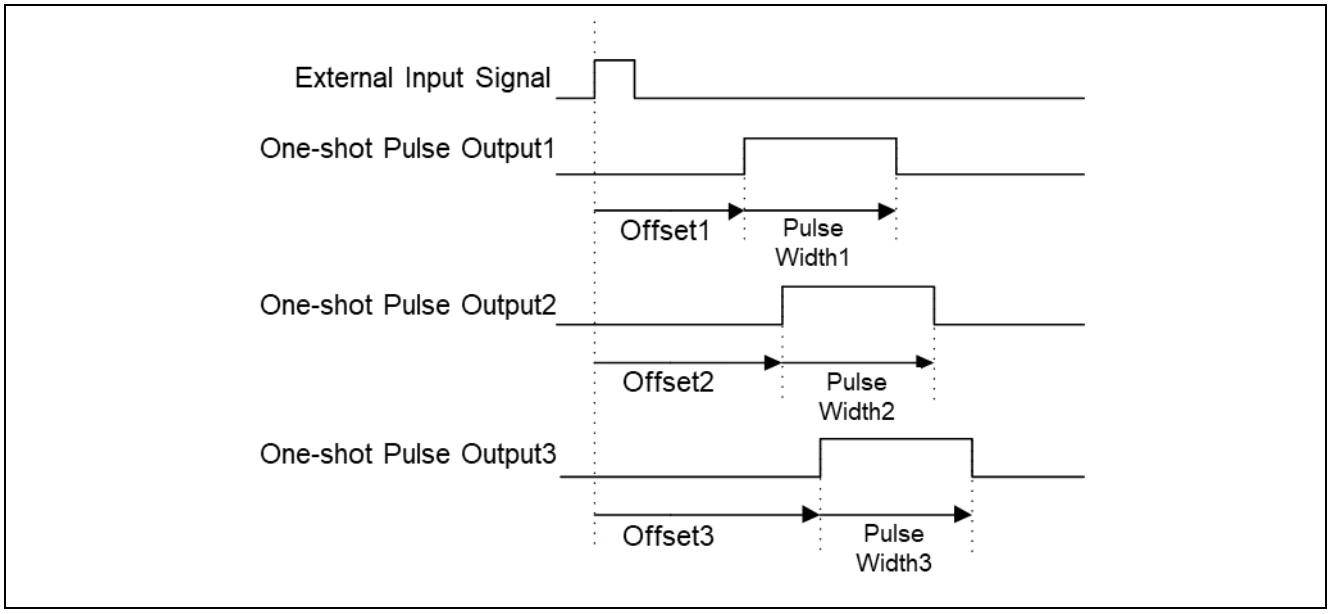


Figure 2.19 One-shot Pulse Output with Offset

2.11.2 Explanation for Use Function

Table 2.10 shows the functions allocations of the ports used and related registers.

Table 2.10 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIOC20	Input the extaernal signal.
	TIOC21	Output the one-shot pulse 1.
	TIOC22	Output the one-shot pulse 2.
	TIOC23	Output the one-shot pulse 3.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR3	Set the division ration of the prescaler 3.
Timer C register	TIORC2	Set the input/output function of Timer C
	TIERC2	Set the enable/disable of input capture/compare match.
	TCRC2	Perform the forced caompare match, and set the clock bus.
	TSRC2	The flag is set in input capture/compare match generation.
	TSCRC2	Clear the flag of the input capture/conpare match.
	GRC20	The value input-captured is stored.
	OCRC21, OCRC22, OCRC23	Set the output start timing of the one-shot pulse.
	GRC21, GRC22, GRC23	Set the output end timing of the one-shot pulse.
	TSTRC	Set the counter operation of the each sub block of the Timer C.
PORT register	PCR20_0, PCR20_1, PCR20_2, PCR20_4	Set the port function of the Port P20_0, P20_1, P20_2, and P20_4.
INTC register	EIBD112	Specify the bind destination of IMIC20 input capture interrupt.
	EIC112	Set the interrupt vector method and the interrupt priority.

2.11.3 Operation Explanation

Figure 2.20 shows the operation principle. According to this, the one-shot pulse output is performed by the hardware and software processing of RH850/U2Bx.

The different offset time and pulse width for each channel is possible to set by setting the expecting value of OCRC register and GRC register for each channel. In addition, the active level of the pulse can be selected from high active and low active. In this operation example, low active is set.

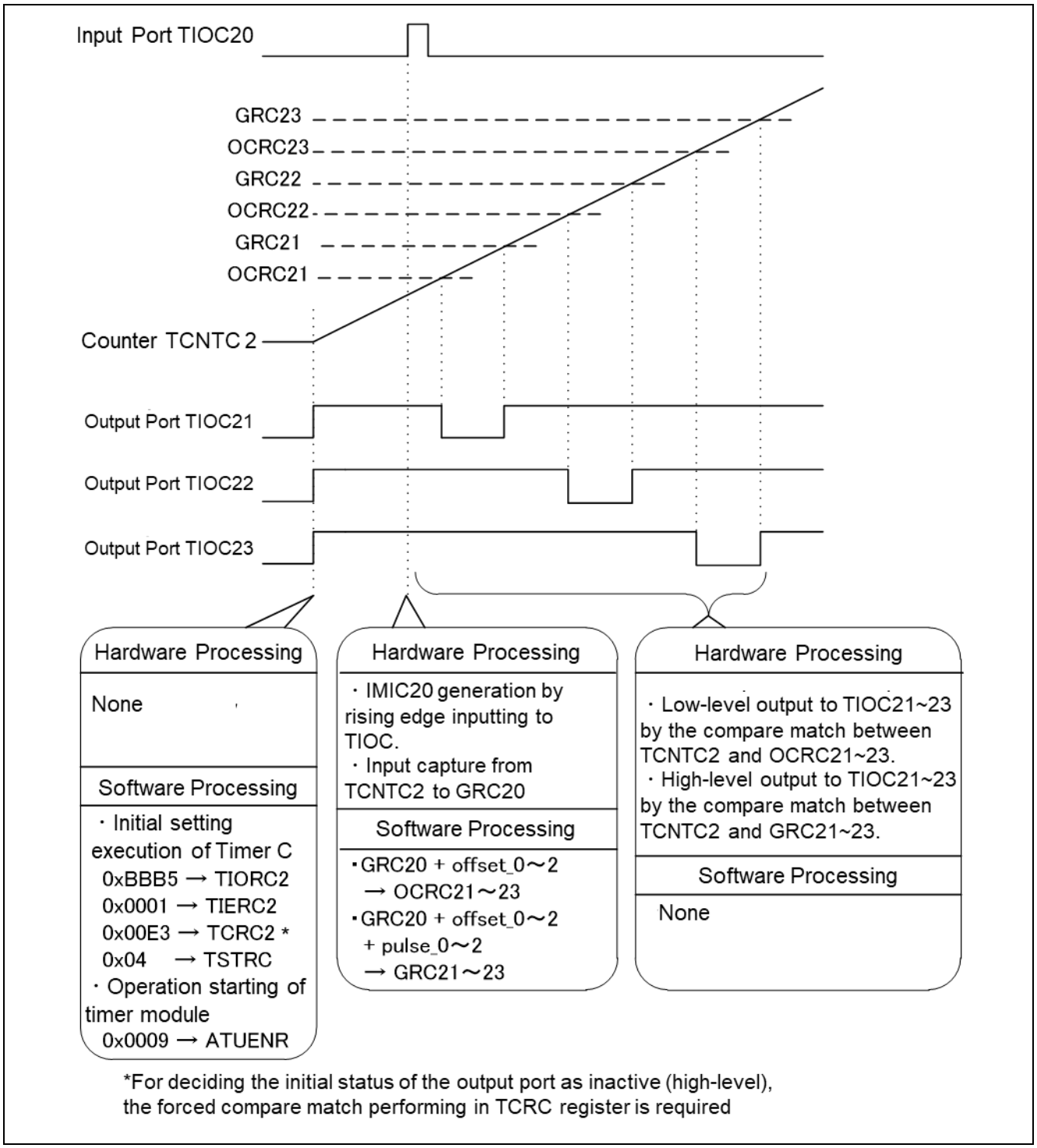


Figure 2.20 Operation Principle of One-shot Pulse Output

2.11.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Perform the port setting. (P33_0~P33_3)
ATU setting	atu_init	Perform the initial setting of Timer C.
Interrupt setting	intc_init	Perform the initial setting of interrupt function.
Pulse setting routine	eiint112	Set the offset time and pulse width of the one-shot pulse that is started and outputted by IMFC20.

Explanation for Use Macro

Label Name	Function	Setting Value	Use Module Name
offset_0	Set the offset time of the pulse outputted to TIOC21.	0x00000064	Pulse setting routine
offset_1	Set the offset time of the pulse outputted to TIOC22.	0x000000C8	Pulse setting routine
offset_2	Set the offset time of the pulse outputted to TIOC23.	0x0000012C	Pulse setting routine
pulse_0	Set the pulse width outputted to TIOC21.	0x000000C8	Pulse setting routine
pulse_1	Set the pulse width outputted to TIOC22.	0x000000C8	Pulse setting routine
pulse_2	Set the pulse width outputted to TIOC23.	0x000000C8	Pulse setting routine

Explanation for Use Variable

Not use the variable in this task

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Release the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer C and prescaler.	0x09	
PCR20_0	Set the port P20_0 to the TIOC20 output.	0x00000059	Port setting
PCR20_1, PCR20_2, PCR20_4	Set the port P20_1, P20_2, and P20_4 to the TIOC21, TIOC22, and TIOC23 output.	0x00000049	
PSCR3	Set the “4” to the division ration of the prescaler 3.	0x0003	ATU setting
TIORC2	TIOC20 への立ち上がりエッジ入力でインプットキャプチャ、TIOC21,22,23 をワンショットパルス出力モード(アクティブロウ)に設定します。	0xBBB5	
TIERC2	Enable the input capture of TIOC20.	0x0001	
TCRC2	Perform the compare match for GRC21, GRC 22, and GRC23 to be decided the initial status of the one-shot pulse output port as in-active (active-low). Disable the PMW mode. Select clock bus 3 to the counter clock.	0x00E3	
TSCRC2	Clear the status register.	0x0F1F	
TSTRC	Enable the counter operation of the sub block 2.	0x0004	
EIBD112	Bind the input capture interrupt IMIC20 corresponding to TIOC20 to PE0 (CPU0).	0x00000000	Interrupt setting
EIC112	Set the table reference method and interrupt priority method 0.	0x0040	
OCRC21	Set 10us to the offset time of the one-shot pule outputted form TIOC21.	GRC20 + offset_0(0x00000064)	Pulse setting routine
OCRC22	Set 20us to the offset time of the one-shot pule outputted form TIOC22.	GRC20 + offset_1(0x000000C8)	
OCRC23	Set 30us to the offset time of the one-shot pule outputted form TIOC23.	GRC20 + offset_2(0x0000012C)	
GRC21	Set 20us to the pulse width of the one-shot pule outputted form TIOC21.	GRC20 + offset_0(0x00000064) + pulse_0(0x000000C8)	
GRC22	Set 20us to the pulse width of the one-shot pule outputted form TIOC22.	GRC20 + offset_1(0x000000C8) + pulse_1(0x000000C8)	
GRC23	Set 20us to the pulse width of the one-shot pule outputted form TIOC23.	GRC20 + offset_2(0x0000012C) + pulse_2(0x000000C8)	
TSCRC2	Clear the flag of the input capture generation.	0x0001	

2.12 Operation Ex.11 One-shot Pulse Output (with Offset) [Timer D]

2.12.1 Overview

1） As shown in Figure 2.21, a one-shot pulse with offset is outputted in synchronization with the rising edge of the external signal. The offset and pulse width set the internal clock count value.

2) In this operation example, the offset and pulse width by external signal rising can be changed within the range shown below.

2.5μs＜Offset＜250ns (Prescaler output cycle)×65535
250ns (Prescaler output cycle) <= Pulse width < 250ns (Prescaler output cycle)×65535

Note: The offset should be smaller than the external signal cycle, and longer than the execution time of the offset setting routine (about 2.5μs).

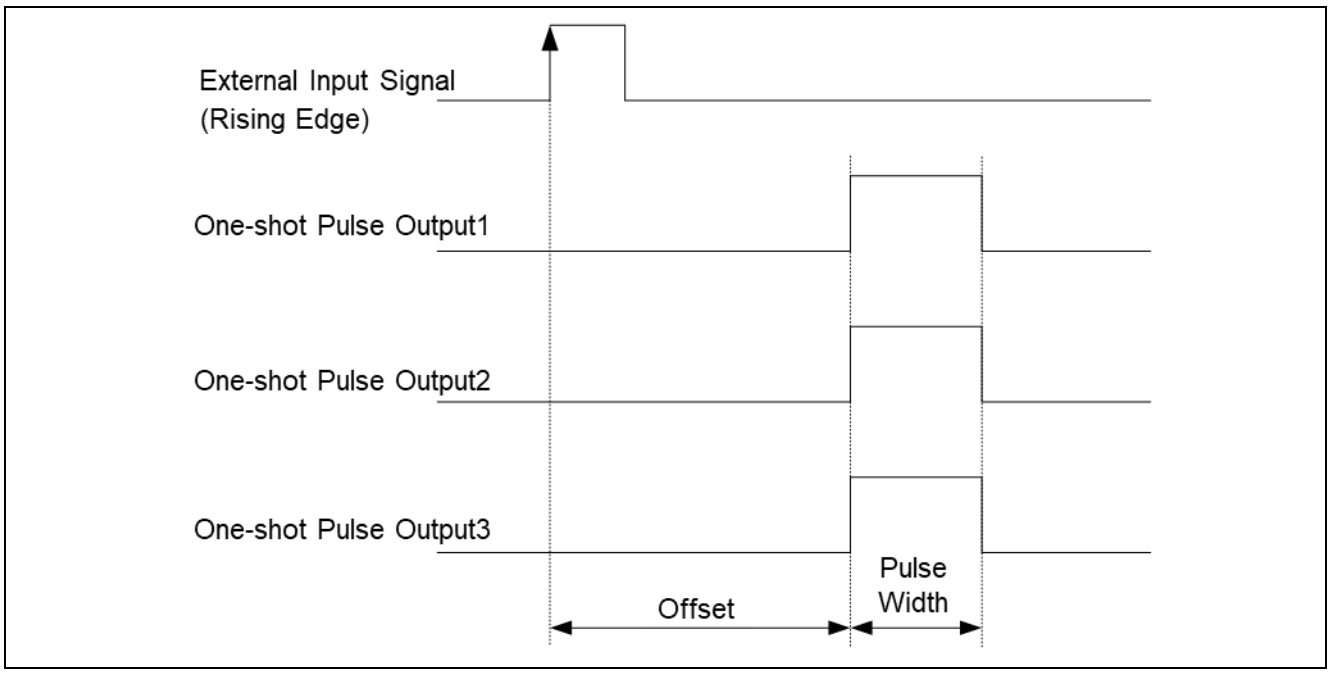


Figure 2.21 One-shot Pulse Output

2.12.2 Explanation for Use Function

Table 2.11 shows the functions allocations of the ports used and related registers.

Table 2.11 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Input the external signal for starting.
	TOD00B～02B	Output the on-shot pulse.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Set the division ration of the prescaler 0.
Timer A register	TIOR1A	Set the edge destination of external input to capture.
	TCR3A	Perform the extended settings for the event output 2A.
	TSRA	The flag is set if the input capture of the external input is generated.
	TSCRA	Clear the flag of input capture generation.
	TIERA	Set the input capture interrput setting.
Timer D register	OSBRD0	Capture the value of the timer count TCNT1D0 by the trigger signal from Timer A.
	TIOR1D0	Perform the enable for the compare match coresponding OCR1D00, and set the operation for copare match generation.
	DCRD0	Set the down-count start and stop conditions.
	TSRD0	The flag is set if the compare match and over/under flow is generated.
	TSCRD0	Clear the Timer D flag.
	TSTRD	Set the counter operation of the each sub block of the Timer D.
	OCR1D00～02	The output compare register of Timer D.
	DCNTD00～02	The down-count of Timer D.
INTC register	EIBD86	Specify the bind destination of TIA00 input capture interrupt.
	EIC86	Set the interrupt vector method and the interrupt priority.
PORT fregister	PCR23_0	Set the port function of the Port P23_0.
	PCR22_7, PCR22_6, PCR22_9	Set the port function of the Port P22_7, P22_6, and P22_9.

2.12.3 Operation Explanation

Figure 2.22 shows the operation principle. According to this, the one-shot pulse output is performed by the hardware and software processing of RH850/U2Bx. One-shot pulses with different waveforms are generated to perform the three compare registers setting corresponding the timer and the down count length setting.

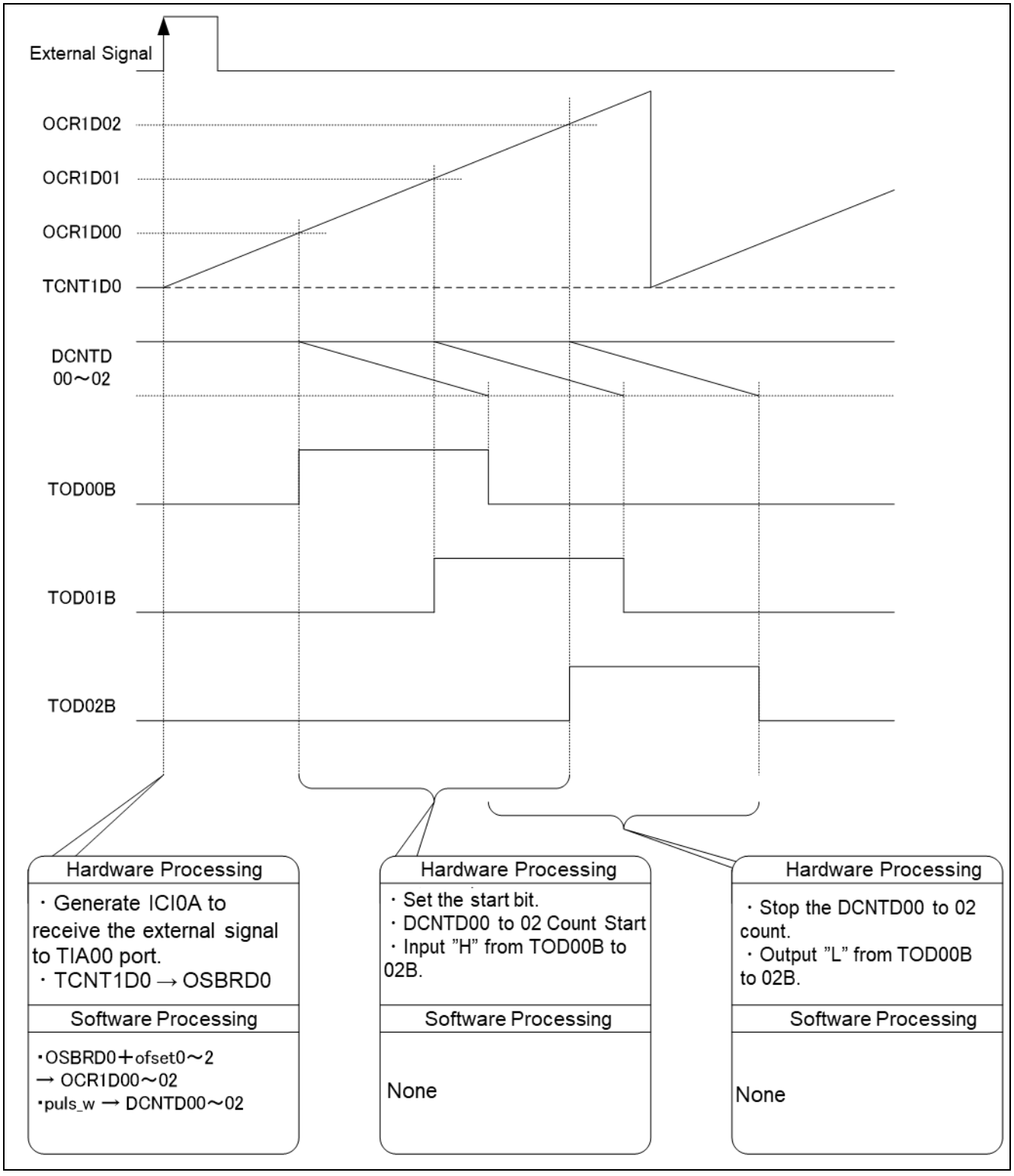


Figure 2.22 Operation Principle of One-shot Pulse Output Operation

2.12.4 Software Explanation

Module Explanation

Module Name	Rebel Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Perform the port setting. (P23_0, P22_4, P22_5, and P22_7)
ATU setting	atu_init	Perform the initial setting of Timer A and D.
Interrupt setting	intc_init	Perform the initial setting of interrupt function.
One-shot pulse output routine	eiint86	Start by ICFA0, set the offset and pulse width, and output the one-shot pulse.

Explanation for Use Constant

Label Name	Function	Data Length	Use Module Name
ofset0～2	Set the timer value corresponding to the offset of the one-shot pulse. The offset is calculated by the following formula. Offset (ns)=Timer Value × Unmodulated slow clock period (25ns when operating at 40MHz) × 10 (Prescaler division ratio)	unsigned short	One-shot pulse output
puls_w	Set the timer value corresponding to the pulse width of the one-shot pulse. The pulse width is calculated by the following formula. Pulse width (ns)=Timer Value × Unmodulated slow clock period × 10 (Prescaler division ratio)	unsigned short	

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Release the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A,D and prescaler.	0x13	
PCR23_0	Set the port P23_0 pin to TIA00 output.	0x00000058	Port setting
PCR22_7, PCR22_6, PCR22_9	Set P22_7, P22_6, and P23_0 to TOD00B, 01B, and 02B. output.	0x0000004B	
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TCR3A	Set the event output 2A to the input edge of TIA0.	0x8001	
TIOR1A	Set to input capture to ICRA0 at the rising edge of TIA0.	0x0001	
TSCRA	Clear the Timer A flag.	0x80FF	
TIERA	Set the TIA00 input capture interrupt enable.	0x0001	
TIOR1D0	Set the compare match factor of Timer D OCR1D00 to 02.	0x0153F	
DCRD0	Set the compare match of OCR1D00 to 02 to the down-count start trigger.	0x0222	
TSCRD0	Clear the Timer D flag.	0x3FFF	
TSTRD	Enable the operation of Timer D sub block 0.	0x0001	
EIBD86	Bind the TIA00 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC86	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRA	Clear the input capture flag of Timer A.	0x0001	One-shot pulse output routine
OCR1D00～02	Set the offset of the one-shot pulse.	OSBRD0 + ofset0～2	
OSBRD0	TCNT1D0 value is transferred by TIA00 input capture.	—	
DCNTD00～02	Set the pulse width of one-shot pulse.	Puls_w	

2.13 Operation Ex.12 One-shot Pulse Output (with Offset and Terminate) [Timer D]

2.13.1 Overview

1） As shown in Figure 2.23, a one-shot pulse with offset is outputted in synchronization with the rising edge of the external signal. The offset and pulse width set the internal clock count value.

2) End the pulse output forcibly and control the pulse width by the DCRD register setting.

3） In this operation example, the offset and pulse width by external signal rising can be changed within the range shown below.

3.5μs＜ Offset ＜250ns (Prescaler output cycle)×65535
250ns (Prescaler output cycle) <= Pulse Width < 250ns (Prescaler output cycle)×65535

Note: The offset should be smaller than the external signal cycle, and longer than the execution time of the offset setting routine (about 3.5μs).

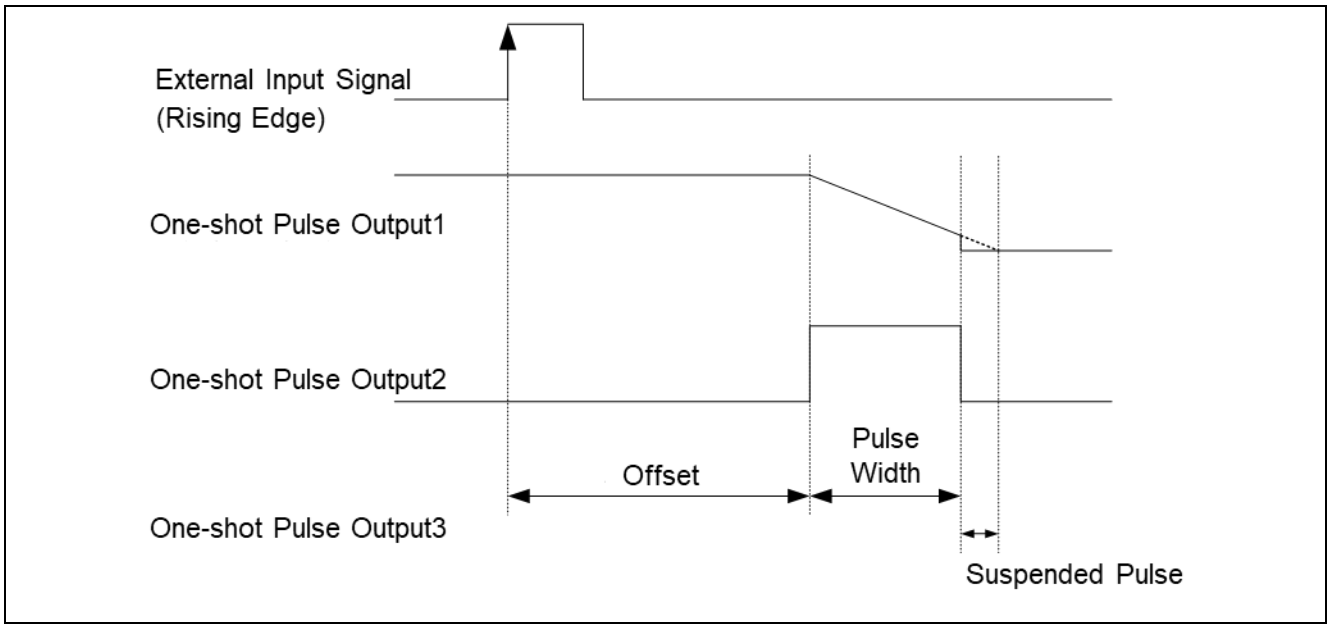


Figure 2.23 One-shot Pulse Output

2.13.2 Explanation for Use Function

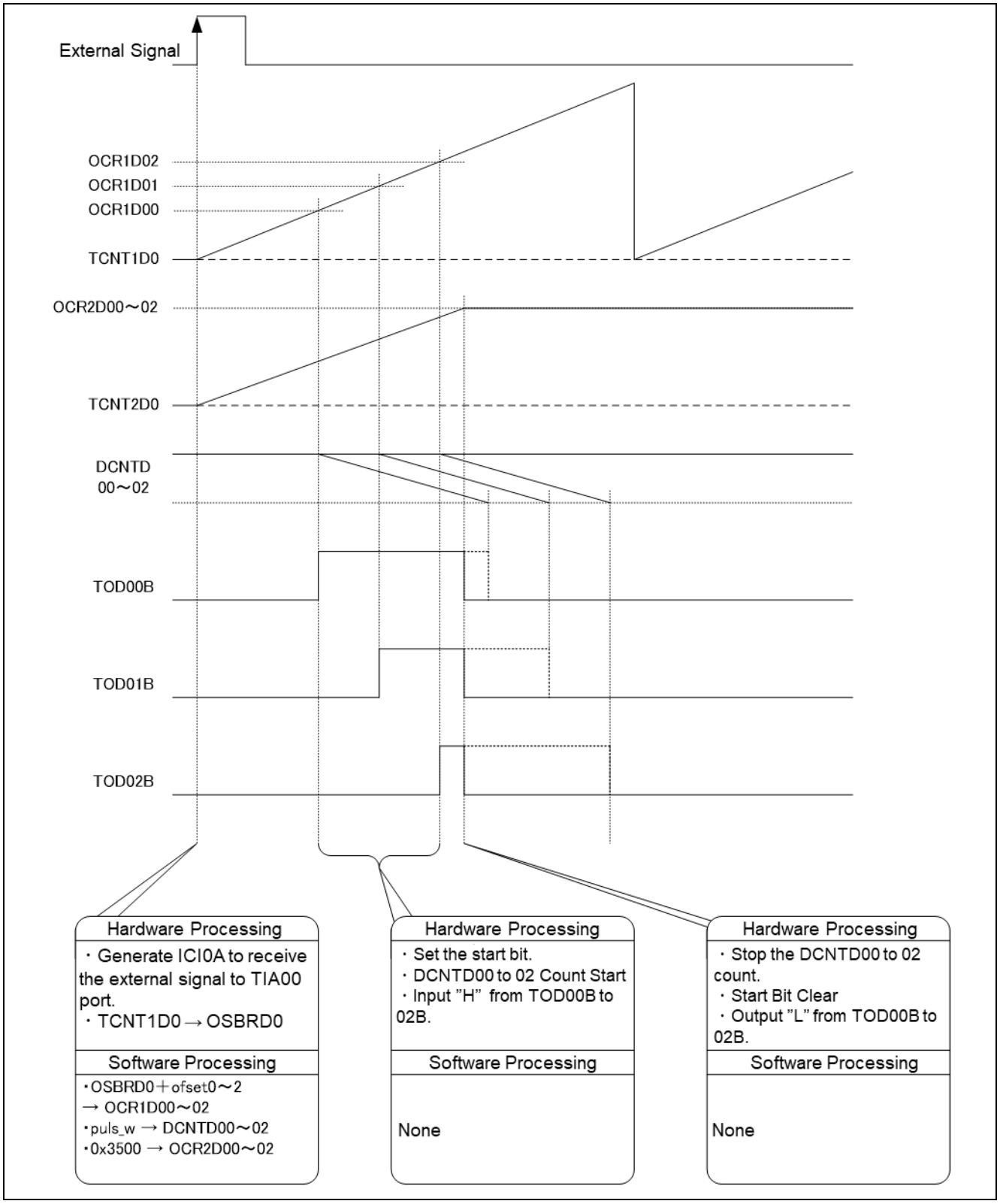
Table 2.12 shows the functions allocations of the ports used and related registers.

Table 2.11 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Input the external signal for starting.
	TOD00～02B	Output the on-shot pulse.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Set the operation of each timer and prescaler.
	PSCR0	Set the division ration of the prescaler 0.
Timer A register	TIOR1A	Set the edge destination of external input to capture.
	TCR3A	Perform the extended settings for the event output 2A.
	TSRA	The flag is set if the input capture of the external input is generated.
	TSCRA	Clear the flag of input capture generation.
	TIERA	Set the input capture interrput setting.
Timer D register	OSBRD0	Capture the value of the timer count TCNT1D0 by the trigger signal from Timer A.
	TIOR1D0	Perform the enable for the compare match and set the operation for copare match generation coresponding OCR1D00 to 02.
	TIOR2D0	Set the OCR2D00 to 02 function.
	DCRD0	Set the start/stop comdition of the down-count.
	OCR1D00～02	Output compare register of Timer D.
	OCR2D00～02	Output compare register of Timer D.
	DCNTD00～02	Down-conter of Timer D.
	TSRD0	The flag is set if the compare match and over/under flow is generated.
	TSCRD0	Clear the Timer D flag.
	TSTRD	Set the counter operation of the sub block of the Timer D.
INTC register	EIBD86	Specify the bind destination of TIA00 input capture interrupt.
	EIC86	Set the interrupt vector method and the interrupt priority.
PORT register	PCR23_0	Set the port function of the Port P23_0.
	PCR22_7, PCR22_6, PCR22_9	Set the port function of the Port P22_7, P22_6, and P22_9.

2.13.3 Operation Explanation

Figure 2.24 shows the operation principle. According to this, the one-shot pulse output is performed by the hardware and software processing of RH850/U2Bx. Set the period until the forced termination (Low level output) of the one-shot pulse output by adjusting the length of the down-counter.



Figurte 2.24 Operation Principle of One-shot Pulse Output Operation

2.13.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and application start.
Port setting	port_init	Perform the port setting. (P23_0, P22_4, P22_5, and P22_7)
ATU setting	atu_init	Perform the initial setting of Timer A and D.
interrupt setting	intc_init	Perform the initial setting of interrupt function.
One-shot pulse output	eiint86	Start by ICFA0, set the offset period, terminate period, and pulse width, and output the one-shot pulse.

Explanation for Use Constant

Label Name	Function	Data Length	Use Module Name
Ofset0～2	Set the timer value corresponding to the offset of the one-shot pulse. The offset is calculated by the following formula. Offset (ns)=Timer Value × Unmodulated slow clock period (25ns when operating at 40MHz) × 10 (Prescaler division ratio)	unsigned short	One-shot pulse output
Puls_w	Set the timer value corresponding to the pulse width of the one-shot pulse. The pulse width is calculated by the following formula. Pulse width (ns)=Timer Value × Unmodulated slow clock period × 10 (Prescaler division ratio)	unsigned short	

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Release the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A, D and prescaler.	0x13	
PCR23_0	Set the port P23_0 pin to TIA00 output.	0x00000058	Port setting
PCR22_7, PCR22_6, PCR22_9	Set P22_7, P22_6, and P23_0 to TOD00B, 01B, and 02B. output.	0x0000004B	
PSCR0	Set the event output 2A to the input edge of TIA0.	0x0009	ATU setting
TCR3A	Set to input capture to ICRA0 at the rising edge of TIA0.	0x8001	
TIOR1A	Clear the Timer A flag.	0x0001	
TSCRA	Set the event output 2A to the input edge of TIA0.	0x80FF	
TIERA	Set the TIA00 input capture interrupt enable.	0x0001	
TIOR1D0	Enable the compare match between TCNT1D0 and OCR1D00 to 02.	0x153F	
TIOR2D0	Enable the compare match between TCNT2D0 and OCR1D00 to 02.	0x0333	
DCRD0	Set the down-count start trigger to OCR1D00 to 02, and the down-count trigger to the compare match of OCR2D00 to 02.	0x0333	
TSCRD0	Clear the Timer D flag.	0x3FFF	
TSTRD	Enable the operation of Timer D sub block 0.	0x0001	
EIBD86	Bind the TIA00 input capture interrupt to PE0 (CPU0).	0x00000000	
EIC86	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRA	Clear the input capture flag of Timer A.	0x0001	One-shot pulse output
OCR1D00～02	Set the offset of the one-shot pulse.	OSBRD0 + ofset0～2	
OCR2D00～02	Set the period until the termination of the one-shot pulse.	OSBRD0 + 0x3500	
OSBRD0	TCNT1D0 value is transferred by TIA00 input capture.	—	
DCNTD00～02	Set the pulse width of one-shot pulse.	puls_w	

2.14 Operation Ex.13 PWM Waveform Output [Timer E]

As shown in Figure 2.25, outputs the pulse that can change the duty and cycle. The pulse width is set to perform the cycle register and duty register setting of Timer E.

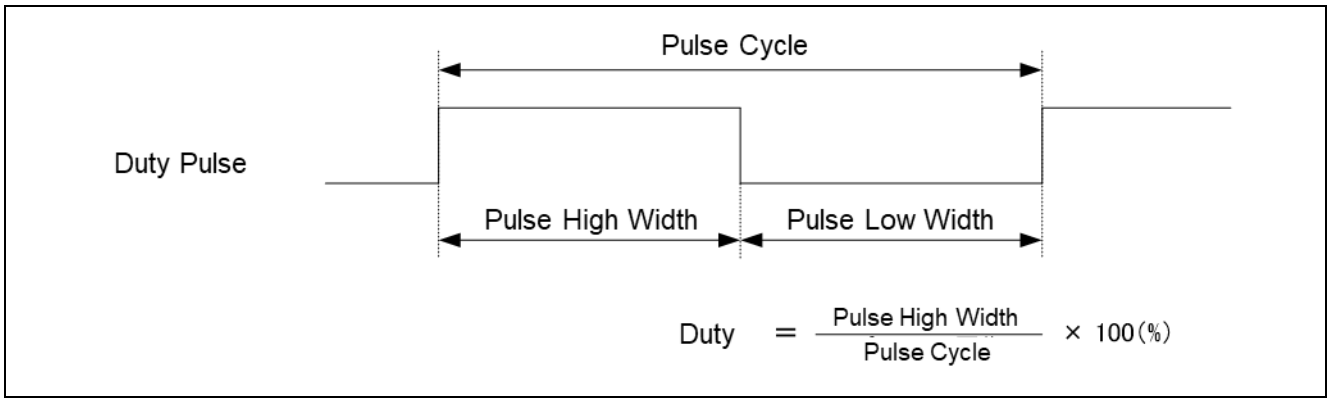


Figure 2.25 Outline Diagram of PWM Output

2.14.1 Explanation for Use Function

Table 2.13 shows the functions allocations of the ports used and related registers.

Table 2.12 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TOE00	Outputs the PWM wave.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer E register	DTRE00	Sets the duty register value.
	DRLDE00	Sets the duty reload register value.
	CYLRE00	Sets the cycle regiser value.
	CRLDE00	Sets the cycle reload register.
	RLDCRE0	Enables the reload function of DTRE.
	TIERE0	Sets the syscle match interrupt.
	TSCRE0	Clears the Timer E flag.
	TSTRE	Sets the counter opartion of each Timer E sub block.
	SSTRE0	Enables the counter operation of the counter opartion Timer E sub block.
PORT register	PCR00_4	Sets the port function.
INTC register	EIBD212	Specifeis the bind destination of the cycle macth interrupt.
	EIC212	Set the interrupt vector method and the interrupt priority.

2.14.2 Operation Explanation

Figure 2.26 shows the operation principle. According to this, the PMW waveform is outputted by the hardware and software processing of RH850/U2Bx. The PMW waveform and the duty ratio is changed by updating the duty reload register value for each of the compare match.

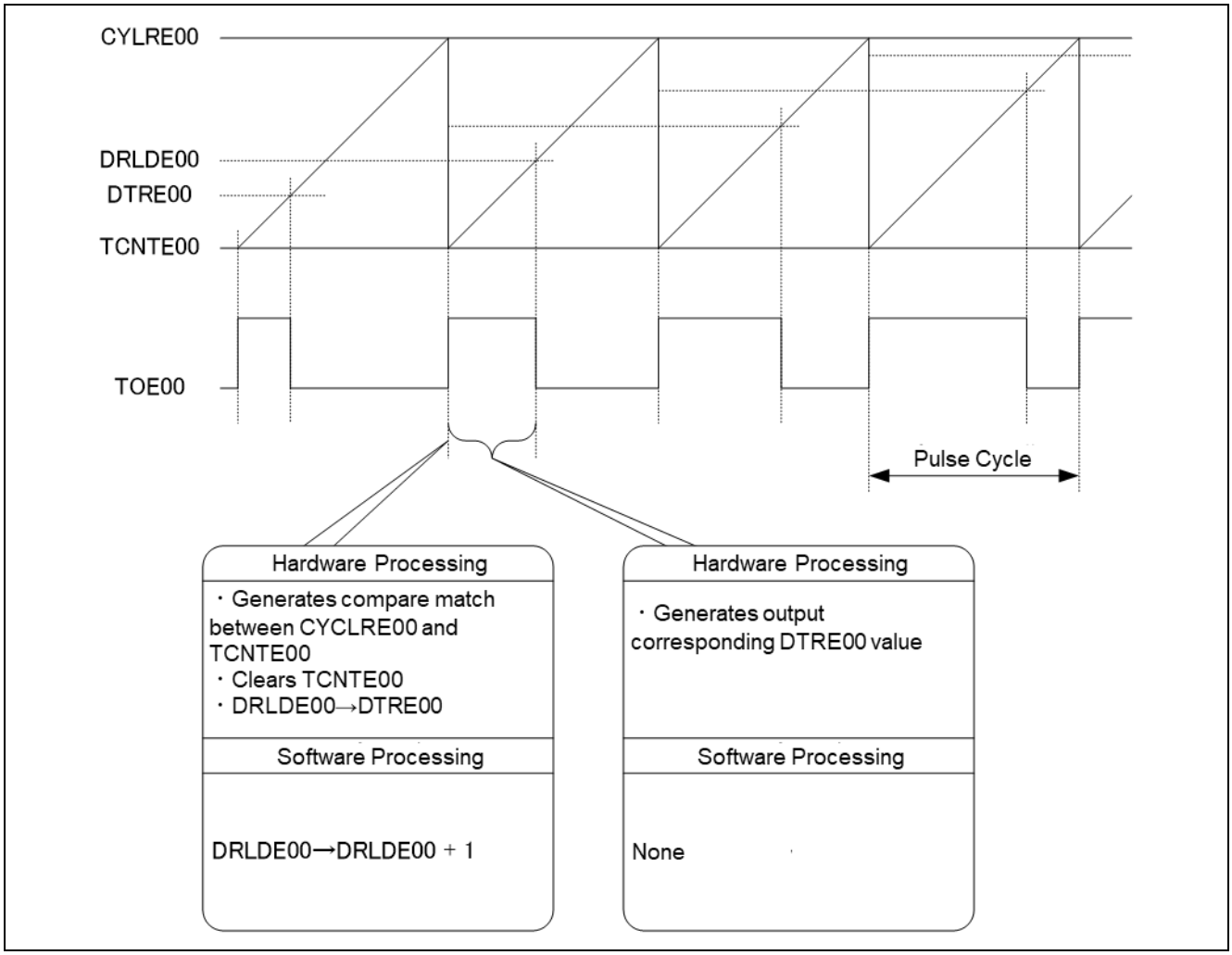


Figure 2.26 Operation Principle of PWM Output

2.14.3 Software Explanation

Module Explanation

Module Name	Rebel Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_4) setting.
ATU setting	atu_init	Performs the initial setting of Timer E.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Cycle match interrupt	eiint212	Starts by CMFE00, and Increases and decreases the DRLDE00 value.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module Name
up	When the cycle match interrupt is generated, the duty reload value is set/clear when it is below/above a certain value. Also, it becomes the flag that sets the increasing/decreasing direction of the duty reload register value.	unsigned char	Cycle match insterrupt

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer E and prescaler.	0x21	
PCR00_4	Sets TOE00 to P00_4 port.	0x00000048	Port setting
PSCR0	Sets the “2” to the division ration of the prescaler.	0x0001	ATU setting
DTRE00	Sets the duty of the PMW waveform.	0x00000100	
DRLDE00	Sets the duty of the PMW wave form for the reload.	0x00000100	
CYLRE00	Sets the cycle of the PMW waveform.	0x00010000	
CRLDE00	Sets the cycle of the PMW waveform for the reload.	0x00010000	
RLDCRE0	Enables the DTRE00 reload function.	0x01	
TIERE0	Enables the cycle match interrupt by cycle register 00.	0x0001	
TSTRE	Enables the operation of Timer E sub block 0.	0x0001	
SSTRE0	Enables the operation of Timer E sub block 0 timer counter 00.	0x0001	
EIBD212	Binds the CMIE00C input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC212	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRE0	Clears the cycle match interrupt flag.	0x0001	Cycle match interrupt
DRLDE00	Sets the duty of the PMW wave form for the reload.	When the up flag is set: +=0x00000100 When the up flag is not set: -=0x00000100	

2.15 Operation Ex.14 Effective Edge Input Interval [Timer F]

2.15.1 Overview

As shown in Figure 2.27, measures the time until the set number of rising edge is inputted. Sets the number of the effective edge by setting the timer operation mode to enable edge input interval measurement.

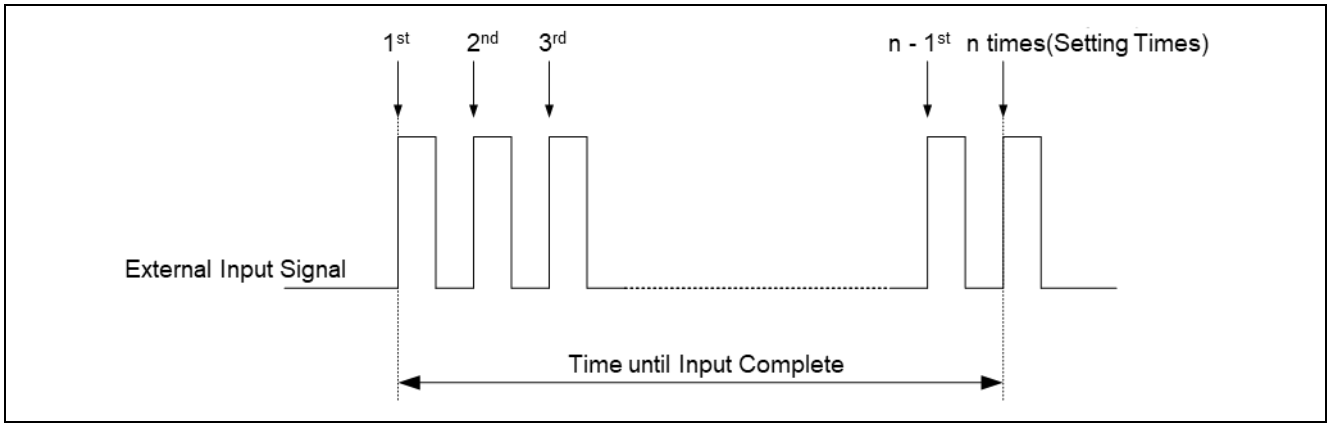


Figure 2.27 Timing of Effective Edge Input Interval (when Counting Rising Edge)

2.15.2 Explanation for Use Function

Table 2.11 shows the functions allocations of the ports used and related registers.

Table 2.13 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIF0A	Inputs the external signal for starting.
Related Register		Function
ATU-VI common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer F register	TCR1F0	Sets the opartion of each Timer F sub block.
	GRBF0	Sets the number of edges to detect.
	ECNTAF0	Mesures the time.
	ECNTBF0	Record the number of the effective external signal.
	TIERF0	Sets the interrup enable/disable.
	CDRF0	The capture value is stored coresponding to the operation mode.
	TSRF0	Timer F flag is stored.
	TSCRF0	Timer F flag is cleared.
	TSTRF	Sets the counter opartion of each Timer F sub block.
INTC register	EIBD252	Specifies the binding destination of the input capture interrupt of ICIF0.
	EIC252	Set the interrupt vector method and the interrupt priority.
PORT register	PCR00_6	Sets the port function.

2.15.3 Operation Explanation

Figure 2.28 shows the operation principle. According to this, measures the effective edge input time by the hardware and software processing of RH850/U2Bx. In this operation example, sets the number of detected edges to 5, and stores the counter value to the variable after the 5 times edge detection.

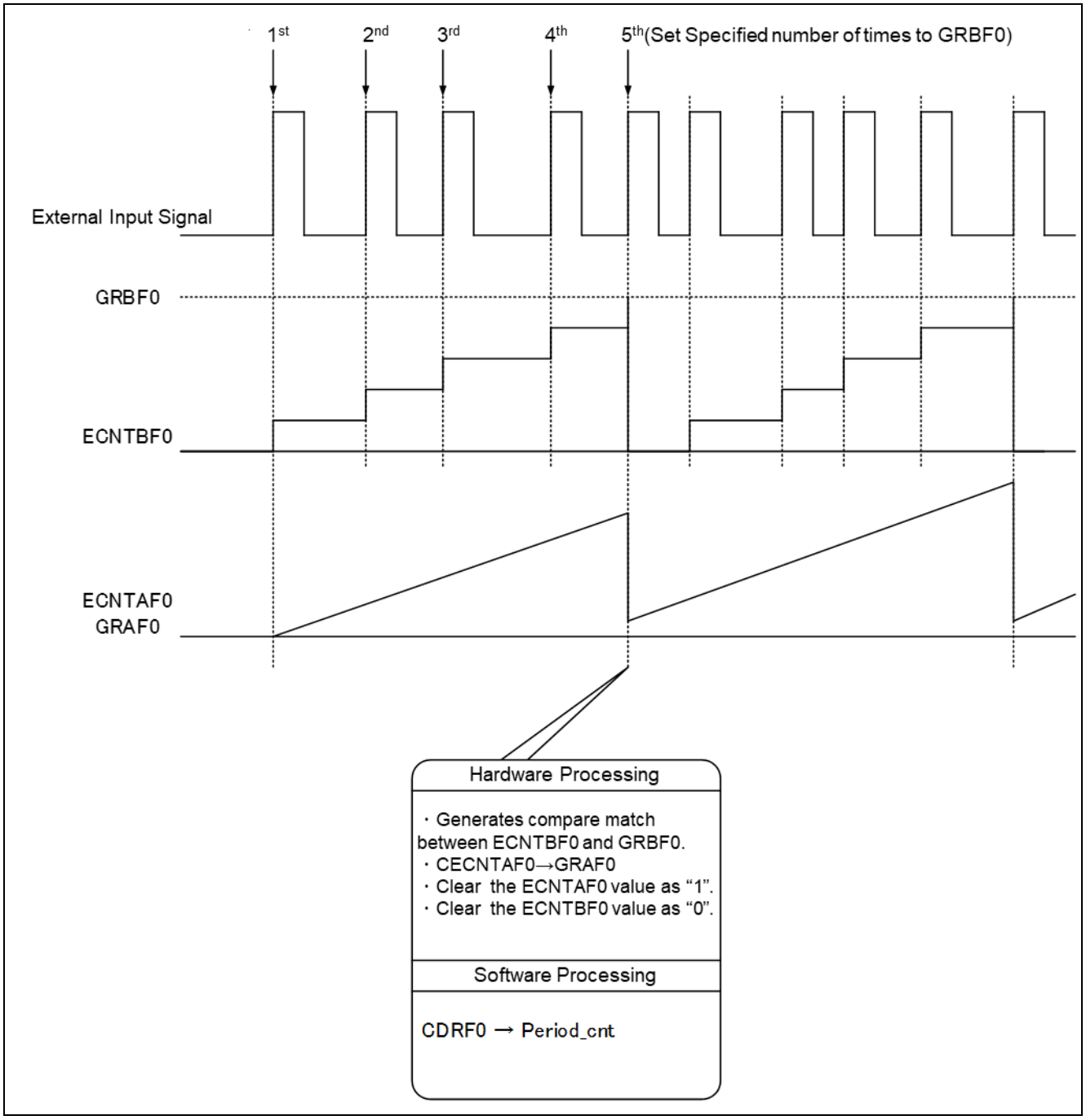


Figure 2.28 Operation Principle of Effective Edge Input Interval Measurement

2.15.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_6) setting.
ATU setting	atu_init	Performs the initial setting of Timer F.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Measurement value saving routine	eiint252	Saves the measured value in the variable.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module
Period_cnt	Save the required period for inputting the specified number of measured edges.	unsigned long	Measurement value saving routine

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer F and prescaler.	0x41	
PCR00_6	Sets TIF0A to PCR00_6 port.	0x00000058	Port setting
PSCR0	Sets the “10” to the division ration of the prescaler.	0x0009	ATU setting
TCR1F0	Sets “counting in the clock bus”, “effective edge input interval measurement”, and “the measurement edge is “rise”” to the sub block 0.	0x05	
GRBF0	Set the number of detected edges to 5.	0x0005	
ECNTBF0	Counts the number of rising edges of external input.	0x0000	
TIERF0	Enables the input capture interrupt.	0x01	
TSTRF	Starts the count of the Timer F sub block.	0x00000001	
EIBD252	Binds the ICIF0 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC252	Set the table reference method and interrupt priority method 0.	0x0040	
CDRF0	The captured value from GRAF0 is stored.	-	Measurement value saving routine
TSCRF0	Clear the flag of Timer F.	0x01	

2.16 Operation Ex.15 Edge Count within a Certain Period[Timer F]

2.16.1 Overview

As shown in Figure 2.29, records the number of effective input edges within a certain period. Sets the operation mode of Timer F to the edge count within a certain period.

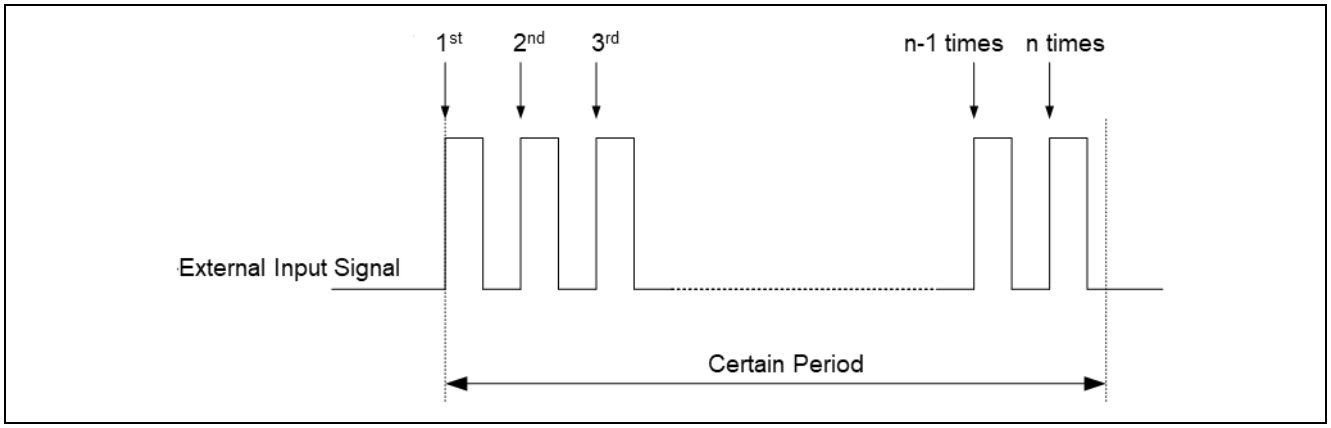


Figure 2.29 Edge Count within a Certain Period (when counting the rising edge)

2.16.2 Explanation for Use Function

Table 2.15 shows the functions allocations of the ports used and related registers.

Table 2.14 ATU-Ⅵ Operation Function

Use Port		Function
Port	TIF0A	Inputs the external signal for starting.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	TCR1F0	Sets the opartion of each Timer F sub block.
	GRAF0	Sets the number of edges to detect.
	ECNTAF0	Performs the up-counting by set clock bus of TCRF.
	ECNTBF0	Record the number of the effective external signal.
	CDRF0	The capture value is stored coresponding to the operation mode.
	TIERF0	Sets the interrup enable/disable.
	TSRF0	Timer F flag is stored.
	TSCRF0	Timer F flag is cleared.
	TSTRF	Sets the counter opartion of each Timer F sub block.
INTC register	EIBD252	Specifies the binding destination of the input capture interrupt of ICIF0.
	EIC252	Set the interrupt vector method and the interrupt priority.
PORT register	PCR00_6	Sets the port function.

2.16.3 Operation Explanation

Figure 2.30 shows the operation principle. According to this, the number of effective edge inputs in a given time is calculated by the hardware and software processing of RH850/U2Bx. The measurement period of the number of edges is set by the time measurement counter register.

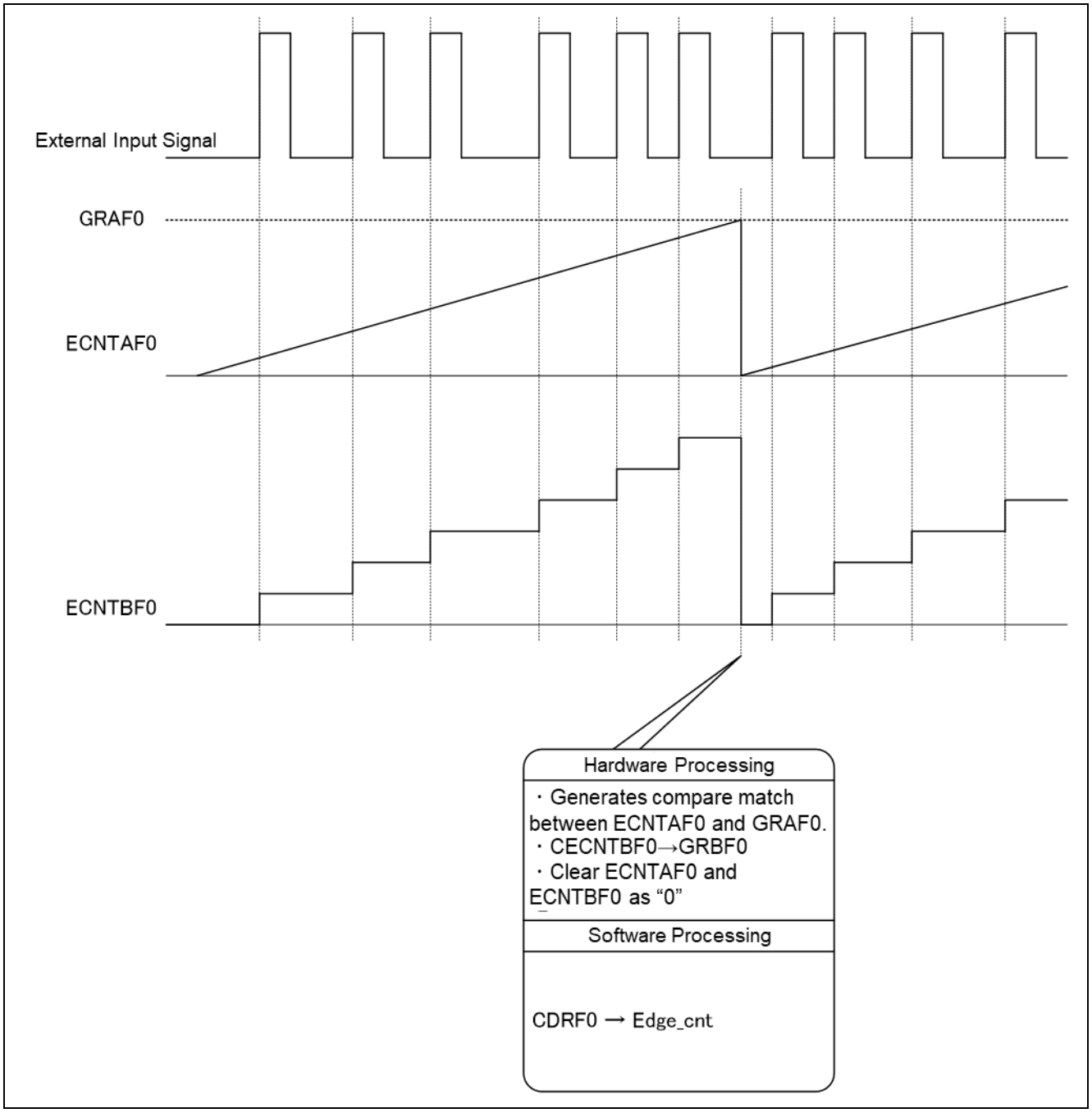


Figure 2.30 Operation Principle of Edge Count within Fixed Time

2.16.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_6) setting.
ATU setting	atu_init	Performs the initial setting of Timer F.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Measurement value saving routine	eiint252	Saves the measured value in the variable.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module
Edge_cnt	Saves the number of measured edges.	unsigned long	Measurement value saving routine

Use Register Setting

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer F and prescaler.	0x41	
PCR00_6	Sets TIF0A to PCR00_6 port.	0x00000058	Port setting
PSCR0	Sets the “10” to the division ration of the prescaler.	0x0009	ATU setting
TCR1F0	Sets “counting in the clock bus 0”, “Edge counting within a certain period”, and “The measurement edge is rise” for the sub block 0.	0x01	
GRAF0	Sets the period measuring the edge to 0x50 count.	0x00000050	
TIERF0	Enables the input capture interrupt.	0x01	
TSTRF	Starts the count of the Timer F sub block.	0x00000001	
EIBD252	Binds the ICIF0 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC252	Set the table reference method and interrupt priority method 0.	0x0040	
CDRF0	The captured value from GRBF0 is stored.	-	Measurement saving value routine
TSCRF0	Clears the flag of the input capture generation.	0x01	

2.17 Operation Ex.16 Input High/Low Period Measurement [Timer F]

2.17.1 Overview

As shown in Figure 2.31, records the high (or low) level output time within the specified number of times in the input pulse. In this operation example, sets the input high/low period measurement mode to the Timer F operation mode, and the High period of the input pulse is the measurement target.

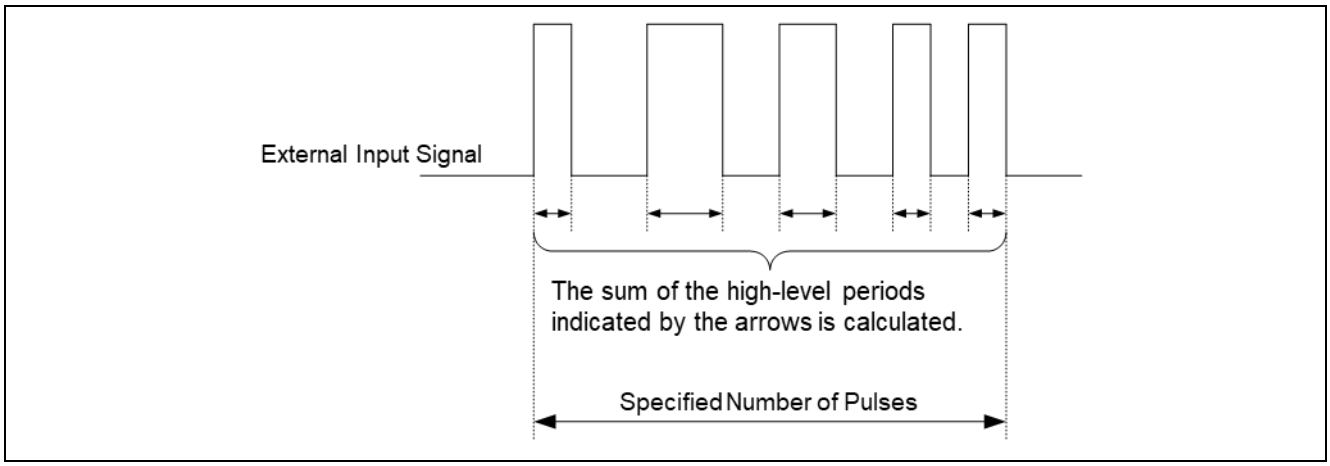


Figure 2.31 Overview of High/Low Period Measurement

2.17.2 Explanation for Use Function

Table 2.13 shows the functions allocations of the ports used and related registers.

Table 2.15 ATU-Ⅵ Function Operation

Use Port		Function
Port	TIF0A	Inputs the external signal for starting.
Related register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	TCR1F0	Sets the opartion of each Timer F sub block.
	GRBF0	Sets the number of the detected pulse.
	ECNTAF0	Counts the period the set level is entered.
	ECNTBF0	Records the number of the effective external signal.
	CDRF0	The capture value corresponding to the operation mode is stored.
	TIERF0	Sets the insterrupt enable/disable.
	TSRF0	The Timer F flag is stored.
	TSCRF0	The Timer F flag is cleared.
	TSTRF	Sets the counter opartion of each Timer F sub block.
INTC register	EIBD252	Specifies the binding destination of the input capture interrupt of ICIF0.
	EIC252	Set the interrupt vector method and the interrupt priority.
PORT register	PCR00_6	Sets the port function.

2.17.3 Operation Explanation

Figure 2.32 shows the operation principle. According to this, the number of effective edge inputs in a given time the is calculated by the hardware and software processing of RH850/U2Bx. In the input high/low level period measurement mode, sets the number of the detected pulse, and performs the input capture interrupt after completed the set number of times detection. In that time, the period is measured by using the counter value.

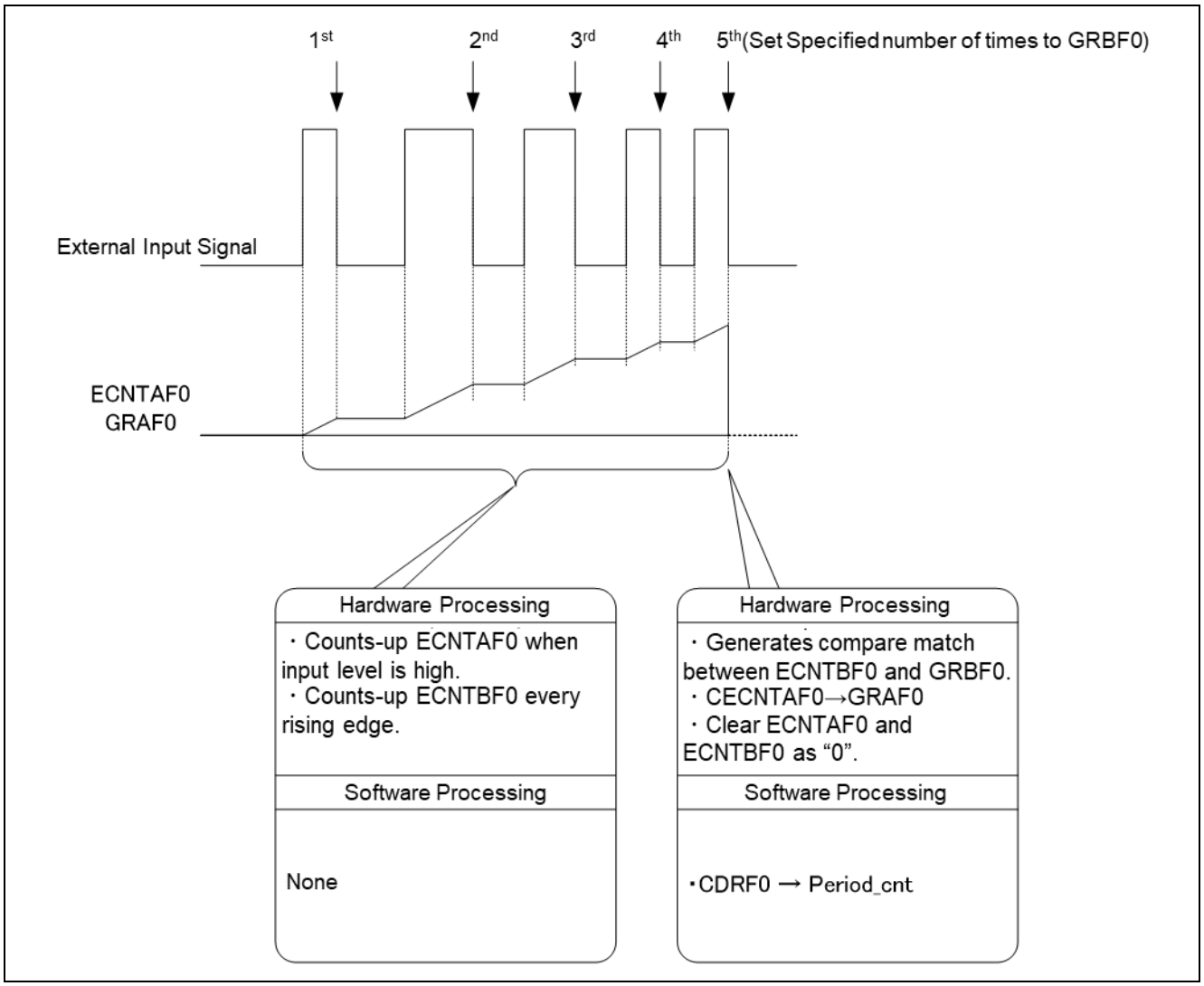


Figure 2.32 Operation Principle of Input High/Low Period Measurement

2.17.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_6) setting.
ATU setting	atu_init	Performs the initial setting of Timer F.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Measurement saving value routine	eiint252	Generates the interrupt in ICIF0 set, and stores the measured value to the variable.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module
Period_cnt	Stores the sum of the measured High (Low) period.	unsigned long	Measurement saving value routine

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer F and prescaler.	0x41	
PCR00_6	Sets TIF0A to PCR00_6 port.	0x00000058	Port setting
PSCR0	Sets the “10” to the division ration of the prescaler.	0x0009	ATU setting
TCR1F0	Sets “counting in the clock bus”, “input High/Low period measuring”, and “the measuring period is “High””.	0x0A	
GRBF0	Set the number of detected edges to 5.	0x0005	
TIERF0	Counts the number of rising edges of external input.	0x01	
TSTRF	Enables the input capture interrupt.	0x00000001	
EIBD252	Starts the count of the Timer F sub block.	0x00000000	Interrupt setting
EIC252	Set the table reference method and interrupt priority method 0.	0x0040	
CDRF0	The captured value from GRAF0 is stored.	-	Measurement saving value routine
TSCRF0	Clear the flag of Timer F.	0x01	

2.18 Operation Ex.17 PWM Input Waveform Measurement [Timer F]

2.18.1 Overview

As shown in Figure 2.33, measure the off-duty and the PWM cycle for the fixed number of inputted PWM waveforms. Sets the PWM input waveform measurement mode to the operation mode of Timer F.

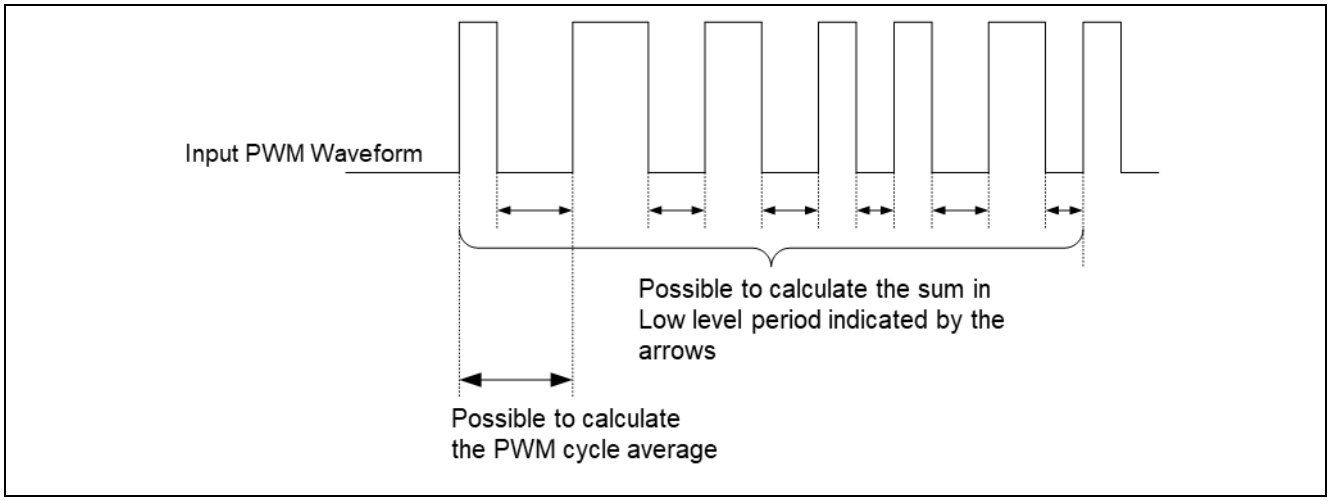


Figure 2.33 Overview of PWM Input Waveform Measurement

2.18.2 Explanation for Use Function

Table 2.17 shows the functions allocations of the ports used and related registers.

Table 2.16 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIF0A	Inputs the external signal for starting.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer F register	TCR1F0	Sets the opartion of each Timer F sub block.
	GRBF0	Set the number of the detected pulse.
	ECNTAF0	Counts the period during which the set level is entered.
	ECNTBF0	Record the number of the effective external signal.
	ECNTCF0	Count the number of the edges inputted from external.
	TSTRF	Sets the counter opartion of each Timer F sub block.
	TIERF0	Sets the interrup enable/disable.
	TSRF0	Timer F flag is stored.
	TSCRF0	Timer F flag is cleared.
	CDRF0	The measured off-duty value is stored.
	GRCF0	The measured cycle value is stored.
INTC register	EIBD252	Specifies the binding destination of the input capture interrupt of ICIF0.
	EIC252	Set the interrupt vector method and the interrupt priority.
PORT register	PCR00_6	Sets the port function.

2.18.3 Operation Explanation

Figure 2.34 shows the operation principle. According to this, measure the off-duty and the PWM cycle of the PWM waveform.

When the set number of input PWM waveforms is detected, detects the input interrupt, and obtains the counter value from the start of measurement and updates the counter value only when the input PWM waveform is OFF.

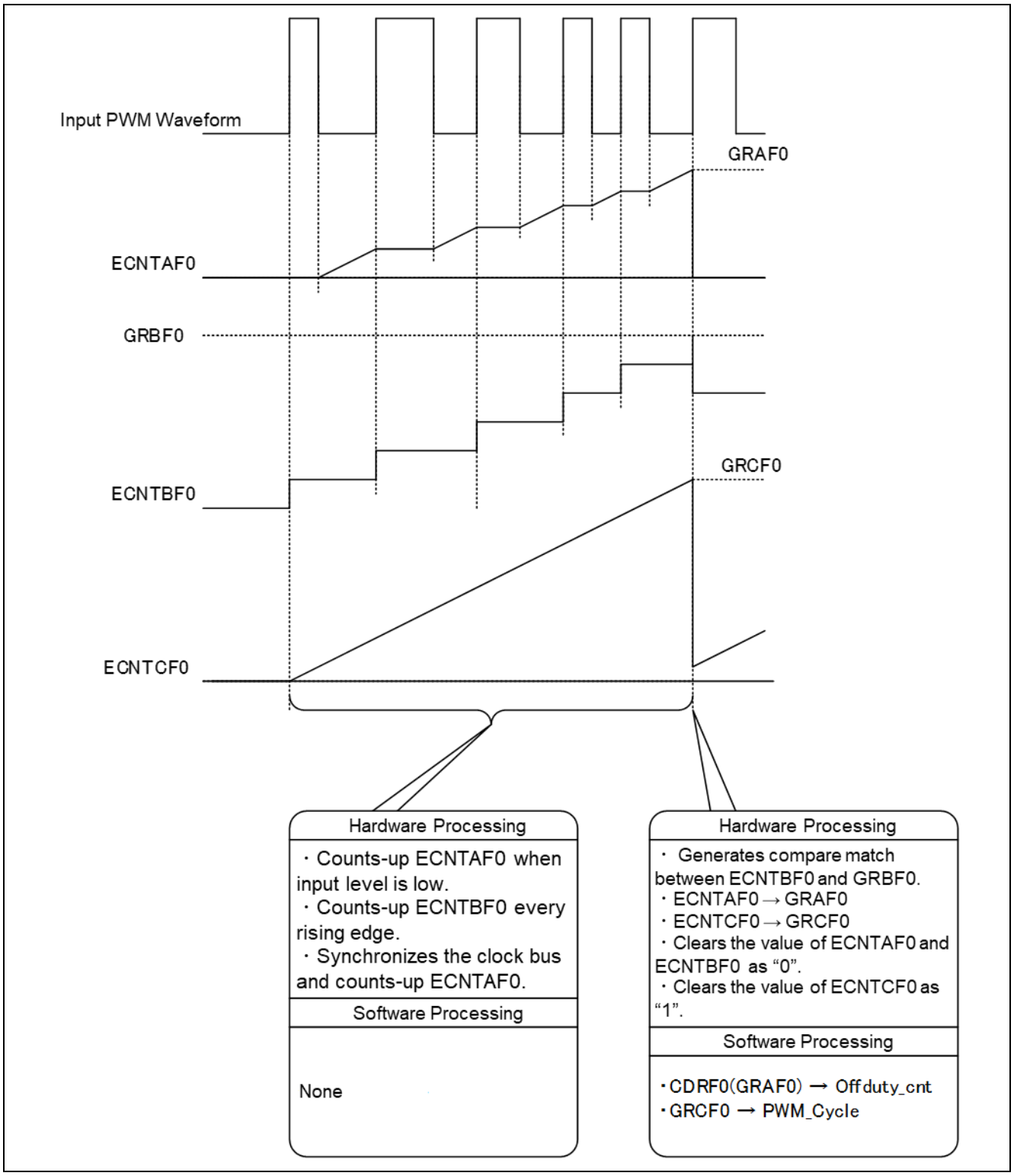


Figure 2.34 Operation Principle of PWM Input Waveform

2.18.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_6) setting.
ATU setting	atu_init	Performs the initial setting of Timer F.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Measurement value saving routine	eiint252	Saves the measured value in the variable.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module
Offduty_cnt	Saves the total value of the off-duty period within the measurement period.	unsigned long	Measurement value saving routine
PWM_Cycle	Saves the time counter value of the measurement period.		

Explanation of Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer F and prescaler.	0x41	
PCR00_6	Sets TIF0A to PCR00_6 port.	0x00000058	Port setting
PSCR0	Sets the “10” to the division ration of the prescaler.	0x0009	ATU setting
TCR1F0	Sets “counting in the clock bus 0”, “PWM input waveform measurement”, and “the measurement edge is rise” for the sub block 0.	0x11	
GRBF0	Sets the number of detected edges to 6.	0x0006	
TIERF0	Sets the input capture enable.	0x01	
TSTRF	Starts the Timer F sub block count.	0x00000001	
EIBD252	Binds the ICIF0 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC252	Set the table reference method and interrupt priority method 0.	0x0040	
CDRF0	The measured off-duty value is stored.	—	Measurement value saving routine
GRCF0	The measured PWM cycle value is stored.	—	
TSCRF0	Clears the flag of the input capture generation.	0x01	

2.19 Operation Ex.18 Rotation Speed/Pulse Measurement [Timer F]

2.19.1 Overview

As shown in Figure 2.35, measures the number of the input edges and the edge input time, and measures the off-duty and the PWM cycle of the PWM waveform that appears between the previous input edge. Sets the operation mode to the rotation speed/pulse measurement mode.

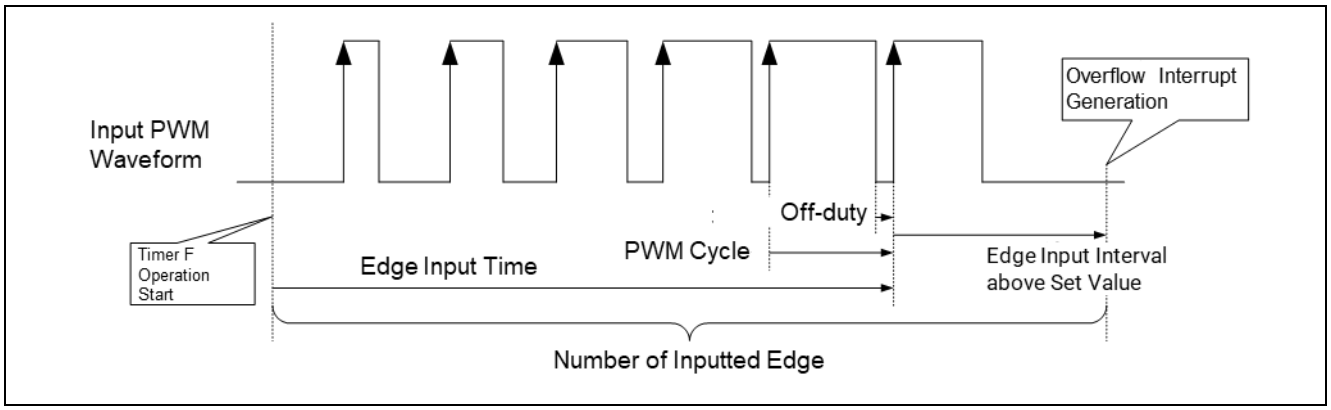


Figure 2.35 Overview of Rotation Speed/Pulse Measurement

2.19.2 Explanation for Use Function

Table 2.18 shows the functions allocations of the ports used and related registers.

Table 2.17 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIF4	Inputs the external signal for starting.
Related Register		**Function**
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer F register	TCR1F4	Sets the opartion of each Timer F sub block.
	ECNTAF4	Set the number of the detected pulse.
	ECNTBF4	Count the number of the edges inputted from external.
	ECNTCF4	Record the number of the effective external signal.
	GRAF4	Capturing the value of the ECNTAF4 when the effective edge inputing of the external signal.
	GRBF4	It functions as a compare match register with ECNTCF4, and the overflow flag of ECNTCF4 is set when the compare match is detected.
	GRCF4	Captures the ECNTCF4 capture when inputing the effective edge of the external signal.
	GRDF4	Accumulas and captures the ECNTCF4 valuec when inputing the effective edge of the external signal.
	CDRF4	In the rotation speed/pulse measurement, the ECNTBF4 is read.
	TIERF4	Sets the interrup enable/disable.
	TSRF4	Stores the flag of the timer F sub block 4.
	TSCRF4	Clears the flag.
	TSTRF	Sets the counter opartion of each Timer F sub block.
PORT register	PCR22_6	Sets the port function.
INTC register	EIBD94	Specifies the bind destination of TIF 4 overflow interrupt.
	EIC94	Set the interrupt vector method and the interrupt priority.

2.19.3 Operation Explanation

Figure 2.36 shows the operation principle. According to this, measure the input PWM waveform, the off-duty, the number of edge input from operation starting, and the edge input time. In the following, generates the ECNTCF4 overflow interrupt and obtains each counter value required for the measurement when the counter value ECNTCF4 reaches the compare match value GRBF4.

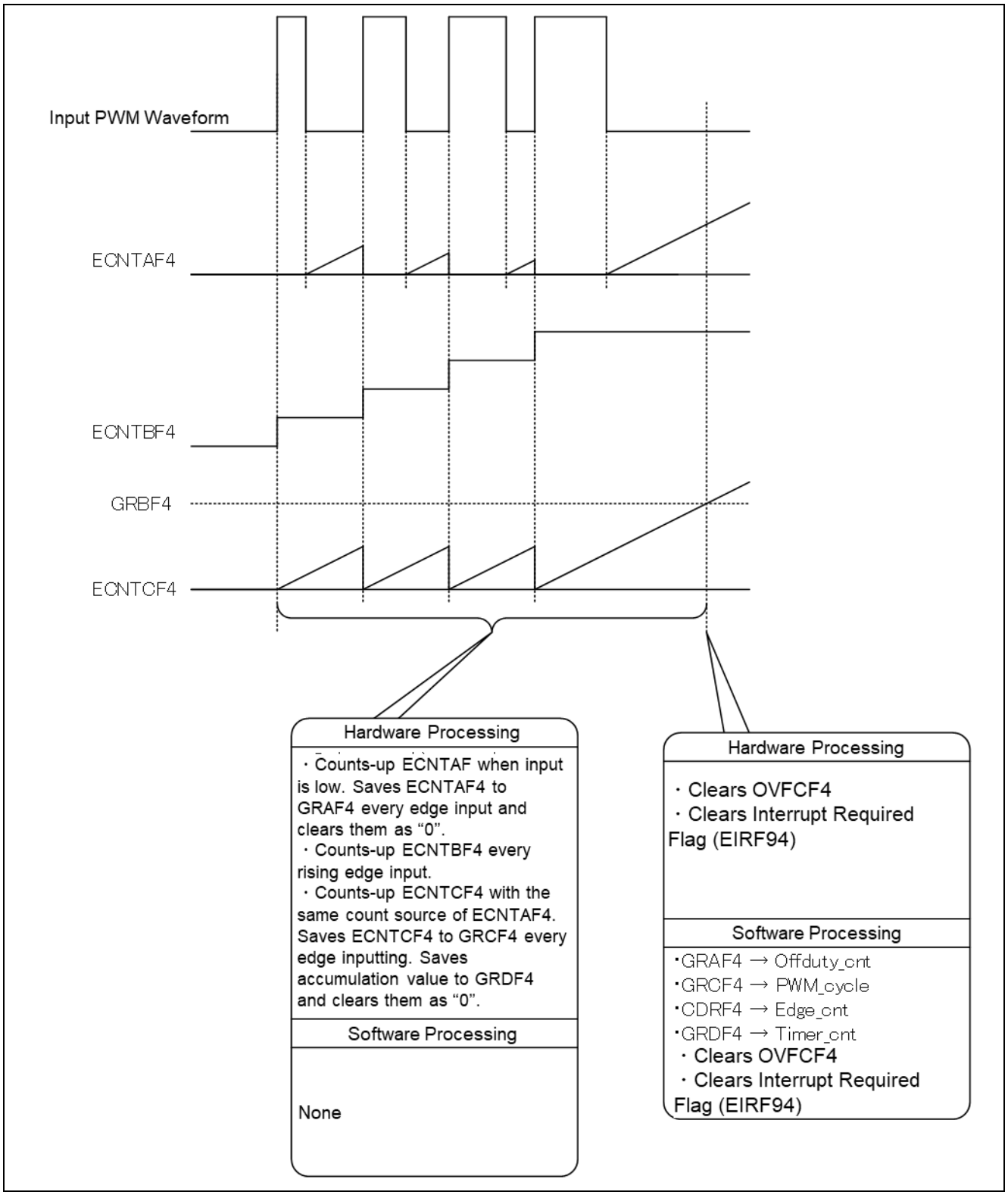


Figure 2.36 Operation Principle of Rotation Speed/Pulse Measurement

2.19.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_6) setting.
ATU setting	atu_init	Performs the initial setting of Timer F.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Measurement value saving routine	eiint94	Saves the measured value in the variable.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module
Edge_cnt	Save the number of input edges from the start of operation to the inputted edge input just before.	unsigned long	Measurement value saving routine
Timer_cnt	Save the number of clock bus from the start of operation to the inputted edge input just before.		
Offduty_cnt	Saves the off-duty value of the inputted PMW waveform just before.		
PWM_Cycle	Saves the cycle of the inputted PMW waveform just before.		

Setting for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer F and prescaler.	0x41	
PCR22_6	Sets TIF14A to PCR00_6 port.	0x00000058	Port setting
PSCR0	Sets the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TCR1F4	Sets “counting in the clock bus 0”, “Rotation Speed/Pulse Measurement”, and “the measurement edge is rise” for the sub block 0.	0x15	
TIERF4	Enables the interrupt request by the ECNTCF overflow.	0x08	
GRBF4	Sets the edge interval that generates the ECNTBF4 overflow. The value of GRBF4 (16-bit register) with the lower 16 bits extended to zero is compared with ECNTCF4 (32-bit register).	0x0001	
TSCRF4	Clears the flag of Timer F.	0x0F	
TSTRF	Enables the counting of Timer F sub block 4.	0x00000800	
EIBD94	Binds the overflow interrupt OVIE4 to PE0 (CPU0).	0x00000000	
EIC94	Set the table reference method and interrupt priority method 0.	0x0040	
GRAF4	The off-duty count value of the previous PWM waveform is saved.	-	Measurement value saving routine
GRCF4	The count value of the cycle of the previous PWM waveform is saved.	-	
CDRF4	The number of input edges from the start of operation to the input edge just before is saved.	-	
GRDF4	The count value on the clock bus from the start of operation to the input edge that was input just before is saved.	-	
TSCRF4	Clears the ECNTCF4 overflow flag.	0x08	
EIC94	Clears the request flag of the overflow interrupt.	EIRF94=0	

2.20 Operation Ex.19 Up-down Event Count [Timer F]

2.20.1 Overview

1) Using two input ports, switches the count at the input edge to a port by switching the input level of another port is weather up-count or down count, and counts.

2) Saves and clears the count value at that time at regular intervals.

2.20.2 Explanation for Use Function

Table 2.19 shows the functions allocations of the ports used and related registers.

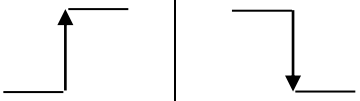
Table 2.18 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIF0A	Inputs the external signal for starting.
	TIF0B	Inputs the signal from the external (level for count destination).
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer F register	TCR1F0	Sets the opartion of each Timer F sub block.
	ECNTAF0	Mesures the time by the specfied clock bus.
	ECNTBF0	Performs the Up/Down cont operation according to the input to the two ports.
	GRAF0	Sets the compare match value correspondin to ECNTAF0.
	GRBF0	Captures the ECNTBF0 value when the ECNTAF compare match is generated.
	TIERF0	Sets the insterrupt enable/disable.
	TSRF0	The flag of Timer F sub block 0 is stored.
	TSCRF0	The flag of Timer F sub block 0 is cleared.
	TSTRF	Sets the conter opeartion of each Timer F sub block.
PORT register	PCR00_6	Sets the P00_6 port function.
	PCR00_7	Sets the P00_7 port function.
INTC register	EIBD252	Specifies the binding destination of the compare match interrupt.
	EIC252	Set the interrupt vector method and the interrupt priority.

2.20.3 Operation Explanation

Table 2.20 and Figure 2.37 show the operation principle corresponding to the two ports inputting. According to this, performs the up/down count by the hardware and software processing of RH850/U2Bx.

Table 2.19 Count Destination in Up/Down Event Count Count Mode

Input	Count Destination	
	Up count	Down count
TIFnA (Input Edge)		
TIFnB (Input Level)	Low level	High level

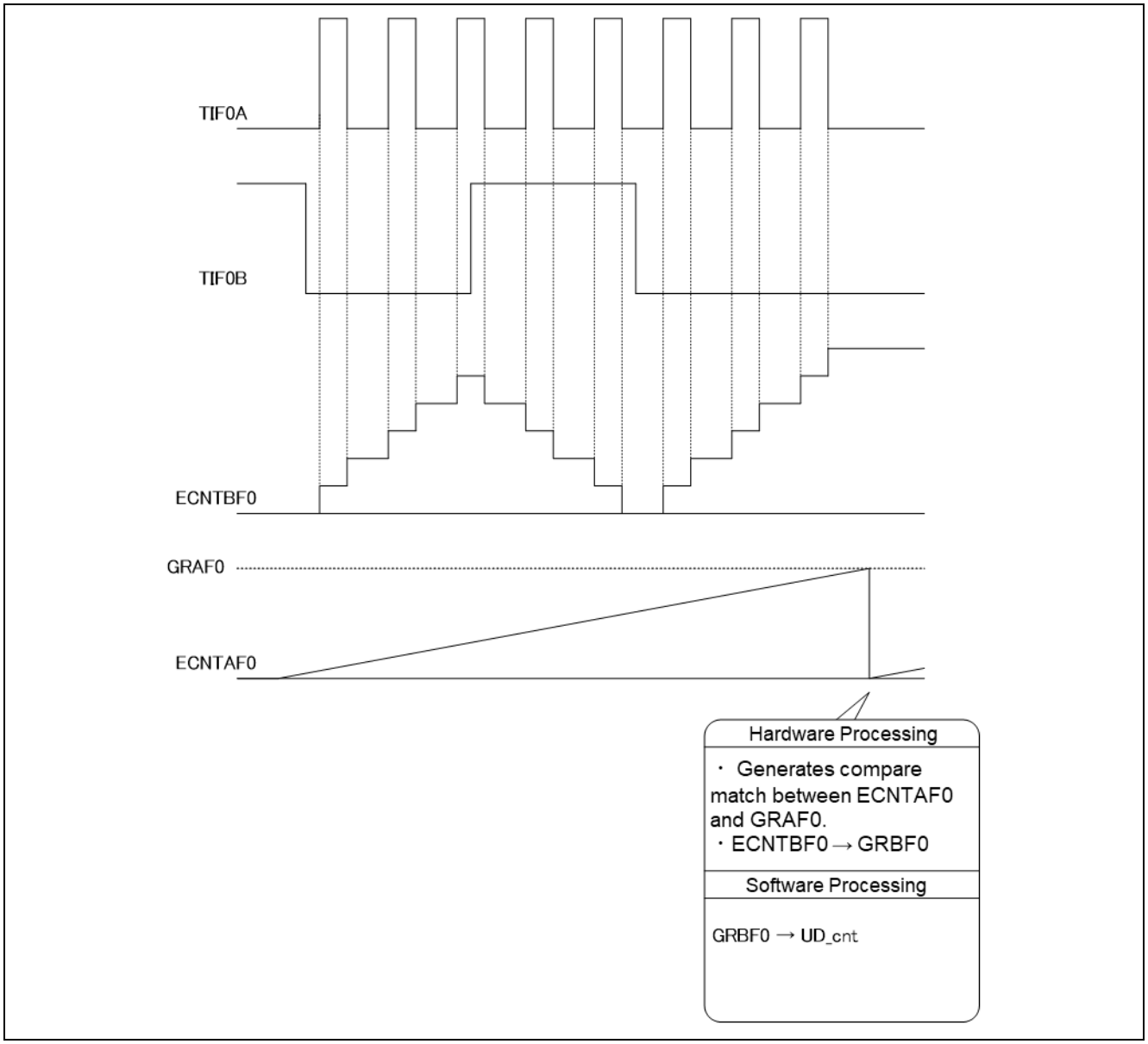


Figure 2.37 Operation Principle of Up-Down Event Cunt

2.20.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_6) setting.
ATU setting	atu_init	Performs the initial setting of Timer F.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Compare match interrupt routine	eiint252	Interrupts in compare mcth between ECNTAF0 and GRAF0, and saves GRBF0 value to UD_cnt.

Explanation for Use Variable

Variable Name	Function
UD_cnt	Saves ECNTBF0 value when compare match interrupt is generated.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer F and prescaler.	0x41	
PCR00_6	Sets TIF0A to PCR00_6 port.	0x00000058	Port setting
PCR00_7	Sets TIF0B to PCR00_7 port.	0x00000058	
PSCR0	Sets the “50” to the division ration of the prescaler 0.	0x0031	ATU setting
TCR1F0	Sets “counting in the clock bus 0”, “up/down count event”, and “the measurement edge is both edge” for the sub block 0.	0x1B	
GRAF0	Sets the measurement period to 255 cycles of clock bus 0.	0x000000FF	
TIERF0	Enables the compare match interrupt.	0x01	
TSTRF	Enables the count operation of the Timer F sub block 0.	0x00000001	
EIBD252	Binds the ICIF0 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC252	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRF0	Clears the flag of Timer F sub block 0.	0x01	Compare match interrupt routine
GRBF0	ECNTBF0 value is stored in compare match generation.	-	

2.21 Operation Ex. 20 4 Multiplication Event Count [Timer F]

2.21.1 Overview

Using two input ports, switch between up-count and down-count depending on both input edges and input levels, and counts.

2.21.2 Explanation for Use Function

Table 2.21 shows the functions allocations of the ports used and related registers.

Table 2.20 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIF0A	Inputs the signal from external.
	TIF0B	Inputs the signal from external.
Related Register		Function
ATU-Ⅵ common regisetr	ATUENR	Inputs the external signal for starting.
	PSCR0	Inputs the signal from the external (level for count destination).
Timer F register	TCR1F0	Function
	ECNTAF0	Sets the operation of each timer and prescaler.
	ECNTBF0	Performs the 4 multiplication evnet according to the inpting to two ports.
	GRAF0	Sets the compare match value corresponding to ECNTAF0.
	GRBF0	Captures the ECNTBF0 value when the ECNTAF compare match is generated.
	TIERF0	Sets the insterrupt enable/disable.
	TSRF0	The flag of Timer F sub block 0 is stored.
	TSCRF0	The flag of Timer F sub block 0 is cleared.
	TSTRF	Sets the conter opeartion of each Timer F sub block.
PORT register	PCR00_6	Sets the P00_6 port function.
	PCR00_7	Sets the P00_7 port function.
INTC register	EIBD252	Specifies the binding destination of the compare match interrupt.
	EIC252	Set the interrupt vector method and the interrupt priority.

2.21.3 Operation Explanation

Table 2.22 and Figure 2.38 show the operation principle corresponding to the two ports inputting. According to this, performs the 4-multiplication event count by the hardware and software processing of RH850/U2Bx.

Table 2.21 Count Direction in 4 Multiplication Event Count Mode

Input	Count Direction							
	Up-count				Down-count			
TIFnA (Input Edge)	High level	↓	Low level	↑	High level	↓	Low level	↑
TIFnB (Input level)	↑	High level	↓	Low level	↓	Low level	↑	High level

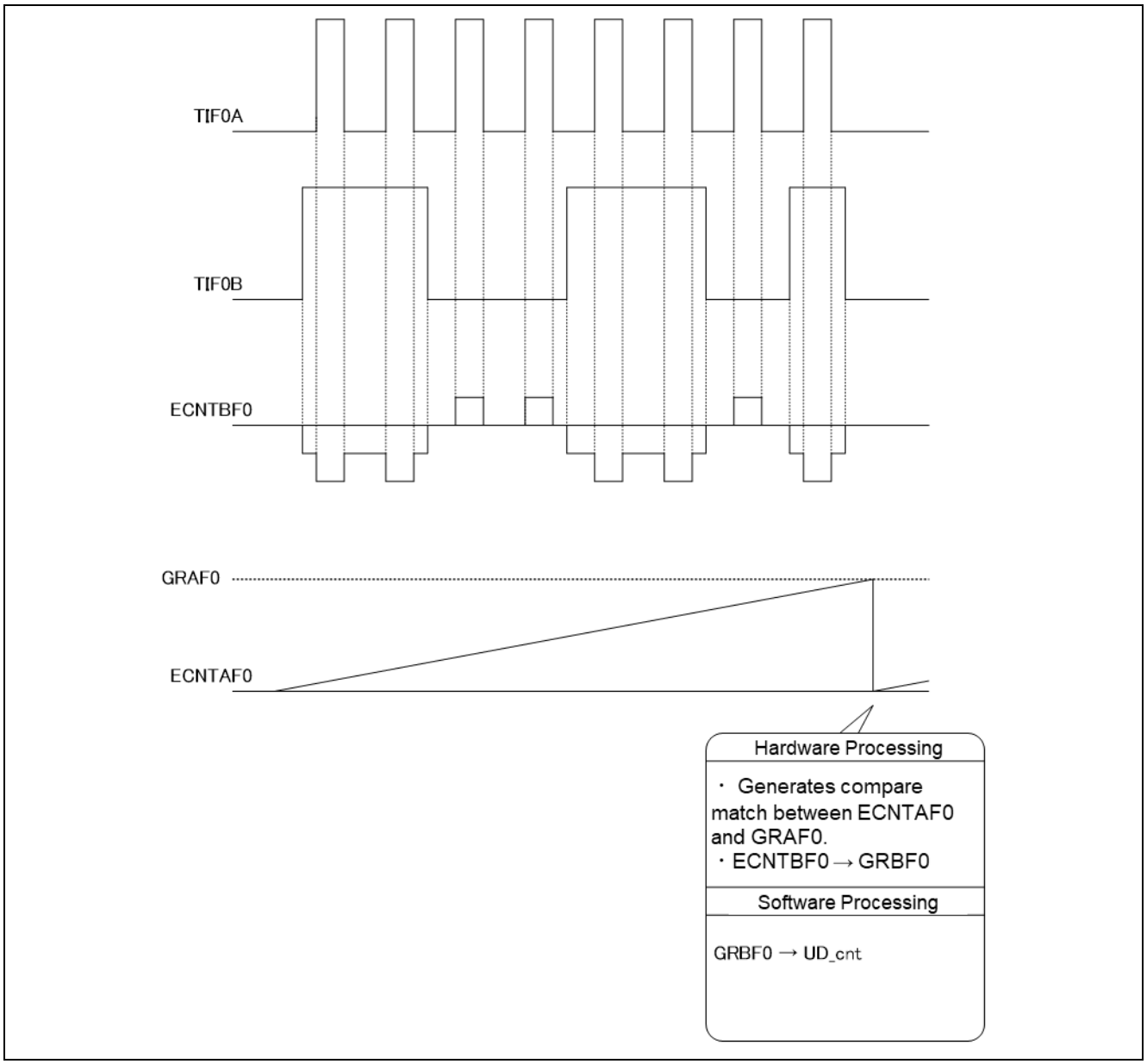


Figure 2.38 Operation Principle of 4 Multiplication Up-Down Count Event

2.21.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the port (P00_6, P00_7) setting.
ATU setting	atu_init	Performs the initial setting of Timer F.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Compare match interrupt routine	eiint252	Interrupts in compare mcth between ECNTAF0 and GRAF0, and saves GRBF0 value to UD_cnt.

Explanation for Use Variable

Variable Name	Function
UD_cnt	Saves ECNTBF0 value when compare match interrupt is generated.

Explanation for Use Register

Register Name	Function	Setting value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer F and prescaler.	0x41	
PCR00_6	Sets TIF0A to PCR00_6 port.	0x00000058	Port setting
PCR00_7	Sets TIF0B to PCR00_7 port.	0x00000058	
PSCR0	Sets the “50” to the division ration of the prescaler 0.	0x031	ATU setting
TCR1F0	Sets “counting in the clock bus 0”, “4 multiplication event count”, and “the measurement edge is both edge” for the sub block 0.	0x1F	
GRAF0	Sets the measurement period to 255 cycles of clock bus 0.	0x000000FF	
TIERF0	Enables the compare match interrupt.	0x01	
TSTRF	Starts the Time F sub block 0 count.	0x00000001	
EIBD252	Binds the ICIF0 input capture interrupt to PE0 (CPU0).	0x00000000	
EIC252	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRF0	Clears the flag of Timer F sub block 0.	0x01	Compare match interrupt routine
GRBF0	ECNTBF0 value is stored in compare match generation.	—	

2.22 Operation Ex.21 Compare Math Interrupt Generation [Timer G]

2.22.1 Overview

Generates the compare match when the timer count matches with the compare match value.

2.22.2 Explanation for Use Function

Table 2.23 show the functions allocations of the related registers.

Table 2.22 ATU-Ⅵ Function Allocation

Related Register		Function
ATU-Ⅵ Common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer G register	TCRG0	Sets each function of Timer G.
	OCRG0	Sets the compare match value.
	TCNTG0	Performs the timer count by the set clock bus in TCRG.
	TIERG	Performs the compare match interrupt setting.
	TSTRG	Enables the Timer G sub block timer count.
	TSRG0	The flag is set when the overflow and compare match are generated.
	TSCRG0	Clears the flag.
INTC register	EIBD232	Specifies the bind destination of the compare match.
	EIC232	Set the interrupt vector method and the interrupt priority.

2.22.3 Operation Explanation

Figure 2.39 shows the operation principle. According to this, generates the compare match by the hardware and software processing of RH850/U2Bx. The count value of Timer G (TCNTG0) is cleared when the compare match is generated.

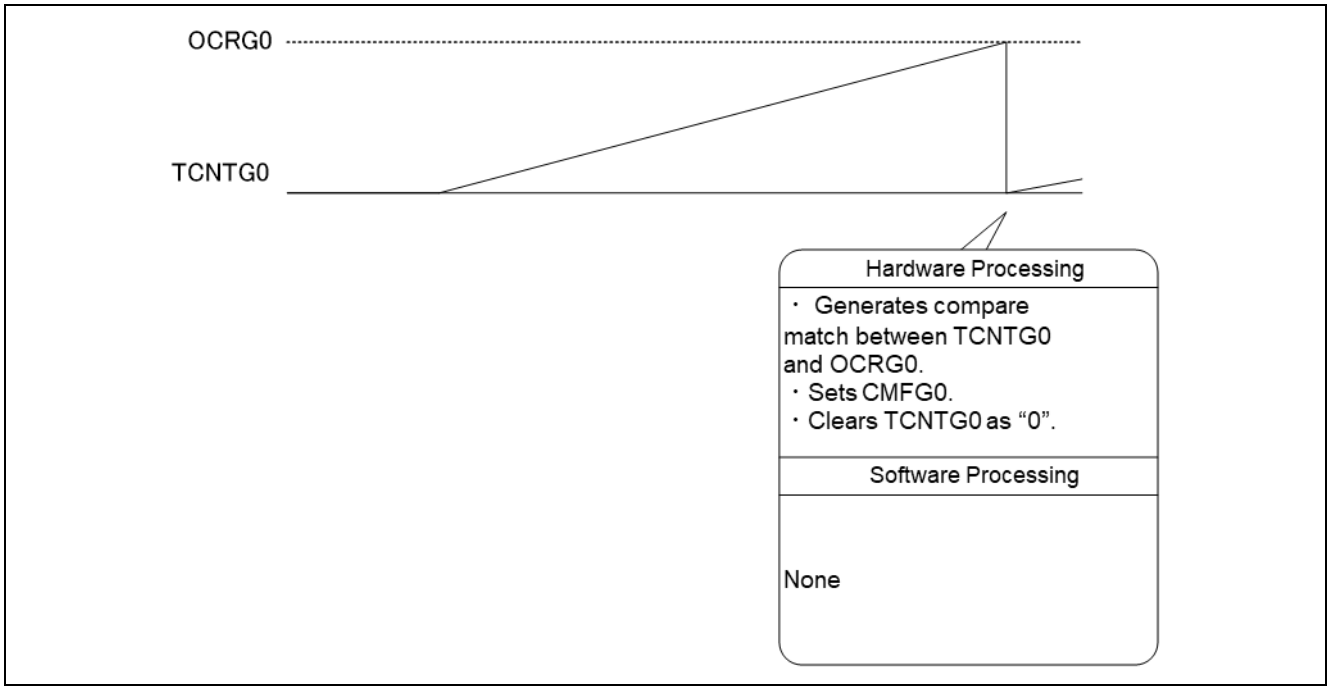


Figure 2.39 Operation Principle of Compare Match

2.22.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
ATU setting	atu_init	Performs the initial setting of Timer G.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Compare match interrupt routine	eiint232	Clears the flag of the compare match generation.

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer G and prescaler.	0x81	
TCRG0	Sets “counting at clock bus 0” to Timer G.	0x00	ATU setting
OCRG0	Sets the compare match value corresponding to TCNTG0.	0x00000400	
TIERG	Enables the compare match interrupt.	0x0001	
TSCRG0	Clears the flag of Timer G.	0x03	
TSTRG	Enables the count operation of Timer G sub block 0.	0x0001	
EIBD232	Binds the CMIG0 input capture interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC232	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRG0	Clears the flag of the Timer G.	0x01	Compare match interrupt routine

2.23 Operation Ex.22 Activation of Other Module by Compare Match Generation [Timer G]

2.23.1 Overview

Generates the one-cycle positive logic pulse signal when compare match is generated, and start the A/D converter using the signal as the trigger.

2.23.2 Explanation for Use Register

Table 2.24 show the functions allocations of the related registers.

Table 2.23 ATU-Ⅵ Function Allocation

Use Port		Function
Port	AN000	Analog input port of A/D convertor.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR1	Sets the division ration of the prescaler 1.
Timer G register	TCRG1	Sets each function of Timer G.
	OCRG1	Sets the compare match value of Timer G.
	TIERG	Sets the compare match interrupt setting.
	TCNTG1	Performs the timer count by the set clock bus in TCRG1.
	TSTRG	Starts the timer counter of Timer G.
	TSRG1	The flag is set when the overflow and the compare match are generated.
	TSCRG1	Clears the flag.
A/D convertor register	ADCK0VCR00	Sets the virtual channel operation.
	ADCK0SGCR0	Sets the scan group operation.
	ADCK0SGVCSP0	Specifies the start virtual channel pointer.
	ADCK0SGVCEP0	Specifies the end virtual channel pointer.
	ADCK0SGMCYCR0	Set the number of multi-cycle.
	ADCK0SGSTCR0	Controls the operation start of the scan group 0.
	ADCK0DR00	The variable result of A/D is stored.
PIC2 register	PIC21ADCK0TSEL0	Selects the trigger source of the A/D conversion.
	PIC21ADTEN500	Selects the trigger source of the A/D conversion.
INTC register	EIBD233	Specifies the binding destination of the compare match interrupt.
	EIC233	Set the interrupt vector method and the interrupt priority.

2.23.3 Operation Explanation

Figure 2.40 shows the operation principle. According to this, generates the compare match by the hardware and software processing of RH850/U2Bx. The compare match pulse is generated as the positive logic pulse when the compare match is generated. Performs the A/D conversion using the positive logic pulse generated at this time as a trigger.

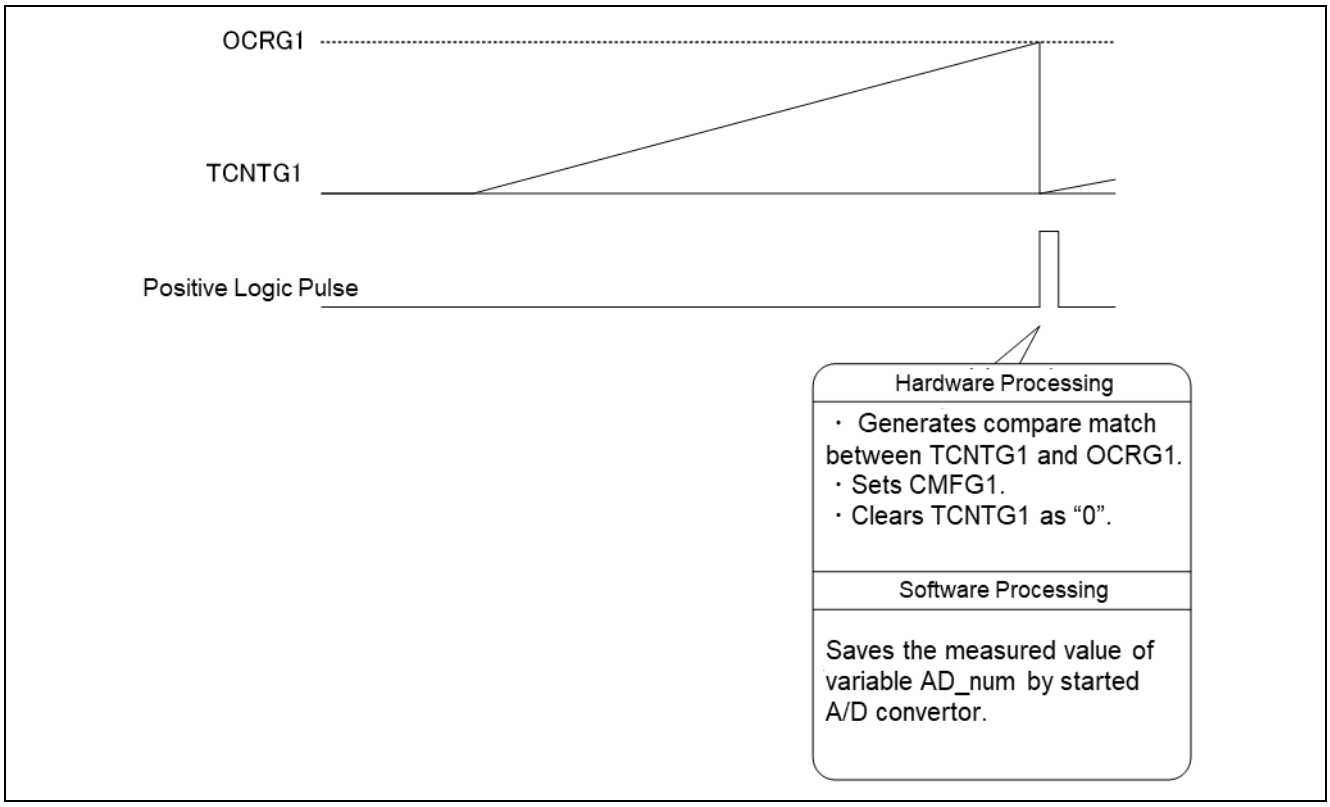


Figure 2.40 Operation Principle of A/D Conversion by Compare Match

2.23.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
ATU setting	atu_init	Performs the initial setting of Timer G.
ADCK setting	ADCK_init	Performs the initial setting of ADCK.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Compare match interrupt routine	eiint233	Interrupts in the compare match between TCNTG1 and OCRG1, and saves the converted value by the A/D convertor.

Explanation for Use Variable

Label Name	Function	Data Length	Use Module Name
AD_num	Saves the converted value by the A/D convertor.	unsigned short	Compare match interrupt

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
MSR_SAD	Releases the ADCK module standby.	0x000000FE	
ATUENR	Enable the count operation of Timer F and prescaler.	0x81	
PSCR1	Sets the “10” to the division ration of the prescaler 1.	0x0009	ATU setting
TCRG1	Sets to count on clock bus 1.	0x10	
OCRG1	Sets the compare match value corresponding to TCNTG1	0x00000400	
TIERG	Enables the compare match interrupt.	0x0002	
TSCRG1	Clears the flag.	0x03	
TSTRG	Enables the count operation of Timer 1 sub block 1.	0x0002	
EIBD233	Binds the compare match interrupt of CMIG1 to PE0 (CPU0).	0x00000000	Interrupt setting
EIC233	Set the table reference method and interrupt priority method 0.	0x0040	
ADCK0VCR00	Sets the physical channel AN000 to the virtual channel 0.	0x00000000	ADCK setting
ADCK0SGCR0	Selects the SG0_TRG hardware trigger to the trigger input of the scan group 0.	0x00000001	
ADCK0SGVCSP0	Sets “0” to the start visual channel 0 of the scan group 0.	0x00000000	
ADCK0SGVCEP0	Sets “0” to the end visual channel 0 of the scan group 0.	0x00000000	
ADCK0SGMCYCR0	Sets “1” to the number of multicycles for scan group 0.	0x00000000	
ADCK0ADCR2	Sets the signed 12-bit integer format.	0x00000010	
ADCK0SGSTCR0	Sets the operation start of the scan group.	0x00000001	
PIC21ADTEN500	Sets the trigger source to the compare match of Timer G1.	0x00000200	
PIC21ADCK0TSEL0	Set the trigger source to be selected in the register PIC2ADTEN500.	0x00000004	
TSCRG1	Clears the flag of Timer G1.	0x01	Compare match interrupt routine
ADCK0DR00	A/D conversion result is stored.	-	

2.24 Operation Ex.23 Activation of Other Module by Compare Match Generation [Timer G]

2.24.1 Overview

1) When the compare match is generated, generates the positive logic pulse signal of the 1 cycle, and activates the A/D convertor.

2) When the compare match is generated, activates the DMA, and transfers the A/D converted valve.

2.24.2 Explanation for Use Function

Table 2.25 show the functions allocations of the related registers.

Table 2.24 ATU-Ⅵ Function Allocation

Use Port		Function
Port	AN000	Analog input port of A/D convertor.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR1	Sets the division ration of the prescaler 0.
Timer G register	TCRG1	Sets each function of Timer G.
	OCRG1	Sets the compare match value of Timer G.
	TIERG	Sets the compare match interrupt setting.
	TCNTG1	Performs the timer count by the set clock bus in TCRG.
	TSTRG	Starts the timer counter of Timer G.
	TSRG1	The flag is set when the overflow and the compare match are generated.
	TSCRG1	Clears the flag.
A/D convertor register	ADCK0VCR00	Sets the virtual channel operation.
	ADCK0SGCR0	Sets the scan group operation.
	ADCK0SGVCSP0	Specifies the start virtual channel pointer.
	ADCK0SGVCEP0	Specifies the end virtual channel pointer.
	ADCK0SGMCYCR0	Set the number of multi-cycles.
	ADCK0SGSTCR0	Controls the operation start of the scan group 0.
	ADCK0DR00	The variable result of A/D is stored.
PIC2 register	PIC21ADCK0TSEL0	Selects the trigger source of the A/D conversion.
	PIC21ADTEN500	Selects the trigger source of the A/D conversion.
DMA register	DMA0CM_0	Sets the DMA channel master.
	DCEN0	Sets the channel operation enable/disable.
	DMA0SAR_0	Specifies the transfer source address.
	DMA0DAR_0	Specifies the transfer destination address.
	DMA0TSR_0	Sets the transfer size.
	DMA0TMR_0	Performs each function of transfer.
	DMA0RS_0	Sets the hardware DMA transfer source.
	DMA0CHFCR_0	Clears the DMA transfer status.
	DMA0OR	Sets the DMA operation enable/disable
	DMA0CHCR_0	Sets the channel operation enable/disable.
INTC register	EIBD70	Specifies the bind destination of the DMA ch0 transfer complete interrupt.
	EIC70	Set the interrupt vector method and the interrupt priority.

2.24.3 Operation Explanation

Figure 2.41 shows the operation principle. According to this, generates the compare match by the hardware and software processing of RH850/U2Bx. The compare match pulse is generated as the positive logic pulse when the compare match is generated. Perform the A/D conversion and DMA transfer using the positive logic pulse generated at this time as a trigger.

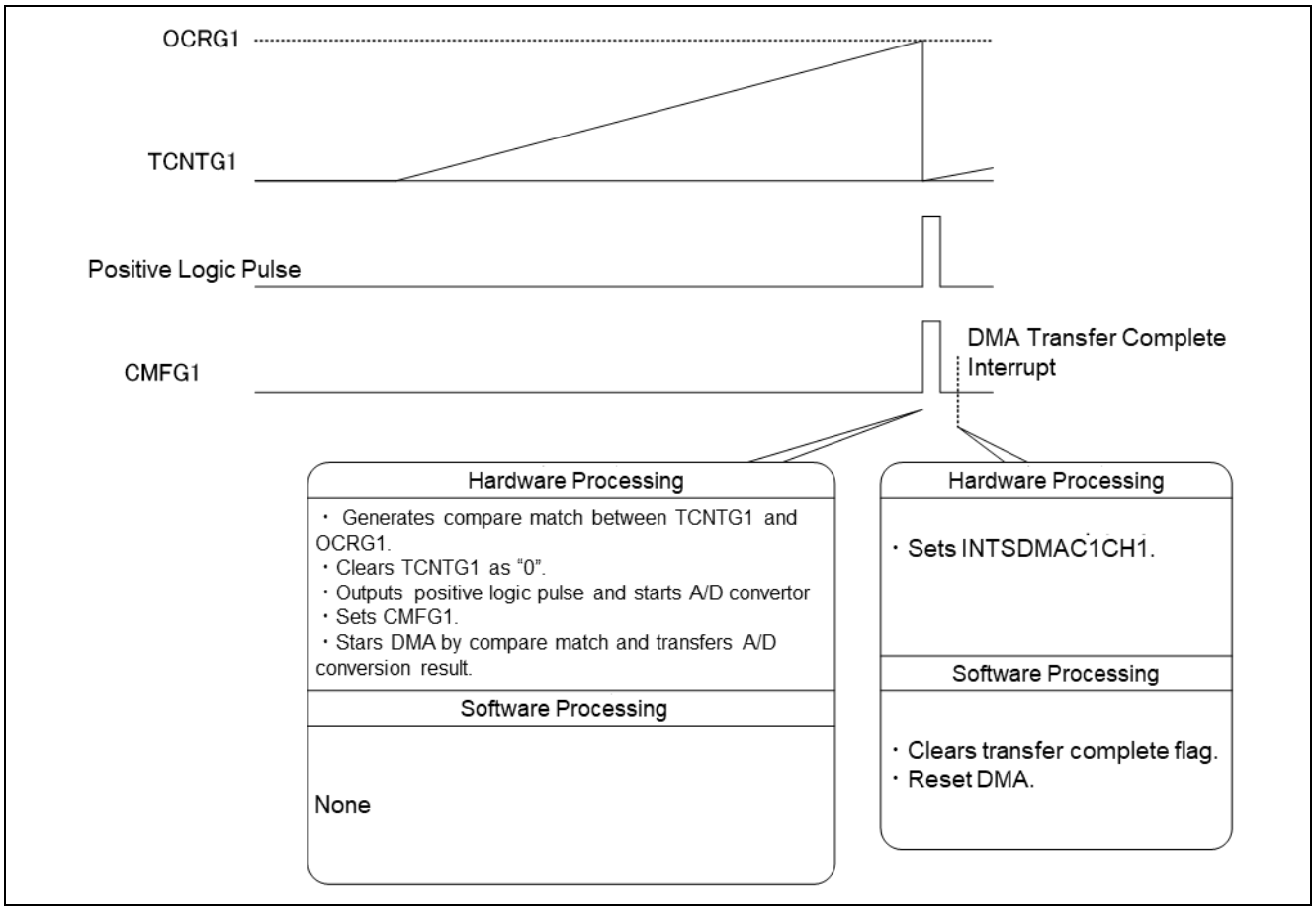


Figure 2.41 Operation Principle of A/D Conversion Activation by Compare Match

2.24.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
ATU setting	atu_init	Performs the initial setting of Timer G.
ADCK setting	ADCK_init	Performs the initial setting of ADCK.
DMA setting	sdmac_init	Performs the initial setting of DMA transfer.
Interrupt setting	intc_init	Perform the various settings and the application start.
DMA transfer end interrupt	eiint70	Perform the clearing of the transfer complete flag and DMA resetting.

Explanation of Use Variable

Label Name	Function	Data Length	Use Module Name
Trans_Data	Saves the converted value by A/D convertor.	unsigned short	DMA setting

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
MSR_SAD	Releases the ADCK module standby.	0x000000FE	
ATUENR	Enable the count operation of Timer G and presaler.	0x81	
PSCR1	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TCRG1	Sets t “0” to the Timer G sub block 1.	0x10	
OCRG1	Sets the compare match value corresponding to TCNTG1	0x00000400	
TSCRG1	Clears the flag.	0x03	
TSTRG	Enables the count operation of Timer G sub block 1.	0x0002	
EIBD70	Binds the compare match interrupt of DMA ch0 to PE0 (CPU0).	0x00000000	Interrupt setting
EIC70	Set the table reference method and interrupt priority method 0.	0x0040	
ADCK0VCR00	Sets the physical channel AN000 to the virtual channel 0.	0x00000000	ADCK setting
ADCK0SGCR0	Selects the SG0_TRG hardware trigger to the trigger input of the scan group 0.	0x00000001	
ADCK0SGVCSP0	Sets “0” to the start visual channel 0 of the scan group 0.	0x00000000	
ADCK0SGVCEP0	Sets “0” to the end visual channel 0 of the scan group 0.	0x00000000	
ADCK0SGMCYCR0	Sets “1” to the number of multicycles for scan group 0.	0x00000000	
ADCK0ADCR2	Sets the signed 12-bit integer format.	0x00000010	
ADCK0SGSTCR0	Sets the operation start of the scan group 0.	0x00000001	
PIC20ADTEN500	Sets the trigger source to the compare match of Timer G1.	0x00000200	
PIC20ADCK0TSEL0	Sets the trigger source to the compare match of Timer G1.	0x00000004	

Register Name	Function	Setting Value	Use Module Name
DMA0CM_0	Sets the DMA channel master.	0x00001C00	DMA setting
DMA0SAR_0	Specifies the register address of the A/D conversion of the A/D conversion value to the transfer source address.	ADCK0.DR00	
DMACSEL0_1	Sets “0” to the DMA transfer request group.	0x0C000000	
DMA0DAR_0	Specifies the address of the variable Trans_Data to the transition destination address.	Trans_Data	
DMA0TSR_0	Sets 2byte to the transfer size.	0x00000002	
DMA0TMR_0	Sets the following settings. ・Enables the reception of the hardware DMA transfer request. ・Enables the transfer complete interrput. ・Fixes the transfer transition address. ・Fixes the transfer source address. ・The transfer data size is 16bit.	0x00001011	
DMA0RS_0	Sets the hardware DMA transfer factor to the Timer G CMIG (OCRG1) compare match.	0x0001001D	
DMA0CHFCR_0	Clears each DMA flag.	0x0000320F	
DMA0OR	Enables the DMA operation.	0x0001	
DMA0CHCR_0	Enables the channel operation.	0x0003	
DMA0CHFCR_0	Clears the DMA transfer complete flag.	0x00000002	DMA transfer complete interrupt routine
DMA0TSR_0	Sets 2byte to the transfer size.	0x00000002	
DMA0CHCR_0	Enables the channel operation.	0x0003	
TSCRG1	Clears the Timer G compare match flag.	0x01	

2.25 Operation Ex.24 Multiplied Clock Generation [Timer B]

2.25.1 Overview

1） As shown in Figure 2.42, measures the external signal cycle, and generates the multiplied clock for it.

Performs the Timer D count-up in this multiplied clock and toggle output at regular intervals.

2） The cycle of the multiplied clock can be calculated by the following formula.

［Multiplied clock cycle (ns) = External input signal cycle ÷ Setting value of pulse interval multi plyer register］

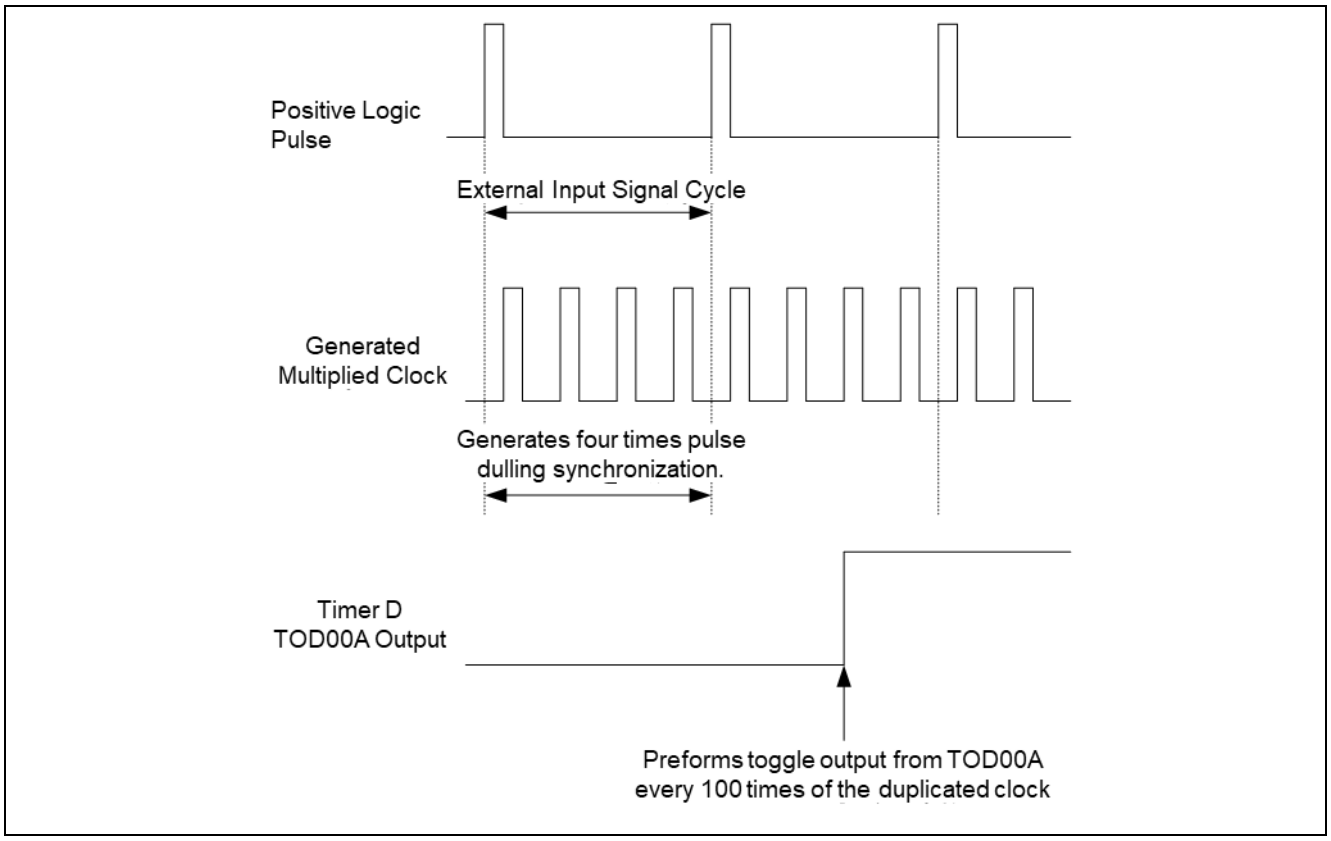


Figure 2.42 Multiplied Clock Generation (For PIMR1=4）

2.25.2 Explanation for Use Function

Table 2.26 shows the functions allocations of the ports used and related registers.

Table 2.25 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Inputs the measured pulse to this port.
	TDO00A	The compare match input port of Timer D.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	CBCNT	Sets the clock source of the clock bus 5.
Timer A register	TCR1A	Sets the event output of the operation clock and the external input edge of Timer A.
	TIOR1A	Detects the TIA0 rising edge.
Timer B register	TCRB	Sets the counter source of TCNTB0 and TCNTB2.
	TIORB	Performs the setting related with the counter operation enable and the multipled clock genaration.
	PIMR1	Sets the multiplication ration of the multiplied clock generated for the external input signal.
	OCRB10	Comprae register withTCNTB1.
	TCNTB3	Correction event counter.
	TCNTB5	Multiplied correction clock generation counter.
	TCCLRB	Correction counter clear register.
Timer D register	TCRD0	Sets the Timer D operation.
	TIOR1D0	Sets the Timer D input/output.
	TSRD0	Timer D status register.
	TSCRD0	Clears the Timer D status flag.
	OCR1D00	Sets the compare match value to TCNT1D0.
	TIER2D0	Performs the compare match interrupt setting.
	TSTRD	Enables the operation of Timer D sub block 0.
PORT register	PCR23_0	Sets the port function for the TIA00.
	PCR00_4	Sets the port function of TDO00A.
INTC register	EIBD164	Specifies the bind destination of the compare match interrupt between TCNT1D0 and OCR1D00 of Timer D.
	EIC164	Set the interrupt vector method and the interrupt priority.

2.25.3 Operation Explanation

Figure 2.43 shows the operation principle. According to this, generates the multiplied clock AGCK1 corresponding to the TIA0 input signal by the hardware and software processing of RH850/U2Bx. TCNTB2 performs a reloaded down-count on the captured value from the input edge measurement counter B0 (TCNTB0) of the edge measurement block. The pulse for multiplied clock is generated and it is used as the timer D clock when the TCNTB2 is reloaded.

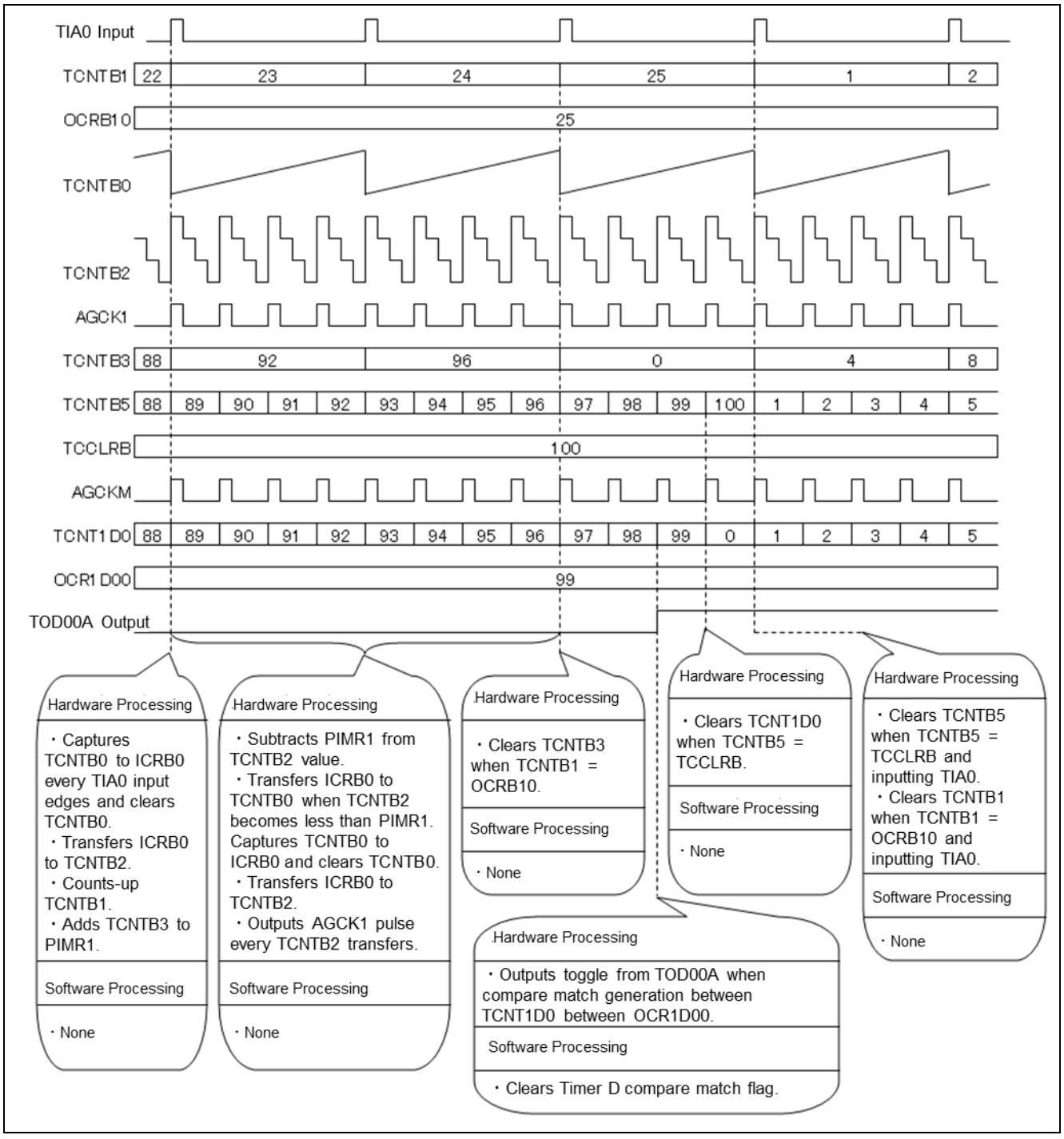


Figure 2.43 Operation Principle of Multiplied Clock Generation (For PIMR1=4)

2.25.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the setting of the port (P23_0, P00_4).
ATU setting	atu_init	Performs the initial setting of Timer A, B, and D.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Compare match interrupt routing	eiint164	Clears the flag of Timer D compare match.

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A, B, and D and presaler.	0x17	
PCR23_0	Sets P23_0 port to the input port TIA00.	0x00000058	Port setting
PCR00_4	Sets P00_4 port to the input port TOD00A.	0x0000004A	
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
CBCNT	Selects the angle clock of Timer B to the clock bus 5.	0x04	
TCR1A	Output the input signal for TIA0 to Timer B as the event.	0x08	
TIOR1A	Detects the rising edge of the input signal for TIA0.	0x0001	
TIORB	Enables the external event input for Timer B.	0x20	
PIMR1	Sets “4” to the multiplication ration of the multiplied clock corresponding to the external input cycle.	0x0004	
TCRB	Set TCNTB3 and TCNTB1 to be cleared by the compare match between TCNTB1 and OCRB10.	0x60	
OCRB10	Sets “25” to the compare match value with TCNTB1 to be cleared TCNTB1 and TCNTB3.	0x19	
TCCLRB	Sets “100” to the upper limit of TCNTB5.	0x00064000	
TCNTB5	Sets “100” to the initial value of TCNTB5.	0x00064000	
TCRD0	Set CNT1D0 to be up-counted on clock bus 5 and DCNTD00 to 03 to be down-counted on clock bus 5. Set to clear TCNT1D0 with the signal from timer B.	0x1055	
TIOR1D0	Performs the toggle output from TOD00A port when the compare match A of OCR1D00 is generated.	0x0103	
TSCRD0	Clears each flag of Timer D.	0x03FF	
OCR1D00	For OCR1D00, sets “100” to the condition of the compare match A corresponding to TCNT1D0.	0x00000063	
TIER2D0	Enables the compare match interrupt.	0x00000001	
TSTRD	Enables the Timer D sub block 0 operation.	0x0001	
EIBD164	Binds the CMID00 interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC164	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRD0	Clears the compare match flag of Timer D.	0x0010	Compare match interrupt routine

2.26 Operation Ex.25 Detection of Missing Teeth in Input Signal Using Multiplied Clock [Timer B]

2.26.1 Overview

1) As shown in Figure 2.44, measures the external signal cycle and generates the multiplied clock corresponding the cycle.

2) Detects the missing teeth from the count of the generated multiplied clock.

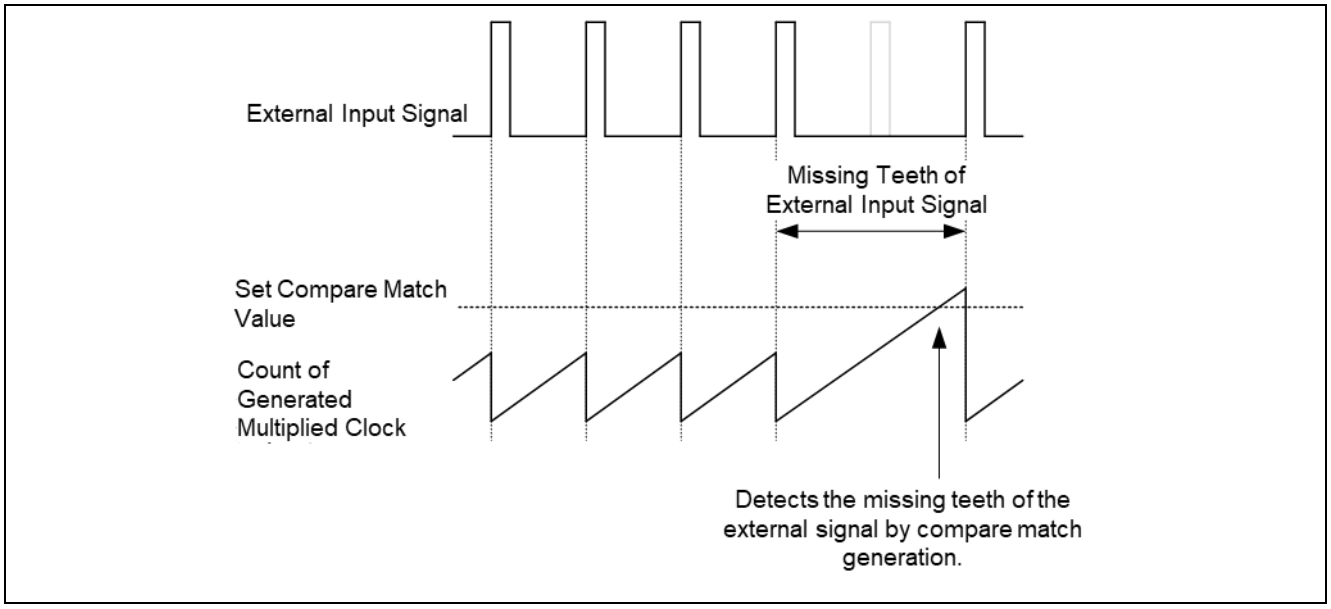


Figure 2.44 Detection of Missing Tooth of Multiplied Clock

2.26.2 Explanation of Use Function

Table 2.27 shows the functions allocations of the ports used and related registers.

Table 2.26 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Inputs the measured pulse to the port.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer A resgiter	TCR1A	Sets the event output of the operation clock and the external input edge of Timer A.
	TIOR1A	Detects the TIA0 rising edge.
Timer B register	TCRB	Sets the counter source of TCNTB0 and TCNTB2.
	TIORB	Performs the setting related with the counter operation enable and the multipled clock genaration.
	PIMR1	Sets the multiplication ration of the multiplied clock generated for the external input signal.
	TICRB	Sets the interrupt request enables.
	TIERB	Performs the compare match interrupt setting.
	TCNTB6	Perfoms the count operation by the generated multiplied clock.
	OCRB6	Sets the input edge spacing to detect as missing teeth.
	TSRB	The status flag of Timer B is stored.
	TSCRB	Clears the flag of Timer B.
PORT register	PCR23_0	Sets P23_0 to TIA00.
INTC register	EIBD97	Specifies the bind destination of the compare match interrupt between TCNTB6 and OCRB6 of Timer B.
	EIC97	Set the interrupt vector method and the interrupt priority.

2.26.3 Operation Explanation

Figure 2.45 shows the operation principle. According to this, detects the missing teeth of the input signal by the hardware and software processing of RH850/U2Bx. It is found that there is a missing tooth when the compare match between TCNTB6 and OCRB6 occurs, and an interrupt request can be generated at any of the timings (A), (B), and (C) in the figure below. In this operation example, the interrupt request is set to be generated at the timing of (A).

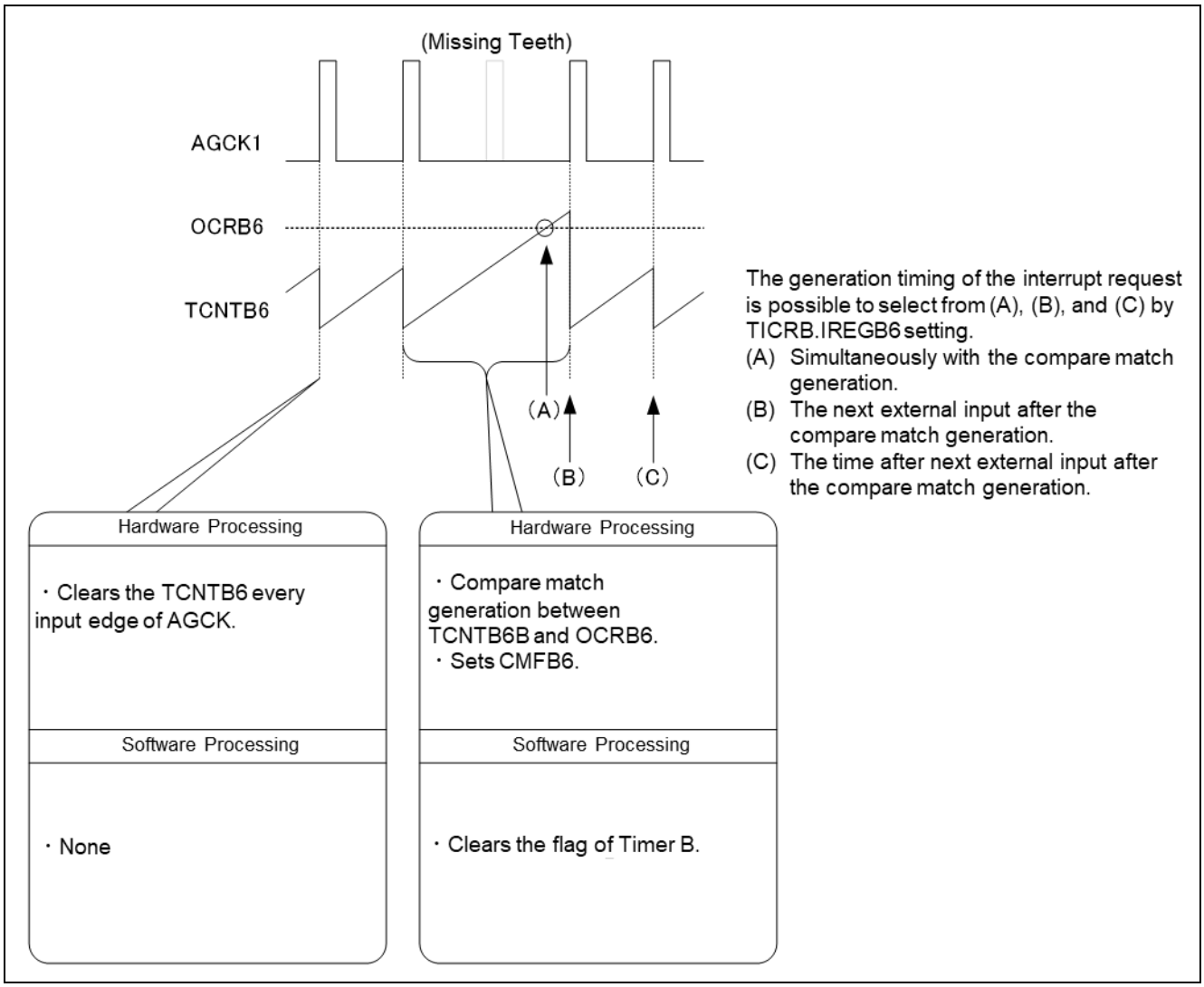


Figure 2.45 Operation Principle of Missing Teeth Detection

2.26.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the setting of the port (P23_0).
ATU setting	atu_init	Performs the initial setting of Timer A and B.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Missing Teeth Detection Routine	eiint97	Jumps to this routine if the missing teeth is detected.

Explanation of Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A and B and presaler.	0x07	
PCR23_0	Sets P23_0 port to the input port TIA00.	0x00000058	Port setting
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TCR1A	Output the input signal for TIA0 to Timer B as the event.	0x08	
TIOR1A	Detects the rising edge of the input signal for TIA0.	0x0001	
TIORB	Sets the reload value of TCNTB2 to the value of ICRB and enables the external event input. Enables the compare match between TCNTB6 and OCRB6.	0x21	
PIMR1	Sets “4” to the multiplication ration of the multiplied clock corresponding to the external input cycle.	0x0004	
TCRB	Sets the use clock of TCNTB0 and TCNTB2 to the clock bus 0.	0x00	
TICRB	Sets the interrupt output timing in OCRB6 compare match to “simultaneously with compare match”.	0x00	
TIERB	Sets the compare match interrupt enable.	0x0008	
TCNTB6	Sets “0” to the initial value of the multiplied clock counter.	0x00000000	
OCRB6	Sets “5” to the compare match value with TCNTB6 for judging the missing teeth detection. *	0x00005000	
EIBD97	Binds the CMIB6 interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC97	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRB	Clears the flag of Timer B.	0x0008	Missing teeth detection routine

*The sample program sets the value to detect from one tooth missing.

2.27 Operation Ex.26 Detection of Missing Teeth Using Input Interval Ratio of Input Events [Timer B]

2.27.1 Overview

Figure 2.46 shows the method of the missing teeth detection to compare the input intervals of two external event signals.

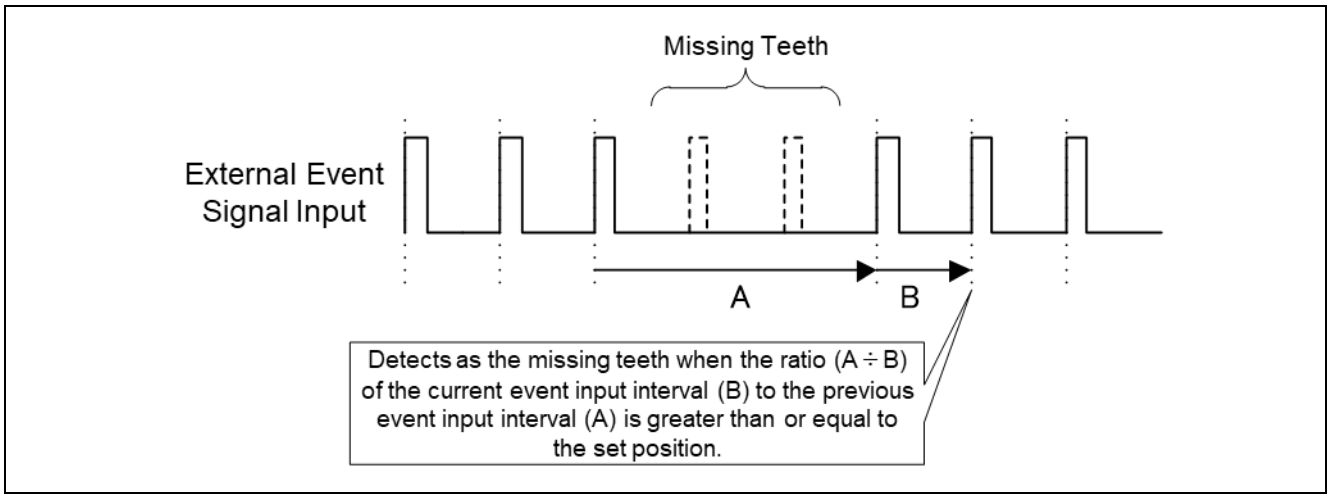


Figure 2.46 Detection of Missing Teeth Comparing Input Interval Ratio of Input Events

2.27.2 Explanation of Use Function

Table 2.28 shows the functions allocations of the ports used and related registers.

Table 2.27 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	The port for inputing the external event.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer A register	TCR1A	Sets the event output of the operation clock and the external input edge of Timer A.
	TIOR1A	Detects the TIA00 rising edge.
Timer B register	TCRB	Sets the counter source of TCNTB0 and TCNTB2.
	TIORB	Performs the setting related with the counter operation enable and the multipled clock genaration.
	PIMR1	Sets the multiplication ration of the multiplied clock generated for the external input signal.
	PIMR2	Sets the multiplication ration of the mutiplied clock after the missing teeth input.
	TICRB	Sets the generation timing of the interrupt request.
	TIERB	Perfroms the setting of the compare match interrupt.
	TCNTB1	Count the number of external event inputs.
	TCNTB6	Perfomrs the count operation by the generated multiplied clock.
	TCNTB6M	Perfomrs the count operation by the multiple of TCNTB6 set in RARB6.
	RARB6	Sets the count-up value of TCNTB6M.
	OCRB6	Sets the input edge interval deteced as the missing teeth.
	OCRB10	This is the compare match value for TCNTB1. TCRB setting value clears TCNTB1 and TCNYB3 when the compare match is generated.
	OCRB11	This is the compare match value for TCNTB1.TCRB setting value selects PIMR2 instead of PIMR1 duling the compre match.
	TSRB	The status flag of Timer B is stored.
	TSCRB	Cleras the flag of Timer B.
PORT register	PCR23_0	Sets P23_0 to TIA00.
INTC register	EIBD97	Specifies the bind destination of the compare match interrupt between TCNTB6 and OCRB6 of Timer B.
	EIC97	Set the interrupt vector method and the interrupt priority.
	EIBD101	Specifies the bind destination of TCNTB6M interrupt of Timer B.
	EIC101	Set the interrupt vector method and the interrupt priority.
	EIBD102	Specifies the bind destination of TCNTB6E interrupt of Timer B.
	EIC102	Set the interrupt vector method and the interrupt priority.

2.27.3 Operation Explanation

Figure 2.47 shows the operation principle.

TCNTB6M is the counter that counts-up TCNTB6 by the multiple set by RARB6. ICRB6 captures TCNTB6 at the input timing of the external event (TIA). The comparison between TCNTB6M and ICRB6 is performed every input timing of the external event. When TCNTB6M <ICRB6, it is detected that there is a missing tooth and CMIB6M interrupt is generated.

Also, it is possible to generate the CMIB6E interrupt depending on the combination condition of CMIB6 interrupt and CMIB6M interrupt. In this operation example, the CMIB6E interrupt is generated under the AND Condition of the CMIB6 interrupt and the CMIB6M interrupt.

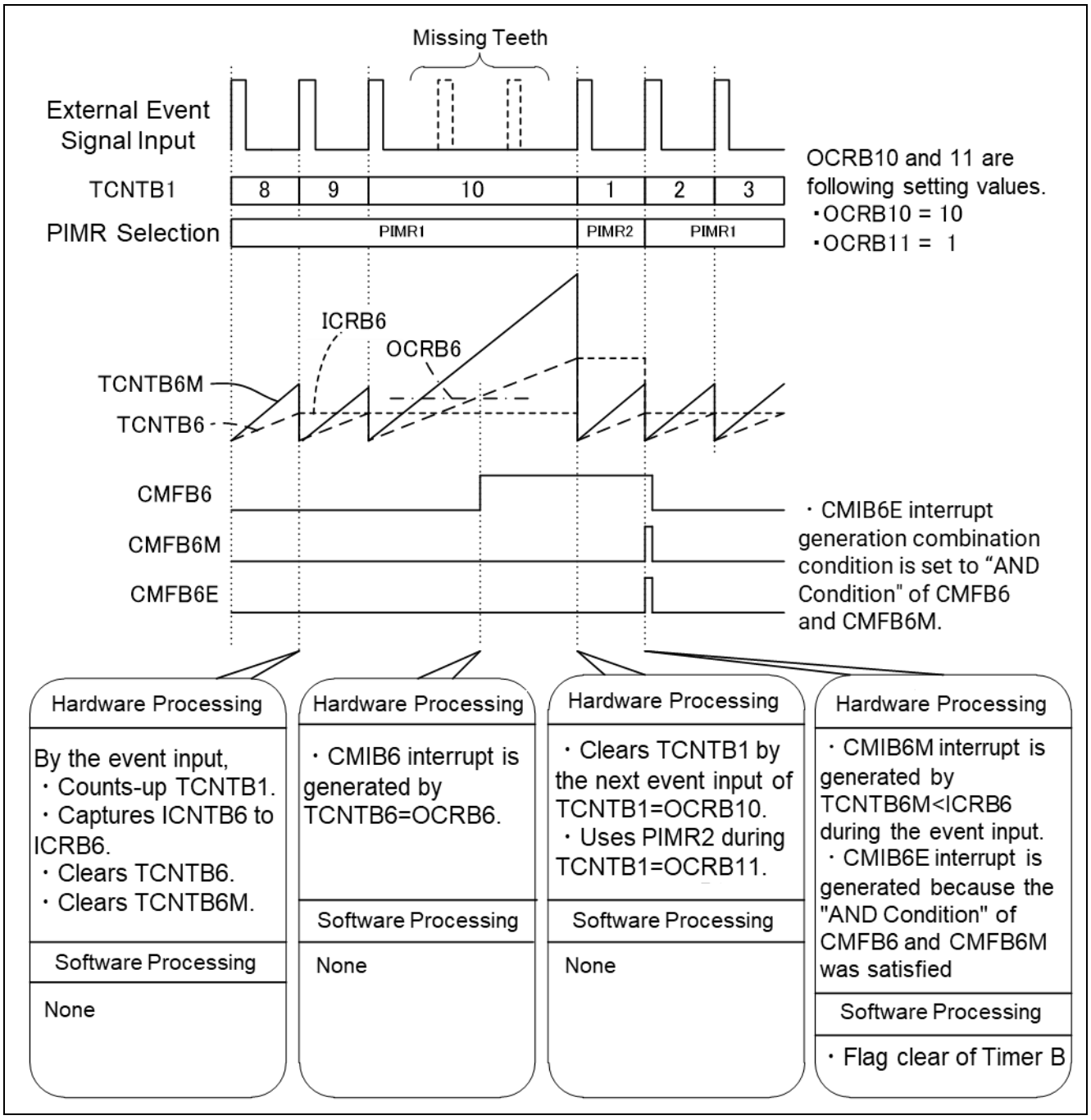


Figure 2.47 Operation Principle of Missing Teeth Detection

2.27.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the setting of the port (P23_0).
ATU setting	atu_init	Performs the initial setting of Timer A and B.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Missing teeth detection routine 1	eiint97	This is the CMIB6 (compare match between TCNTB6 and OCRB6) interrupt function. Jumps to this routine when the input interval for external events exceeds the set value.
Missing teeth detection routine 2	eiint101	This is the CMIB6M (compare match between TCNTB6M and ICRB6) interrupt function. Compares the previous and current external event input intervals, and jumps to this routine if it is greater than or equal to the set value.
Missing teeth detection condition match routine	eiint102	This is the CMIB6E (combination condition match between CMIB6 and CMIB6M) interrupt function. Clears each interrupt flag.

Explanation of Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A and B and presaler.	0x07	
PCR23_0	Sets P23_0 port to the input port TIA00.	0x00000058	Port setting
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TCR1A	Output the input signal for TIA0 to Timer B as the event.	0x08	
TIOR1A	Detects the rising edge of the input signal for TIA0.	0x0001	
TCRB	Sets the use clock of TCNTB0 and TCNTB2 to the clock bus 0. Sets the compare match of TCNTB1 and OCRB10 to the clear trigger of TCNTB1 and TCNTB3.	0xE0	
TIORB	Sets the reload value of TCNTB2 to the value of ICRB and enables the external event input. Enables the compare match between TCNTB6 and OCRB6.	0x29	
PIMR1	Sets “4” to the multiplication ration of the multiplied clock corresponding to the external input cycle.	0x0004	
PIMR2	Sets “12” to the multiplication ration during the compare match between TCNTB1 and OCRB11.	0x000C	
TICRB	Sets the CMIB6 interrupt output timing at the same time as the compare match. Sets the combination condition of CMIB6E interrupt output to the AND Condition of CMIB6 and CMIB6M.	0x04	
TIERB	Sets the compare match interrupt enable.	0x0308	
OCRB6	Sets “6” to the compare match value with TCNTB6.	0x00006000	
OCRB10	Sets “10” to the compare match value with TCNTB1.	0x0A	
OCRB11	Sets “1” to the compare match value with TCNTB1.	0x01	
RARB6	Sets “2.5” to the count-up value of the multiplied clock counter TCNTB6M.	0xA0	
EIBD97	Binds the CMIB6 interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC97	Set the table reference method and interrupt priority method 0.	0x0040	
EIBD101	Binds the CMIB6M interrupt to PE0 (CPU0).	0x00000000	
EIC101	Set the table reference method and interrupt priority method 0.	0x0040	
EIBD102	Binds the CMIB6E interrupt to PE0 (CPU0).	0x00000000	
EIC102	Set the table reference method and interrupt priority method 0.	0x0040	
TSCRB	Clear each flags of CMFB6, CMFB6M, and CMFB6E of Timer B.	0x0308	Missing teeth detection condition match routine

2.28 Operation Ex.27 One Shot Pulse Output by Multiplied Correction Clock [Timer B]

2.28.1 Overview

For external input signals containing missing teeth, the following shows the operation example which the pulse is output at fixed position based on the missing tooth. Outputs the one-shot pulse by operating the down-counter with the multiplied correction clock generated from the external input signal, high-outputting at the start of the operation of this down-counter, and low-outputting at the time of the underflow.

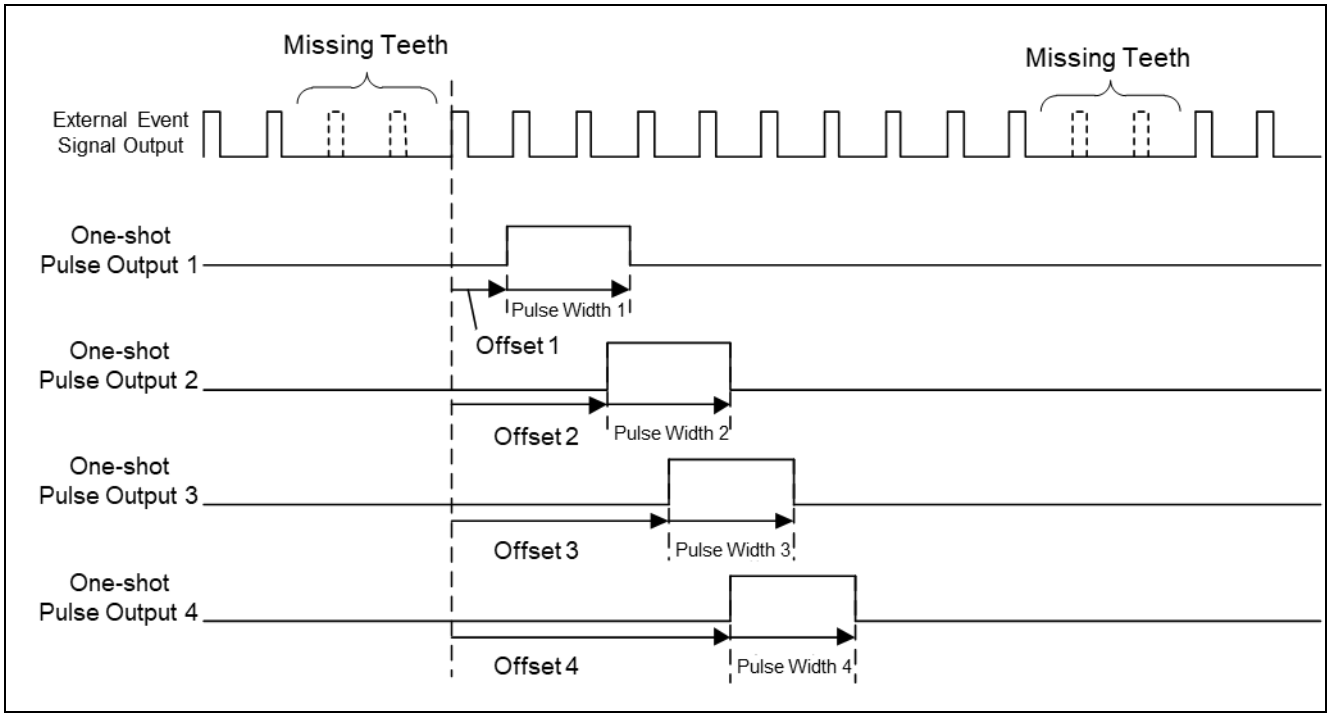


Figure 2.48 Generation of One-shot Pulse Based on Missing Tooth (Overview)

2.28.2 Explanation for Use Function

Table 2.29 shows the functions allocations of the ports used and related registers.

Table 2.28 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA01	Input the external input signal using the multiplied clock generation to this port.
	TOD00～03B	Outputs the one-shot pulse to this port.
Related Register		**Function**
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	CBCNT	Sets the clock source of the clock bus 5.
	ATUINTSELD0	Selects the Timer D interrupt.
Timer A register	TCR1A	Set the operation clock of Timer A and the event output of the external input edge.
	TIOR1A	Sets the detection dege of TIA01.
	TIERA	Performs the input capture interrupt setting.
	TSRA	The input capture flag is stored.
	TSCRA	Clears the input capture flag.
Timer B register	TCNTB2	The value of the external event input is updated.
	LDB	Used for the TCNTB2 and RLDB updates.
	RLDB	It is updated to the value obtained by subtracting PIMR1 from the value of ICRB0 or LDB.
	TICRB	Enables the interrupt.
	TIERB	Performs the setting of the compare match interrupt.
	TCRB	Sets the counter source of TCNTB0 and TCNTB2.
	TIORB	Performs the setting related with the count operation enable and the multipled clock genaration.
	PIMR1	Sets the multiplication ration of the generating multiplied clock.
	TCNTB3	Transfers the value to TCNTB4 every external input signal, and the value of PIMR1 is added.
	TCNTB4	Reads the TCNTB3 value every external input signal, and performs the up-count operation at the multiplied clock.
	TCNTB5	Perfoms the up-count operation with the unmodulated low-speed clock when it is smaller than the TCNTB4 value.
	TCCLRB	Functions as the TCNTB5 upper limit. TCNTB5 is cleared to “1” when TCNTB3=0 and TCNTB5 matches this register when an external event is input.
	TCNTB6	Counts-up by AGCK1.
	OCRB6	Sets the compare match value corresponding to TCNTB6.
	TSRB	The compare match flag of Timer B is stored.
	TSCRB	The compare match flag of Timer B is cleared.

Related Register		Function
Timer D register	TCRD0	Sets the operation clock bus of each Timer D counter.
	TIOR1D0	Set wether or not each compare match generates and the operation when it generates.
	TIOR2D0	Enables the compare match of OCR2D.
	DCRD0	Set the operation start and stop condtion of the down-count.
	TSRD0	The compare match flag of Timer D is stored.
	TSCRD0	Clears the compare match flag of Timer D.
	TIER2D0	Performs the setting of the compare match interrupt.
	OCR1D00 ～03	Sets the conditon value OCR1D00 to OCR1D03 of the compare match A corresponding to TCNT1D0.
	OCR2D00	Sets the condition of the compare match B corresponding to TCNT2D0.
	DCNTD00 ～03	The counter register of the down-counter.
	TCNT2D0	Clears TCNT2D0 of Timer D.
	TSTRD	Starts the Timer D count.
PORT register	PCR23_1	Sets P23_1 to TIA01.
	PCR22_7	Sets P22_7 to TOD00B.
	PCR22_6	Sets P22_6 to TOD01B.
	PCR22_9	Sets P22_9 to TOD02B.
	PCR22_8	Sets P22_8 to TOD03B.
INTC register	EIBD87	Specifies the bind destination of the input capture interrupt of TIA01 of Timer A.
	EIC87	Set the interrupt vector method and the interrupt priority.
	EIBD97	Specifies the bind destination of the compare match interrupt between TCNTB6 and OCRB6 of Timer B.
	EIC97	Set the interrupt vector method and the interrupt priority.
	EIBD164	Specifies the bind destination of the compare match interrupt between TCNT2D0 and OCR2D00 of Timer D.
	EIC164	Set the interrupt vector method and the interrupt priority.

2.28.3 Operation Explanation

（1） Operating Principle of One-shot Pulse Output at Fixed Position Based on Missing Tooth

Figure 2.49 shows the operating principle of one-shot pulse output at a fixed position with respect to the missing tooth. It is possible to output a pulse at a fixed position based on the missing tooth by the hardware and software processing of RH850/U2Bx.

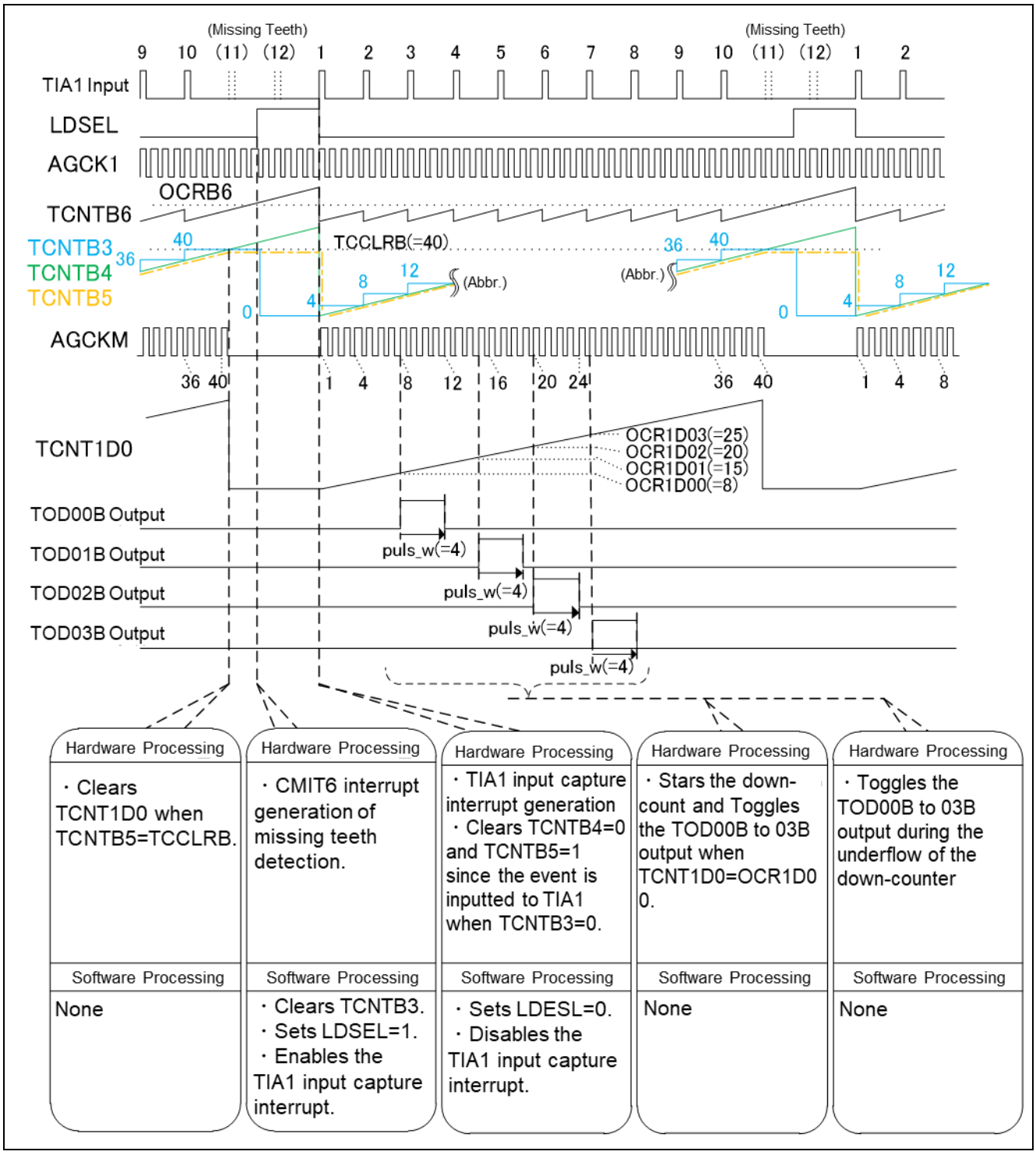


Figure 2.49 One-shot Pulse Output at Fixed Position Based on Missing Tooth

（2） Generation Principle of Multiplied Correction Clock

Figure 2.50 shows the principle of correction clock generation during deceleration and Figure 2.51 shows the principle of correction clock generation during acceleration. According to this, performs the generation of the multiplied correction clock corresponding to the input signal by the hardware processing of RH850/U2Bx.

［Common Processing］

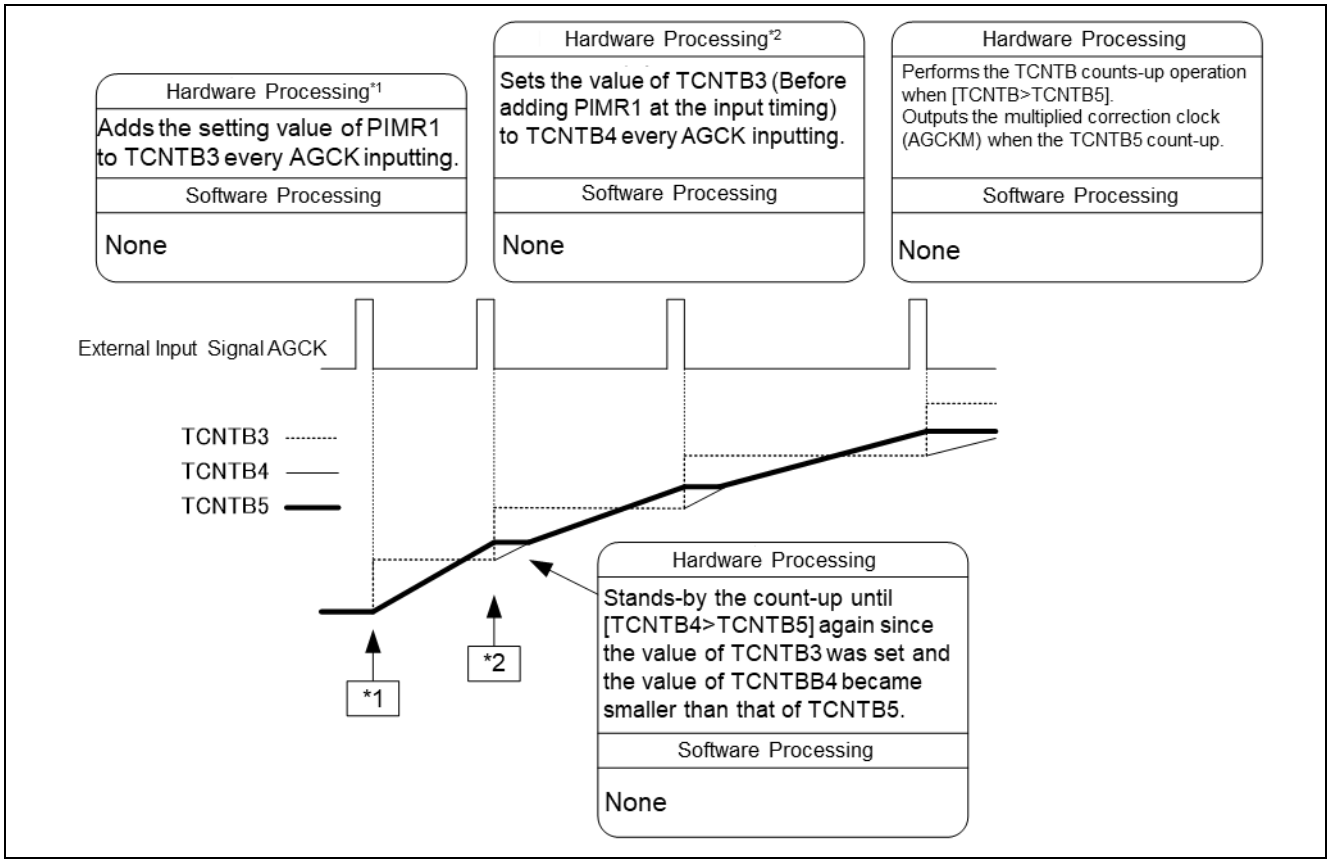


Figure 2.50 Generation Principle of Multiplied Correction Clock (Deceleration)

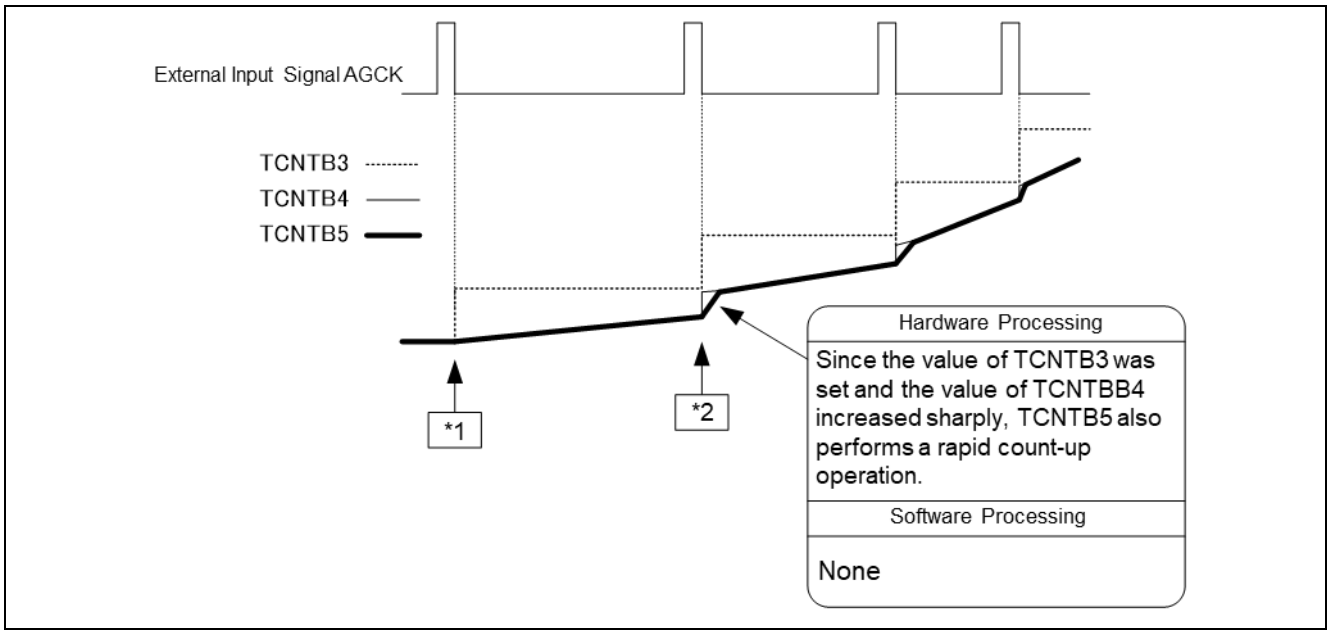


Figure 2.51 Generation Principle of Multiplied Correction Clock (Acceleration)

（3） Use Example for Multiplied Correction Clock

When generating the multiplied clock from the external input signal with the changing period, the operation is different when the correction is not used and when it is used as shown in the figure below. Using each signal for the clock, Figure 2.52 and 2.53 shows the waveforms when the software “outputs the pulses by 12 counts (3 tooth of external input) from the certain external input” is executed. (When the PIM value is 4.)

［1］ When interval of Input Signal Increases (Decelerating)

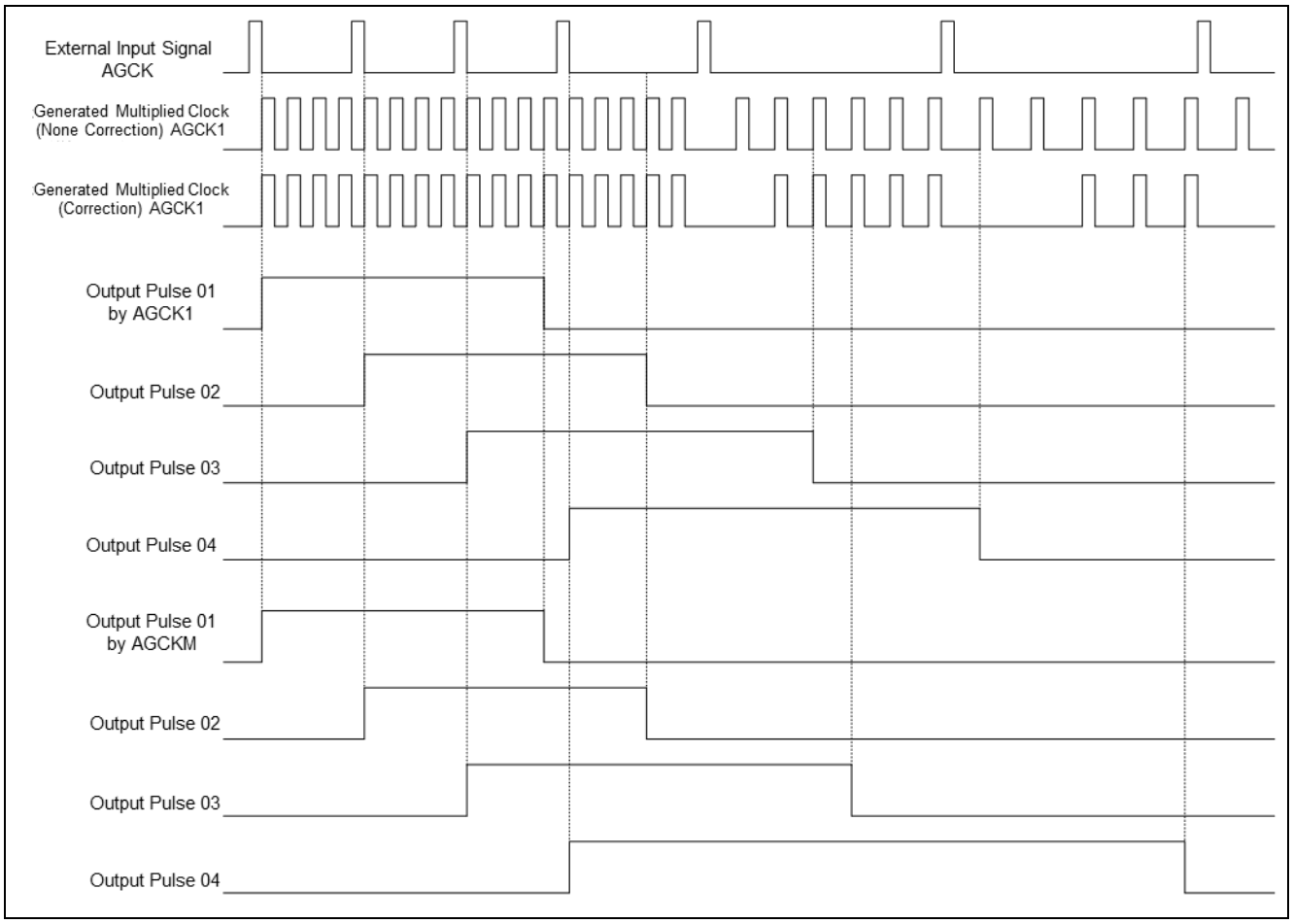


Figure 2.52 Comparison regarding Multiplied Function Use (When Decelerating and PIM=4)

［2］When interval of Input Signal Decreases (Accelerating)

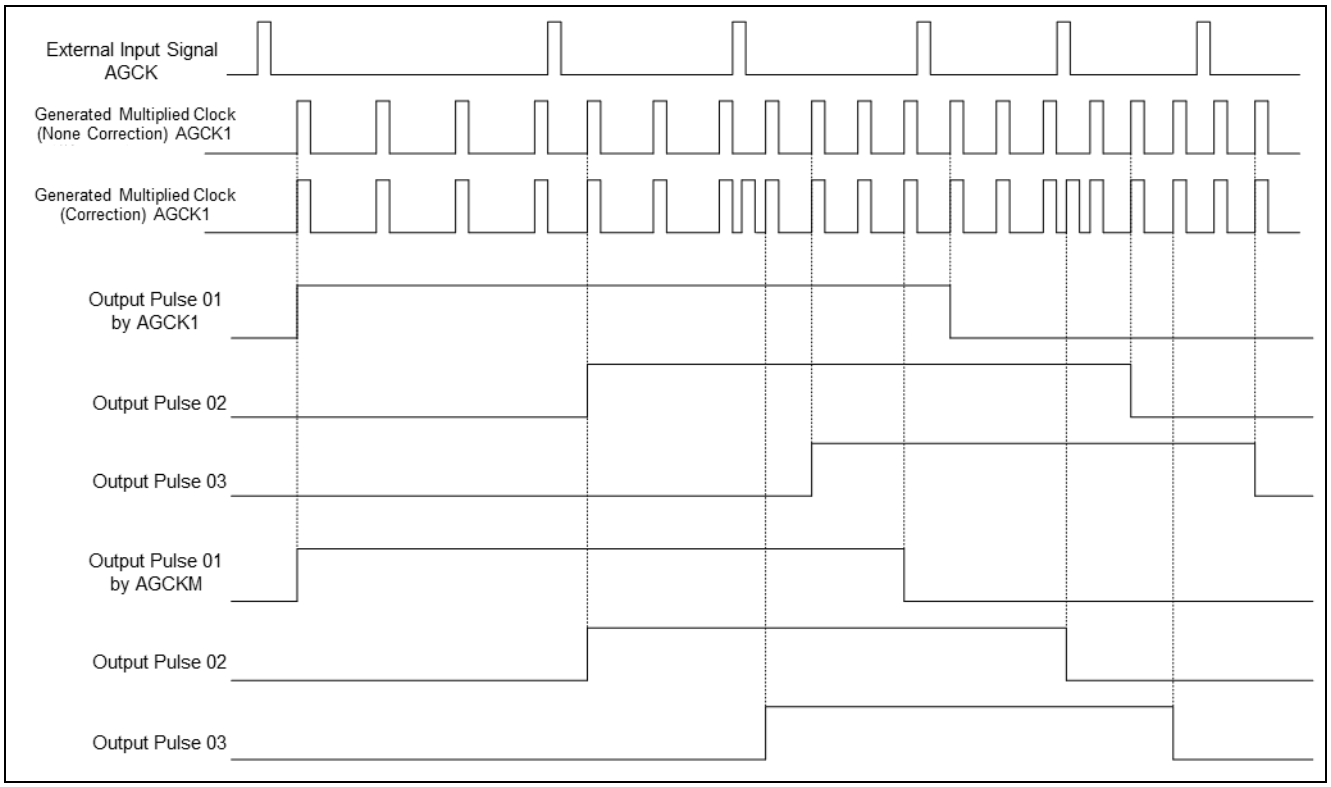


Figure 2.53 Comparison regarding Multiplied Function Use (When Accelerating and PIM=4)

In this way, when the wavelength of the input signal changes to be based on the count operation using the multiplied clock, it is possible to perform the processing according to the wavelength even without the soft processing for waveform length. And it corresponds to the interval of the external input signal more accurately by using the correction function.

2.28.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the setting of the port (P32_4 and P22_7 to 7).
ATU setting	atu_init	Performs the initial setting of Timer A, B and D.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Input capture interrupt handler	eiint87	Performs this routine when the external signal is detected.
Compare match interrupt handler	eiint164	Performs this routine when the compare match between TCNT3D0 and OCR2D00 is generated.
Pulse output routine	eiint97	Performs this routine when the compare match between TCNTB6 and OCRB6 is generated.

Explanation for Use Constant

Label Name	Function	Setting Value	Use Module Name
offset_0	Sets the offset time of the TOD00B output pulse.	0x00000008	ATU setting
offset_1	Sets the offset time of the TOD01B output pulse.	0x0000000F	ATU setting
offset_2	Sets the offset time of the TOD02B output pulse.	0x00000014	ATU setting
offset_3	Sets the offset time of the TOD03B output pulse.	0x00000019	ATU setting
pulse_w	Set the output pulse widths of TOD00B to 03B.	0x00000004	Pulse output routine

Explanation of Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A , B, and D and presaler.	0x17	
PCR23_1	Sets P23_0 port to the input port TIA01.	0x00000058	Port setting
PCR22_7 PCR22_6 PCR22_9 PCR22_8	Set the ports P22_7, P22_6, P22_9, and P22_8 to TOD00B,01B,02B, and 03B.	0x0000004B	
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
CBCNT	Sets the clock source of the clock bus 5 to the multiplied correction clock of Timer B.	0x04	
ATUINTSELD0	Sets Interrupt Number 140 (NTATUDSLID00 interrupt) to OCR2D0_0.	0x00000001	
TCR1A	Outputs the input signal for TIA01 to Timer B as the event.	0x10	
TIOR1A	Detects the rising edge of the input signal for TIA1.	0x0004	
TIERA	Enables the input capture interrupt.	0x0002	
TSCRA	Clears the input capture flag.	0x80FF	

Register Name	Function	Setting Value	Use Module Name
TIORB	Uses the ICRB value as the reload value of TCNTB2, enables the input of the external event, and sets not to stop the TCNTB4 counting when TCNTB3=TCNTB4.	0x21	ATU setting
PIMR1	Sets “4” to the multiplication ration of the multiplied clock regarding to the external input cycle.	0x0004	
TCRB	Sets the use clock of TCNTB0 and TCNTB2 to the clock bus 0.	0x00	
TICRB	Outputs the interrupt request when CMFB6 is enabled.	0x00	
TIERB	Sets the compare match interrupt enable.	0x0002	
TCCLRB	Sets the TCNTB5 upper limit to 0x28(= PIMR1 × Number of external inputs to set).	0x00028000	
TCNTB5	Set the initial value of the multiplied correction clock generation counter B5 to the same value as TCCLRB.	0x00028000	
TCNTB6	Sets “0” to the initial value of the multiplied clock counter B6.	0x00000000	
OCRB6	Sets “6” to the compare match value regarding to TCNTB6.	0x00006000	
LDB	Sets “0x7D0” to the LDB value.	0x000007D0	
TCRD0	Set TCNT1D0, DCNTD00, and TCNT2D0 to perform up/down-counts on clock bus 5 respectively.	0x1555	
TIOR1D0	Enables the compare match of OCR1D00 to 03.	0x00FF	
TIOR2D0	Enables the compare match of OCR2D.	0x0003	
DCRD0	Starts the down-count when the compare match A is generated.	0x2222	
TSCRD0	Clears the compare match flag.	0x3FFF	
TIER2D0	Sets the compare match interrupts to enabled.	0x00000100	
OCR1D00～03	Sets the offset value.	0x00000008 0x0000000F 0x00000014 0x00000019	
OCR2D00	Set the condition of compare match B corresponding to TCNT2D0.	0x00000001	
TSTRD	Starts the count of Timer D sub block 0.	0x0001	

Register Name	Function	Setting Value	Use Module Name
EIBD87	Binds the TIA1 input capture interrupt of Timer A to PE0 (CPU0).	0x00000000	Interrupt setting
EIC87	Set the table reference method and interrupt priority 0.	0x0040	
EIBD97	Binds the Timer B compare match interrupt between TCNTB6 and OCRB6 to PE0 (CPU0).	0x00000000	
EIC97	Set the table reference method and interrupt priority 0.	0x0040	
EIBD164	Binds the Timer D compare match interrupt between TCNT2D0 and OCR2D00 to PE0 (CPU0).	0x00000000	
EIC164	Set the table reference method and interrupt priority 0.	0x0040	
TIORB	Set to use the LDB value for the calculation of TCNTB2 load data and RLDB load data.	LDSEL=1	Pulse output routine
TSCRB	Clears the compare match flag of Timer B.	0x037F	
TSCRA	Clears the input capture flag of Timer A.	0x8002	
TIERA	Enables the input capture interrupt of Timer A.	0x0002	
TCNTB3	Clears the correction event counter as “0”.	0x00000000	
DCNTD00～03	Sets the down-counter value.	0x00000004	
TIORB	Set to use the ICRB0 value for the calculation of TCNTB2 load data and RLDB load data.	LDSEL=0	Input capture interrupt handler
TSCRA	Clears the input capture flag of Timer A.	0x8002	
TIERA	Disables the input capture interrupt of Timer A.	0x0000	
TCNT2D0	Clears TCNT2D0 of Timer D.	0x00000000	Compare match interrupt handler (2D0)

2.29 Operation Ex.28 One-shot Pulse Outputs Using Multiplication Ration Automatic Switching Function [Timer B]

2.29.1 Overview

The operation example is shown in which a pulse is output at the fixed position regarding to the missing tooth for the external input signal containing the missing tooth. Operates the down-count by the generated multiplied correction clock from the output input signal, high-outputs at the start of the down-counter, and outputs the one-shot pulse to perform the low-output during the underflowing.

In this operation example, the multiplication ration setting of the multiplied clock immediately after the missing teeth is changed by the hardware.

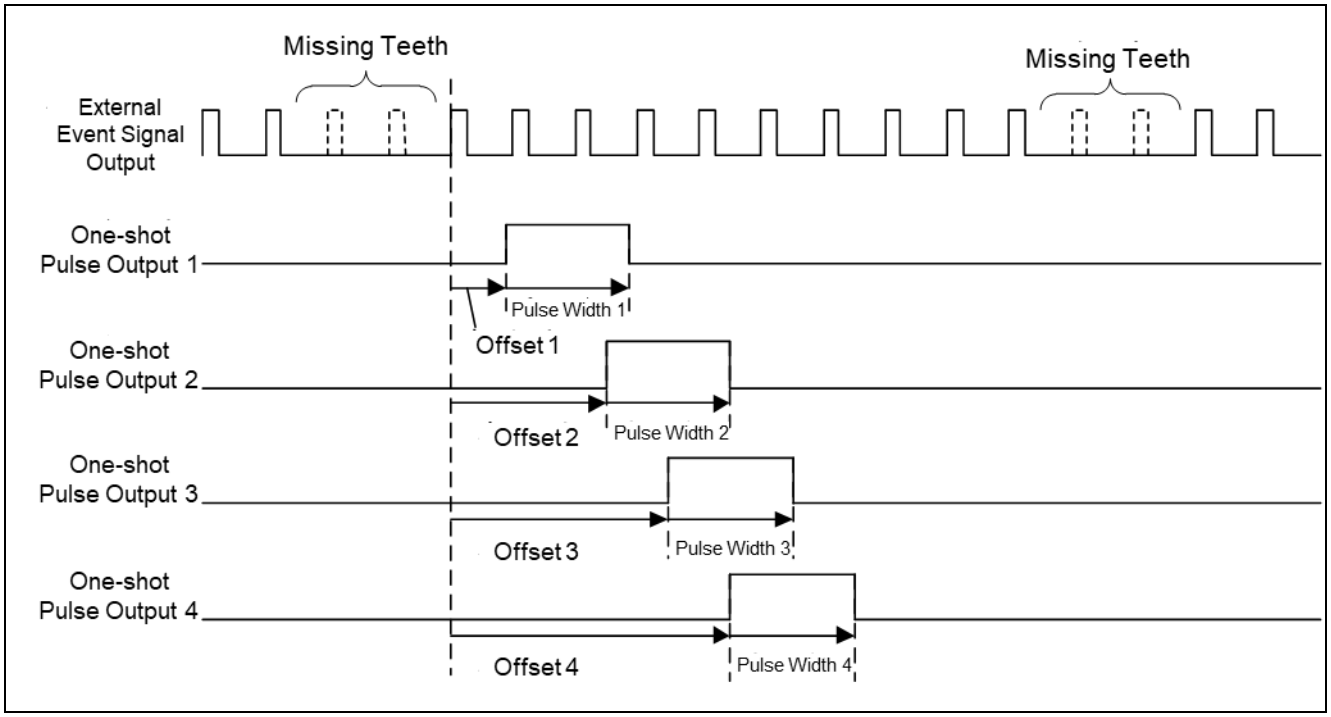


Figure 2.54 One-shot Pulse Generation Based on Missing Teeth (Overview)

2.29.2 Explanation for Use Function

Table 2.30 shows the functions allocations of the ports used and related registers.

Table 2.29 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Input the external input signal using the multiplied clock generation to this port.
	TOD00～03B	Outputs the one-shot pulse to this port.
Related Register		**Function**
ATU-Ⅵ Common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	CBCNT	Sets the clock source of the clock bus 5.
Timer A register	TCR1A	Set the operation clock of Timer A and the event output of the external input edge.
	TIOR1A	Sets the detection dege of TIA00.
Timer B register	TCRB	Set the counter sources of TCNTB0 and TCNTB2.
	TIORB	Performs the setting related to the multiplied clock generation such as permission of count operation.
	PIMR1	Sets the multiplication ration of the generating multiplied clock.
	PIMR2	Sets the multiplication ration of the multiplied clock imediatery after the missing teeth inputing.
	TICRB	Enables the interrupt.
	TIERB	Performs the setting of the compare match interrupt.
	TCNTB1	Counts the input edge of the external input signal.
	TCNTB5	Perfoms the up-count operation with the unmodulated low-speed clock when it is smaller than the TCNTB4 value.
	TCCLRB	Functions as the TCNTB5 upper limit. TCNTB5 is cleared to “1” when TCNTB3=0 and TCNTB5 matches this register when an external event is input.
	TCNTB6	Counts-up by AGCK1.
	OCRB6	Sets the compare match value corresponding to TCNTB6.
	OCRB10	The compare match value regarding to TCNTB1. Clear TCNTB1 and TCNTB3 when the compare match is generated by the TCRB setting value.
	OCRB11	The compare match value regarding to TCNTB1. Selects PIMR2 instead of PIMR1 during the compare match by the TCRB setting value.
	TSRB	The compare match flag of Timer B is stored.
	TSCRB	The compare match flag of Timer B is cleared.
Timer D register	TCRD0	Sets the operation clock bus of the each counter of Timer D.
	TIOR1D0	Set wether or not each compare match generates and the operation when it generates.
	DCRD0	Set the operation start and stop condtion of the down-count.
	OCR1D00～03	Sets the conditon value OCR1D00 to OCR1D03 of the compare match A corresponding to TCNT1D0.
	DCNTD00～03	The counter register of the down-counter.
	TSTRD	Starts the Timer D count.

Related register		Function
PORT register	PCR23_0	Sets P23_1 to TIA00.
	PCR22_7	Sets P22_7 to TOD00B.
	PCR22_6	Sets P22_6 to TOD01B.
	PCR22_9	Sets P22_9 to TOD02B.
	PCR22_8	Sets P22_8 to TOD03B.
INTC register	EIBD97	Specifies the bind destination of the compare match interrupt between TCNTB6 and OCRB6 of Timer B.
	EIC97	Set the interrupt vector method and the interrupt priority.

2.29.3 Operation Explanation

（1）Operating Principle of One-shot Pulse Output at Fixed Position Based on Missing Tooth

As shown in Figure 2.55, TCNTB1 performs the count-up by the inputting of the external event. While this TCNTB1 matches OCRB11, PIMR2 will be applied instead of PIMR1 for the multiplication ration setting. By setting PIMR2 to the value of PIMR1 × (number of missing teeth + 1), it is possible to generate the multiplied clock based on the input cycle of the missing tooth period.

Operates Timer D by the multiplied correction clock of Timer B, and outputs the four one-shot pulses.

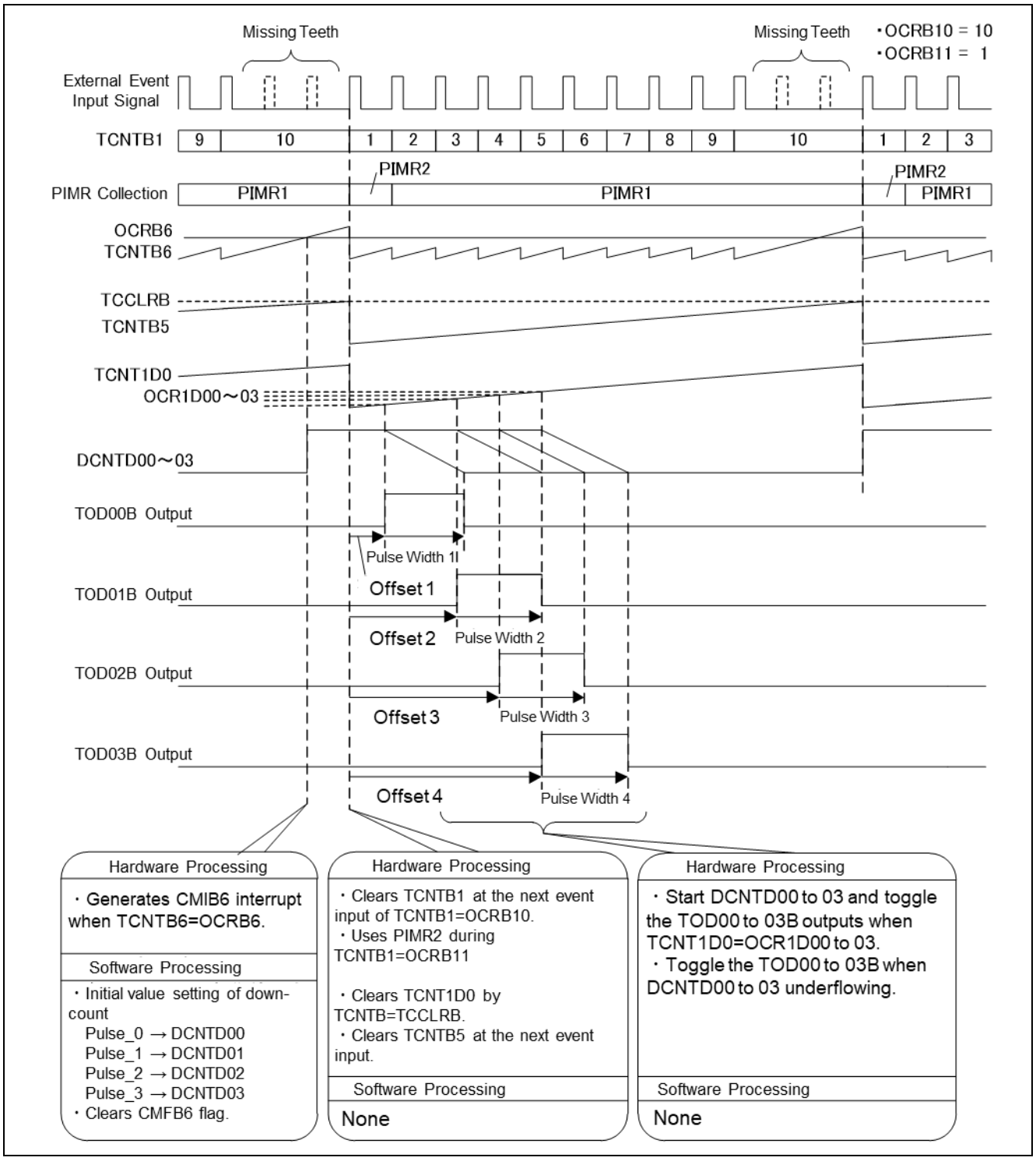


Figure 2.55 One-shot Pulse Output at Fixed Position Based on Missing Tooth

（2） Operation of One-shot Pulse Output by Multiplied Correction Clock during Acceleration/Deceleration

Figure 2.56 shows the principle of correction clock generation during deceleration and Figure 2.57 shows the principle of correction clock generation during acceleration. By using the automatic multiplication ration switching function, it is possible to output the clock to timer D based on the cycle (T2) at the time of missing tooth during the period of T3 in the figure.

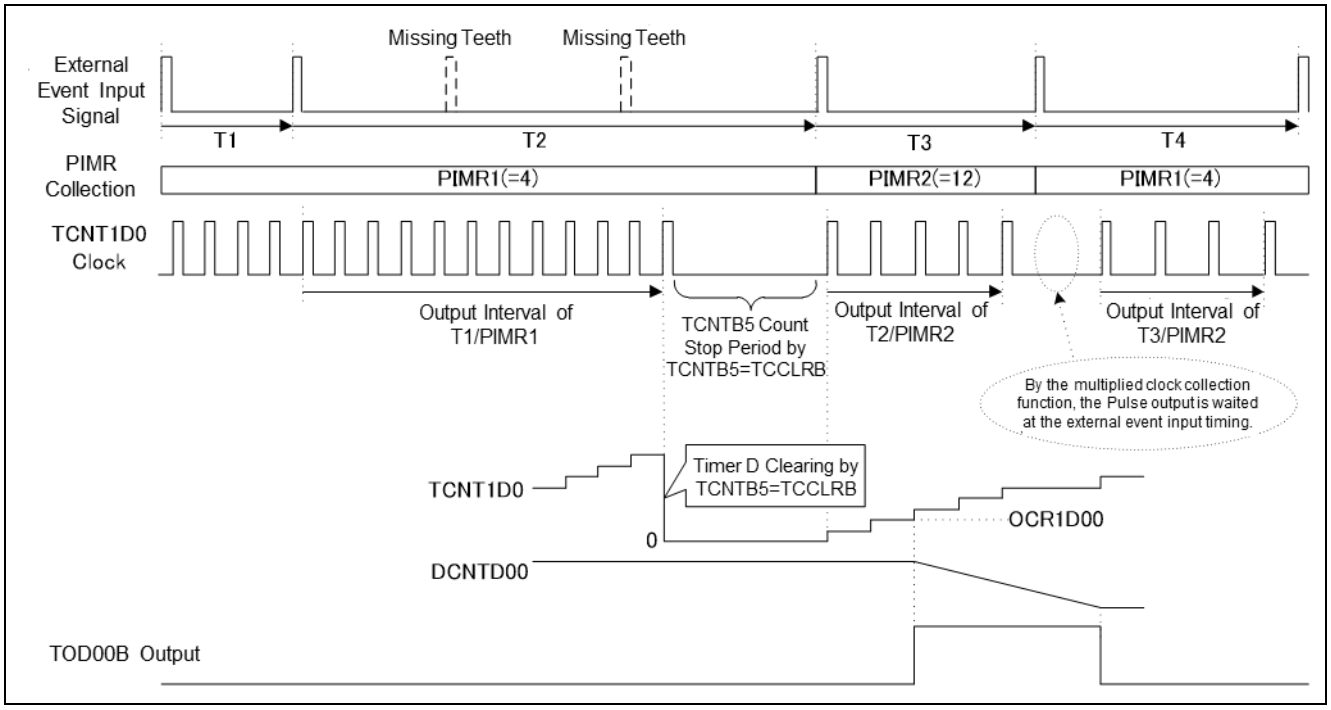


Figure 2.56 One-shot Pulse Output Based on Missing Teeth (Deceleration)

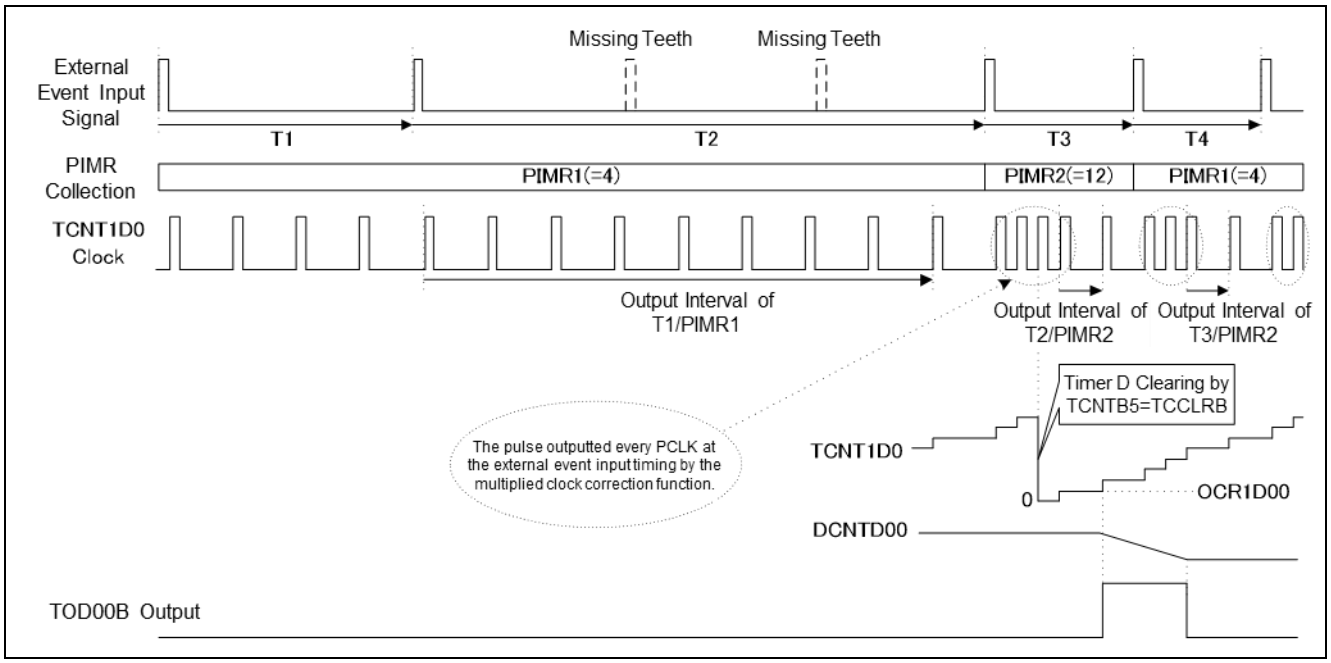


Figure 2.57 One-shot Pulse Output Based on Missing Teeth (Acceleration)

2.29.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the setting of the port (P23_0 and P22_7 to 7).
ATU setting	atu_init	Performs the initial setting of Timer A, B and D.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Missing teeth detection routine	eiint97	This interrupt is performed when the compare match between TCNTB6 and OCRB6 is generated. Sets the down-counter value of Timer D.

Explanation of Use Variable

Label Name	Function	Setting Value	Use Module Name
offset_0	Sets the offset time of the TOD00B output pulse.	0x00000002	Missing teeth detection routine
offset_1	Sets the offset time of the TOD01B output pulse.	0x00000004	Missing teeth detection routine
offset_2	Sets the offset time of the TOD02B output pulse.	0x00000008	Missing teeth detection routine
offset_3	Sets the offset time of the TOD03B output pulse.	0x00000010	Missing teeth detection routine
pulse_0	Sets the offset pulse width of TOD00B.	0x00000003	Missing teeth detection routine
pulse_1	Sets the offset pulse width of TOD01B.	0x00000003	Missing teeth detection routine
pulse_2	Sets the offset pulse width of TOD02B.	0x00000003	Missing teeth detection routine
pulse_3	Sets the offset pulse width of TOD03B.	0x00000003	Missing teeth detection routine

Explanation of Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A, B, and D and presaler.	0x17	
PCR23_0	Sets P0_8 port to the input port TIA00.	0x00000058	Port setting
PCR22_7 PCR22_6 PCR22_9 PCR22_8	Set the ports P22_7, P22_6, P07_2, and P22_8 to TOD00B,01B,02B, and 03B.	0x0000004B	
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
CBCNT	Sets the clock source of the clock bus 5 to the multiplied correction clock of Timer B.	0x04	
TCR1A	Outputs the input signal for TIA0 to Timer B as the event.	0x08	
TIOR1A	Detects the rising edge of the input signal for TIA0.	0x0001	

Register Name	Function	Setting Value	Use Module Name
TCRB	Enable the automatic switching function of PIMR and the hardware clearing function of TCNTB1 and TCNTB3. Sets the clock bus 0 to the Timer B clock.	0xE0	ATU setting
TIORB	Enables the input of the external event. Not stop the TCNTB4 count when TCNTB3=TCNTB4. Sets the compare match enable between TCNTB6 and OCRB8.	0x21	
PIMR1	Sets “4” to the multiplication ration of the multiplied clock regarding to the external input cycle.	0x0004	
PIMR2	Sets “12” to the multiplication ration during compare matching between TCNTB1 and OCRB11.	0x000C	
TICRB	Outputs the interrupt request when CMFB6 is enabled.	0x00	
TIERB	Sets the compare match interrupt enable.	0x0008	
OCRB6	Sets “6” to the compare match value regarding to TCNTB6.	0x00006000	
OCRB10	Sets “10” to the compare match value regarding to TCNTB1.	0x0A	
OCRB11	Sets “1” to the compare match value regarding to TCNTB1.	0x01	
TCCLRB	Sets the TCNTB5 upper limit to 0x30(= PIMR1 × Number of external inputs to set).	0x00030000	
TCNTB5	Set the initial value of the multiplied correction clock generation counter B5 to the same value as TCCLRB.	0x00030000	
TCRD0	Enables the clearing request of TCNT1Dx from Timer B. Set each counter to perform the up/down-count on the clock bus 5.	0x1055	
TIOR1D0	Enables the compare match of OCR1D00 to 03.	0x00FF	
DCRD0	Starts the down-count when the compare match A is generated.	0x2222	
OCR1D00～03	Sets the offset value of the one-shot pulse.	offset_0～3	
TSTRD	Starts the count of the sub block 0 of Timer D.	0x0001	
EIBD97	Binds the Timer B compare match interrupt between TCNTB6 and OCRB6 to PE0 (CPU0).	0x00000000	Interrupt setting
EIC97	Set the table reference method and interrupt priority 0.	0x0040	
TSCRB	Clears CMFB6 of Timer B.	0x0008	Missing teeth detection routine
DCNTD00～03	Sets the initial value of the down-counter.	pulse_0~3	

2.30 Operation Ex. 29 External Event Count Operation by Sequencer [Timer B]

2.30.1 Overview

For an external input signal containing a missing tooth, the counter and the compare operation of the compare register that counts-up every signal inputting based on the missing teeth are executed. The sequencer status is reflected by the compare match. The 3 compare registers are used, and the sequencer shows the 3 types of status by the inputted external signal.

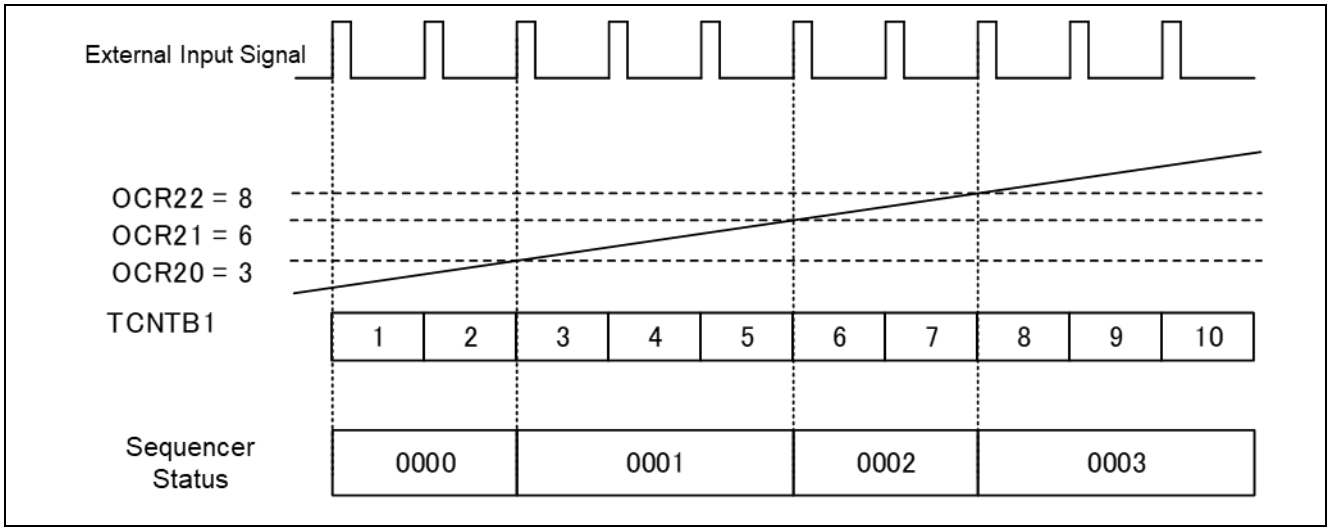


Figure 2.58 Sequencer Operation by External Input Signal

2.30.2 Explanation for Use Function

Table 2.31 shows the functions allocations of the ports used and related registers.

Table 2.30 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIA00	Input the external input signal using the multiplied clock generation to this port.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
	CBCNT	Sets the clock source of the clock bus 5.
Timer A register	TCR1A	Set the operation clock of Timer A and the event output of the external input edge.
	TIOR1A	Sets the detection dege of TIA00.
Timer B register	TCRB	Set the counter sources of TCNTB0 and TCNTB2.
	TIORB	Performs the setting related to the multiplied clock generation such as permission of count operation.
	PIMR1	Sets the multiplication ration of the generating multiplied clock.
	PIMR2	Sets the multiplication ration of the multiplied clock imediatery after the missing teeth inputing.
	TICRB	Enables the interrupt.
	TIERB	Performs the setting of the compare match interrupt.
	TSEQCRB	Enables the sequencer operation.
	TSEQENB0	Enables the compare match of the sequencer.
	OCRB20	The compare match value regarding to TCNTB1. The status of the sequencer is updated when the compare match is genrated.
	OCRB21	The compare match value regarding to TCNTB1. The status of the sequencer is updated when the compare match is genrated.
	OCRB22	The compare match value regarding to TCNTB1. The status of the sequencer is updated when the compare match is genrated.
	TCNTB1	Counts the input edge of the external input signal.
	TCNTB6	Counts-up by AGCK1.
	OCRB6	Sets the compare match value corrsponding to TCNTB6.
	OCRB10	The compare match value regarding to TCNTB1. The compare match value regarding to TCNTB1. Clears TCNTB1 by TCRB setting value when the compare match is generated.
	OCRB11	The compare match value regarding to TCNTB1. Selects PIMR2 instead of PIMR1 during the compare match by the TCRB setting value.
	TSRB	The compare match flag of Timer B is stored.
	TSCRB	The compare match flag of Timer B is cleared.

Related Register		Function
PORT register	PCR23_0	Sets P23_1 to TIA00.
INTC register	EIBD97	Specifies the bind destination of the compare match interrupt between TCNTB6 and OCRB6 of Timer B.
	EIC97	Set the interrupt vector method and the interrupt priority.

2.30.3 Operation Explanation

As shown in Figure 2.59, TCNTB1 performs the count-up by the inputting of the external even, and it is cleared when the missing teeth is detected. The status of the sequencer is changed from 0000 to 0003 every compare matching between TCNTB1 and OCR20 to OCR22.

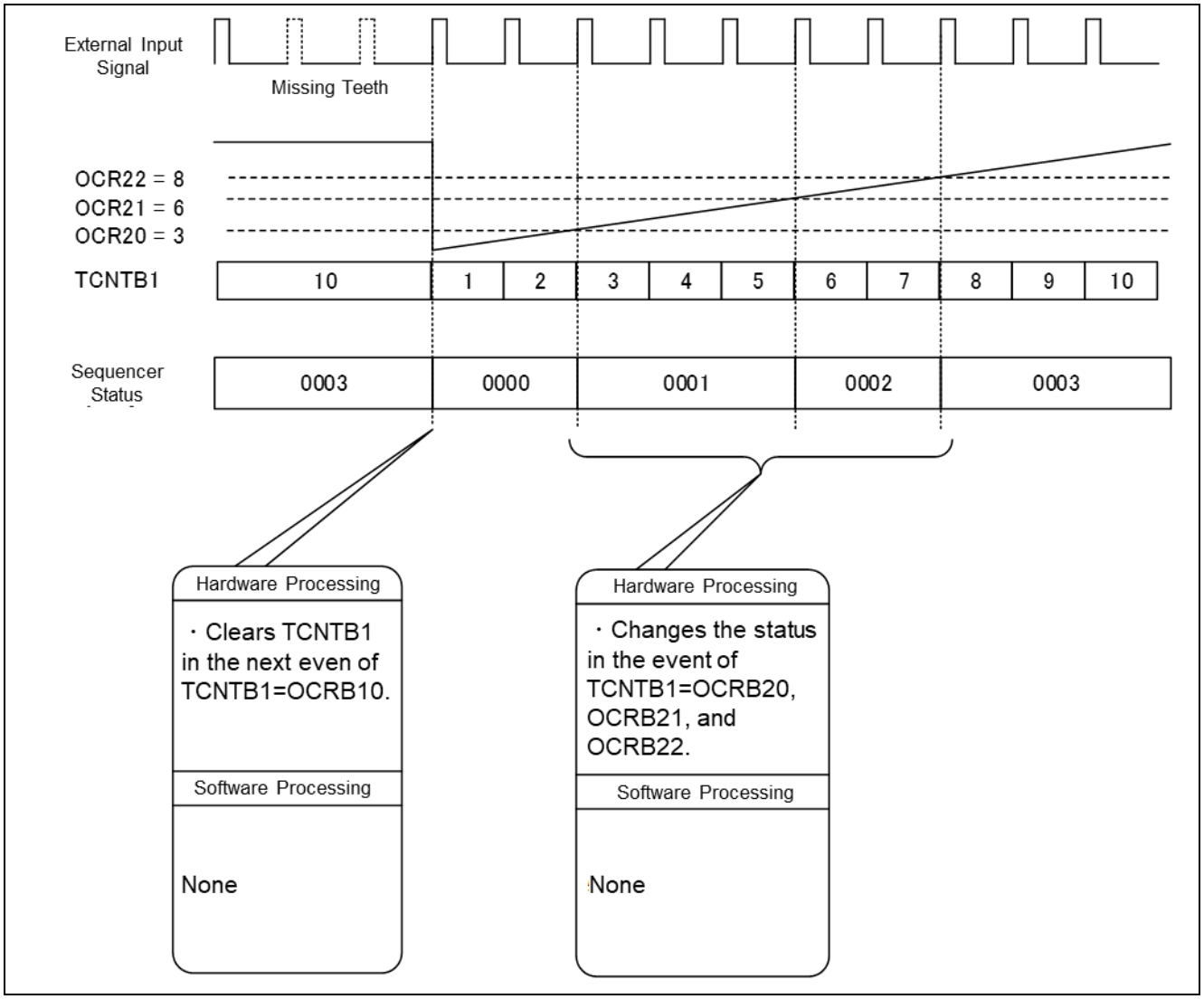


Figure 2.59 Sequencer Status Output based on Missing Teeth

2.30.4 Software Explanation

Module Explanation

Module Name	Port	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Performs the setting of the port (P23_0).
ATU setting	atu_init	Performs the initial setting of Timer A and B.
Interrupt setting	intc_init	Performs the initial setting of interrupt function.
Missing teeth detection routine	eiint97	This interrupt is performed when the compare match between TCNTB6 and OCRB6 is generated.

Explanation for Use Constant

Not use the constant in this task.

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer A, and B and presaler.	0x07	
PCR23_0	Sets P0_8 port to the input port TIA00.	0x00000058	Port setting
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
CBCNT	Sets the clock source of the clock bus 5 to the multiplied correction clock of Timer B.	0x04	
TCR1A	Outputs the input signal for TIA0 to Timer B as the event.	0x08	
TIOR1A	Detects the rising edge of the input signal for TIA0.	0x0001	

Register Name	Function	Setting Value	Use Module Name
TCRB	Enable the automatic switching function of PIMR and the hardware clearing function of TCNTB1 and TCNTB3. Sets the clock bus 0 to the Timer B clock.	0xA0	ATU setting
TIORB	Enables the input of the external event. Not stop the TCNTB4 count when TCNTB3=TCNTB4. Sets the compare match enable between TCNTB6 and OCRB8.	0x21	
TSEQCRB	Enables the sequencer operation.	0x01	
TSEQENB0	Enables the compare match 2-0 of the sequencer.	0x07	
OCRB20	Sets “3” to the compare match value regarding to TCNTB1.	0x03	
OCRB21	Sets “6” to the compare match value regarding to TCNTB1.	0x06	
OCRB22	Sets “8” to the compare match value regarding to TCNTB1.	0x08	
PIMR1	Sets “4” to the multiplication ration of the multiplied clock regarding to the external input cycle.	0x0004	
PIMR2	Sets “12” to the multiplication ration during compare matching between TCNTB1 and OCRB11.	0x000C	
TICRB	Outputs the interrupt request when CMFB6 is enabled.	0x00	
TIERB	Sets the compare match interrupt enable.	0x0008	
OCRB6	Sets “6” to the compare match value regarding to TCNTB6.	0x00006000	
OCRB10	Sets “10” to the compare match value regarding to TCNTB1.	0x0A	
OCRB11	Sets “1” to the compare match value regarding to TCNTB1.	0x01	
EIBD97	Binds the Timer B compare match interrupt between TCNTB6 and OCRB6 to PE0 (CPU0).	0x00000000	Interrupt setting
EIC97	Set the table reference method and interrupt priority 0.	0x0040	
TSCRB	Clears CMFB6 of Timer B.	0x0008	Missing teeth detection routine

2.31 Operation Ex. 30 Ranged Compare Match [Timer C]

2.31.1 Overview

Figure 2.60 shows the operation example of the ranged compare match.

When range compare is disabled, if the counter value (TCNTCx) of timer C exceeds the set value while the compare match output register (OCRCxy) is being set, a compare match will occur in the next timer C count cycle (Refer to Fig. 2.60 (2)).

When the range compare match is enabled, if the counter value (TCNTCx) of Timer C is within the range set when the compare match output register (OCRCxy) is set, the compare match is established, and the compare match interrupt can be generated. (Refer to Figure 2.60 (1)) According to this, the compare match interrupt is generated without waiting for the next timer C count cycle.

For operation check, port P11_0 is inverted-outputted in reverse when the compare match interrupt is generated, and port P11_1 is inverted-outputted when OCRC00 is reset.

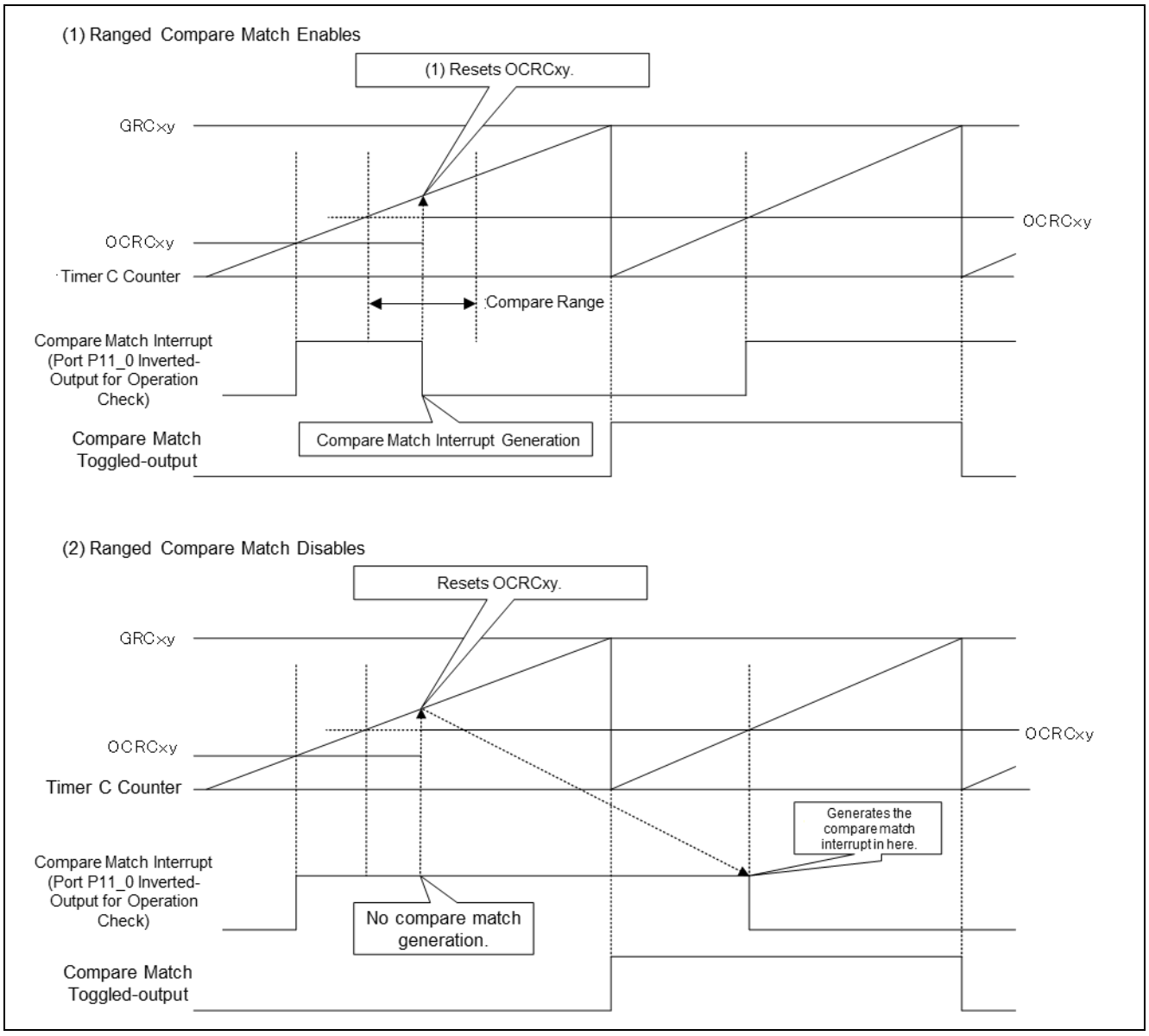


Figure 2.60 Overview of Range Compare Match Interrupt

2.31.2 Explanation of Use Function

Table 2.32 shows the functions allocations of the ports used and related registers.

Table 2.31 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIOC00	Toggled-outputs the compare match.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer A register	TCNTA	Sets the up-count value of Timer A.
	TSCRA	Clears the status of Timer A.
Timer C register	TIORC0	Sets the function of Timer C.
	TCRC0	Set the operation and the clock bus of Timer C.
	TIERC0	Enables/Disables the Timer C interrupt.
	GRC00	Sets the toggled output cycle.
	CUCRC0	Sets the upper limit to clear the counter (TCNTCx) of each subblock of Timer C.
	OCRC00	Sets the output value of the compare macth.
	RCR1C0	Sets the range of the ranged compare macth.
	TSTRC	Sets the operation clock bus of the each counter of Timer C.
PORT register	PCR00_4	Sets the port function.
	PCR11_0	Sets the port function. (for operation check)
	PCR11_1	Sets the port function. (for operation check)
INTC register	EIBD104	Specifies the bind destination of the compare match interrupt between TCNTC0 and OCRC00 of Timer C.
	EIC104	Set the interrupt vector method and the interrupt priority.

2.31.3 Operation Explanation

Figure 2.61 shows the operation principle. According to this, perform the compare match toggled output and the compare match interrupt by the hardware and software processing of RH850/U2Bx.

If the value is set in the compare match output register (OCRCxy) when the counter value (TCNTCx) of timer C is in the following range, the range compare match is established and the compare match interrupt is generated.

Range : OCRCxy ≦ TCNTCx ≦ OCRCxy + RCR1Cx

TIOC00 port performs the toggled output by the compare match of Timer C between the counter value (TCNTCx) and the GRC register.

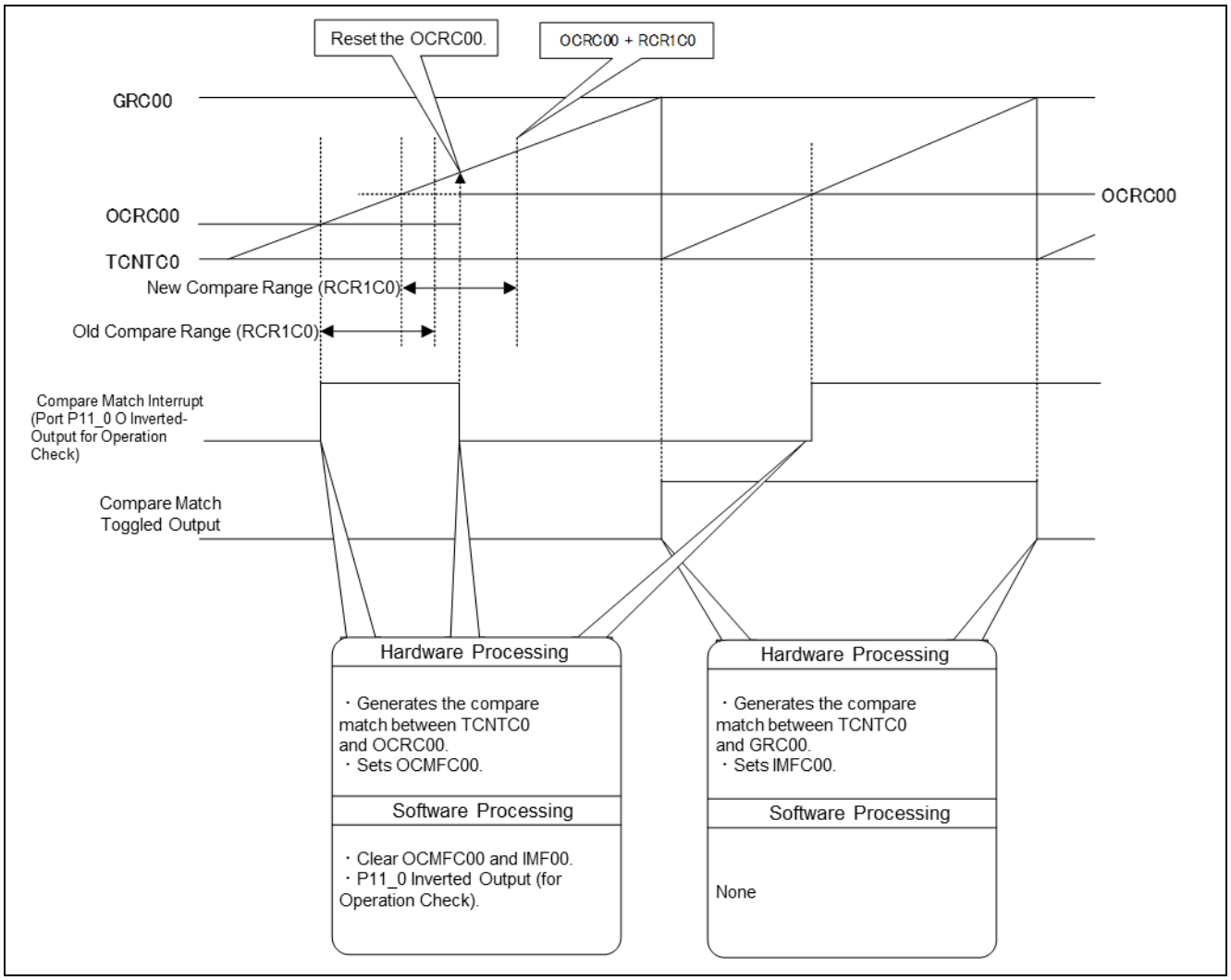


Figure 2.61 Operation Principle of Range Compare Match

2.31.4 Software Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Sets TIOC00 output to the port (P00_4) and the output port (for operation check) to the port (P00_4).
ATU setting	atu_init	Performs the initial setting of Timer C.
Interrupt setting	intc_init	Performs the compare match interrupt of Timer C.
Compare match output register setting routine	TimerA_ Counter	Checks the Timer C counter value at regular intervals (using Timer A), and sets the value of the compare match output setting when it is detected in the range compare. Inverted-outputs the port P11_1 when setting the OCRC00 register (for operation check).
Compare match interrupt routine	eiint104	Clear the interrupt and the compare match flag when compare matching between TCNT00 and OCRC00. Inverted-outputs the port P11_0 (for operation check).

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer C presaler.	0x09	
PCR00_4	Sets P0_4 port to the input port TIOC00.	0x00000049	Port setting
PCR11_0	Sets P11_0 to output port (for operation check: Inverted-output when the compare match is generated).	0x00000000	
PCR11_1	Sets P11_1 to output port (for operation check: Inverted-output when resetting the OCRC00 register).	0x00000000	
PSCR0	Set the “10” to the division ration of the prescaler 0.	0x0009	ATU setting
TCRC0	Perform the clock selection of the Timer C sub block and the operation mode setting, and the forced compare match setting.	0x0100	
TIORC0	Sets to toggled output to TIOC00 by the compare match of GRC00 register.	0x0003	
GRC00	Sets the compare match value with TCNTC0.	0x00000500	
TIERC0	Sets the OCRC00 compare match enable of Timer C.	0x0100	
CUCRC0	Sets the upper limit that clears the counter (TCNTC0) of each block of Timer C.	0x00000500	
RCR1C0	Sets the range of the range compare macth. OCRC00≦ Range ≦(OCRC00+31 counter)	0x05	
TSTRC	Enables the counting operation of the sub block 0.	0x0001	
EIBD104	Binds the OCRC00 compare match interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC104	Set the table reference method and interrupt priority 0.	0x0040	
TSCRC0L	Clears the compare match flag of Timer C.	0x11	Compare match interrupt routine
TSCRC0H	Clears the compare match flag of Timer C.	0x01	
OCRC00	Reset OCRC00 when the counter value of TCNTC0 is in the compare range.	0x00000200	Compare match output register setting routine
TCNTA	Sets 4us to the cycle of Timer A.	0xFFFFFFE0	
ATUENR	Enables the count operation of Timer A.	Bit1=1	
TSCRA	Clears the status of Timer A.	Bit15=1	

2.32 Operation Ex.31 Mirroring［Timer C］

2.32.1 Overview

As shown in Figure 2.62, inputs the signal from the external to the TIOC port. Captures the counter value (TCNTC0) of Timer C to the input capture register (OCRC00 register and GRC00 register) by both edges of the external input signal.

At this time, the captured data is loaded to the mirror register (OCMRC00 register and GMRC00 register). The mirror register uses the captured data to perform the DMA transfer. Then, Using the input capture as the hardware trigger, starts the DMA transfer for the data of the mirror register and saves the transferred data to RAM.

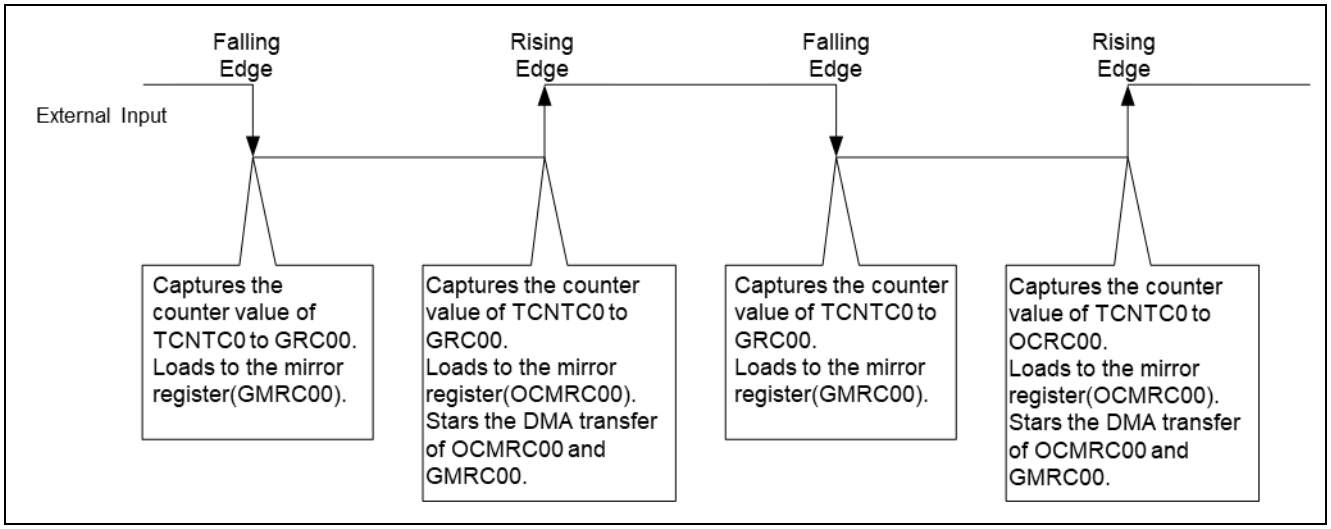


Figure 2.62 Overview of Mirroring

2.32.2 Explanation of Use Function

Table 2.33 shows the functions allocations of the ports used and related registers.

Table 2.32 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TIOC00	Detects the input signal from the external.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer E register	TCRC0	Sets the conter opeartion of each Timer C sub block.
	TIORC0	Sets the input level of OCRC0 and GRC0.
	TIERC0	Sets the input capture interrupt enable/disable.
	TSCRC0L	Clears the interrupt factor.
	TSCRC0H	Clears the interrupt factor.
	TSTRC	Enables the conter opeartion of each Timer C sub block.
INTC register	EIBD70	Specifies the bind destination of the DMA transfer complete interrupt.
	EIC70	Set the interrupt vector method and the interrupt priority.
	EIBD104	Specifies the bind destination of the input capture interrupt of OCRC00.
	EIC104	Set the interrupt vector method and the interrupt priority.
PORT register	PCR22_7	Sets the port function.
	PCR11_0	Sets the port function. (for operation check)
	PCR11_1	Sets the port function. (for operation check)
ATU-Ⅵ common register	DMACSEL0_3	Sets the DMA transfer request group.
	DMA0CM_0	Sets the master mode of DMA channel.
	DMA0SAR_0	Sets the transfer source address of the DMA transfer.
	DMA0DAR_0	Sets the transfer destination address of the DMA transfer.
	DMA0TSR_0	Set the number of the transfer bite of the DMA transfer.
	DMA0TMR_0	Set the DMA start request, transfer source, addrss mode of tramsfer destination, and transfer size.
	DMA0RS_0	Set the number of hardware request and the start trigger number.
	DMA0CHFCR_0	Clears the DAM status.
	DMA0OR	Sets the DMA trasfer enable/diable.
	DMA0CHCR_0	Sets the complete interrupt/transfer enable/diable of DMA trasfer.

2.32.3 Operation Explanation

Figure 2.63 shows the operation principle. According to this, the DMA transfer of the mirror register of the input captured counter value is performed by the hardware and the software processing of RH850/U2Bx.

The counter value (TCNTC0) of Timer C is captured to the OCRO00 register and GRC00 register by both of the edge of the external input. At this time, the value of the OCRC register and GRC00 register are loaded to the mirror register (OCMRC00 register and GMRC00 register) of OCRC00 register and GRC register.

Then, the captured value becomes as the hardware trigger and the DMA transfer starts. The DMA transfer complete interrupt is generated when the DMA transfer is completed.

In addition, inverted-outputs the port P11_0 when the DMA transfer complete interrupt is generated and the port P11_1 when the input capture interrupt is generated for the operation check.

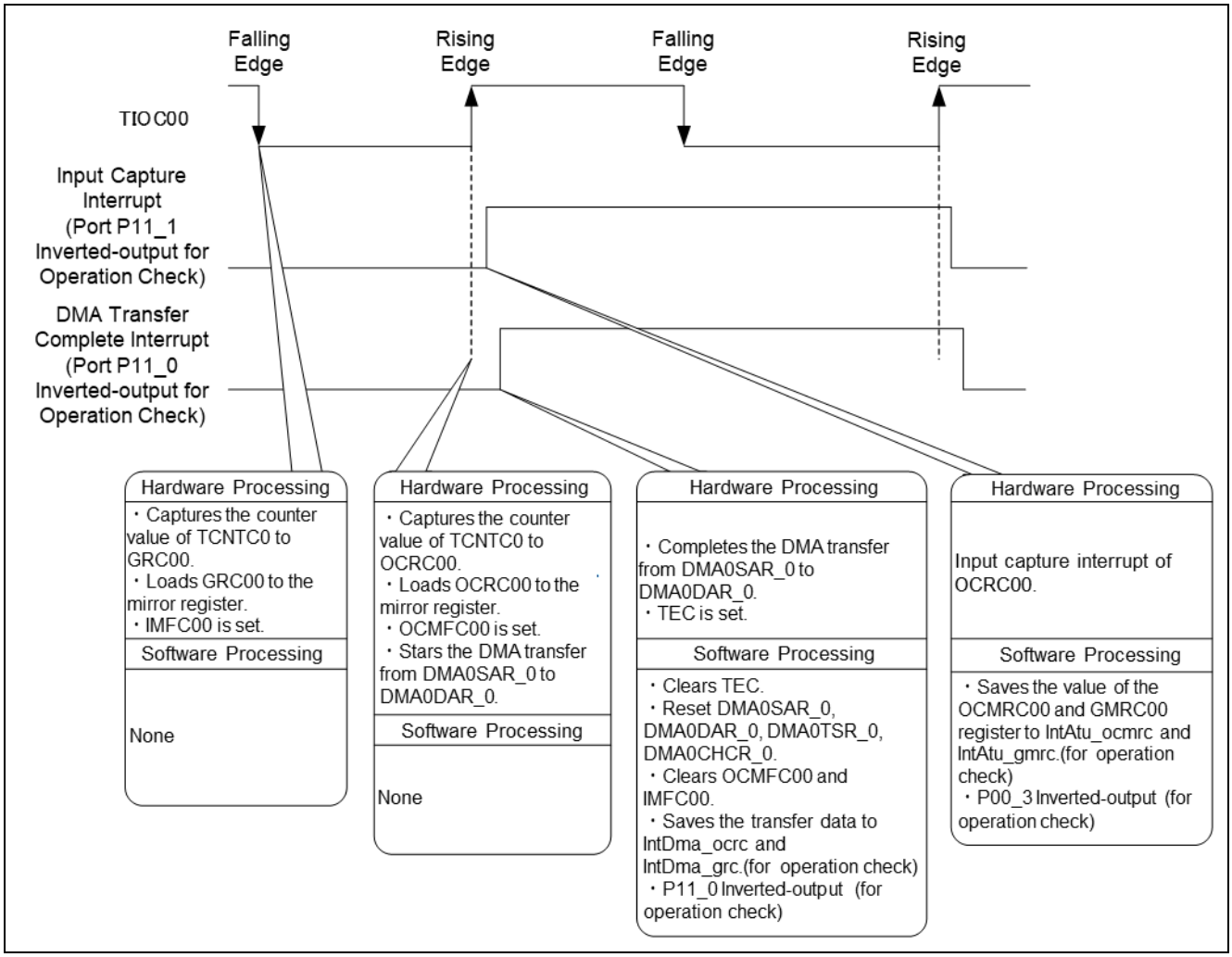


Figure 2.63 Operation Principle of Mirroring

2.32.4 Software Explanation

Module Explanation

Module Name	Lebel Name	Function
Main routine	main_pe0	Perform the various settings and the application start.
Port setting	port_init	Sets TIOC00 input to the port (P00_4) and the output port (for operation check) to the port (P11_0 and P11_1).
ATU setting	atu_init	Performs the initial setting of Timer C.
Interrupt setting	intc_init	Performs the compare match interrupt of Timer C.
DMA setting	sdmac_init	Performs the DMA initial setting.
DMA transfer complete interrupt routine	eiint70	Interrupted when the DMA transfer of the mirror register is completed, saves the transfer data to the IntDma_ocrc and IntDma_grc areas, and resets the transfer source register required to DMA transfer. Inverted-outputs P11_0 (for operation check).
Input capture interrupt routine	eiint104	Interrupted when the input capture is detected, and saves the value of the mirror register to IntAtu_ocmrc and IntAtu_gmrc. Inverted-outputs P11_1 (for operation check).

Explanation for Use Variable

Label Name	Function	Data Length	Use Module Name
IntAtu_ocmrc[5]	Saves the value of the OCMRC00 register when the input capture interrupt is generated.	unsigned long	Input capture interrupt routine
IntAtu_gmrc[5]	Saves the value of the GMRC00 register when the input capture interrupt is generated.	unsigned long	Input capture interrupt routine
Trans_Data[2]	The transfer source area of DMA transfer.	unsigned long	DMA transfer complete interrupt routine
IntDma_ocrc[5]	Saves the transferred data by DMA：Trans_Data[0] (OCMRC00) (for value check with IntAtu_ocmrc).	unsigned long	DMA transfer complete interrupt routine
IntDma_grc[5]	Saves the transferred data by DMA：Trans_Data[1] (GMRC00) (for value check with IntAtu_gmrc).	unsigned long	DMA transfer complete interrupt routine

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer C presaler.	0x09	
PCR22_7	Sets 22_7 port to the input port TIOC00.	0x00000059	Port setting
PCR11_0	Sets 11_0 port to the output port (for operation check: Inverted-outputs when DMA transfer complete interrupt is generated.)	0x00000000	
PCR11_1	Sets 11_1 port to the output port (for operation check: Inverted-outputs when DMA transfer complete interrupt is generated.)	0x00000000	
PSCR0	Set the “0” to the division ration of the prescaler 0.	0x0000	ATU setting
TCRC0	Sets to use the clock bus 0 of the sub block 0.	0x0000	
TIORC0	Set the capture by OCRC0=TIOC00 rising edge and GRC0=TIOC0 falling edge.	0x0006	
TIERC0	Set the OCRC00 input capture interrupt enable.	0x0101	
TSCRC0L	Clears the input capture interrupt status.	0x1F	
TSCRC0H	Clears the input capture interrupt status.	0x0F	

TSTRC	Starts the count of Timer C sub block 0.	0x0001	
EIBD70	Binds the DMA transfer complete interrupt to PE0 (CPU0).	0x00000000	Interrupt setting
EIC70	Set the table reference method and interrupt priority 0.	0x0040	
EIBD104	Binds the OCRC00 input capture interrupt to PE0 (CPU0).	0x00000000	
EIC104	Set the table reference method and interrupt priority 0.	0x0040	
DMACSEL0_3	Sets “1” to the DMA transfer request group.	0x00000030	DMA setting
DMA0CM_0	Set the SPID and supervisor of the DMA channel master.	0x00001C00	
DMA0SAR_0	Sets the OCMRC00 register to the DMA transfer source address.	OCMRC00	
DMA0DAR_0	Sets the variable (Trans_Data) to the DMA transfer source address.	Trans_Data	
DMA0TSR_0	Sets the DMA transfer size.	0x00000008	
DMA0TMR_0	Set the hardware request to the DMA transfer request class and the increment to the transfer source address and transfer destination address.	0x00001522	
DMA0RS_0	Sets the DMA transfer request resource to the OCRC0 input capture.	0x00020032	
DMA0CHFCR_0	Clears the DMA transfer status.	0x0000320F	
DMA0OR	Enable the DMA transfer of all of channels.	0x0001	
DMA0CHCR_0	Enables the DMA transfer complete and DMA interrupt of channel 0.	0x0003	
DMA0CHFCR_0	Clears the DMA transfer source complete flag.	0x00000002	DMA transfer complete interrupt routine
DMA0SAR_0	Sets the OCMRC00 register to DMA transfer source address.	OCMRC00	
DMA0DAR_0	Sets the area (Trans_Data) on RAM to the DMA transfer source address.	Trans_Data	
DMA0TSR_0	Sets the DMA transfer size.	0x00000008	
DMA0OR	Enable the DMA transfer of all of channels.	0x0001	
DMA0CHCR_0	Enables the DMA transfer complete and DMA interrupt of channel 0.	0x0003	
TSCRC0L	Clears the input capture interrupt status.	0x1F	
TSCRC0H	Clears the input capture interrupt status.	0x0F	

2.33 Operation Ex.32 Minimum Guard［Timer D］

2.33.1 Overview

As shown in Figure 2.64, generate the compare match A and B to use the counter TCNT1D0 and TCNT2D0 of Timer D.

The minimum guard delays the output to the output pin (TODxyA).

The minimum guard of ON-OFF period is enabled when the compare match is generated. In this time, the minimum guard correction of the ON-width is performed. (High period of TOD00A is extended.)

The minimum guard of OFF-ON period is enabled when the compare match B is generated. In this time, the minimum guard correction of the OFF-width is performed. (Low period of TOD00A is extended.)

The minimum guard of ON-ON period is enabled when the compare match A is generated. In this time, the minimum guard correction of the OFF-width is performed. (High-Low period of TOD00A is extended.)

In addition, when the compare match interrupt for operation check is generated, the port P11_1 is inverted-outputted when the port P11_0 and TCNT1D0 is reached to the upper-limit of the counter clear.

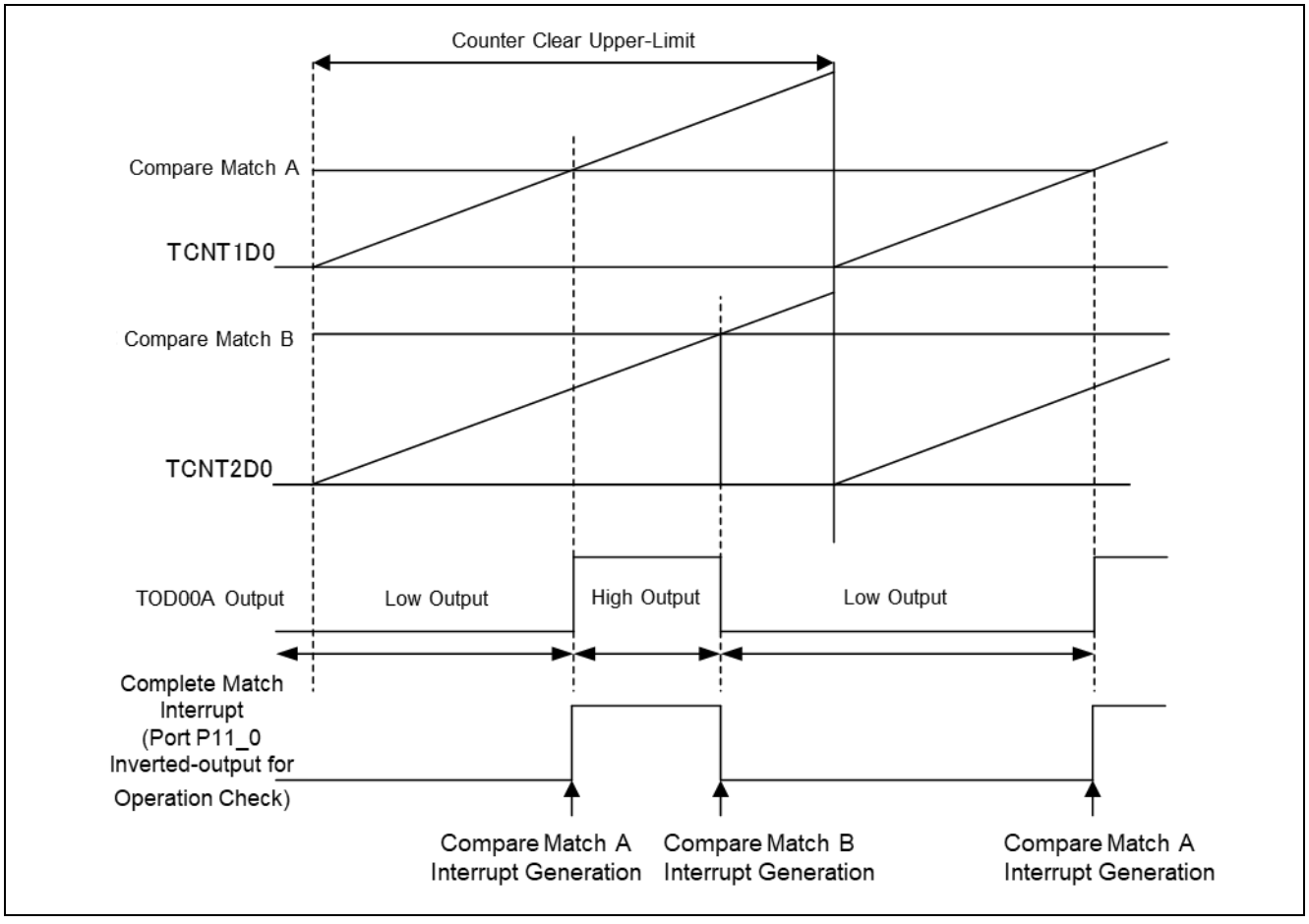


Figure 2.64 Overview of Minimum Guard

2.33.2 Explanation for Use Function

Table 2.34 shows the functions allocations of the ports used and related registers.

Table 2.33 ATU-Ⅵ Function Allocation

Use Port		Function
Port	TOD00A	Toggleed-outputs the compare match.
Related Register		Function
ATU-Ⅵ common register	ATUENR	Sets the operation of each timer and prescaler.
	PSCR0	Sets the division ration of the prescaler 0.
Timer D register	MIGCRD0	Sets the minimun guard enable/disable.
	MIGSELD0	Sets the output destination of the MIN guard (TODxyA and TODxyB).
	TCRD0	Set the clock cellection of TCNT1Dx and TCNT2Dx, and the clearing enable and disable of the counter value, etc.
	TIOR1D0	Sets the TODxyA output by the compare match A of OCRDxy.
	TIOR2D0	Sets the TODxyA output by the compare match B of OCR2Dxy.
	TIORD0	Sets the TODxyA output by the compare match A and B generation of TCNT1Dx.
	TCMPED0	Sets the compare match A and B enable/disable of TCNT1Dx and TCNT2Dx.
	ODRD0	Sets the output from TODxyA of ODRDxy.
	OCR1D00	Sets the compare value of the compare match A.
	OCR2D00	Sets the compare value of the compare match B.
	CUCR1D0	Sets the upper-limit clrearing the counter of the compare match A.
	CUCR2D0	Sets the upper-limit clrearing the counter of the compare match B.
	ONMIND00	Sets the minimum value of the ON period for the minimum guard.
	OFMIND00	Sets the minimum value of the OFF period for the minimum guard.
	OTOMIND00	Sets the minimum value of the ON-ON period for the minimum guard.
	TSCRD0	Clears the status of Timer D.
	TIER2D0	Sets the compare macth A and B eanble/disable.
	TSTRD	Sets the operation of each sub block of Timer D.
INTC register	EIBD164	Specifies the bind destination of the compare match interrupt.
	EIC164	Set the interrupt vector method and the interrupt priority.
PORT register	PCR00_4	Sets the port function.
	PCR11_0	Sets the port function (for operation check).
	PCR11_1	Sets the port function (for operation check).

2.33.3 Operation Explanation

Figure 2.65 shows the operation principle of the minimum guard ON-OFF period. Figure 2.66 shows the operation principle of the minimum guard OFF-ON period. Figure 2.67 shows the operation principle of the minimum guard ON-ON period. According to this, measures the minimum guard by the hardware and software processing of RH850/U2Bx.

(1)Minimum Guard Correction Operation of ON-OFF Width

The setting value of the ONMIND00 register is loaded to the ONMICNTD00 register when the compare match A is generated. Then, the compare match B output is outputted to TOD00A when the ONMINCTD00 register is down-counted and became “0”. By this, the ON width of TOD00A is guarded by ONMICNTD00.

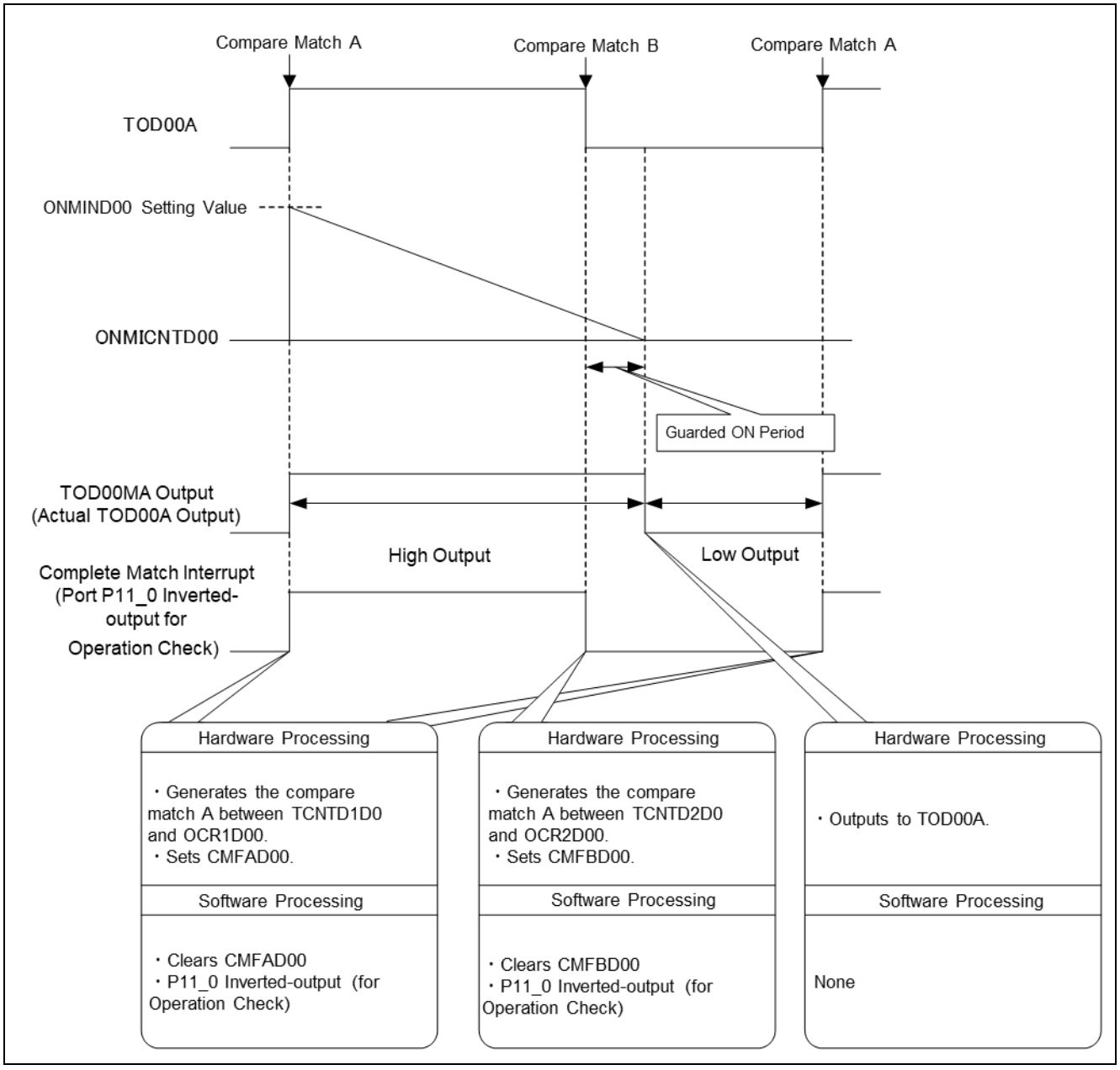


Figure 2.65 Operation Principle of Minimum Guard ON-OFF

(2)Minimum Guard Correction Operation of OFF-ON Width

The setting value of the OFMIND00 register is loaded to the OFMICNTD00 register when the compare match B is generated. Then, the compare match A output is outputted to TOD00A when the OFMINCTD00 register is down-counted and became “0”. By this, the OFF width of TOD00A is guarded by OFMICNTD00.

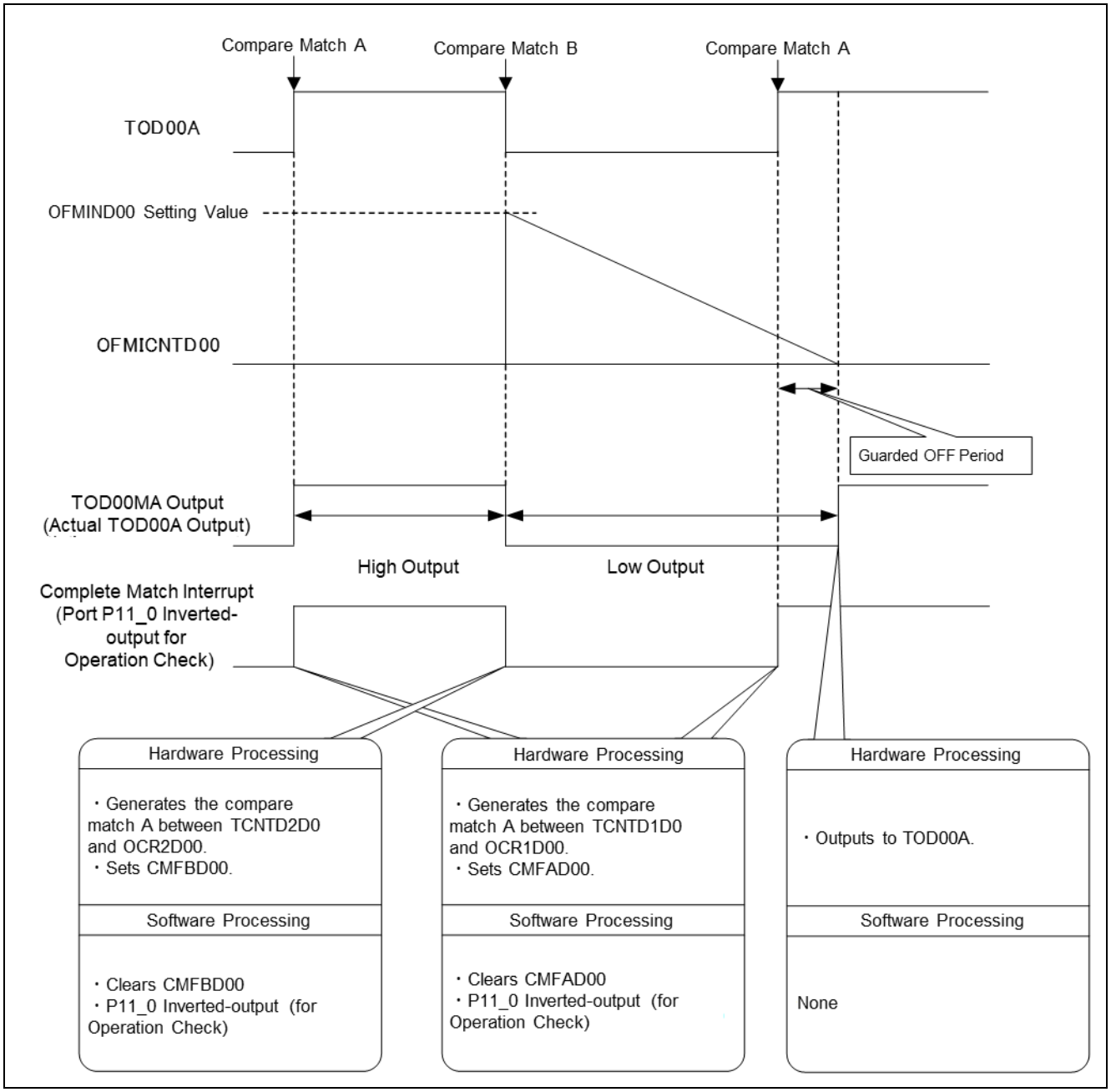


Figure 2.66 Operation Principle of Minimum Guard OFF-ON

(3)Minimum Guard Correction Operation of ON-ON Width

The setting value of the OTOMIND00 register is loaded to the OTOMICNTD00 register when the compare match A is generated. Then, the compare match A output is outputted to TOD00A when the OTOMICNTD00 register is down-counted and became “0”. By this, the ON-ON width of TOD00A is guarded by OTOMICNTD00.

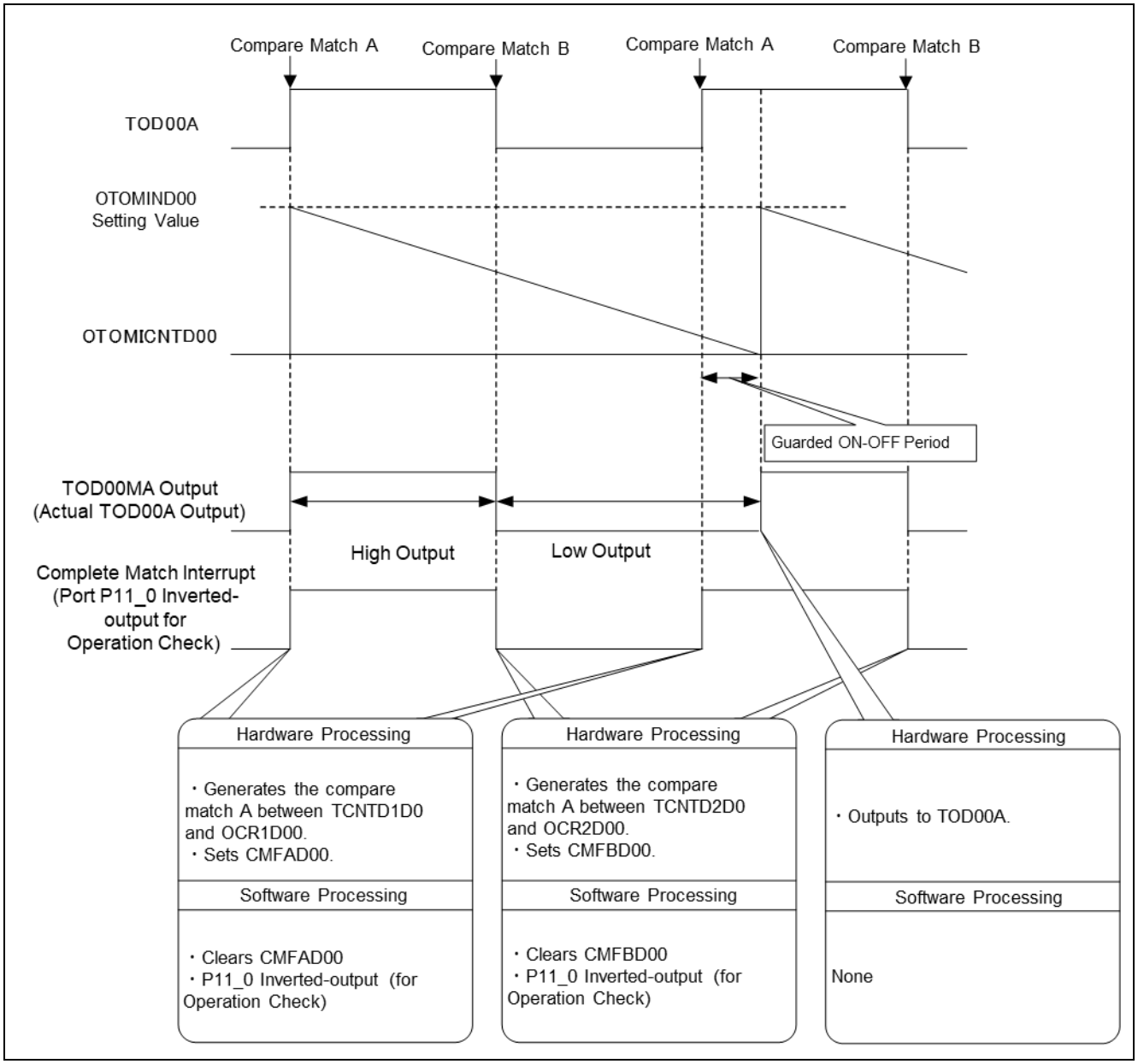


Figure 2.67 Operation Principle of Minimum Guard ON-ON

2.33.4 Soft Explanation

Module Explanation

Module Name	Label Name	Function
Maine routine	main_pe0	Perform the various settings and the application start. Inverted-outputs the port P11_1 when TCNT1D0 is reached to the counter clear upper-limit (for operation check).
Port setting	port_init	Set the port (P00_4) to the TOD00A output and the port (P11_0 and P11_1) to the output port (for operation check).
ATU setting	atu_init	Performs the initial setting of Timer D.
Interrupt setting	intc_init	Performs the initial setting of the interrupt function.
Compare match interrupt routine	eiint164	It is interrupted when the compare match is detected and clears the compare match flag. Inverted-output the port P11_0 (for operation check).

Explanation for Use Variable

Not use the variable in this task.

Explanation for Use Register

Register Name	Function	Setting Value	Use Module Name
MSR_ATU	Releases the ATU module standby.	0x00000000	Maine routine
ATUENR	Enable the count operation of Timer C and presaler.	0x11	
PCR00_4	Sets 00_4 port to the TOD00A output.	0x0000004A	Port setting
PCR11_0	Sets 11_0 port to the output port (for operation check: Inverted-outputs when the compare match interrupt is generated.)	0x00000000	
PCR11_1	Sets 11_1 port to the output port (for operation check: Inverted-outputs when TCNTD1D0 is reached to the counter clear upper-limit).	0x00000000	
PSCR0	Set the “1” to the division ration of the prescaler 0.	0x0000	ATU setting
MIGCRD0	Sets the minimun gard enable.	0x01	
MIGSELD0	The minimun gard sets the addition to TOD00A.	0x00	
TCRD0	Sets the clearing enable of the counter value of TCNTD1D0 and TCNT2D0.	0x0880	
TIOR1D0	Sets TOD00A to the toggled-output by the compare match A of OCR1D00.	0x0303	
TIOR2D0	Sets TOD00A to the toggled-output by the compare match B of OCR2D00.	0x0003	
TIORD0	Sets TOD00A to the toggled-output when the compare match between A and B of TCNT1D0 is generated.	0x0303	
TCMPED0	Sets the enbale of compare match A and B of TCNT1D0 and TCNT2D0.	0x11	
ODRD0	Sets the output destination to TOD00A.	0x01	
OCR1D00	Sets the conpare value of the compare match A.	0x00005000	
OCR2D00	Sets the conpare value of the compare match B.	0x00008000	
CUCR1D0	Sets the upper-limits clears the counter of the compare match A.	0x0000A000	
CUCR2D0	Sets the upper-limits clears the counter of the compare match B.	0x0000A000	
ONMIND00	Sets the minimun value of ON period that performs the minimun gard.	0x00004000	
OFMIND00	Sets the minimun value of OFF period that performs the minimun gard.	0x00008000	

OTOMIND00	Sets the ON-OFF period that performs the minimun gard.	0x0000B000	
TSCRD0	Clears the Timer D status.	0x3FFF	
TIER2D0	Sets the enable/disable of the compar match A and B interrupt.	0x00000101	
TSTRD	Sets the operation of each sub block of Timer D.	0x0001	
EIBD164	Binds the compare match between A and B to PE0 (CPU0).	0x00000000	Interrupt setting
EIC164	Set the table reference method and interrupt priority 0.	0x0040	
TSCRD0	Clears the compare match flag.	0x3011	Compare match interrupt routine

Our Company’s Website and Inquiry

Website

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Inquiry

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Revision History

Rev.	Issue Date	Description	
		Page	Point
1.00	2023.10.5	-	Initial Edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused pins

[Caution] Please dispose of unused pins according to "Handling of unused pins" in the text.

The impedance of the input pins of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

[Caution] The state of the product is undefined when the power is turned on.

When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.

For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.

Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of Access to Reserved Addresses

[Caution] Access to reserved addresses is prohibited.

The address area has a reserved address allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

[Caution] When resetting, release the reset after the clock has stabilized.

When switching the clock during program execution, switch the clock after the switching destination clock is stable.

In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

[Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.

Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

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(Rev.4.0-1 November 2017)

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