

RH850/U2A-EVA Group

Example of capacitor placement

Introduction

This document describes the example of capacitor placement of RH850/U2A-EVA Group in consideration of EMC characteristics. The purpose of this document is to provide examples of PCB board design for reducing EMC noise in ECU. However, the EMC noise value is not necessarily guaranteed.

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Target Device

- RH850/U2A-EVA Group
 - RH850/U2A16
 - RH850/U2A8
 - RH850/U2A6

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1. Decoupling capacitors

1.1 Capacitor placement and number of capacitors

- Please refer Chapter.2 “Example of capacitor placement” and Chapter.3 “PCB layout guidelines -Top layer / Bottom layer-”.
- Capacitors has been kept as close as feasible to the related supply pin.

1.2 Types of capacitors

- 0.1uF, 0.22uF, 10uF or higher*1 ceramic capacitor (Low ESR/ESL is required)
*1: This is expected value. Please follow the Power IC specification.
- 10uF 3-terminal ceramic capacitor (Very low ESR/ESL is required)

1.3 3-terminal capacitor

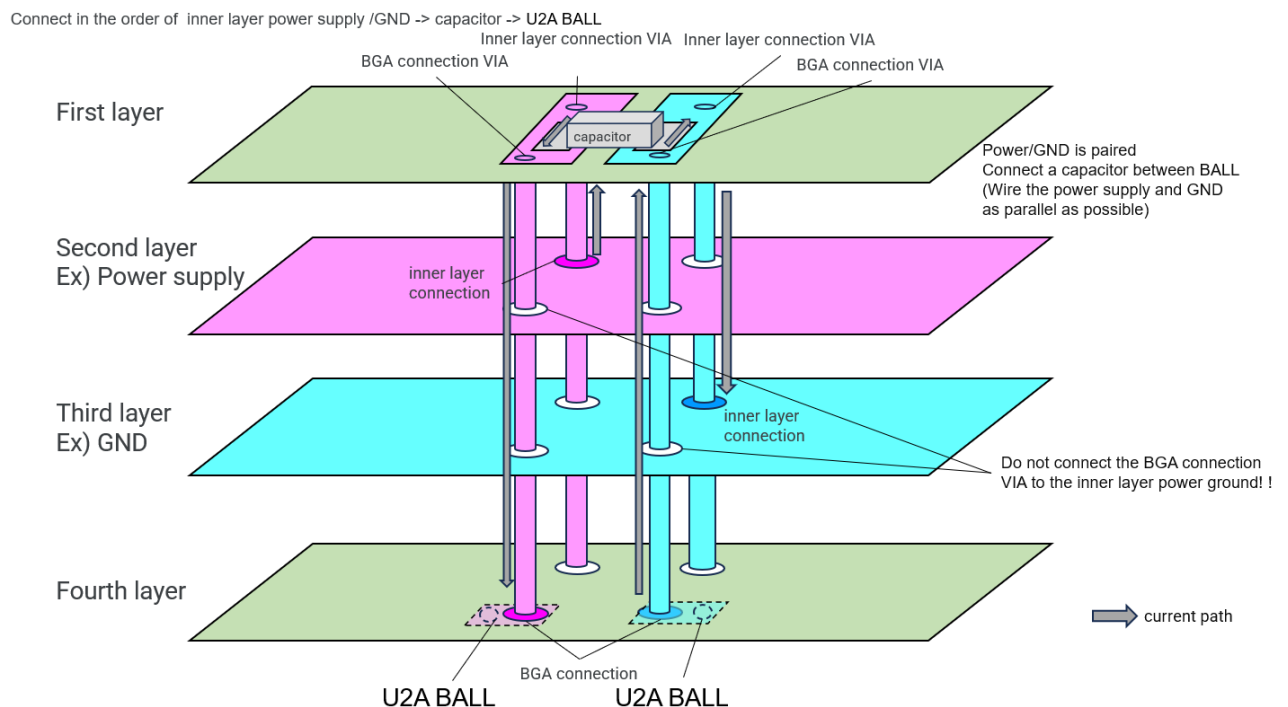
3-terminal capacitor is recommended for reduction of radiation noise.

1.4 How to connect capacitors and power supply/GND

Connections as shown in the diagram below are recommended.

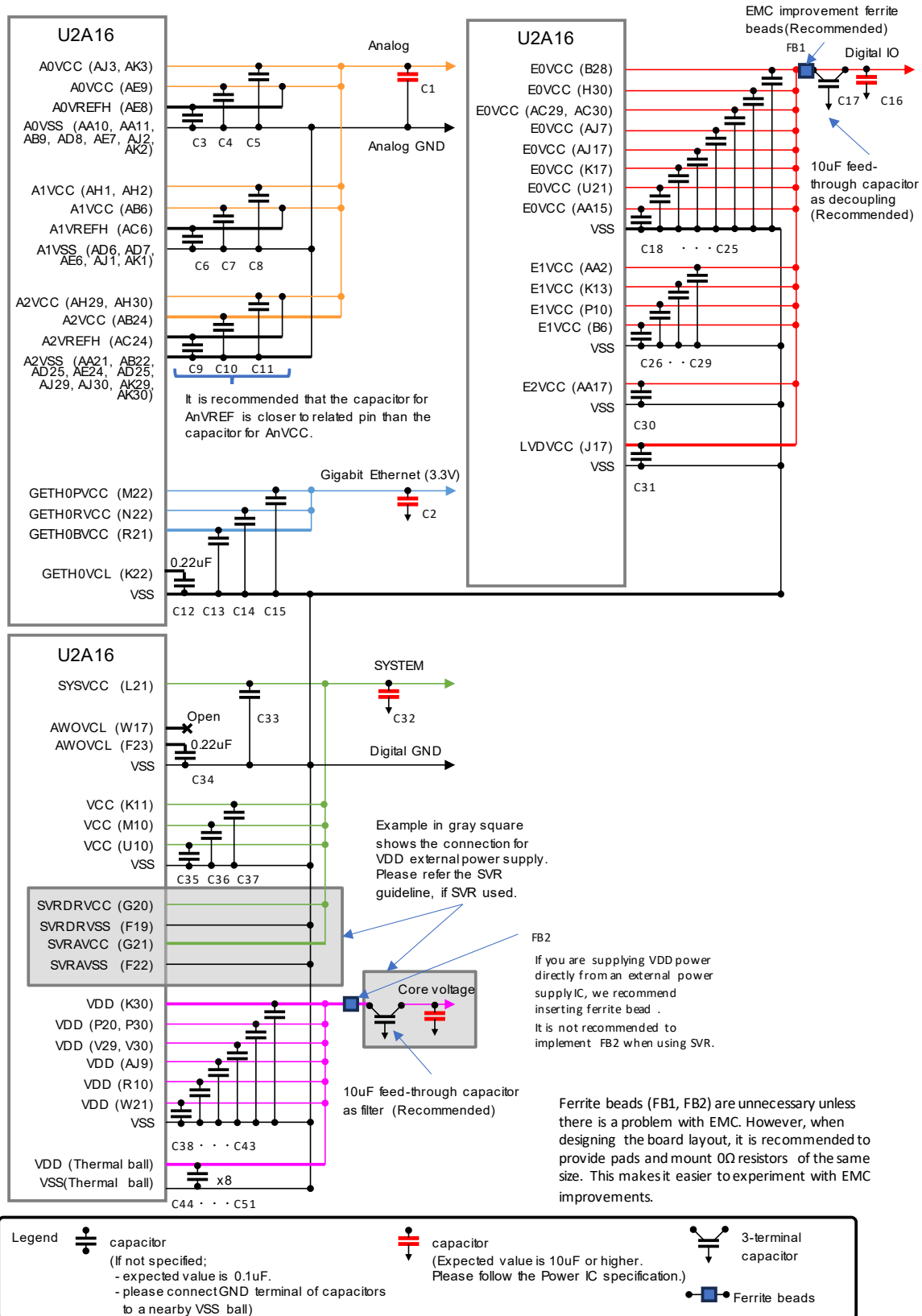
BGA connection VIA is the VIA to connect BGA ball to capacitor. This VIA should not be connected to the inner power/ground layer.

Inner layer connection VIA is the VIA to connect capacitor to inner power/ground layer.



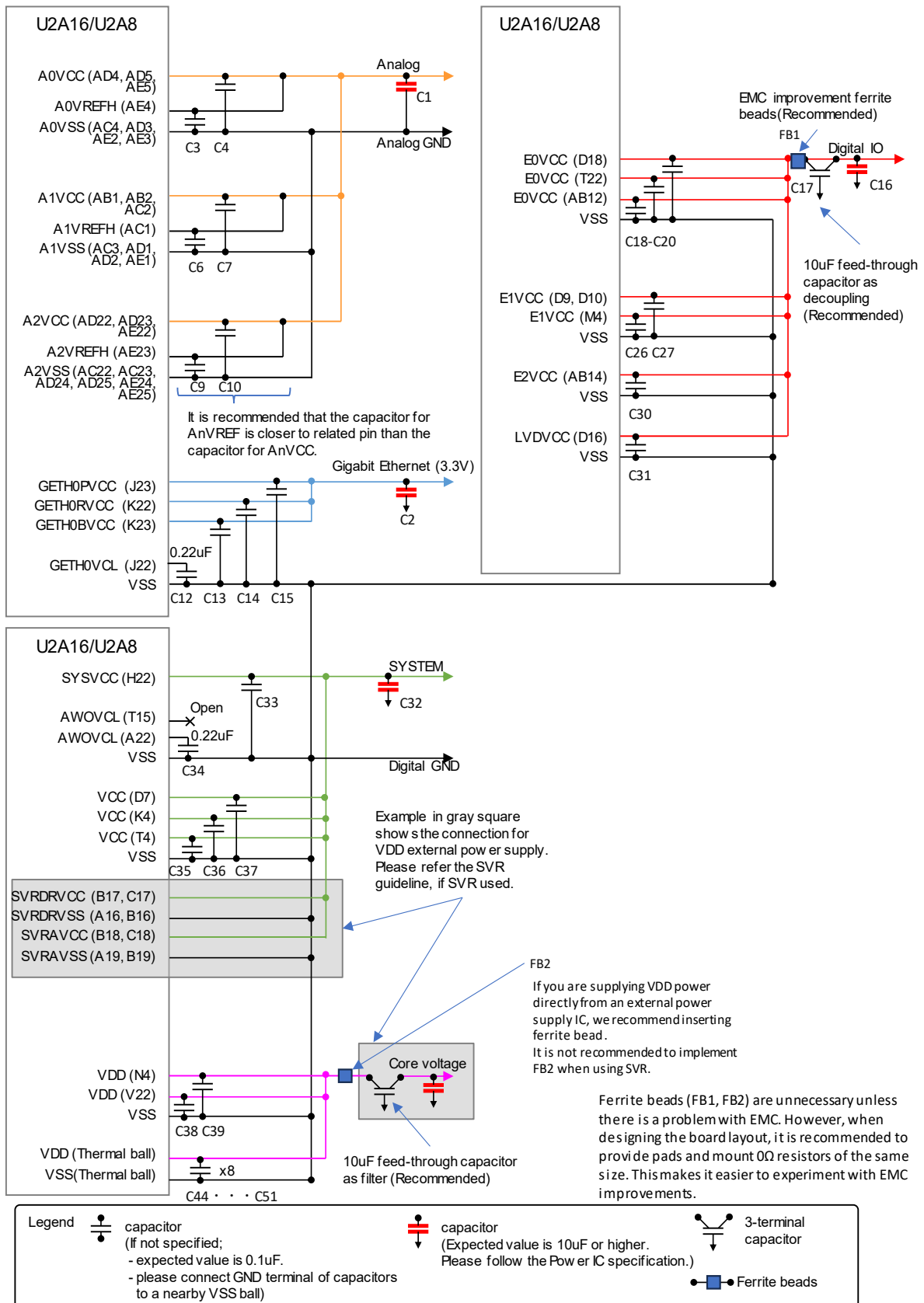
2. Example of capacitor placement

2.1 Example capacitor connection for BGA516 package (U2A16)



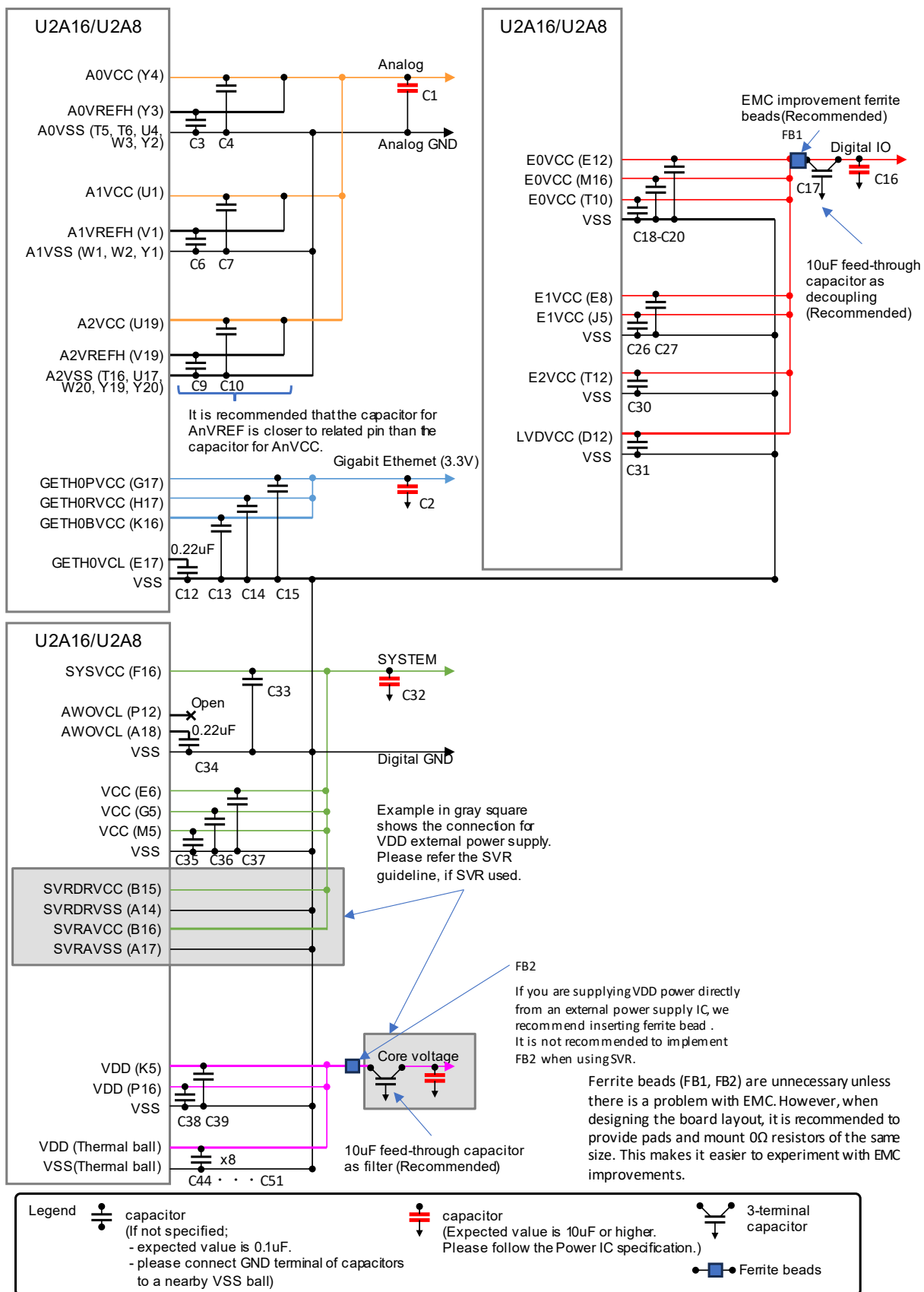
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.2 Example capacitor connection for BGA373 package (U2A16/U2A8)



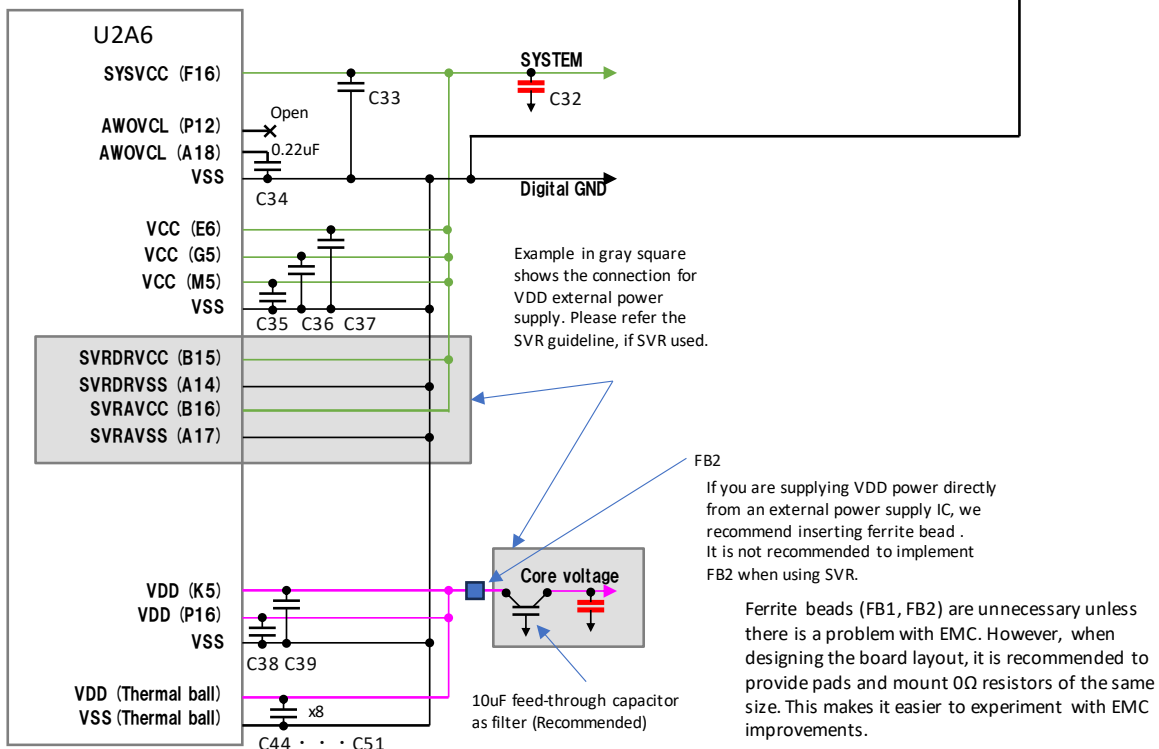
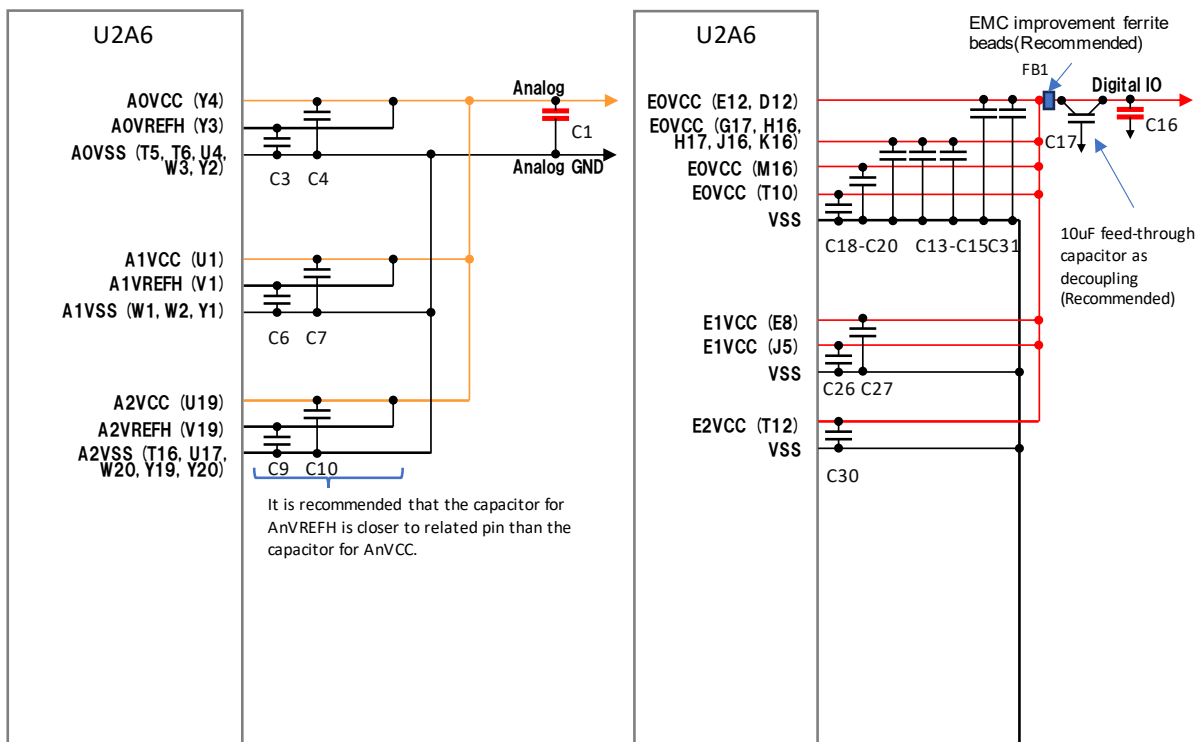
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.3 Example capacitor connection for BGA292 package (U2A16/U2A8)



Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

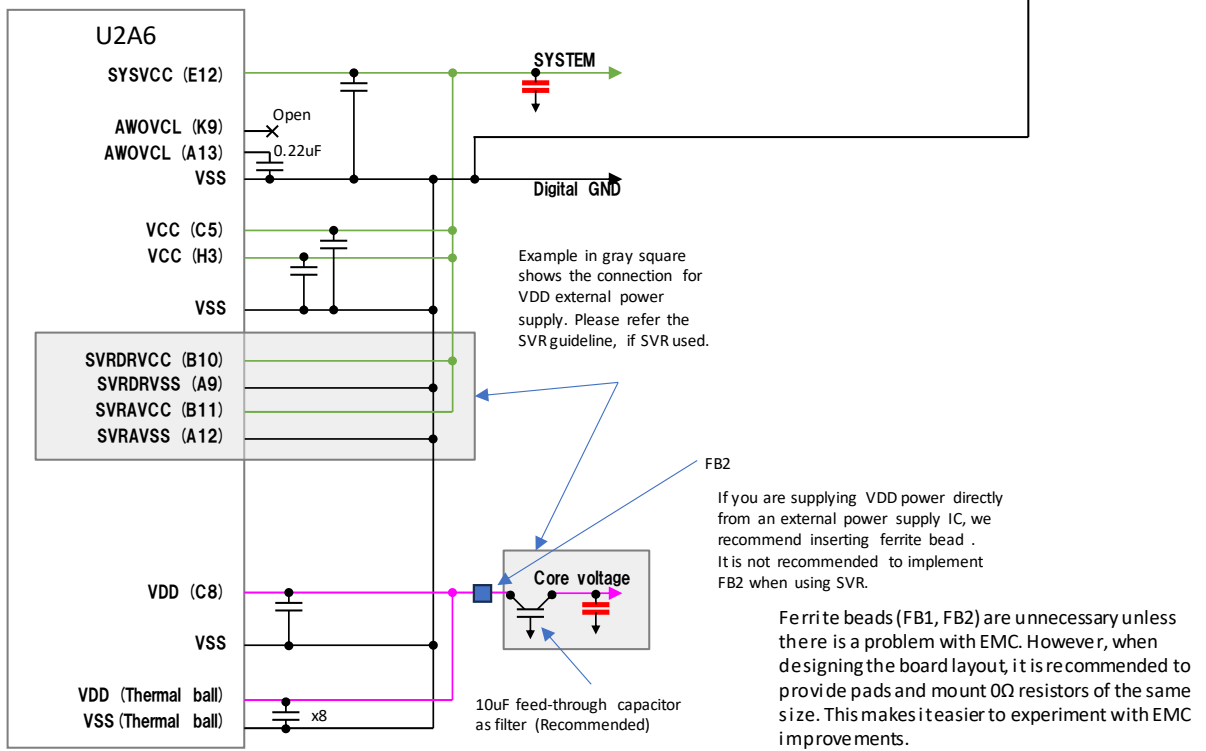
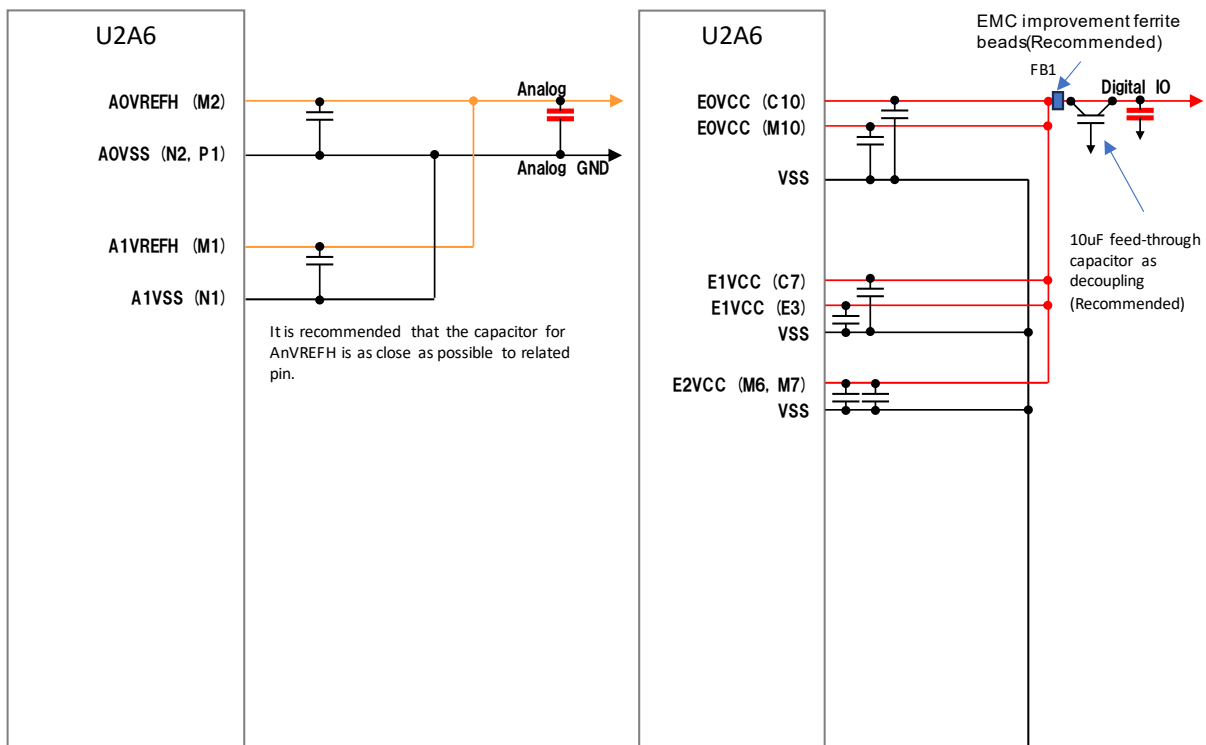
2.4 Example capacitor connection for BGA292 package (U2A6)



Legend	capacitor (If not specified, - expected value is 0.1uF. - please connect GND terminal of capacitors to a nearby VSS ball)	capacitor (Expected value is 10uF or higher. Please follow the Power IC specification.)	3-terminal capacitor
			Ferrite beads

Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

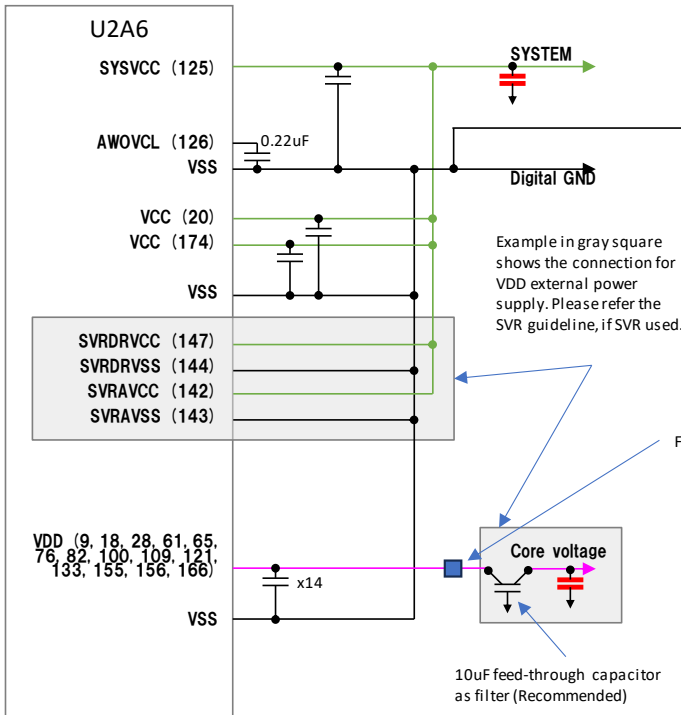
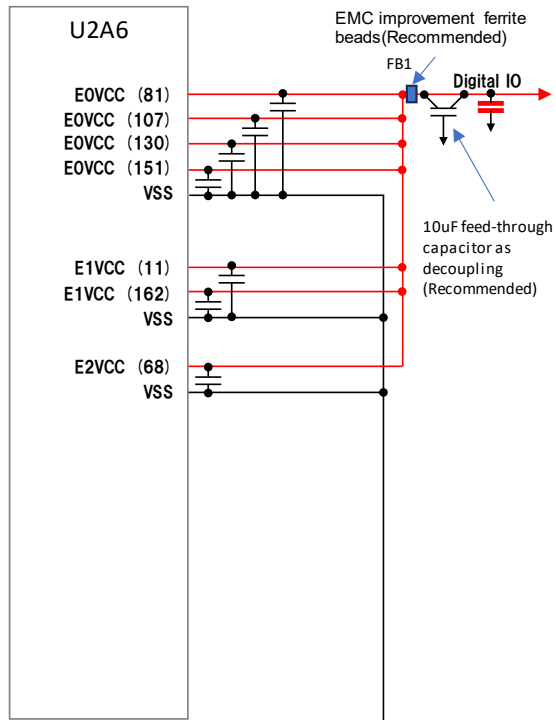
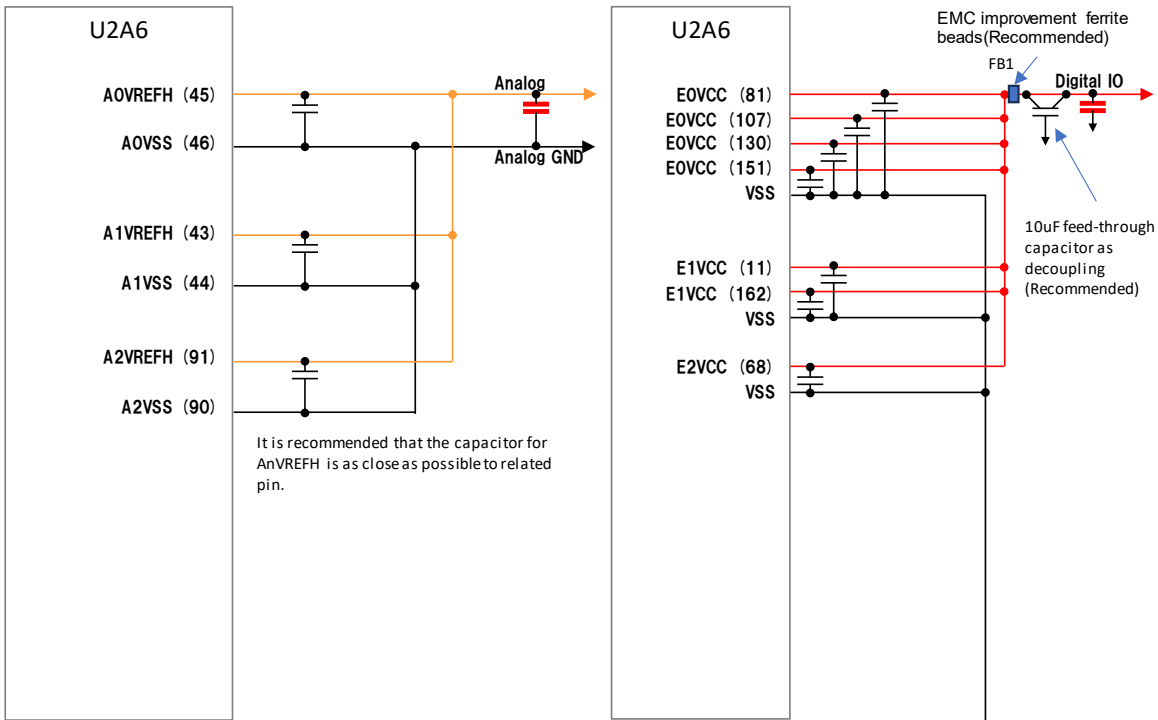
2.5 Example capacitor connection for BGA156 package (U2A6)



Legend	capacitor (If not specified; - expected value is 0.1uF. - please connect GND terminal of capacitors to a nearby VSS ball)	capacitor (Expected value is 10uF or higher. Please follow the Power IC specification.)	3-terminal capacitor
			Ferrite beads

Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.6 Example capacitor connection for HLQFP176 package (U2A6)



FB2

If you are supplying VDD power directly from an external power supply IC, we recommend inserting ferrite bead. It is not recommended to implement FB2 when using SVR.

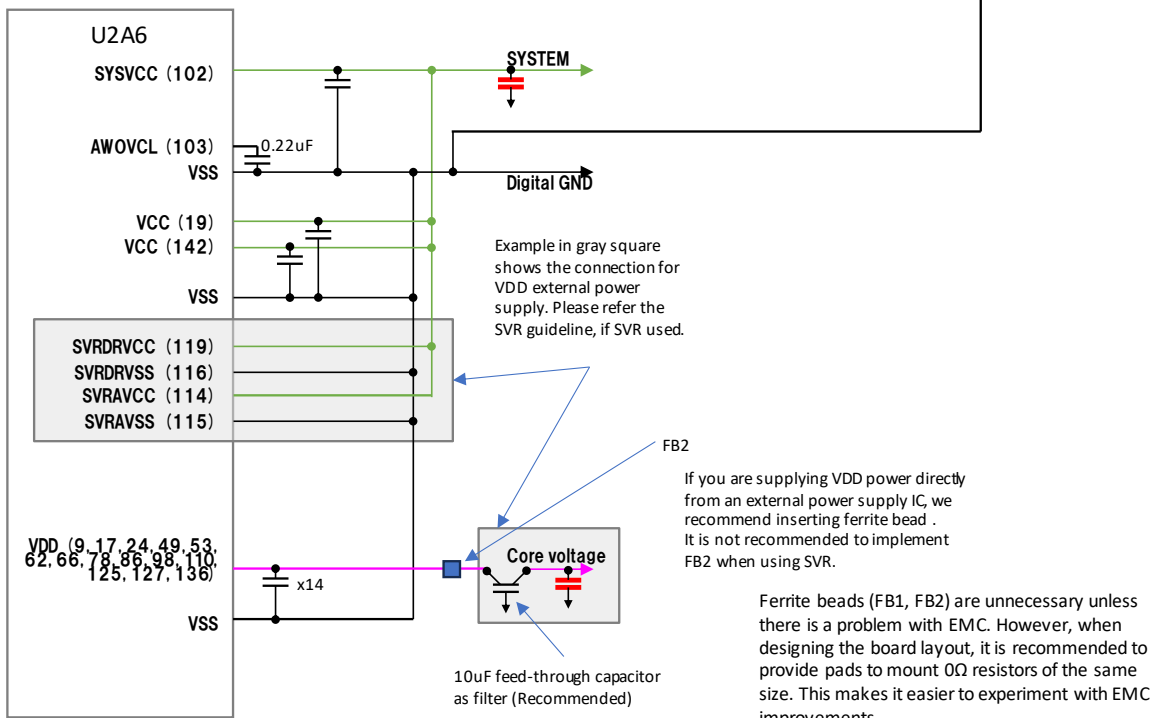
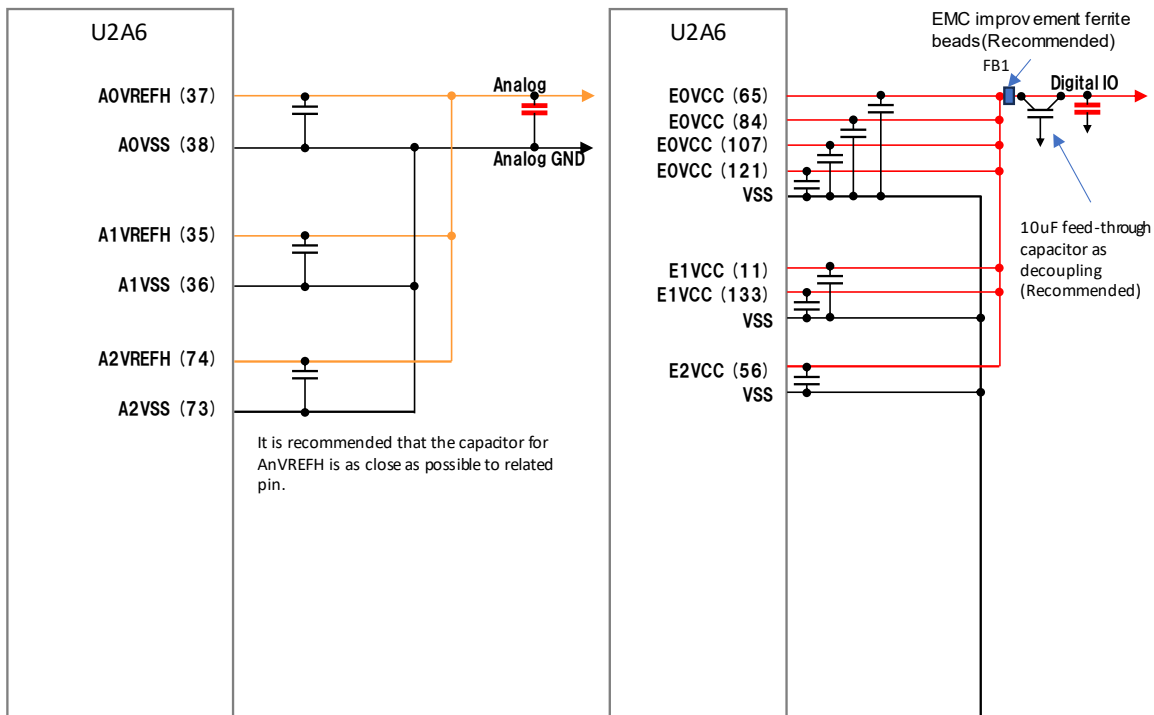
Ferrite beads (FB1, FB2) are unnecessary unless there is a problem with EMC. However, when designing the board layout, it is recommended to provide pads to mount 0Ω resistors of the same size. This makes it easier to experiment with EMC improvements.

Legend

- capacitor (If not specified; - expected value is 0.1uF. - please connect GND terminal of capacitors to a nearby VSS ball)
- capacitor (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor
- Ferrite beads

Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.7 Example capacitor connection for HLQFP144 package (U2A6)











Legend	capacitor (If not specified; - expected value is 0.1uF. - please connect GND terminal of capacitors to a nearby VSS ball)	capacitor (Expected value is 10uF or higher. Please follow the Power IC specification.)	3-terminal capacitor
			Ferrite beads

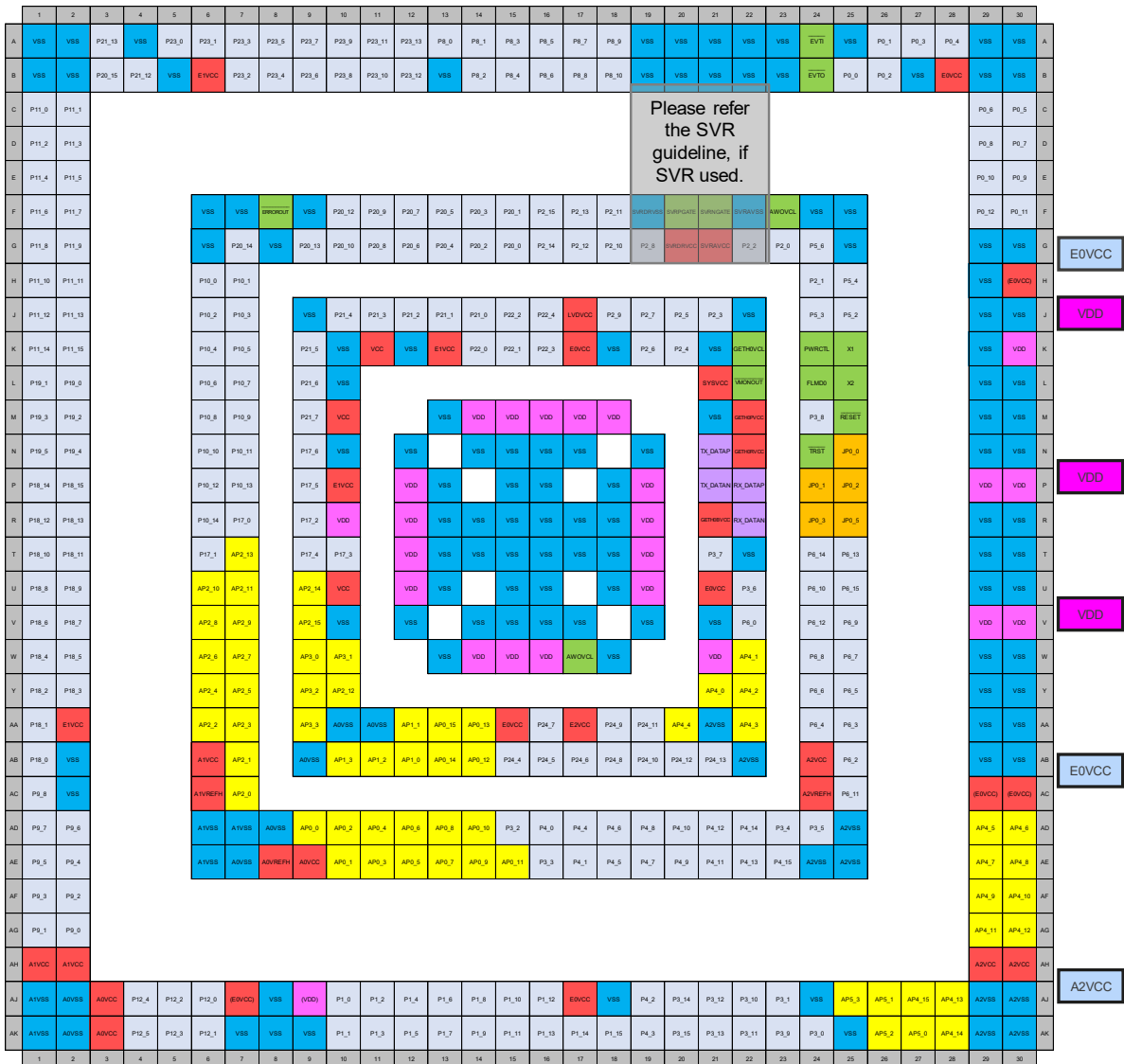
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

3. PCB layout guidelines -Top layer / Bottom layer-

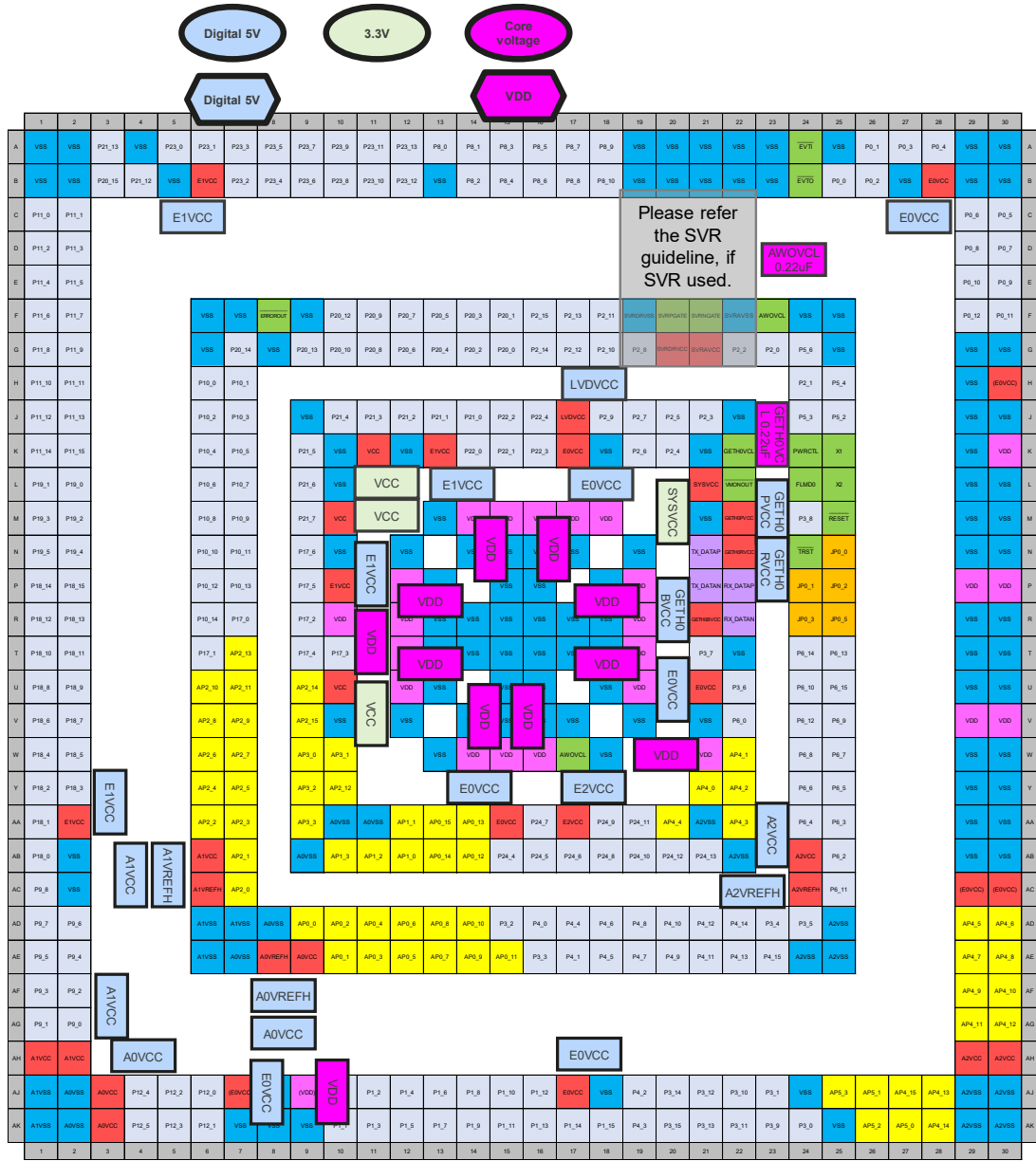
3.1 Example capacitor placement for BGA516 package (U2A16)

Legend

-  capacitor (analog, Digital IO)
(The capacitance is 0.1uF if not specified.)
-  capacitor (system)
(The capacitance is 0.1uF if not specified.)
-  capacitor (Core voltage)
(The capacitance is 0.1uF if not specified.)
-  capacitor (analog, Digital IO)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
-  capacitor (system)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
-  capacitor (Core voltage)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
-  3-terminal capacitor (analog, Digital IO)
-  3-terminal capacitor (Core voltage)



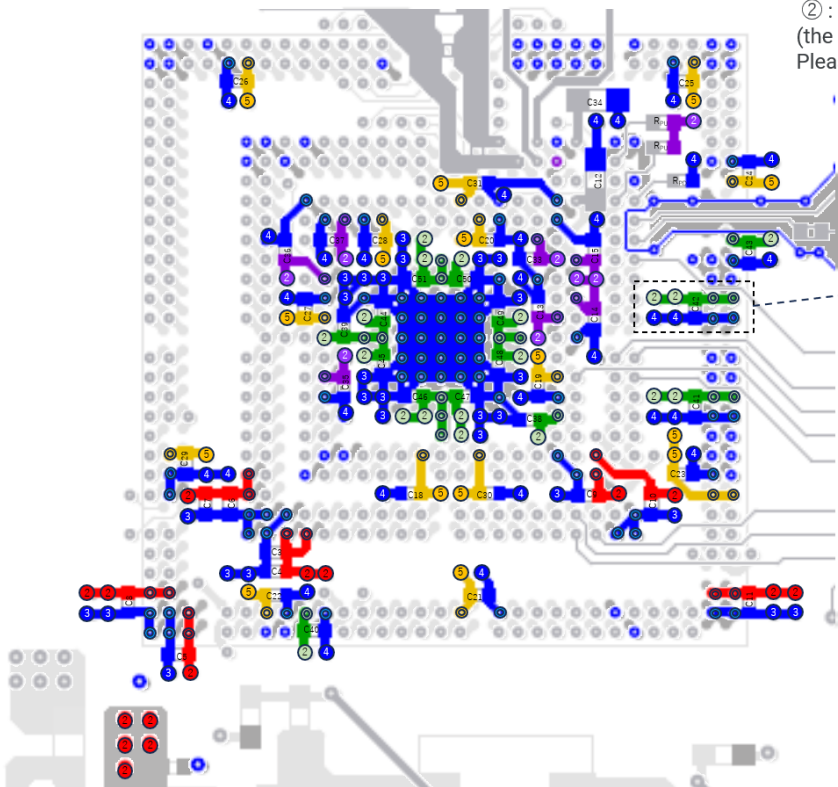
Top Layer



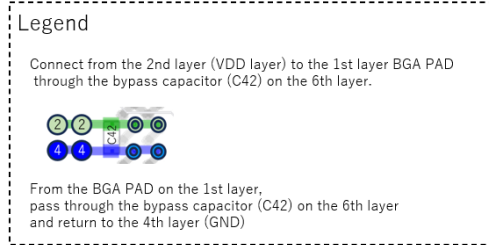
Analog 5V

Bottom Layer

BGA516 Bypass capacitor and VIA placement



⊙ : BGA connection VIA
 ② : Inner layer connection VIA
 (the number is the destination layer number)
 Please see the section 1.4 for the detail of capacitor connection.



green : VDD
 purple : System(VCC/SYSVCC) power supply
 GigabitEthernet power supply[3.3V]
 red : Analog(AxVCC) power supply[5V]
 yellow : Digital IO(ExVCC) power supply[5V]
 blue : VSS

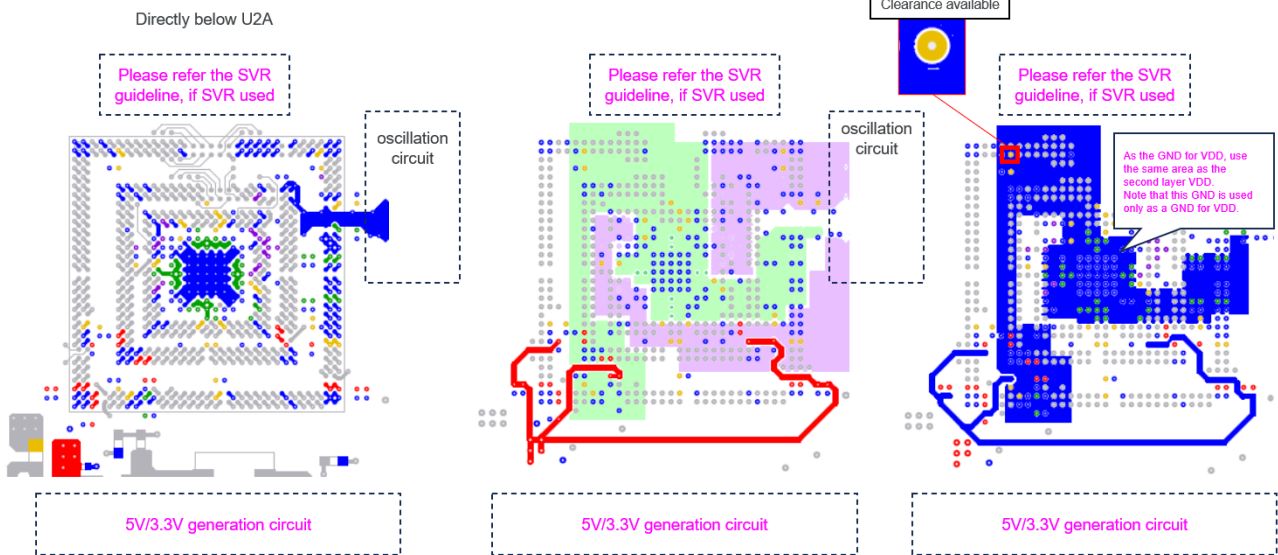
R_{PU} : pull up resistance
 R_{PD} : pull down resistance

The 1st and 6th layers are displayed superimposed (color is the 6th layer)

BGA516 1st layer

2nd layer

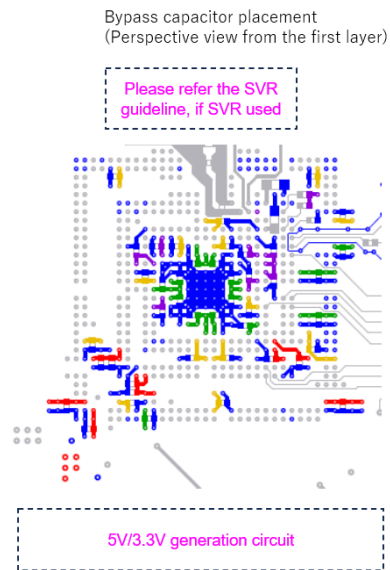
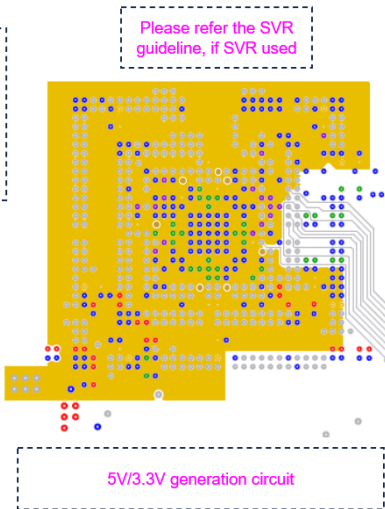
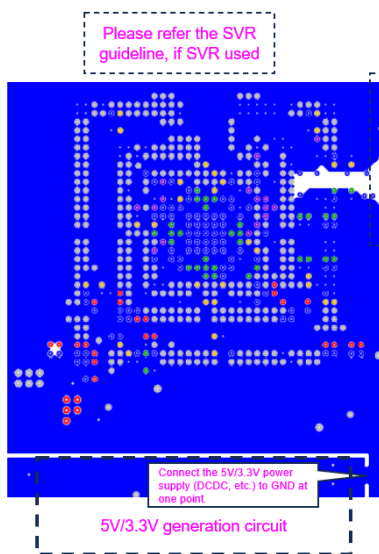
3rd layer



BGA516 4th layer

5th layer

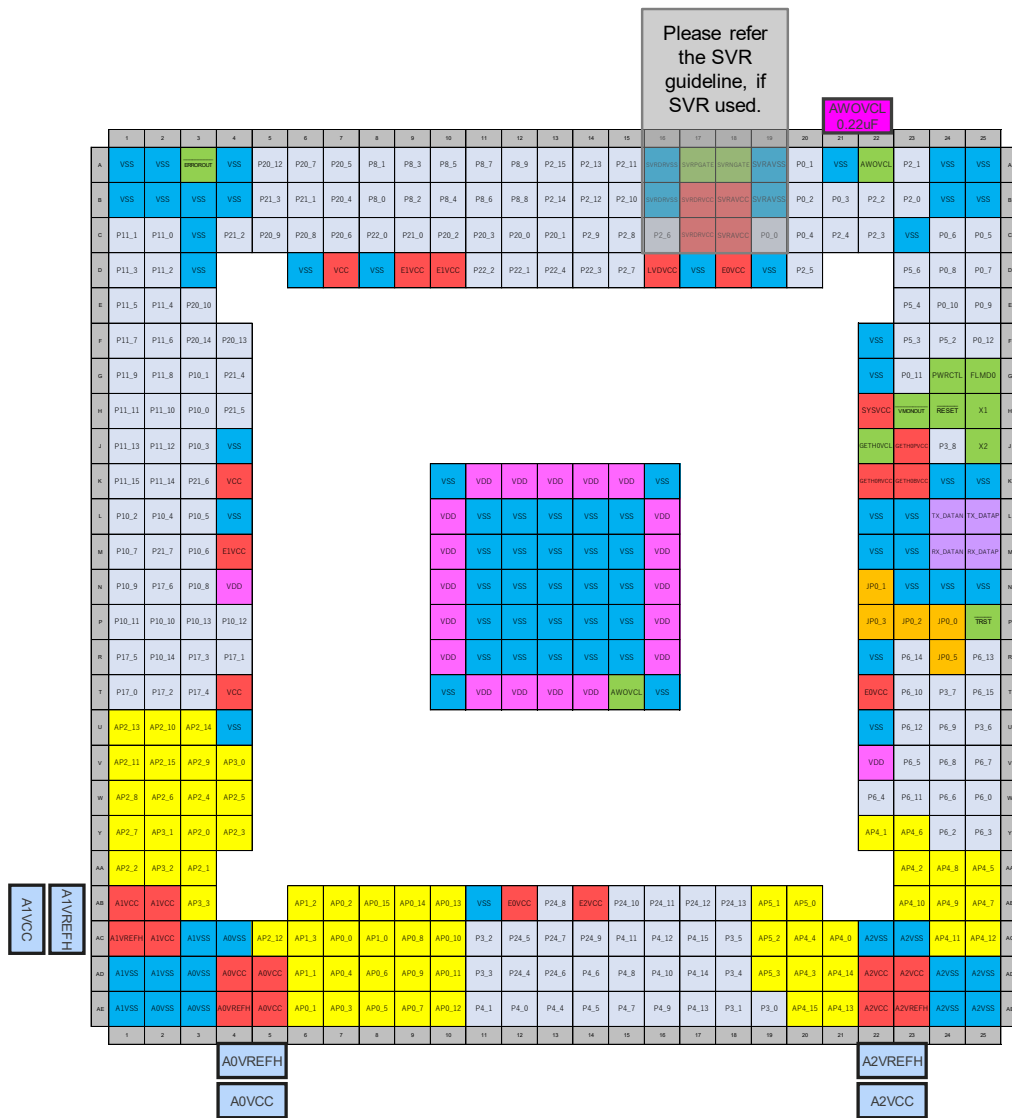
6th layer



3.2 Example capacitor placement for BGA373 package (U2A16/U2A8)

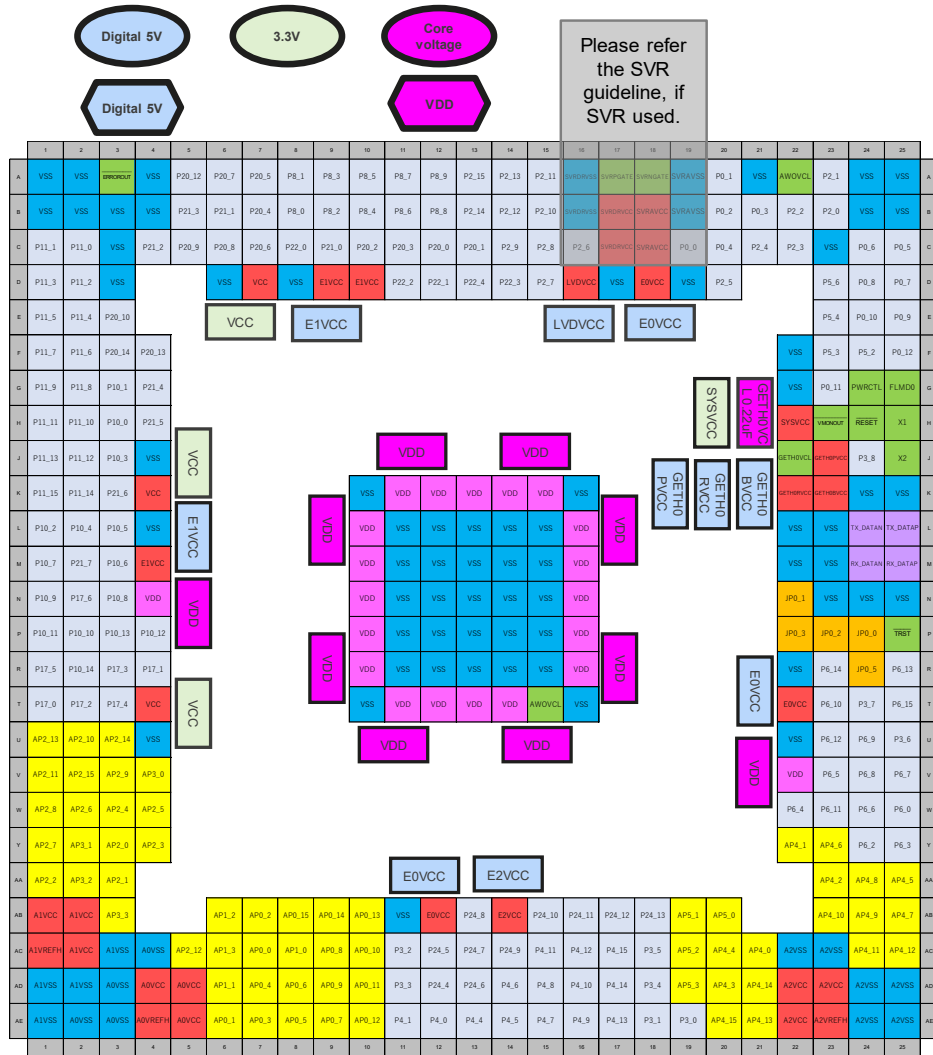
Legend

- capacitor (analog, Digital IO)
(The capacitance is 0.1uF if not specified.)
- capacitor (system)
(The capacitance is 0.1uF if not specified.)
- capacitor (Core voltage)
(The capacitance is 0.1uF if not specified.)
- capacitor (analog, Digital IO)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (system)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (Core voltage)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (analog, Digital IO)
- 3-terminal capacitor (Core voltage)



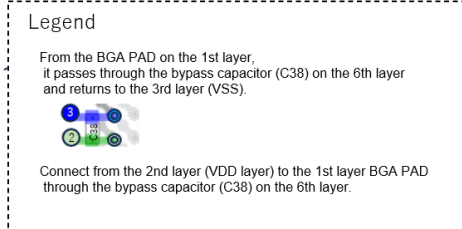
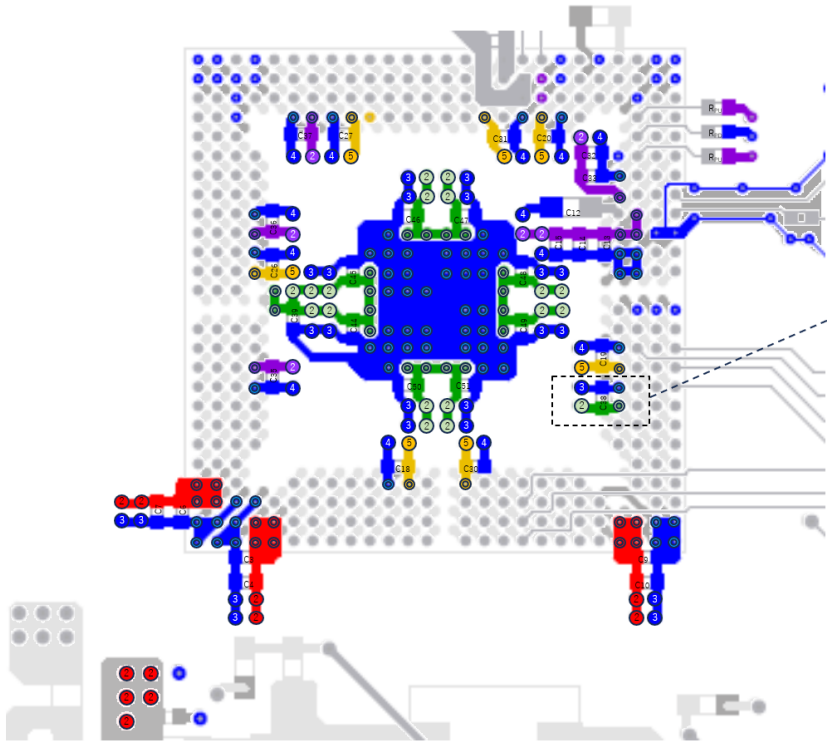
Analog 5V

Top Layer



BGA373 Bypass capacitor and VIA placement

⊙ : BGA connection VIA
 ② : Inner layer connection VIA
 (the number is the destination layer number)
 Please see the section 1.4 for the detail of capacitor connection.



green : VDD
 purple : System(VCC/SYSVCC) power supply
 GigabitEthernet power supply[3.3V]
 red : Analog(AxVCC) power supply[5V]
 yellow : Digital IO(ExVCC) power supply[5V]
 blue : VSS

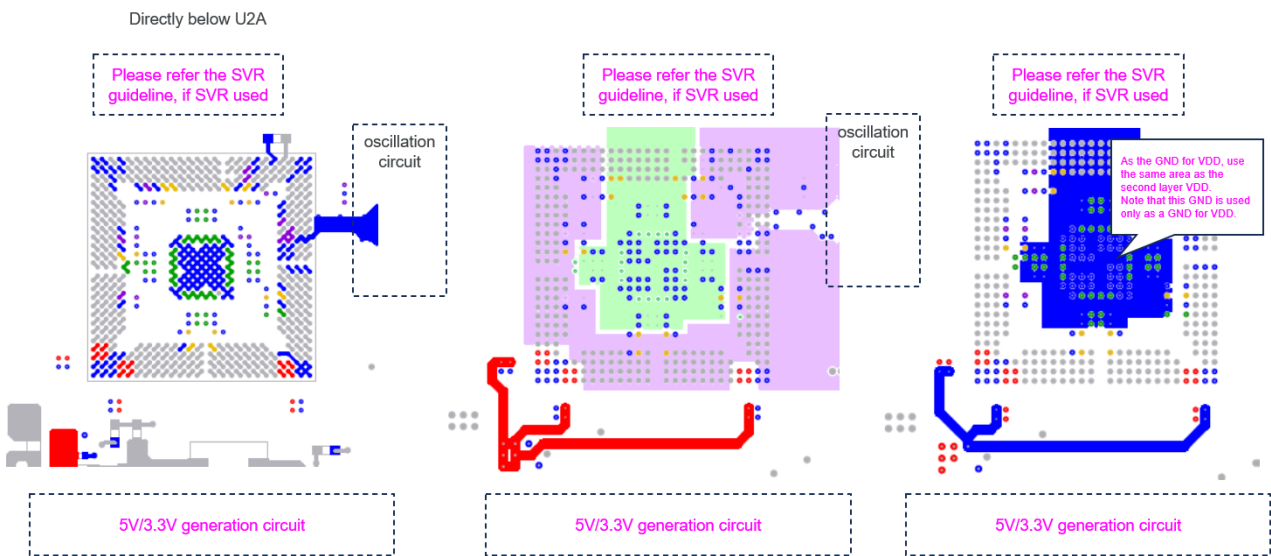
R_{PU} : pull up resistance
 R_{PD} : pull down resistance

The 1st and 6th layers are displayed superimposed (color is the 6th layer)

BGA373 1st layer

2nd layer

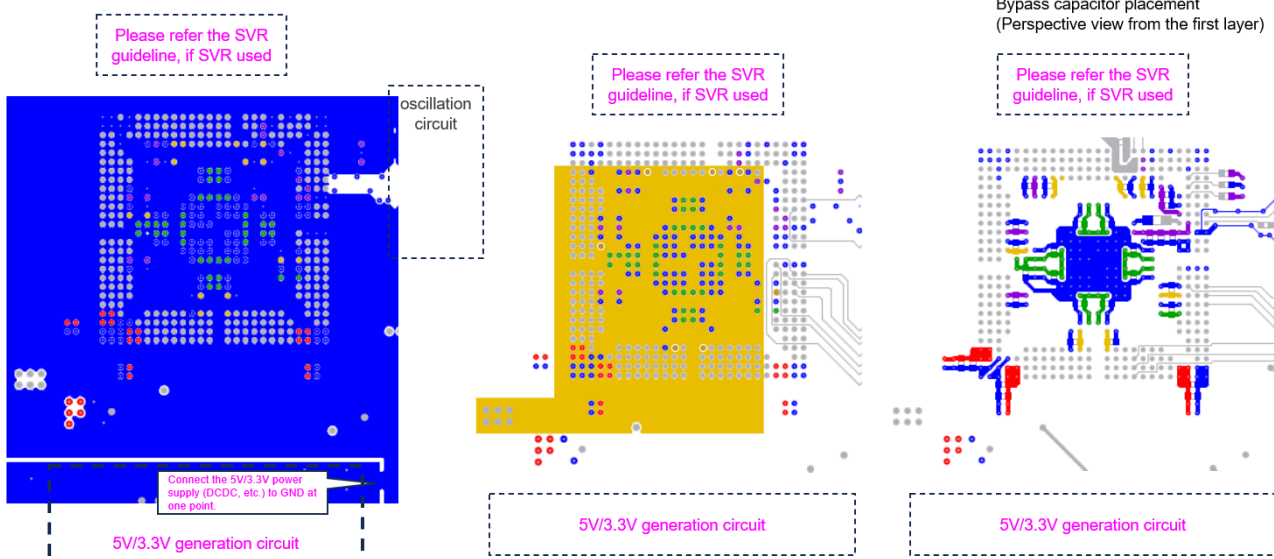
3rd layer



BGA373 4th layer









5th layer

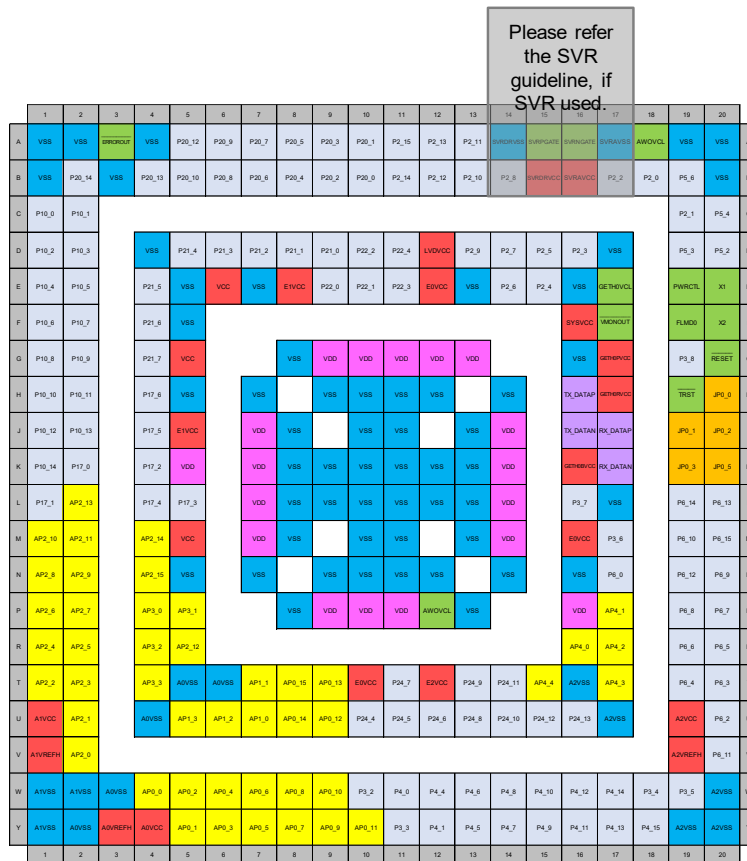
6th layer



3.3 Example capacitor placement for BGA292 package (U2A16/U2A8)

Legend

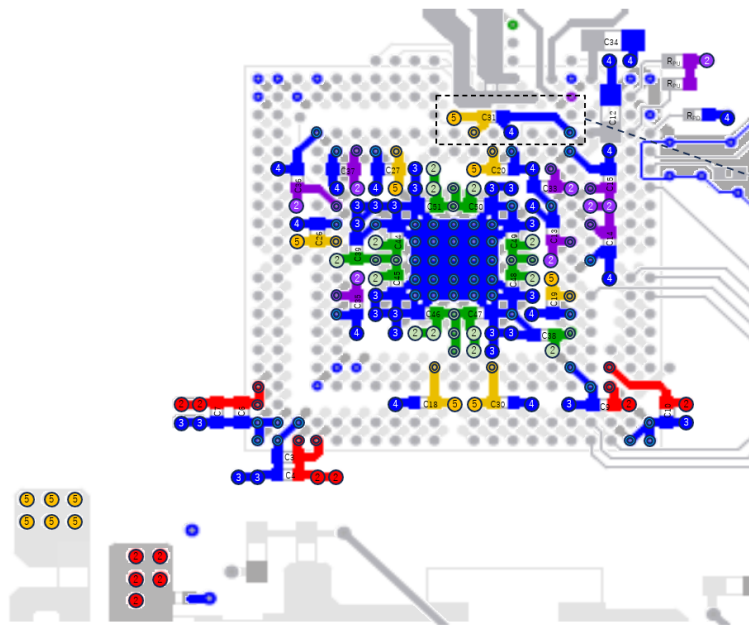
-  capacitor (analog, Digital IO)
(The capacitance is 0.1uF if not specified.)
-  capacitor (system)
(The capacitance is 0.1uF if not specified.)
-  capacitor (Core voltage)
(The capacitance is 0.1uF if not specified.)
-  capacitor (analog, Digital IO)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
-  capacitor (system)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
-  capacitor (Core voltage)
(Expected value is 10uF or higher. Please follow the Power IC specification.)
-  3-terminal capacitor (analog, Digital IO)
-  3-terminal capacitor (Core voltage)



Top Layer

BGA292 Bypass capacitor and VIA placement

⊙ : BGA connection VIA
 ⊚ : Inner layer connection VIA
 (the number is the destination layer number)
 Please see the section 1.4 for the detail of capacitor connection.



Legend

Connect from the 5th layer (Digital IO power layer) to the 1st layer BGA PAD through the bypass capacitor (C31) on the 6th layer.

From the BGA PAD on the 1st layer, pass through the bypass capacitor (C31) on the 6th layer and return to the 4th layer (GND).

- green : VDD
- purple : System(VCC/SYSVCC) power supply
GigabitEthernet power supply[3.3V]
- red : Analog(AxVCC) power supply[5V]
- yellow : Digital IO(ExVCC) power supply[5V]
- blue : VSS

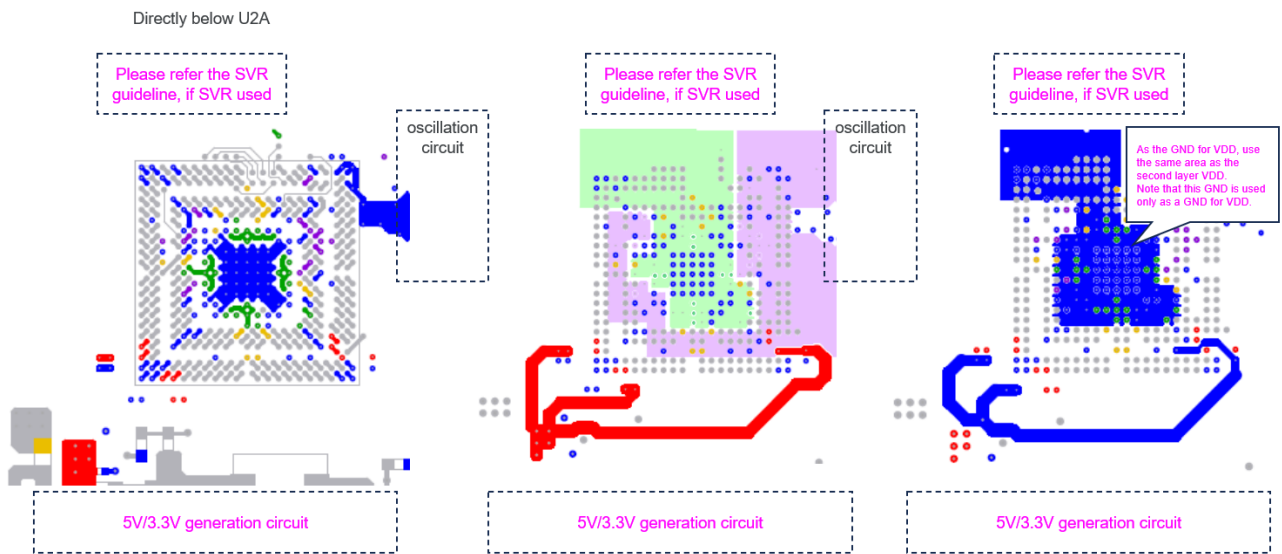
R_{PU} : pull up resistance
 R_{PD} : pull down resistance

The 1st and 6th layers are displayed superimposed (color is the 6th layer)

BGA292 1st layer

2nd layer

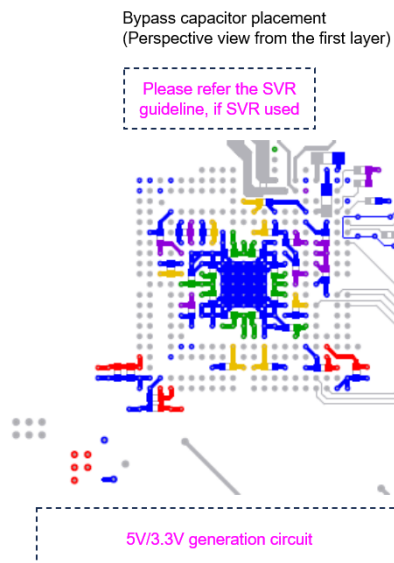
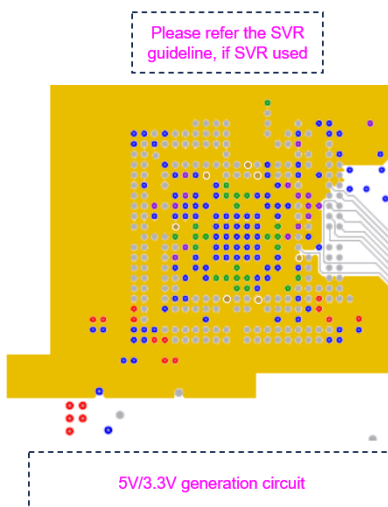
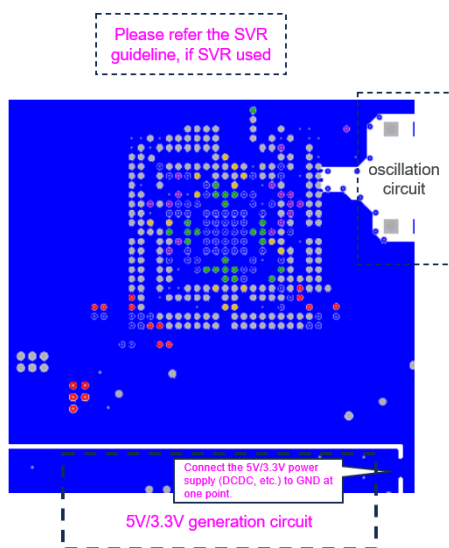
3rd layer



BGA292 4th layer









5th layer

6th layer



3.4 Example capacitor placement for BGA292 package (U2A6)

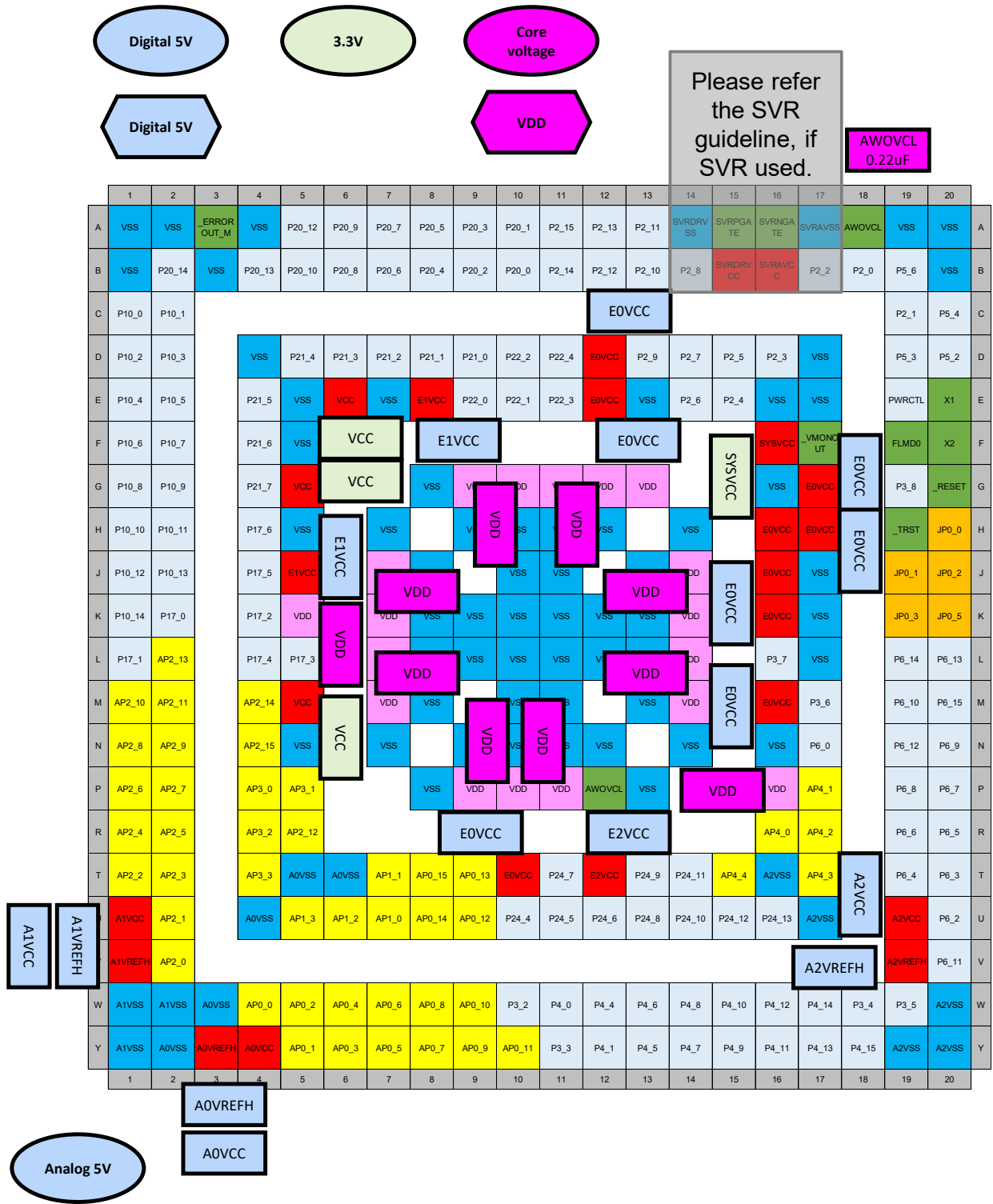
Legend

	capacitor (analog, Digital IO) (The capacitance is 0.1uF if not specified.)		capacitor (system) (Expected value is 10uF or higher. Please follow the Power IC specification.)
	capacitor (system) (The capacitance is 0.1uF if not specified.)		capacitor (Core voltage) (Expected value is 10uF or higher. Please follow the Power IC specification.)
	capacitor (Core voltage) (The capacitance is 0.1uF if not specified.)		3-terminal capacitor (analog, Digital IO)
	capacitor (analog, Digital IO) (Expected value is 10uF or higher. Please follow the Power IC specification.)		3-terminal capacitor (Core voltage)

Please refer the SVR guideline, if SVR used.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
A	VSS	VSS	ERROR_OUT_M	VSS	P20_12	P20_9	P20_7	P20_5	P20_3	P20_1	P2_15	P2_13	P2_11	SVRDRVSS	SVRPGATE	SVRNGATE	SVRAVSS	AWOVCL	VSS	VSS	A	
B	VSS	P20_14	VSS	P20_13	P20_10	P20_8	P20_6	P20_4	P20_2	P20_0	P2_14	P2_12	P2_10	P2_8	SVRDRVCC	SVRAVCC	P2_2	P2_0	P5_6	VSS	B	
C	P10_0	P10_1																	P2_1	P5_4	C	
D	P10_2	P10_3		VSS	P21_4	P21_3	P21_2	P21_1	P21_0	P22_2	P22_4	E0VCC	P2_9	P2_7	P2_5	P2_3	VSS		P5_3	P5_2	D	
E	P10_4	P10_5		P21_5	VSS	VCC	VSS	E1VCC	P22_0	P22_1	P22_3	E0VCC	VSS	P2_6	P2_4	VSS	VSS		PWRCTL	X1	E	
F	P10_6	P10_7		P21_6	VSS											SYSVCC	VMONOUT		FLMD0	X2	F	
G	P10_8	P10_9		P21_7	VCC			VSS	VDD	VDD	VDD	VDD	VDD			VSS	E0VCC		P3_8	_RESET	G	
H	P10_10	P10_11		P17_6	VSS		VSS		VSS	VSS	VSS	VSS		VSS		E0VCC	E0VCC		_TRST	JP0_0	H	
J	P10_12	P10_13		P17_5	E1VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	VSS		JP0_1	JP0_2	J	
K	P10_14	P17_0		P17_2	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		E0VCC	VSS		JP0_3	JP0_5	K	
L	P17_1	AP2_13		P17_4	P17_3		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P3_7	VSS		P6_14	P6_13	L	
M	AP2_10	AP2_11		AP2_14	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P3_6		P6_10	P6_15	M	
N	AP2_8	AP2_9		AP2_15	VSS		VSS		VSS	VSS	VSS		VSS			VSS	P6_0		P6_12	P6_9	N	
P	AP2_6	AP2_7		AP3_0	AP3_1		VSS	VDD	VDD	VDD	AWOVCL	VSS				VDD	AP4_1		P6_8	P6_7	P	
R	AP2_4	AP2_5		AP3_2	AP2_12											AP4_0	AP4_2		P6_6	P6_5	R	
T	AP2_2	AP2_3		AP3_3	A0VSS	A0VSS	AP1_1	AP0_15	AP0_13	E0VCC	P24_7	E2VCC	P24_9	P24_11	AP4_4	A2VSS	AP4_3		P6_4	P6_3	T	
U	A1VCC	AP2_1		A0VSS	AP1_3	AP1_2	AP1_0	AP0_14	AP0_12	P24_4	P24_5	P24_6	P24_8	P24_10	P24_12	P24_13	A2VSS		A2VCC	P6_2	U	
V	A1VREFH	AP2_0																		A2VREFH	P6_11	V
W	A1VSS	A1VSS	A0VSS	AP0_0	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P3_2	P4_0	P4_4	P4_6	P4_8	P4_10	P4_12	P4_14	P3_4	P3_5	A2VSS	W	
Y	A1VSS	A0VSS	A0VREFH	A0VCC	AP0_1	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P3_3	P4_1	P4_5	P4_7	P4_9	P4_11	P4_13	P4_15	A2VSS	A2VSS	Y	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

Top Layer











Bottom Layer

For examples of PCB board design, please refer to "3.3 Example capacitor placement for BGA292 package (U2A16/U2A8)".

3.5 Example capacitor placement for BGA156 package (U2A6)

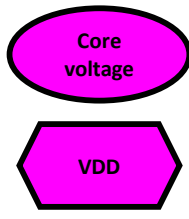
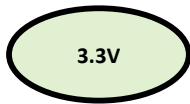
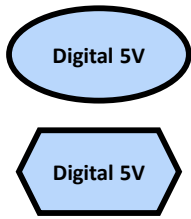
Legend

	capacitor (analog, Digital IO) (The capacitance is 0.1uF if not specified.)		capacitor (system) (Expected value is 10uF or higher. Please follow the Power IC specification.)
	capacitor (system) (The capacitance is 0.1uF if not specified.)		capacitor (Core voltage) (Expected value is 10uF or higher. Please follow the Power IC specification.)
	capacitor (Core voltage) (The capacitance is 0.1uF if not specified.)		3-terminal capacitor (analog, Digital IO)
	capacitor (analog, Digital IO) (Expected value is 10uF or higher. Please follow the Power IC specification.)		3-terminal capacitor (Core voltage)

Please refer the SVR guideline, if SVR used.

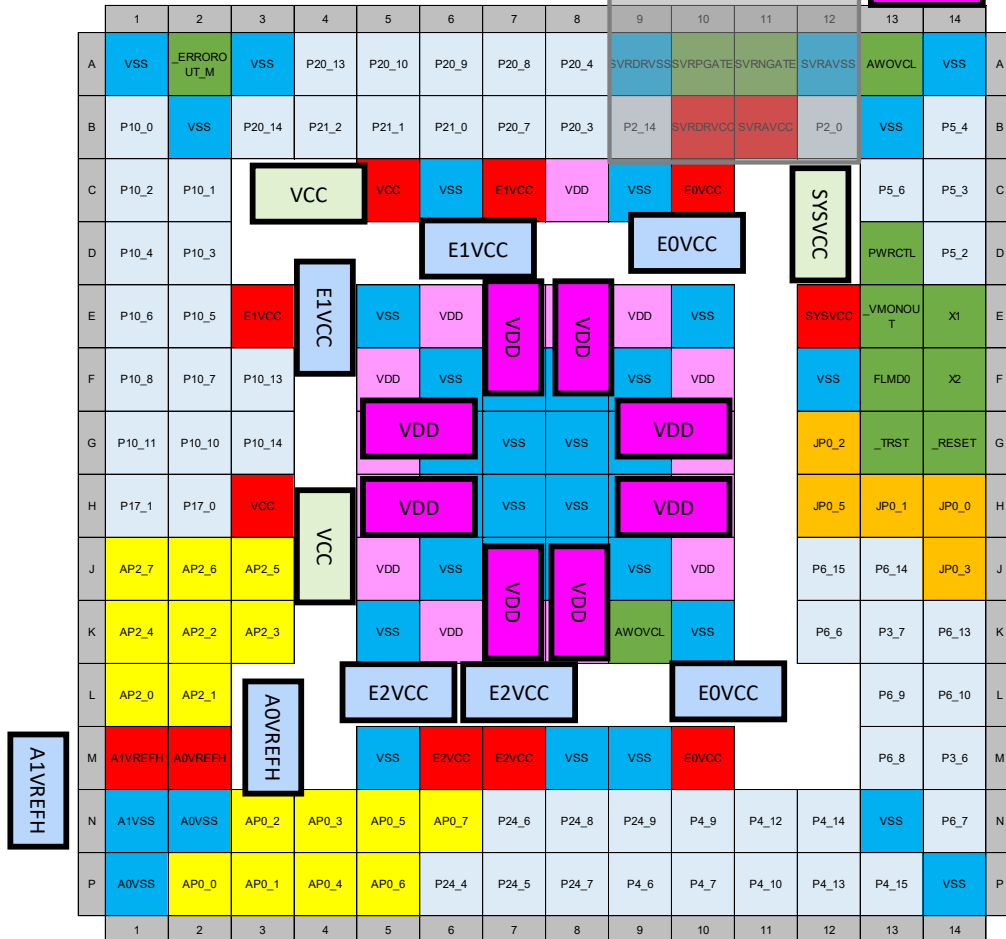
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	_ERRORO UT_M	VSS	P20_13	P20_10	P20_9	P20_8	P20_4	SVRDRVSS	SVRPGATE	SVRNGATE	SVRAVSS	AWOVCL	VSS	A
B	P10_0	VSS	P20_14	P21_2	P21_1	P21_0	P20_7	P20_3	P2_14	SVRDRVCC	SVRAVCC	P2_0	VSS	P5_4	B
C	P10_2	P10_1			VCC	VSS	E1VCC	VDD	VSS	E0VCC			P5_6	P5_3	C
D	P10_4	P10_3											PWRCTL	P5_2	D
E	P10_6	P10_5	E1VCC		VSS	VDD	VDD	VDD	VDD	VSS		SYSVCC	_VMONOU T	X1	E
F	P10_8	P10_7	P10_13		VDD	VSS	VSS	VSS	VSS	VDD		VSS	FLMD0	X2	F
G	P10_11	P10_10	P10_14		VDD	VSS	VSS	VSS	VSS	VDD		JP0_2	_TRST	_RESET	G
H	P17_1	P17_0	VCC		VDD	VSS	VSS	VSS	VSS	VDD		JP0_5	JP0_1	JP0_0	H
J	AP2_7	AP2_6	AP2_5		VDD	VSS	VSS	VSS	VSS	VDD		P6_15	P6_14	JP0_3	J
K	AP2_4	AP2_2	AP2_3		VSS	VDD	VDD	VDD	AWOVCL	VSS		P6_6	P3_7	P6_13	K
L	AP2_0	AP2_1											P6_9	P6_10	L
M	A1VREFH	A0VREFH			VSS	E2VCC	E2VCC	VSS	VSS	E0VCC			P6_8	P3_6	M
N	A1VSS	A0VSS	AP0_2	AP0_3	AP0_5	AP0_7	P24_6	P24_8	P24_9	P4_9	P4_12	P4_14	VSS	P6_7	N
P	A0VSS	AP0_0	AP0_1	AP0_4	AP0_6	P24_4	P24_5	P24_7	P4_6	P4_7	P4_10	P4_13	P4_15	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Top Layer



Please refer the SVR guideline, if SVR used.

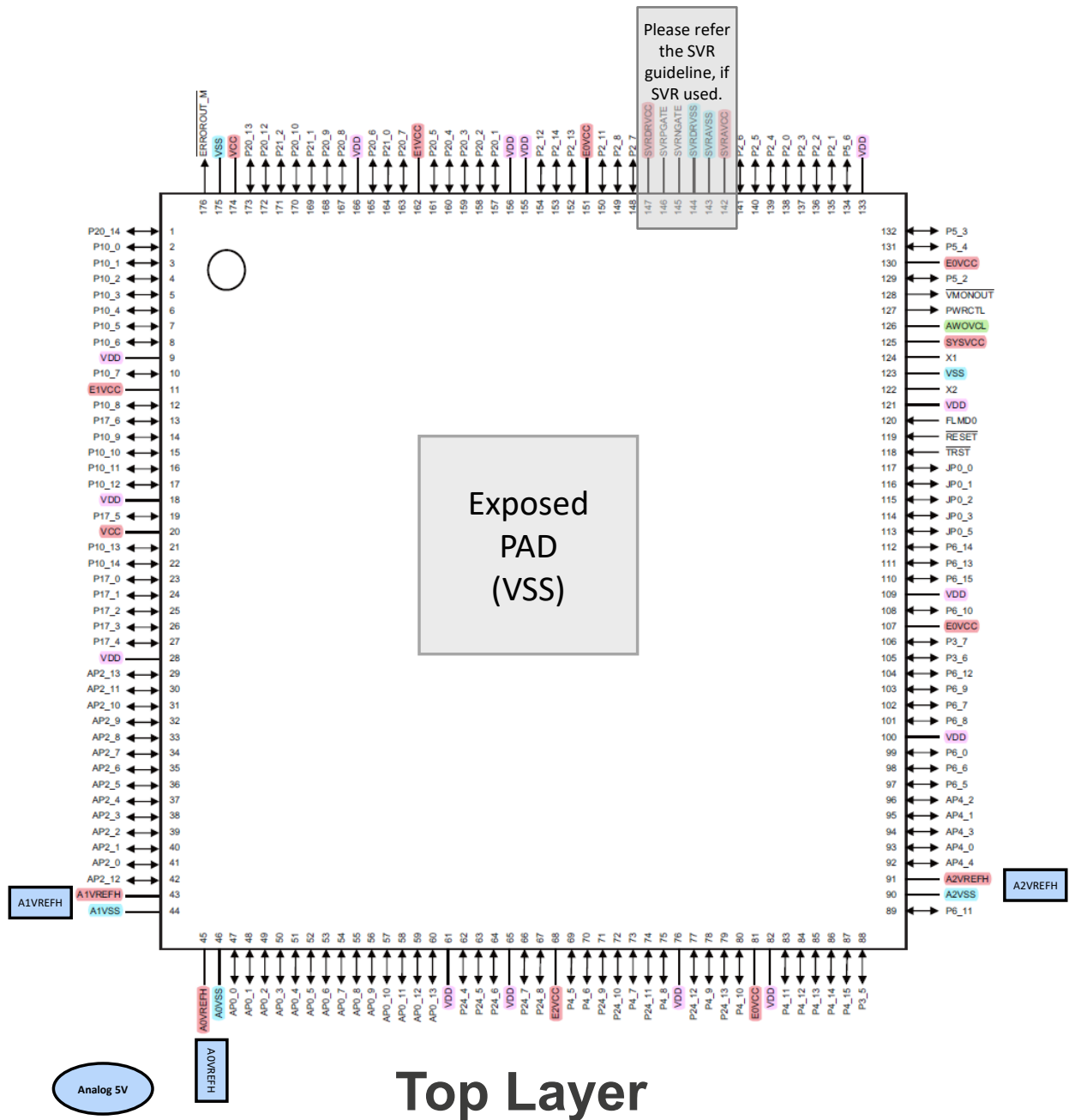
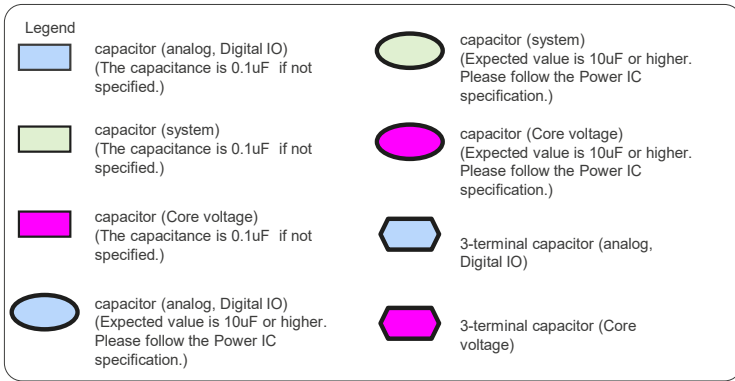
AWOVCL
0.22uF



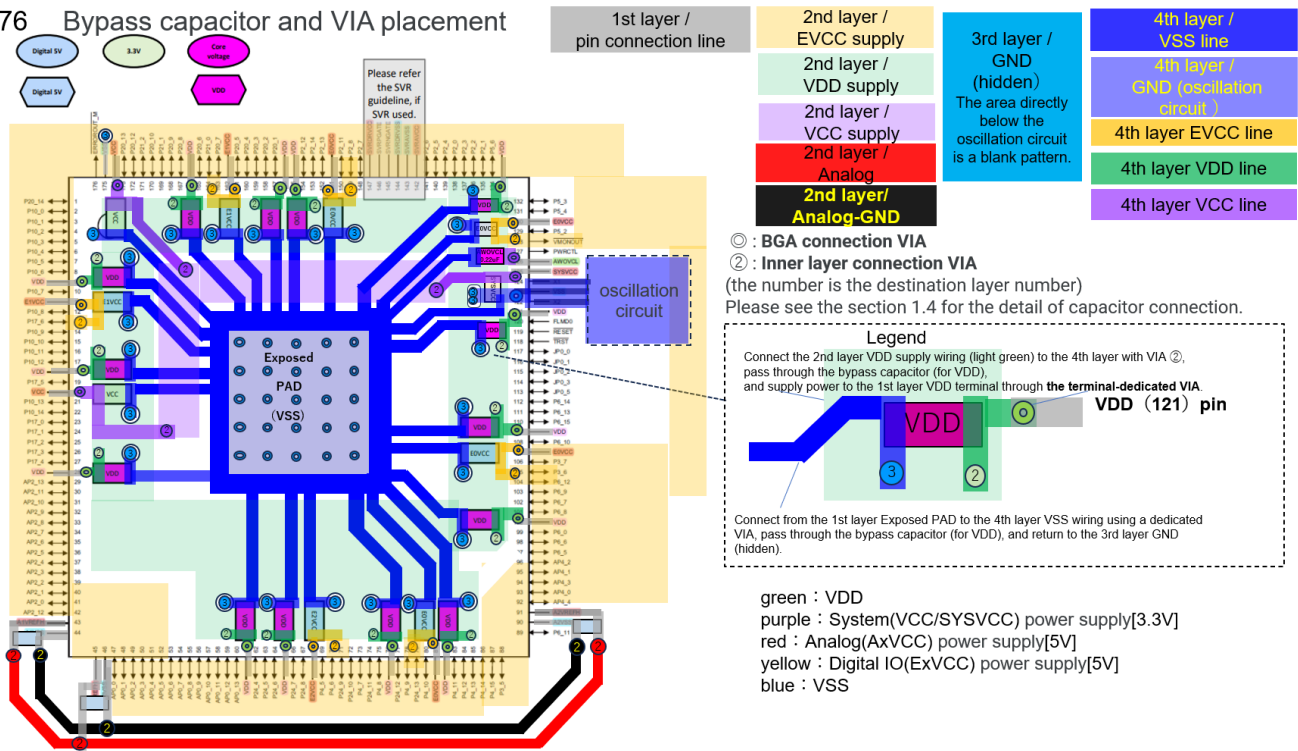
Bottom Layer

For examples of PCB board design, please refer to "3.3 Example capacitor placement for BGA292 package (U2A16/U2A8)".

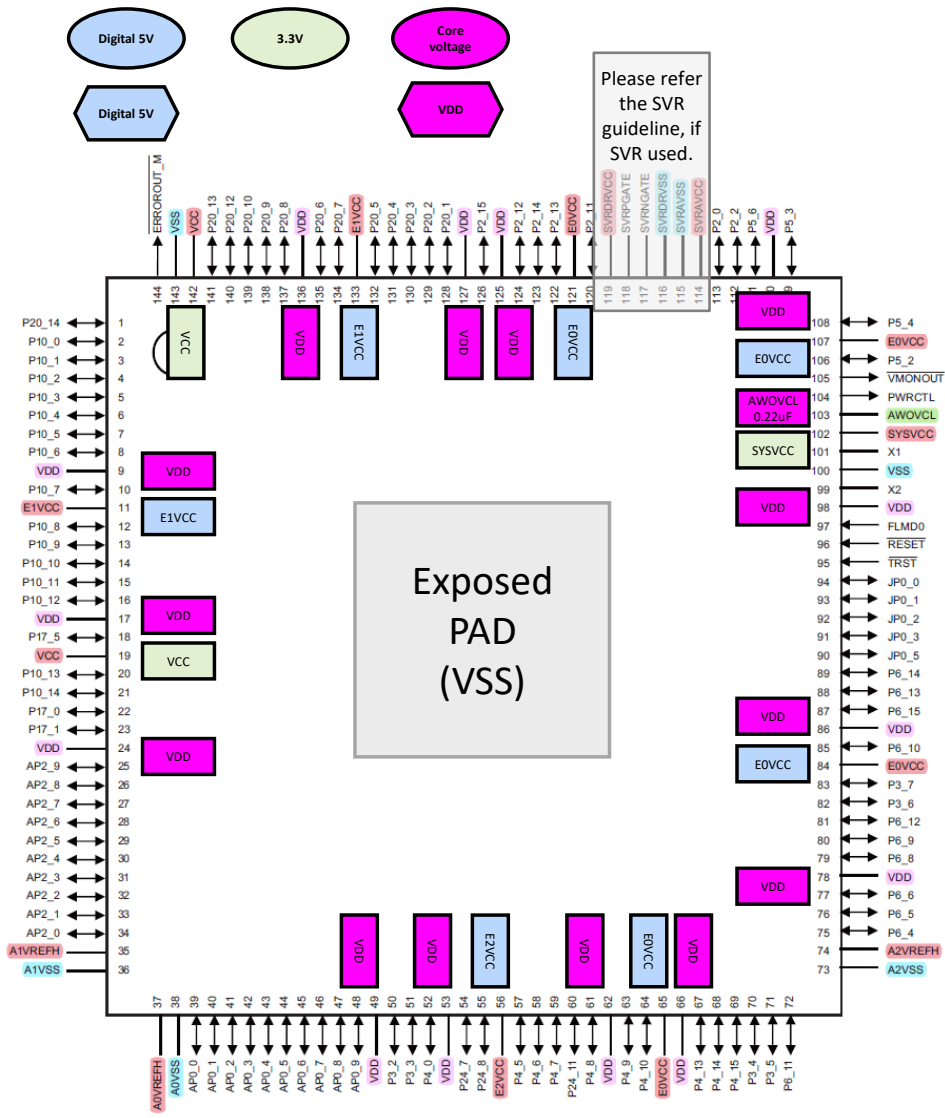
3.6 Example capacitor placement for HLQFP176 package (U2A6)



HLQFP176 Bypass capacitor and VIA placement



The 1st and 4th layers are displayed superimposed(Gray is the 1st layer, color is the 2nd layer, and 4th layer)



Bottom Layer

For examples of PCB board design, please refer to " 3.6 Example capacitor placement for HLQFP176 package (U2A6)".

4. Revision History

Rev.	Date	Description	
		Page	Summary
0.70	Mar.31.20	-	Initial version
1.00	Sep.30.20	all	Add U2A8
1.10	Jun.30.22	all	Add U2A6
1.20	Jan.31.24	Page1 Page3 Page4-7 Page4-10 Page13,14 ,17,18,21, 22,24,26,2 9,31	Add a sentence about the purpose of this document Add "1.4 How to connect capacitor power supply/GND" Add capacitor number (for use in Chapter 3) Add reference text regarding capacitance value for VDD Add ferrite beads(FB1,FB2) Add examples of PCB board design

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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