RH850/U2A-EVA Group

Example of capacitor placement

Introduction

This document describes the example of capacitor placement of RH850/U2A-EVA Group in consideration of EMC characteristics. The purpose of this document is to provide examples of PCB board design for reducing EMC noise in ECU.However, the EMC noise value is not necessarily guaranteed.
You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these information.

Target Device

- RH850/U2A-EVA Group
  - RH850/U2A16
  - RH850/U2A8
  - RH850/U2A6

Contents

1. Decoupling capacitors

1.1 Capacitor placement and number of capacitors

- Please refer Chapter.2 “Example of capacitor placement” and Chapter.3 “PCB layout guidelines -Top layer / Bottom layer-”.
- Capacitors has been kept as close as feasible to the related supply pin.

1.2 Types of capacitors

- 0.1uF, 0.22uF, 10uF or higher*1 ceramic capacitor (Low ESR/ESL is required)

  *1: This is expected value. Please follow the Power IC specification.
- 10uF 3-terminal ceramic capacitor (Very low ESR/ESL is required)

1.3 3-terminal capacitor

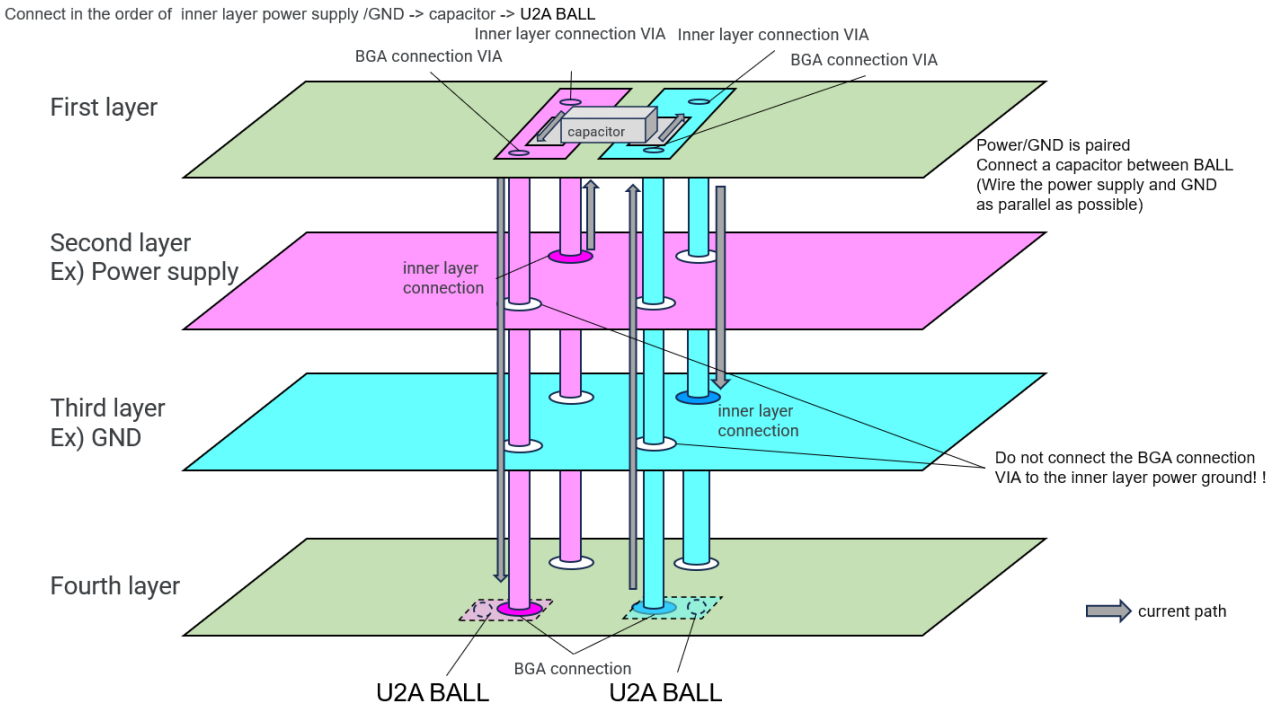
3-terminal capacitor is recommended for reduction of radiation noise.

1.4 How to connect capacitors and power supply/GND

Connections as shown in the diagram below are recommended.

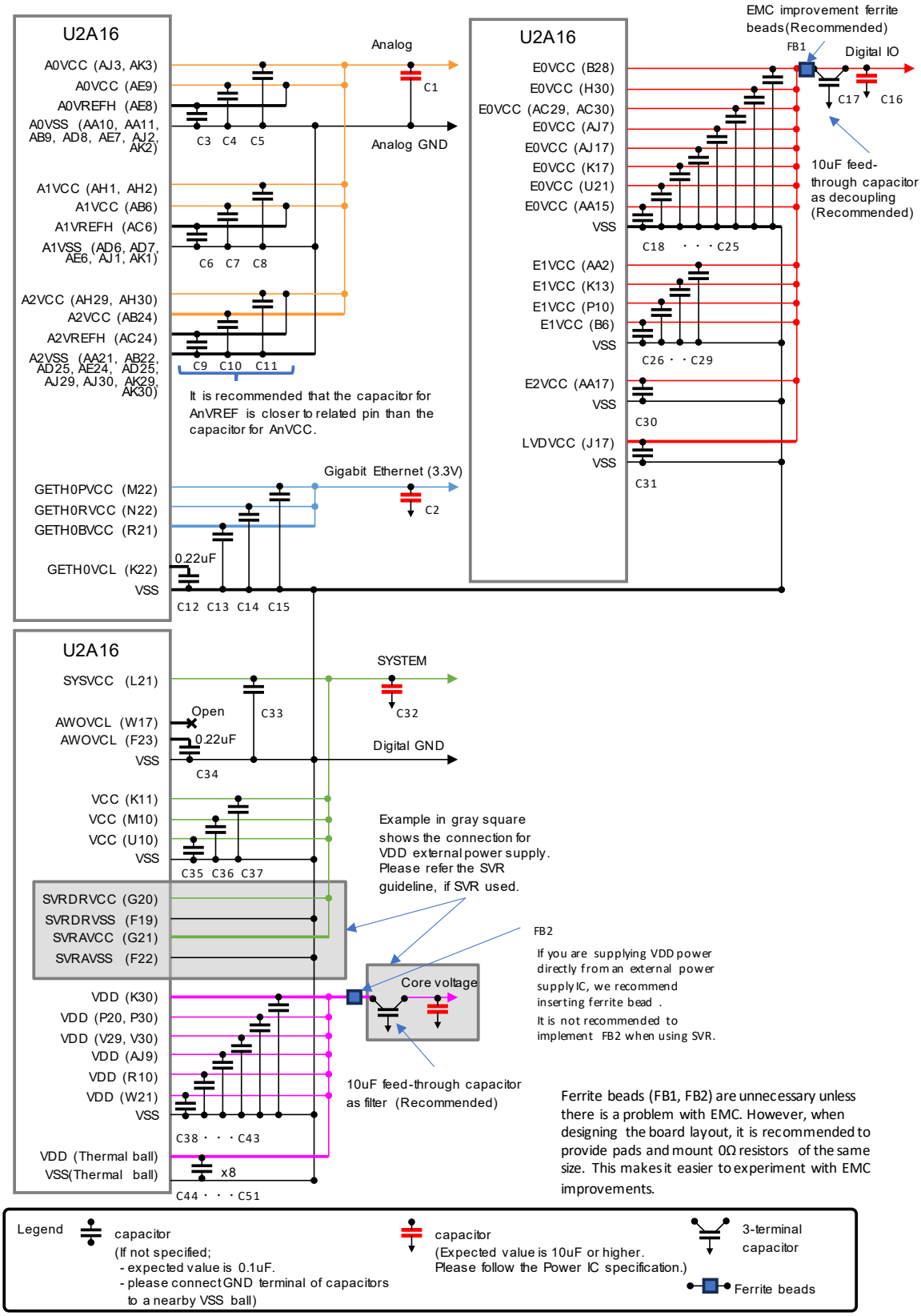
BGA connection VIA is the VIA to connect BGA ball to capacitor. This VIA should not be connected to the inner power/ground layer.

Inner layer connection VIA is the VIA to connect capacitor to inner power/ground layer.



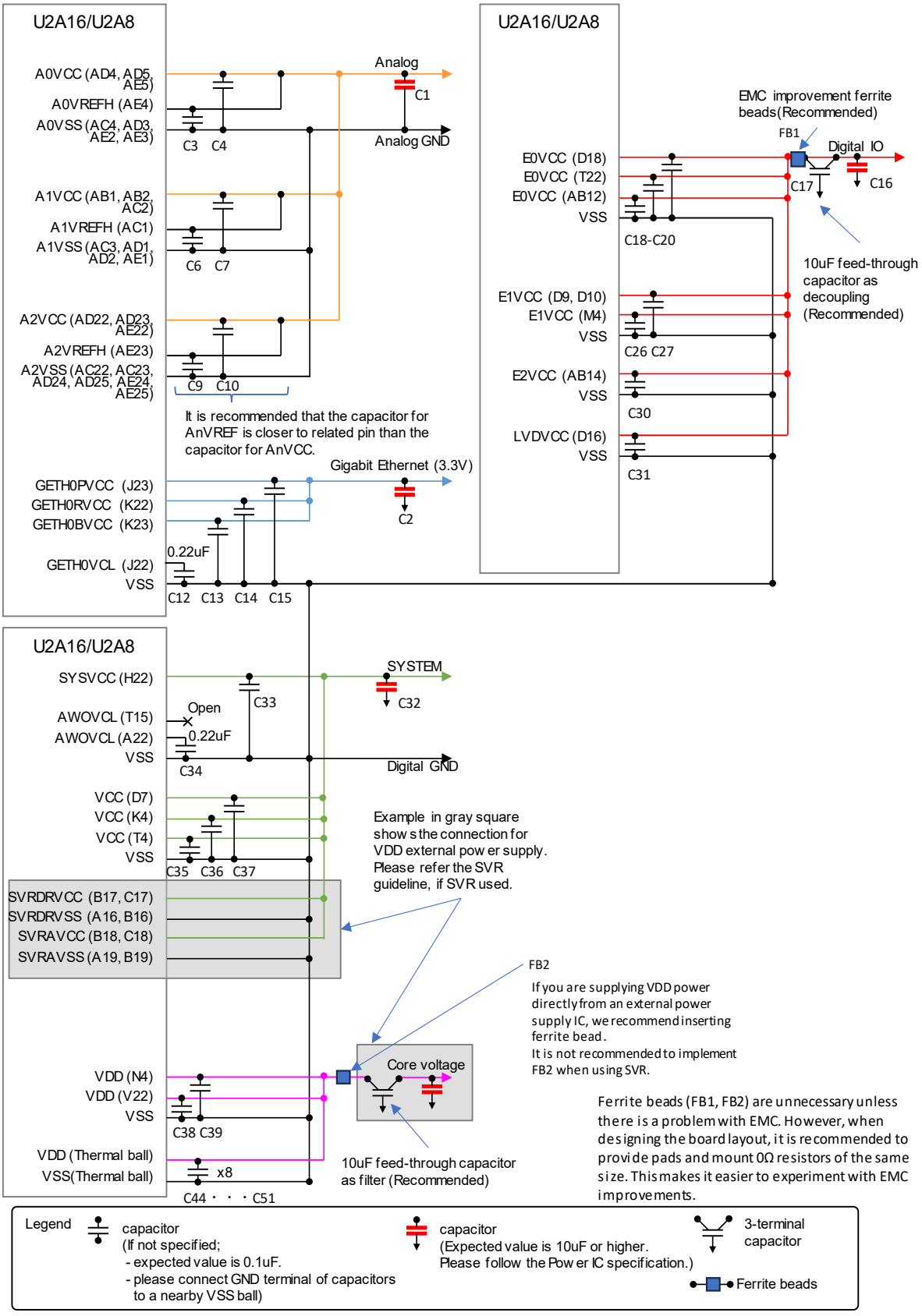
2. Example of capacitor placement

2.1 Example capacitor connection for BGA516 package (U2A16)



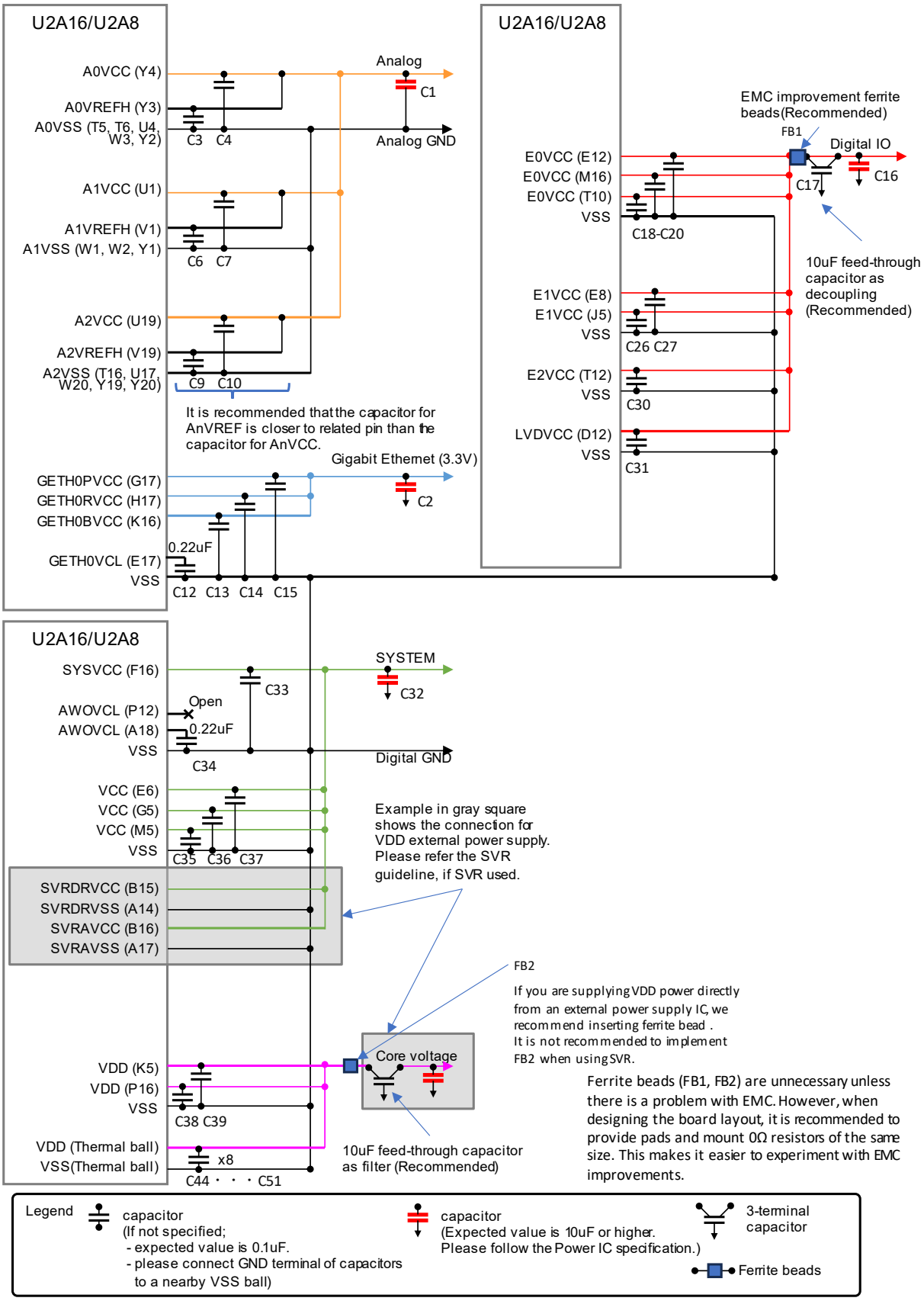
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.2 Example capacitor connection for BGA373 package (U2A16/U2A8)



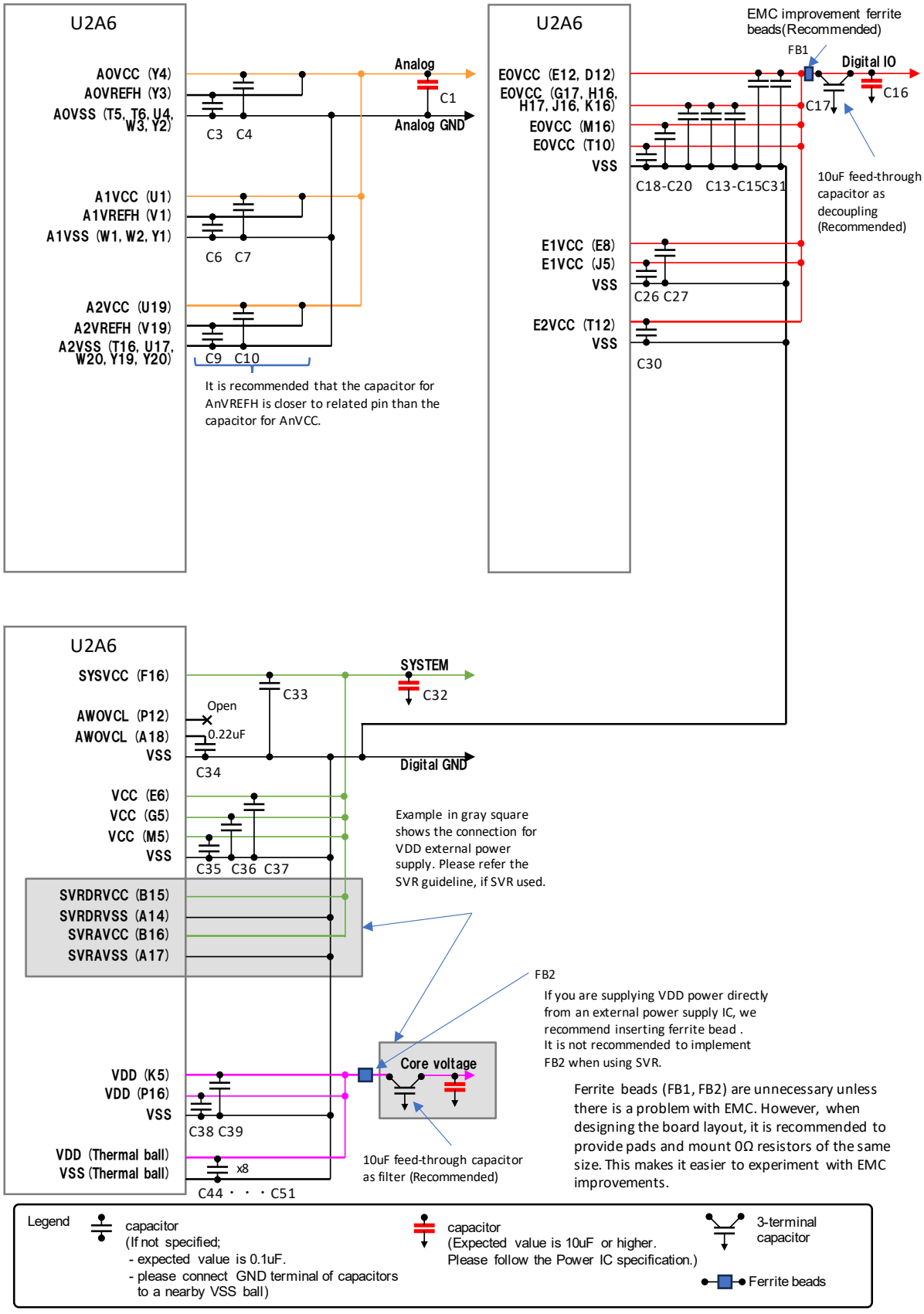
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.3 Example capacitor connection for BGA292 package (U2A16/U2A8)



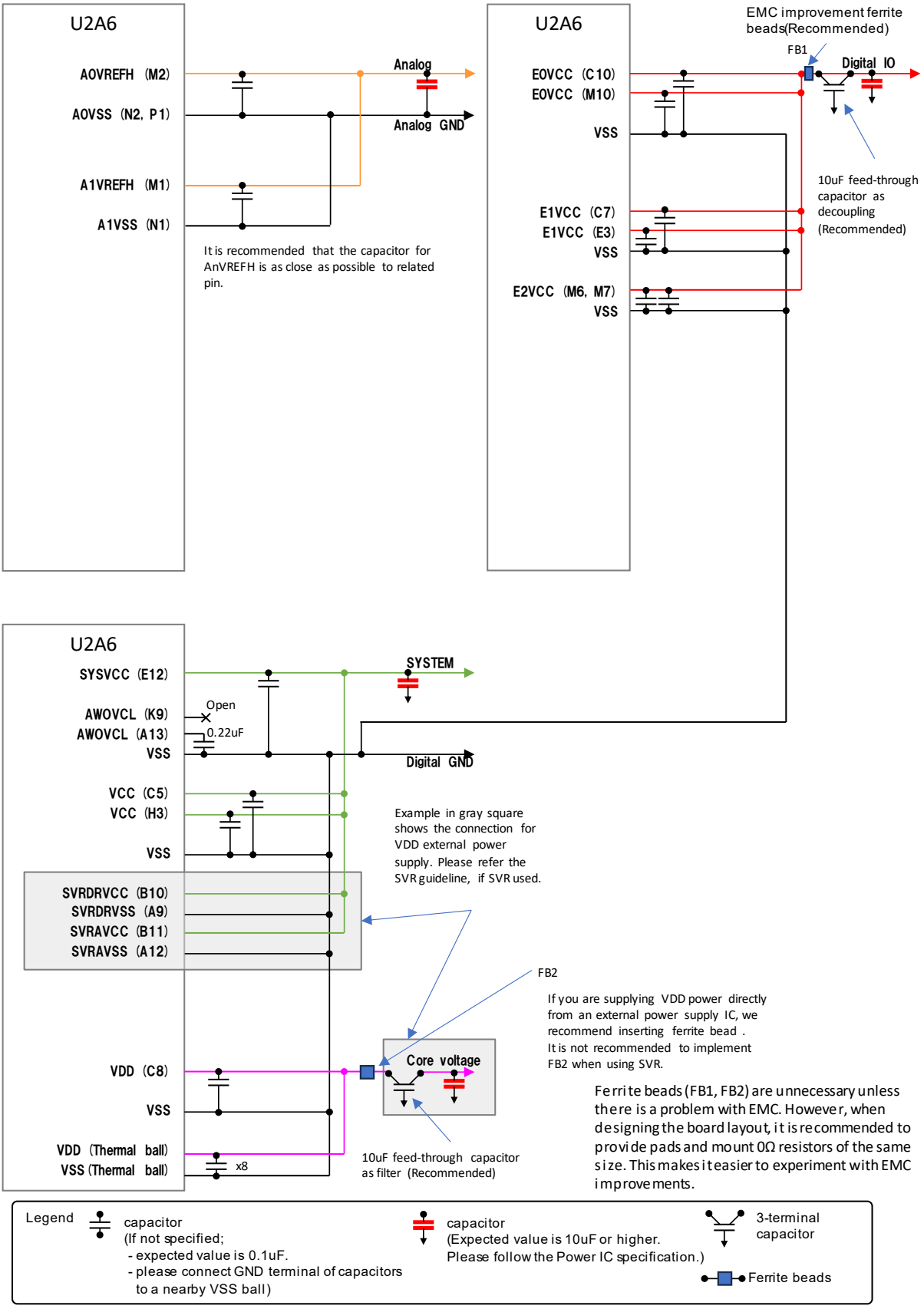
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.4 Example capacitor connection for BGA292 package (U2A6)



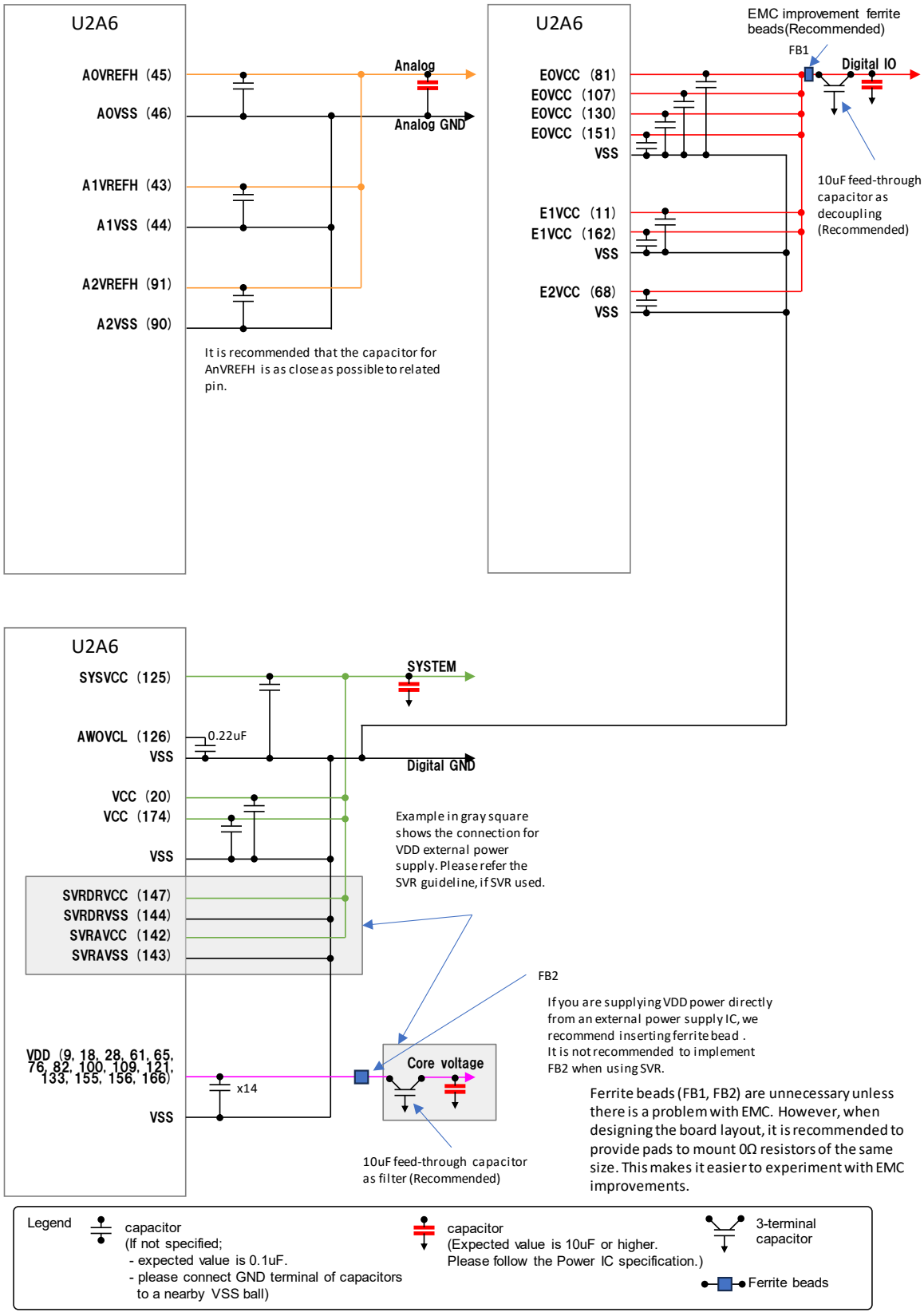
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.5 Example capacitor connection for BGA156 package (U2A6)



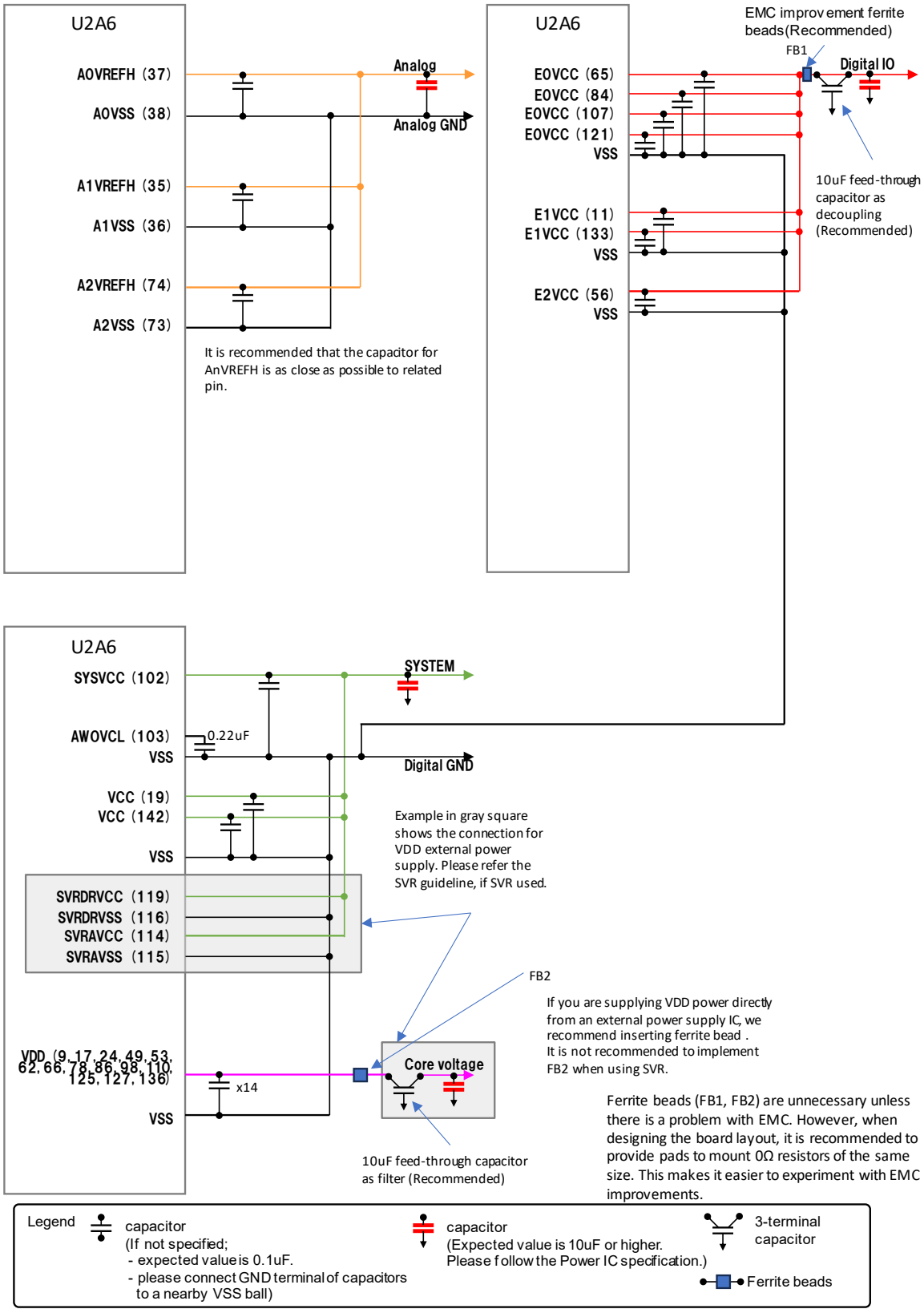
Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

2.6 Example capacitor connection for HLQFP176 package (U2A6)



Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

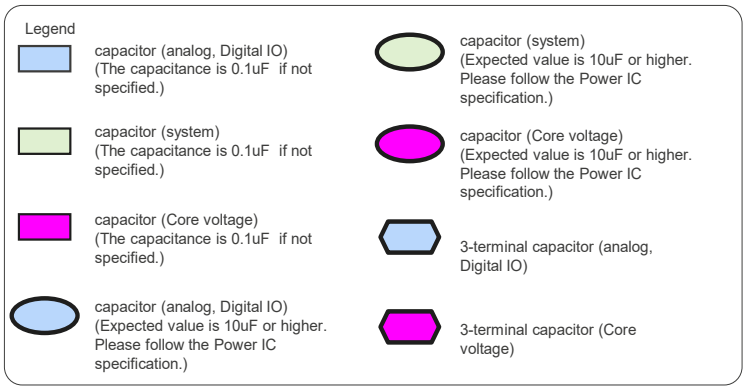
2.7 Example capacitor connection for HLQFP144 package (U2A6)

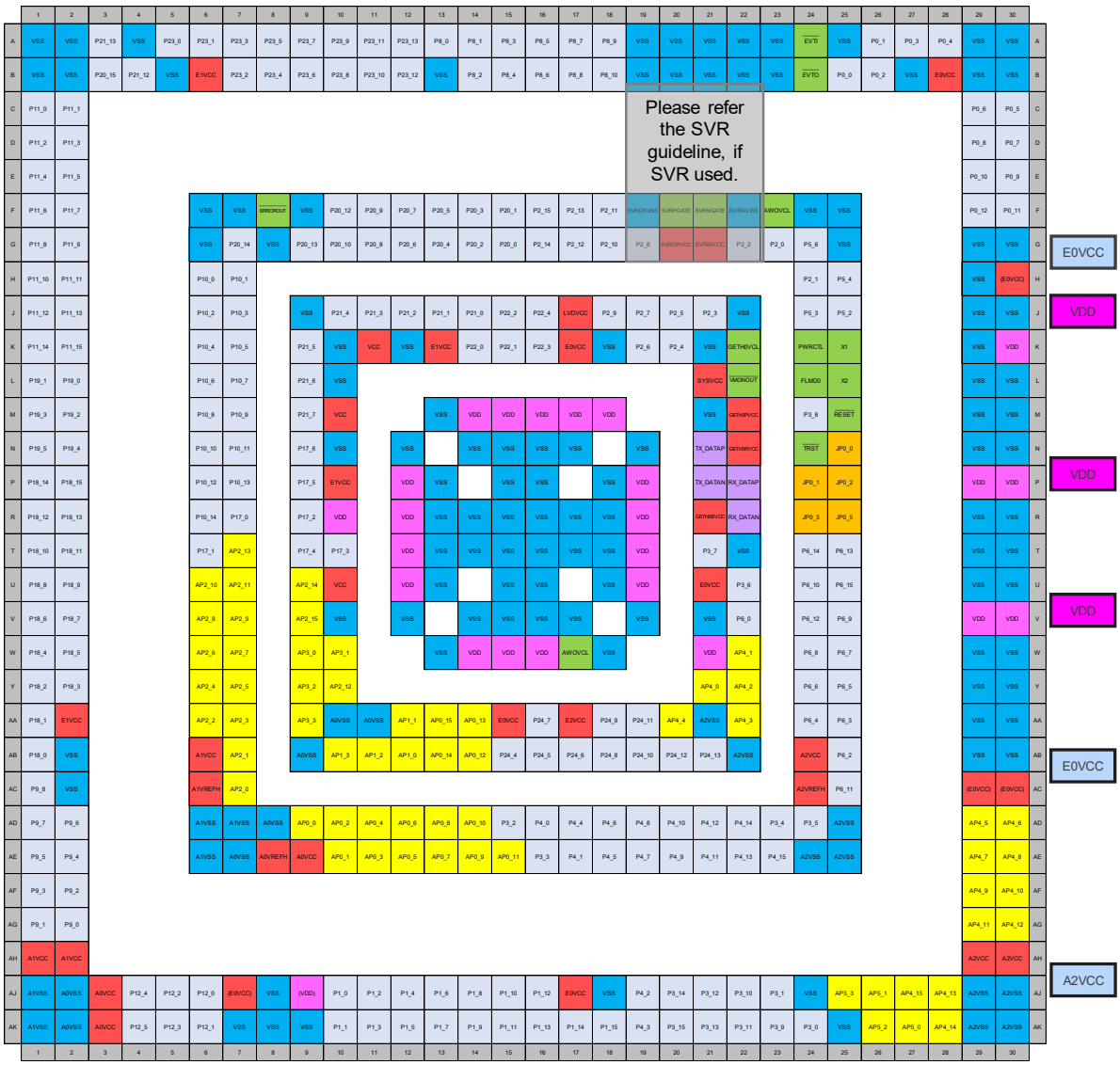


Reference: Regarding the VDD capacitors, if the emission characteristics worsen due to resonance at a specific frequency, it may be improved by changing the capacitance within the range of 1nF to 1uF.

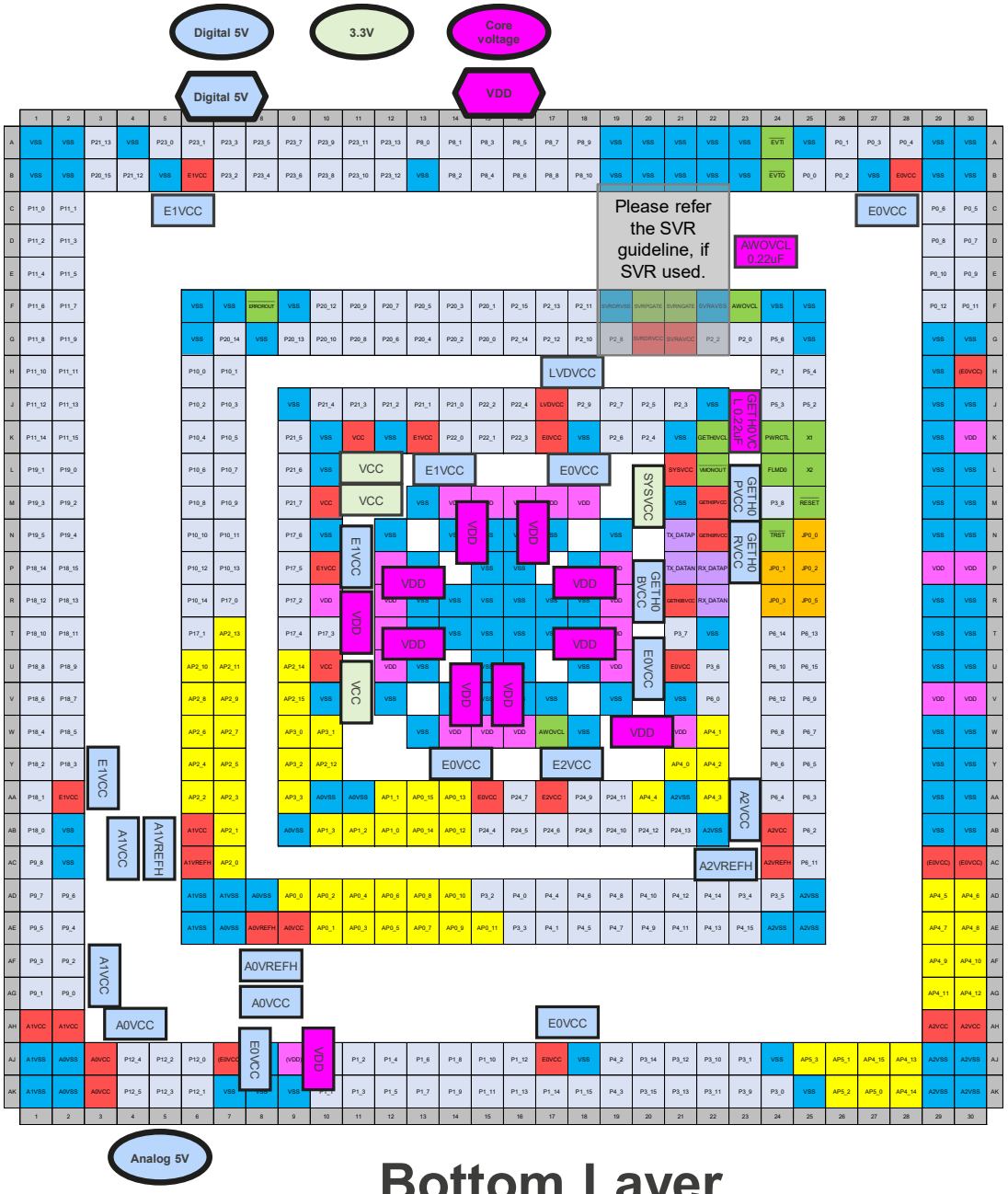
3. PCB layout guidelines -Top layer / Bottom layer-

3.1 Example capacitor placement for BGA516 package (U2A16)





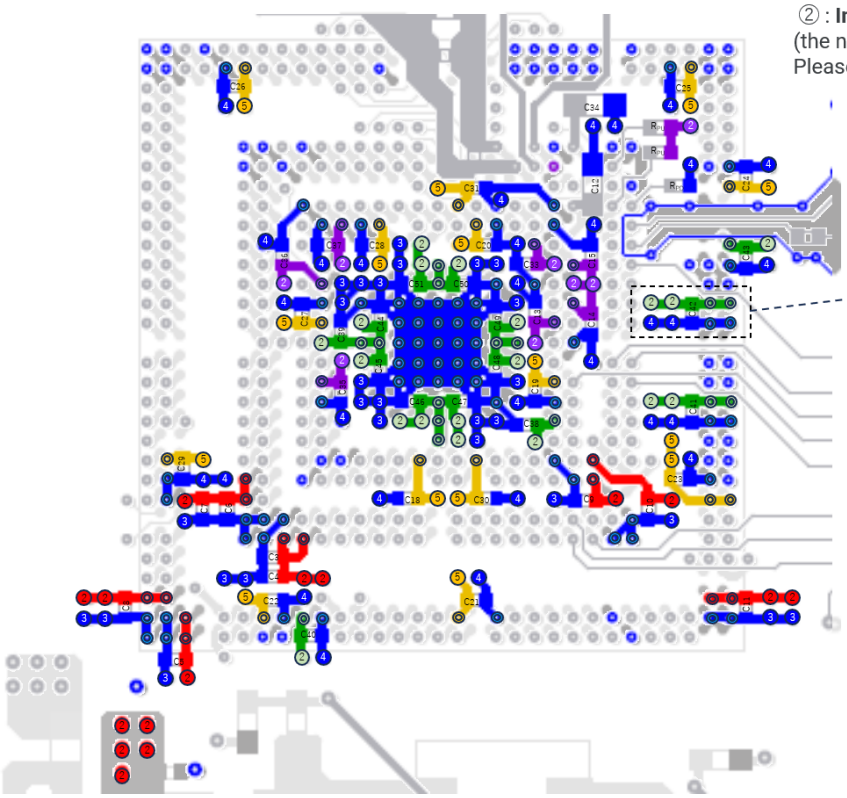
Top Layer



Bottom Layer

BGA516 Bypass capacitor and VIA placement

◎ : **BGA connection VIA**
② : **Inner layer connection VIA**
(the number is the destination layer number)
Please see the section 1.4 for the detail of capacitor connection.



Legend

Connect from the 2nd layer (VDD layer) to the 1st layer BGA PAD through the bypass capacitor (C42) on the 6th layer.

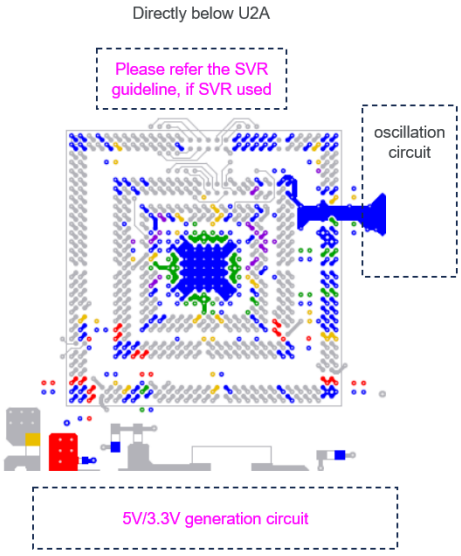
From the BGA PAD on the 1st layer, pass through the bypass capacitor (C42) on the 6th layer and return to the 4th layer (GND)

green：VDD
purple：System(VCC/SYSVCC) power supply
GigabitEthernet power supply[3.3V]
red：Analog(AxVCC) power supply[5V]
yellow：Digital IO(ExVCC) power supply[5V]
blue：VSS

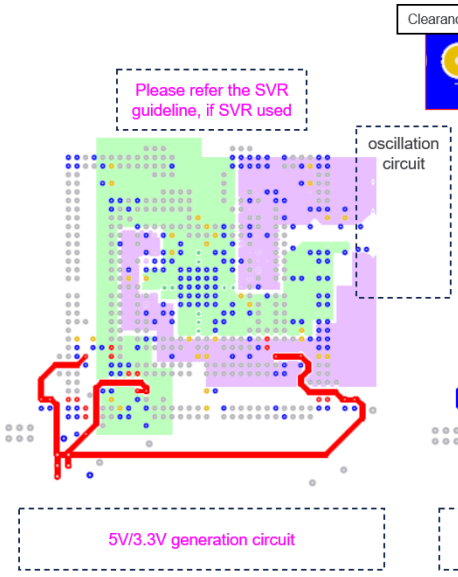
R_{PU}：pull up resistance
R_{PD}：pull down resistance

The 1st and 6th layers are displayed superimposed (color is the 6th layer)

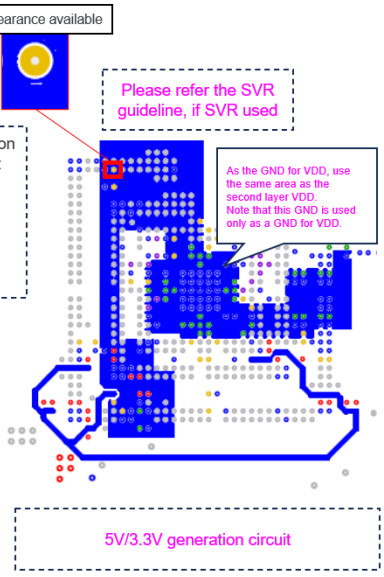
BGA516 1st layer

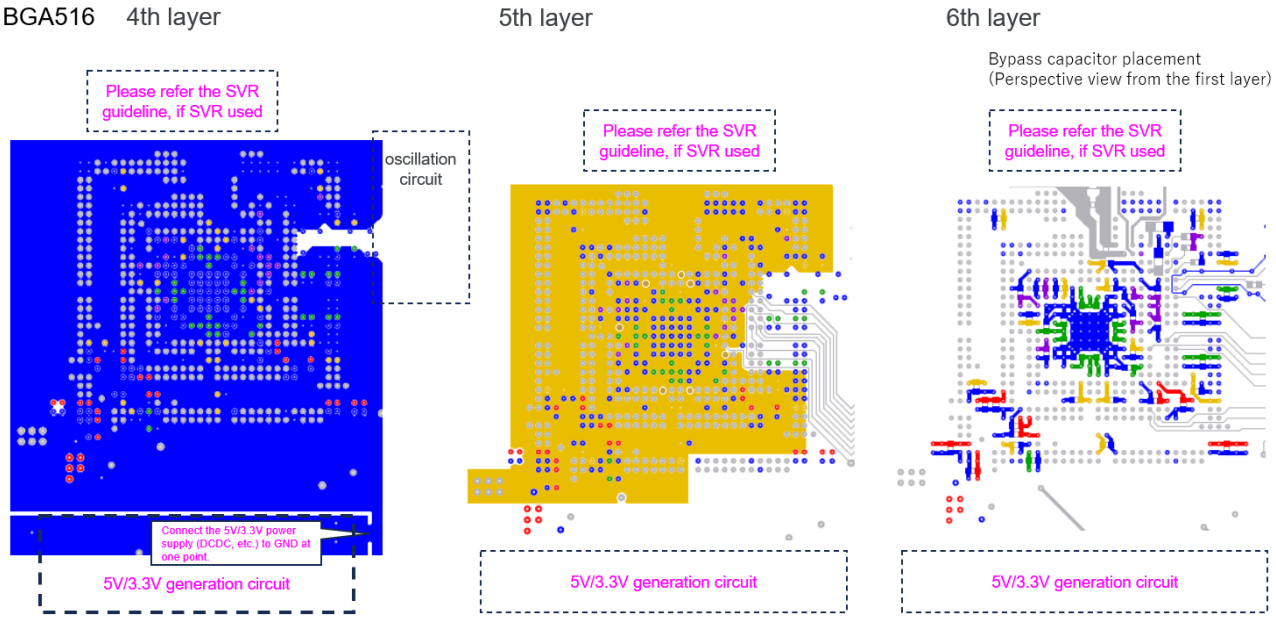


2nd layer

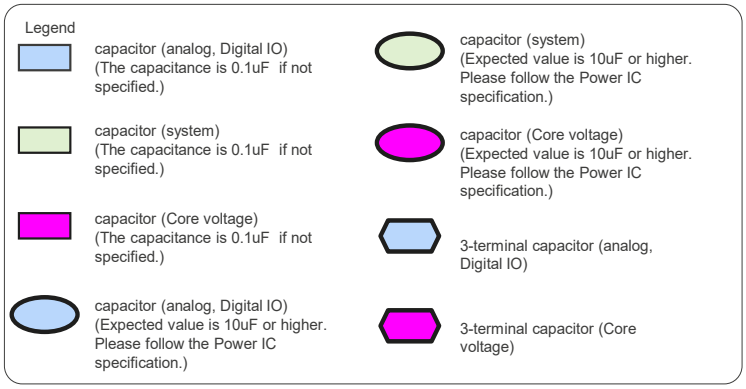


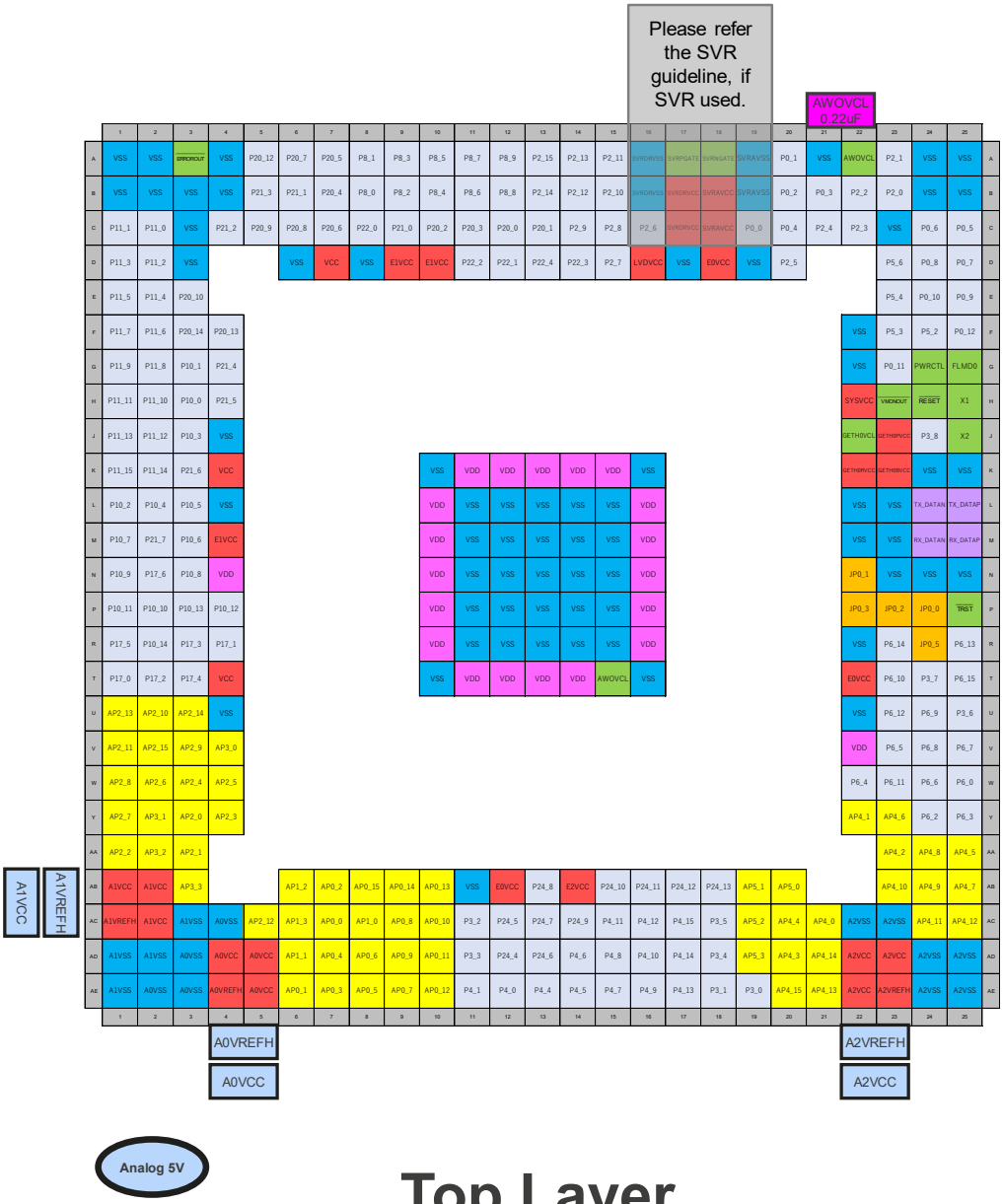
3rd layer



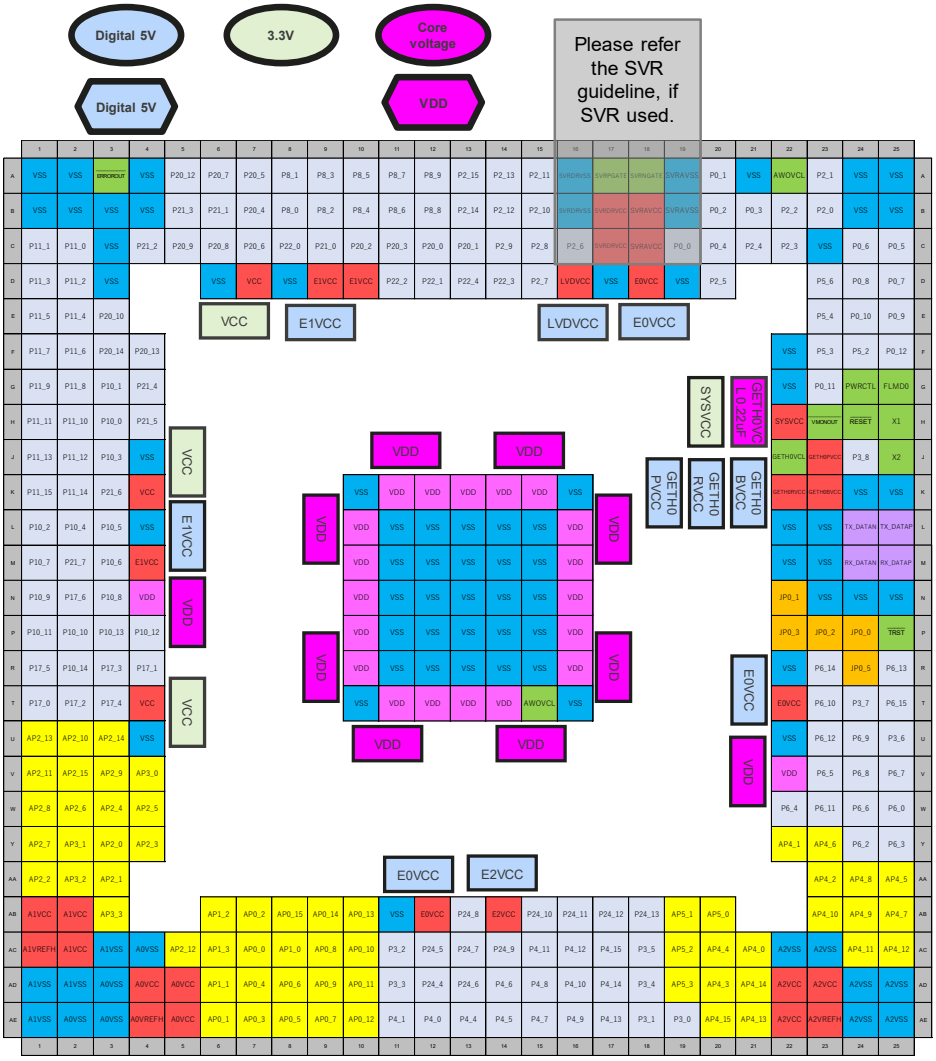

BGA516
4th layer
5th layer
6th layer
Bypass capacitor placement
(Perspective view from the first layer)
Please refer the SVR guideline, if SVR used
oscillation circuit
Please refer the SVR guideline, if SVR used
Please refer the SVR guideline, if SVR used
Connect the 5V/3.3V power supply (DCDC, etc.) to GND at one point.
5V/3.3V generation circuit
5V/3.3V generation circuit
5V/3.3V generation circuit

3.2 Example capacitor placement for BGA373 package (U2A16/U2A8)





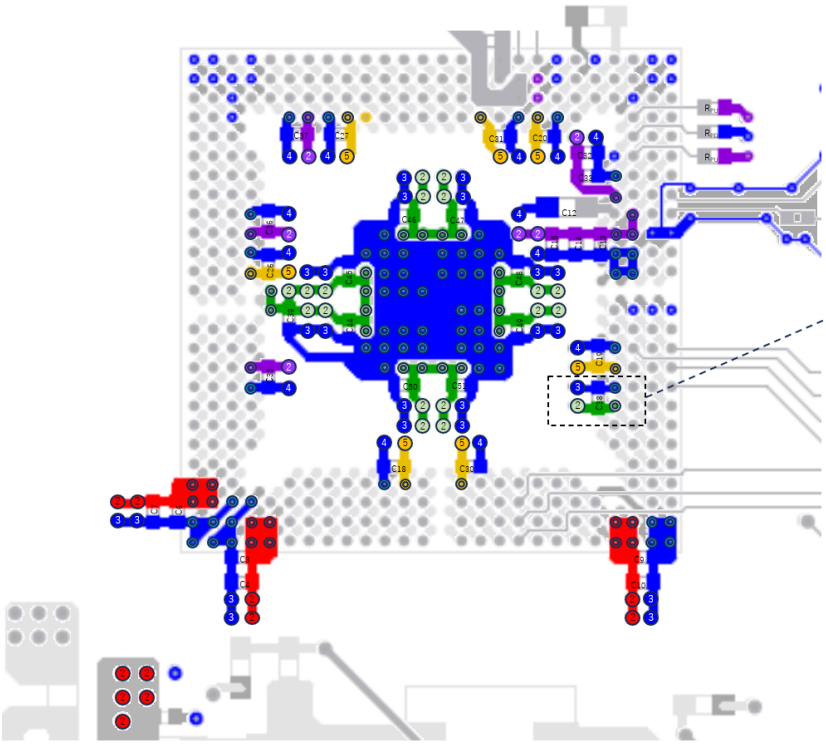
Top Layer



Bottom Layer

BGA373 Bypass capacitor and VIA placement

◎ : **BGA connection VIA**
② : **Inner layer connection VIA**
(the number is the destination layer number)
Please see the section 1.4 for the detail of capacitor connection.



Legend

From the BGA PAD on the 1st layer,
it passes through the bypass capacitor (C38) on the 6th layer
and returns to the 3rd layer (VSS).

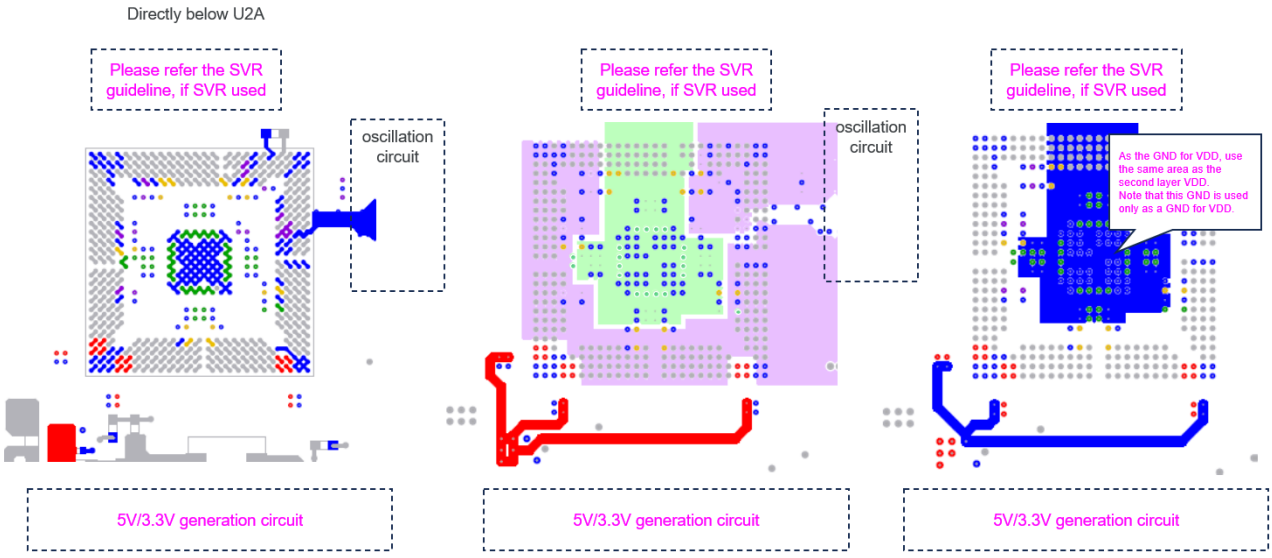
Connect from the 2nd layer (VDD layer) to the 1st layer BGA PAD
through the bypass capacitor (C38) on the 6th layer.

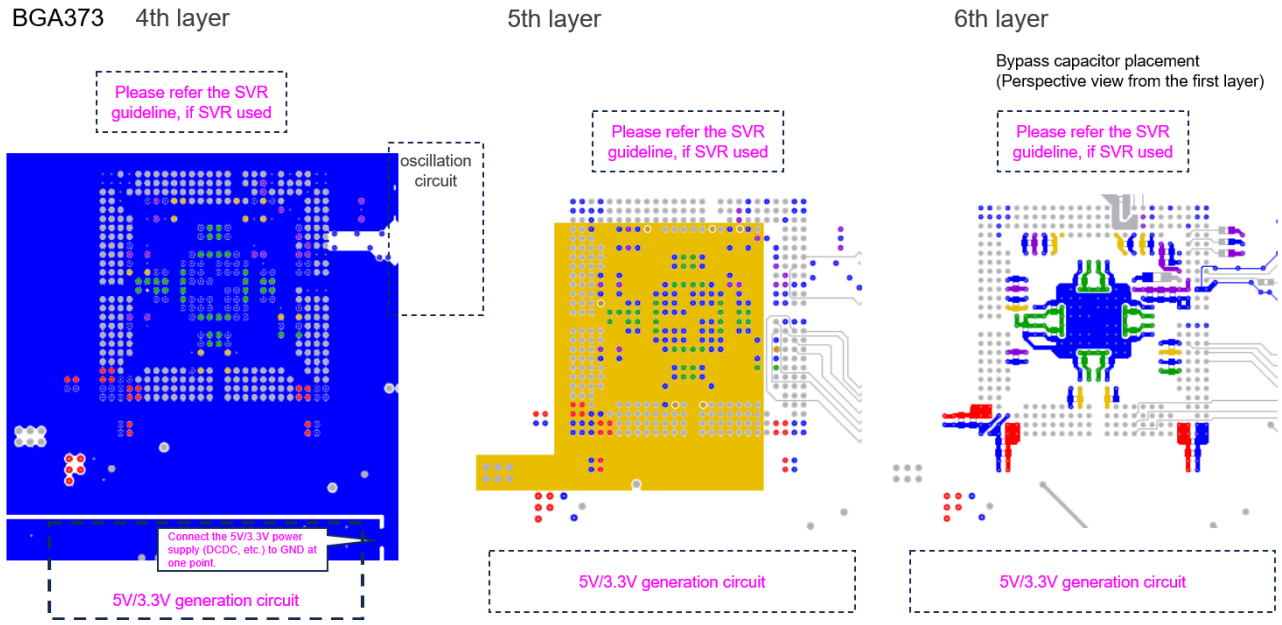
green：VDD
purple：System(VCC/SYSVCC) power supply
GigabitEthernet power supply[3.3V]
red：Analog(AxVCC) power supply[5V]
yellow：Digital IO(ExVCC) power supply[5V]
blue：VSS

R_{PU}：pull up resistance
R_{PD}：pull down resistance

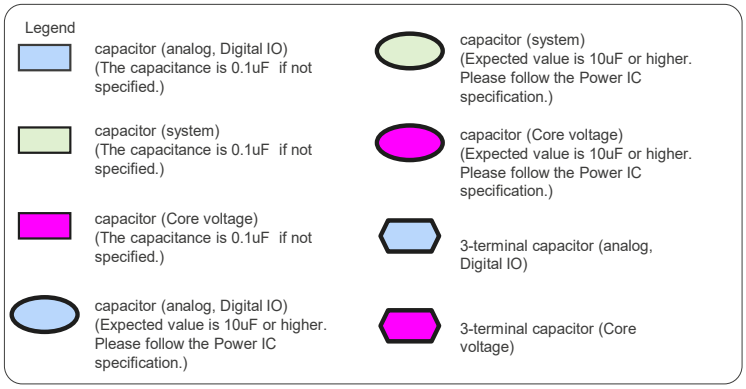
The 1st and 6th layers are displayed superimposed (color is the 6th layer)

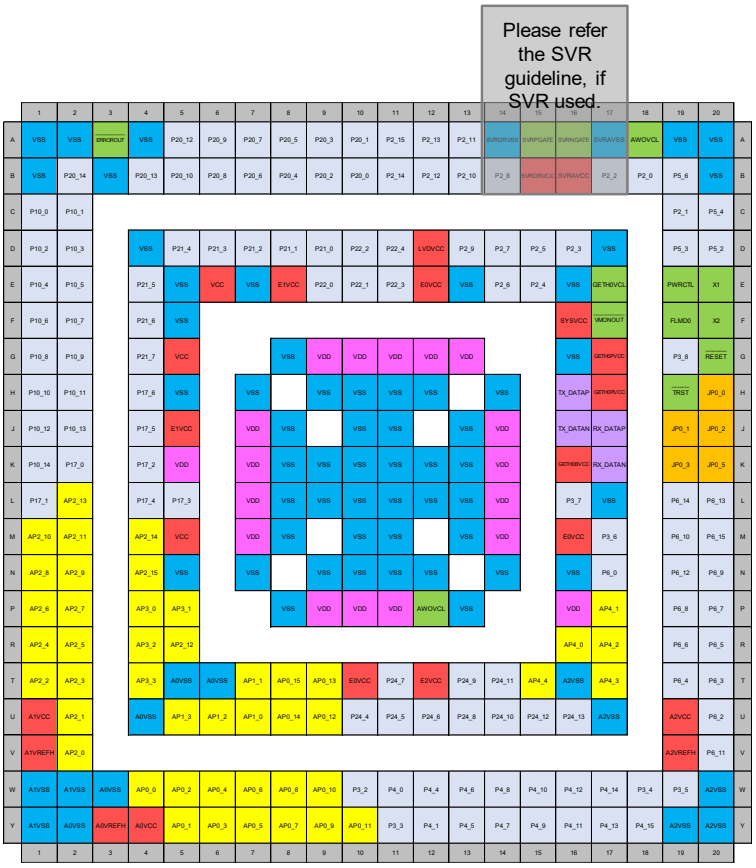
BGA373 1st layer 2nd layer 3rd layer



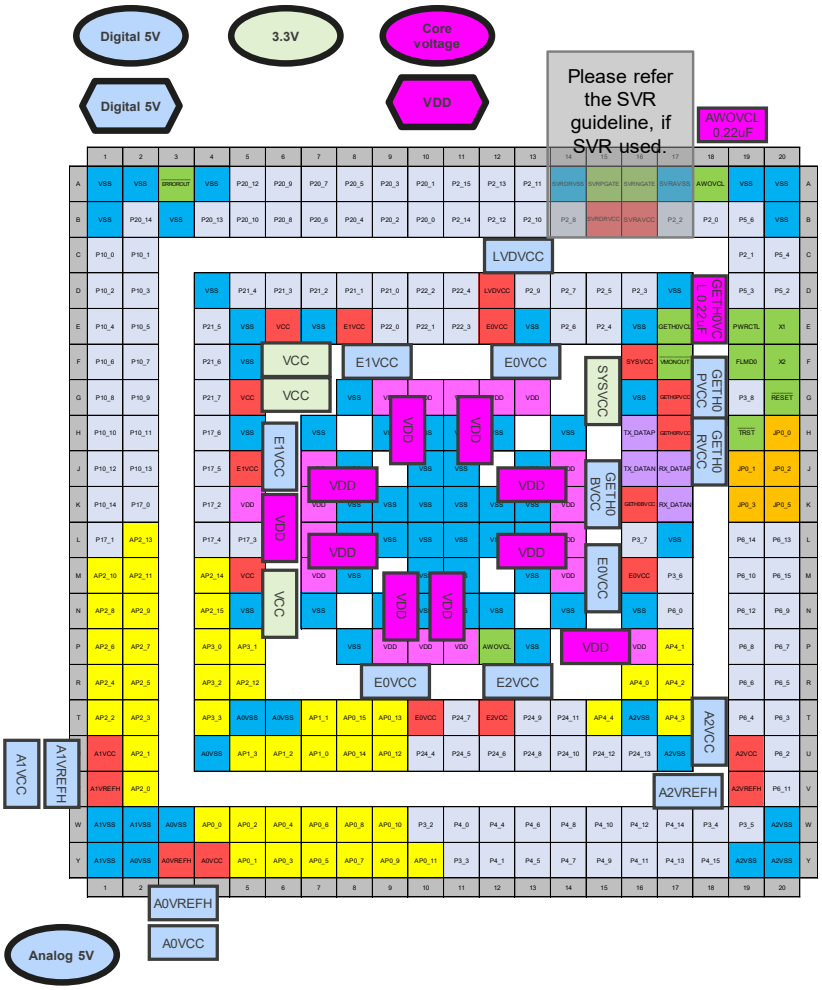

BGA373
4th layer
5th layer
6th layer
Please refer the SVR guideline, if SVR used
oscillation circuit
Connect the 5V/3.3V power supply (DCDC, etc.) to GND at one point.
5V/3.3V generation circuit
Please refer the SVR guideline, if SVR used
5V/3.3V generation circuit
Bypass capacitor placement
(Perspective view from the first layer)
Please refer the SVR guideline, if SVR used
5V/3.3V generation circuit

3.3 Example capacitor placement for BGA292 package (U2A16/U2A8)





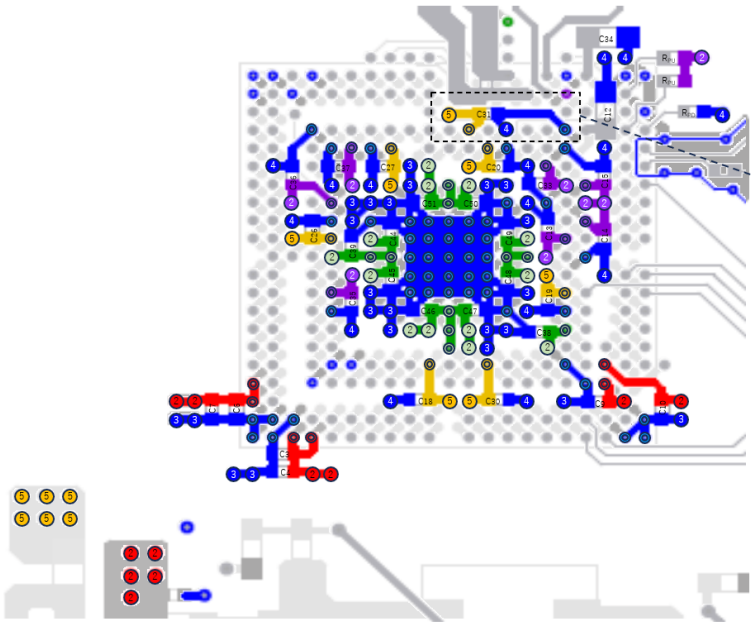
Top Layer

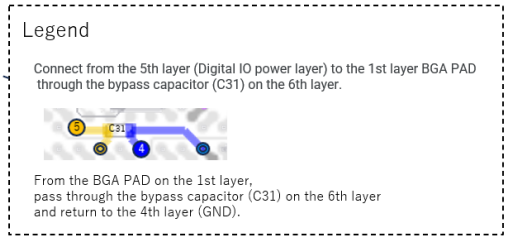


Bottom Layer

BGA292 Bypass capacitor and VIA placement

◎ : **BGA connection VIA**
② : **Inner layer connection VIA**
(the number is the destination layer number)
Please see the section 1.4 for the detail of capacitor connection.



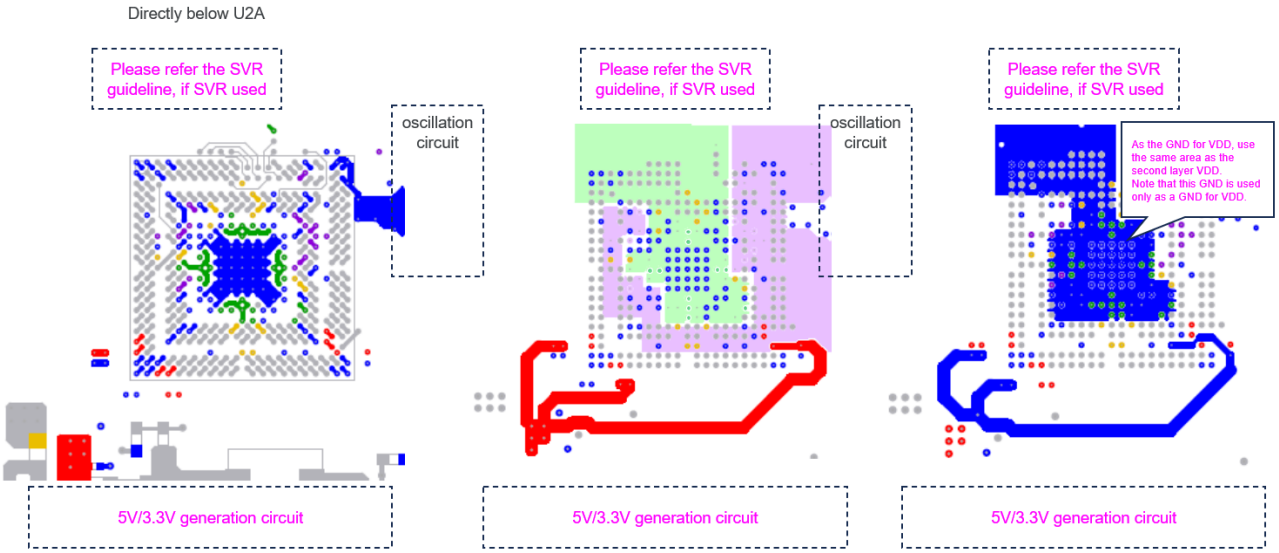


green：VDD
purple：System(VCC/SYSVCC) power supply
GigabitEthernet power supply[3.3V]
red：Analog(AxVCC) power supply[5V]
yellow：Digital IO(ExVCC) power supply[5V]
blue：VSS

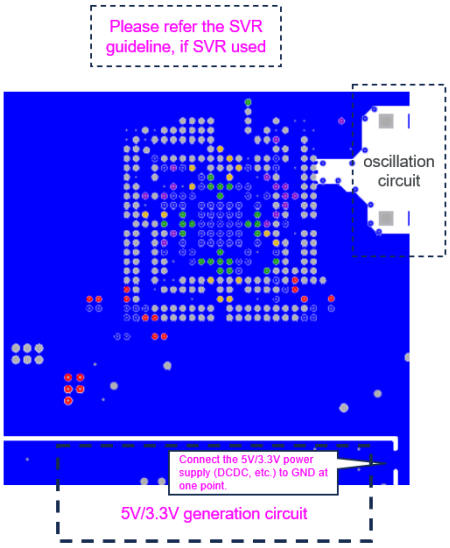
R_{PU}：pull up resistance
R_{PD}：pull down resistance

The 1st and 6th layers are displayed superimposed (color is the 6th layer)

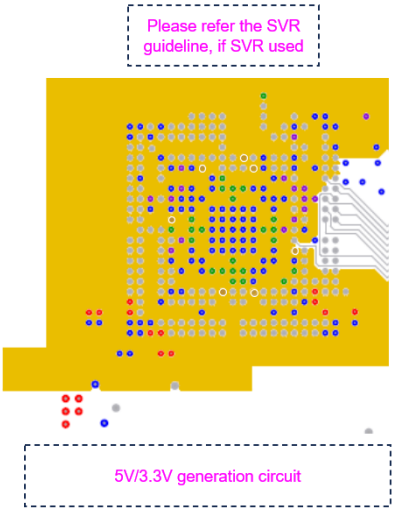
BGA292 1st layer 2nd layer 3rd layer



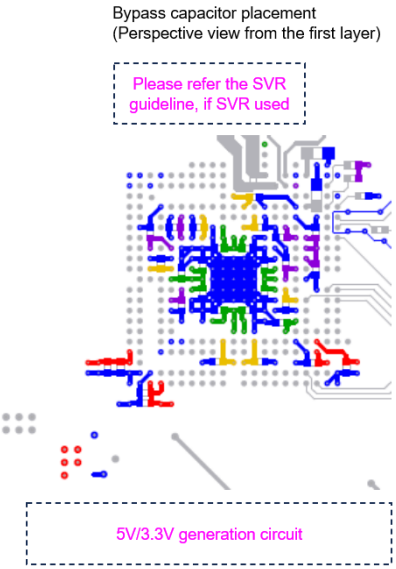
BGA292 4th layer



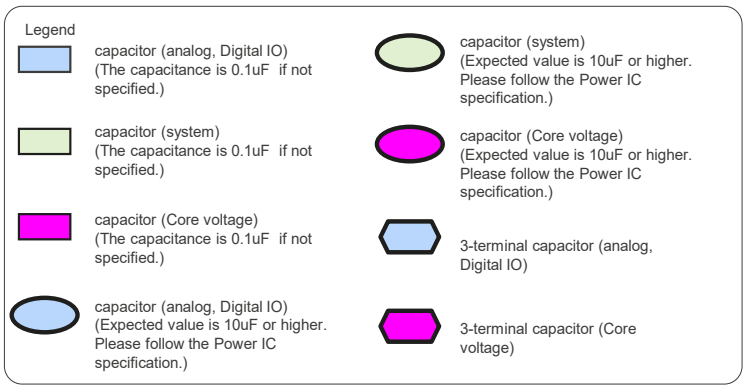
5th layer

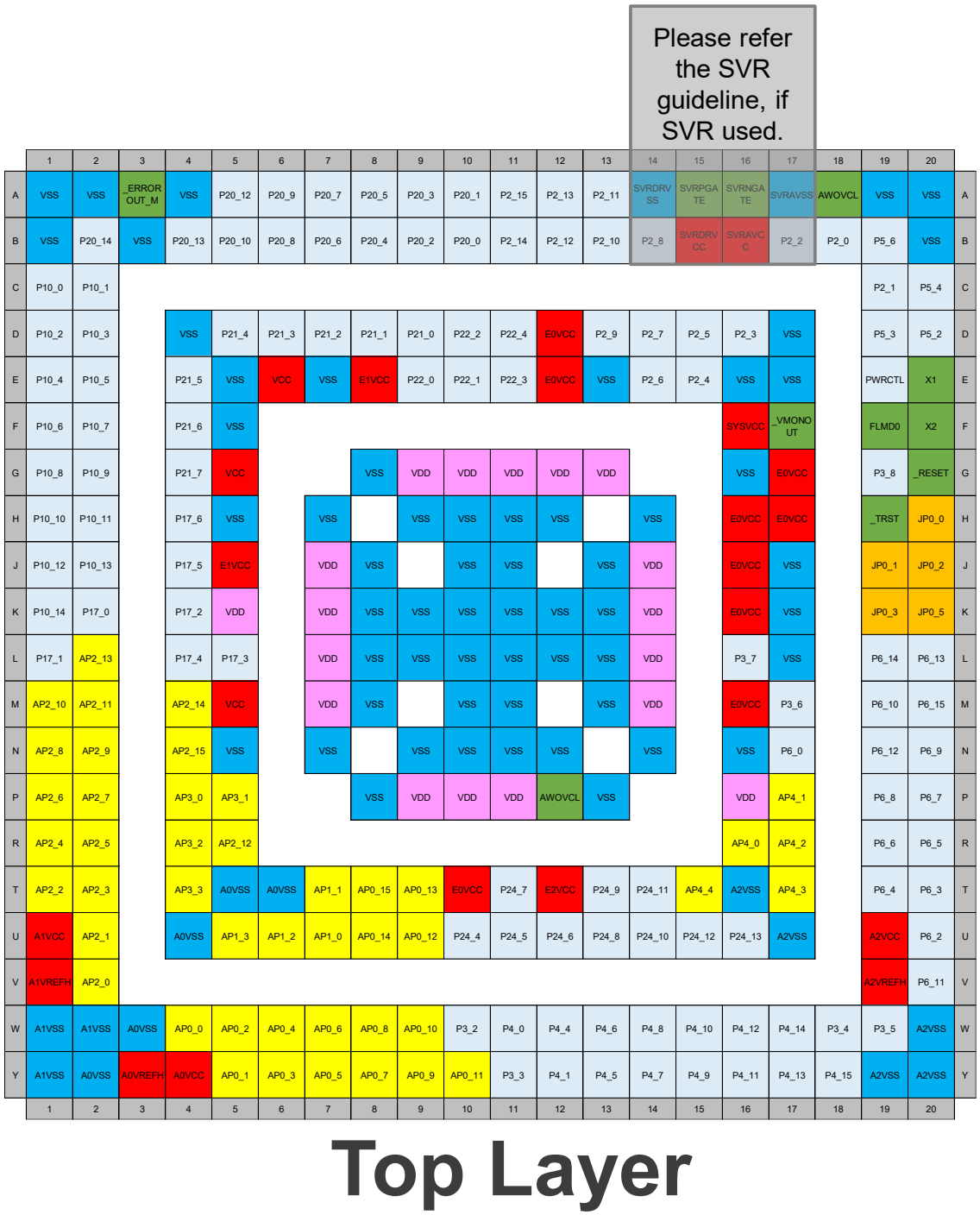


6th layer



3.4 Example capacitor placement for BGA292 package (U2A6)

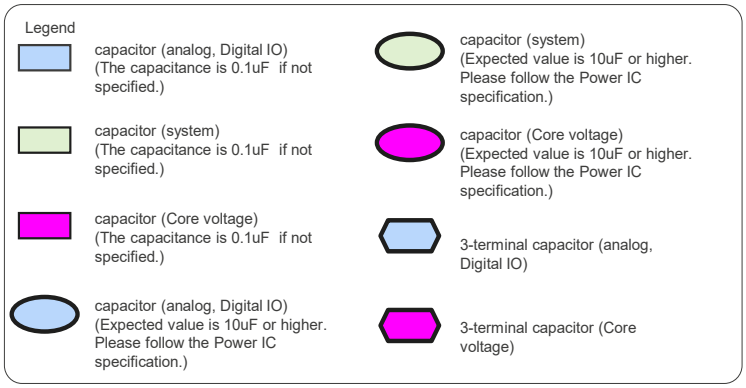


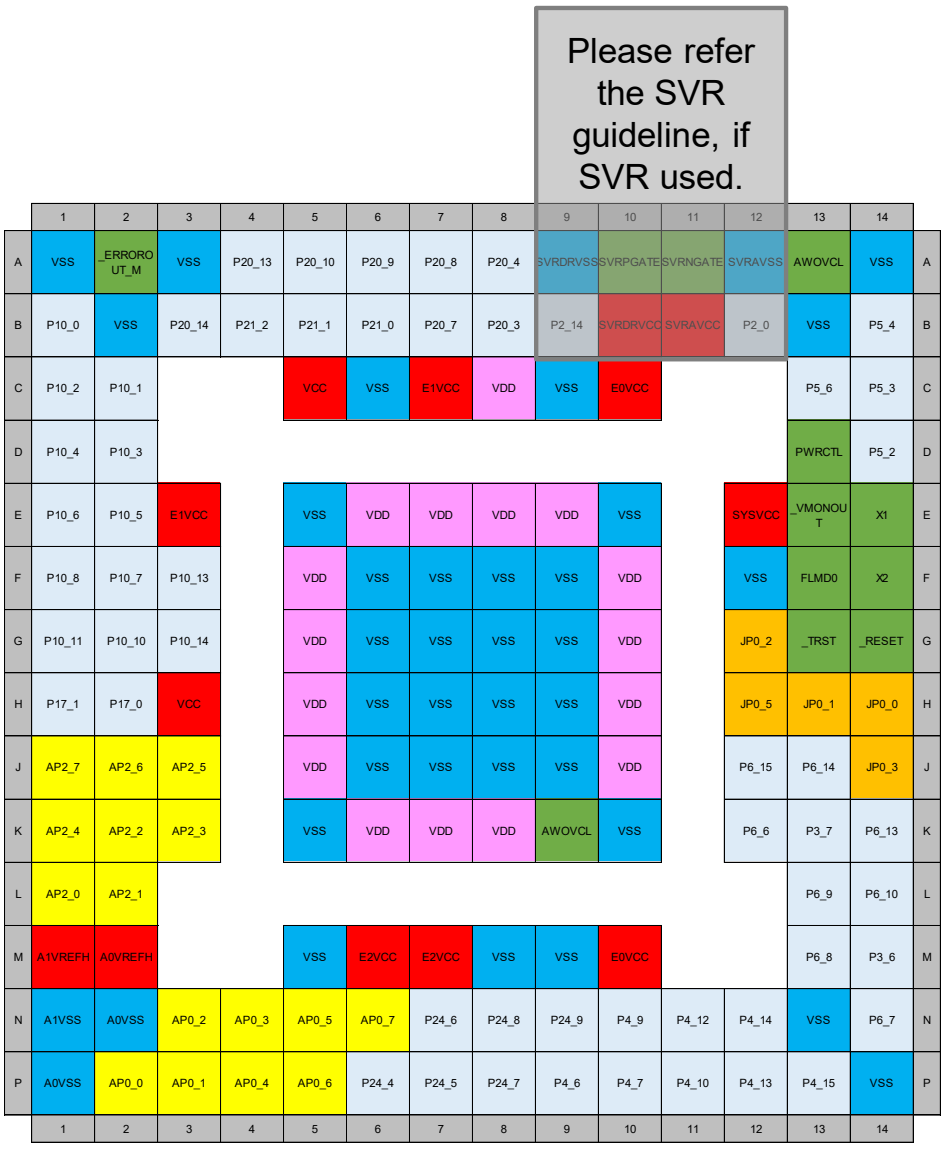


Bottom Layer

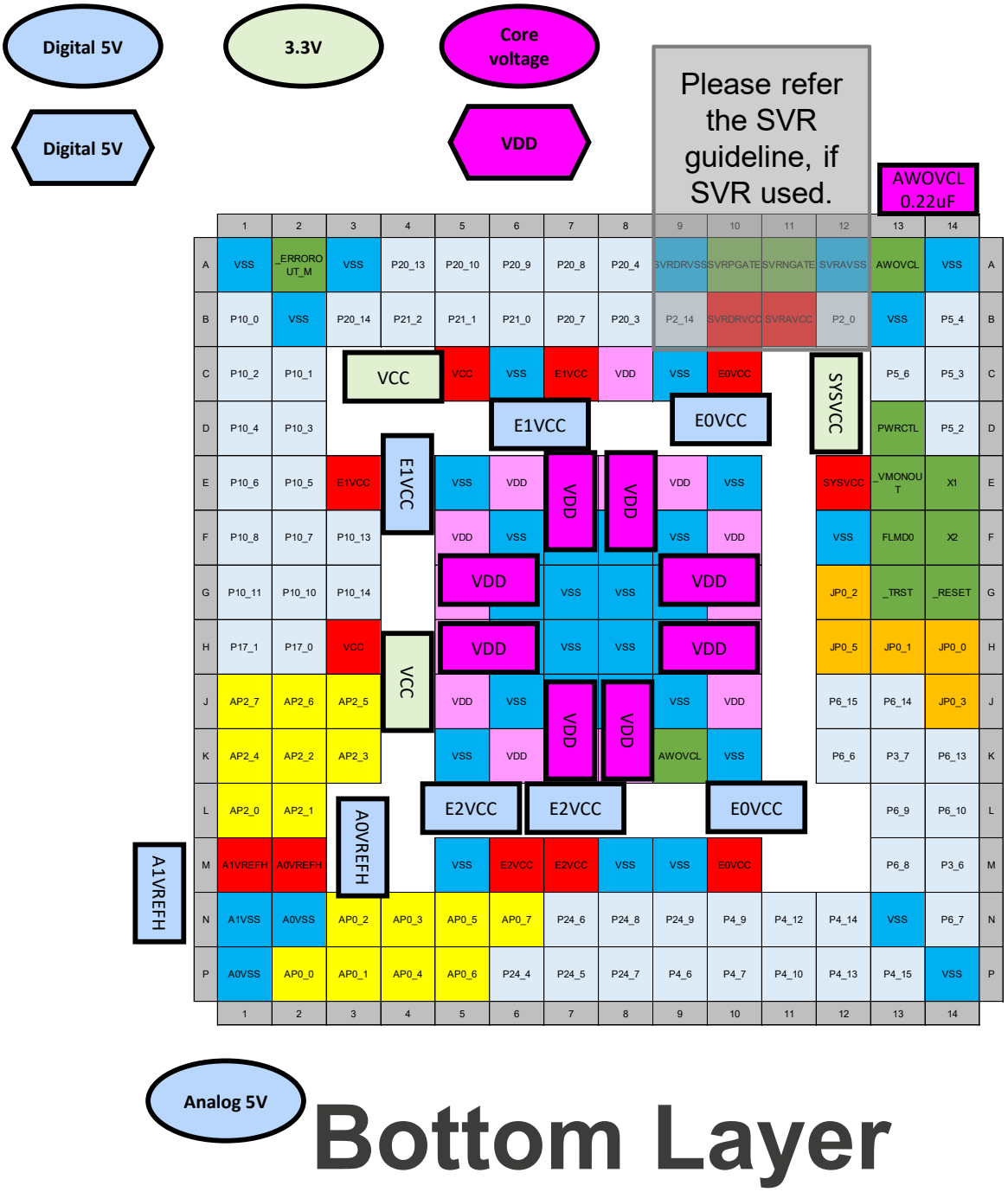
For examples of PCB board design, please refer to "3.3 Example capacitor placement for BGA292 package (U2A16/U2A8)".

3.5 Example capacitor placement for BGA156 package (U2A6)



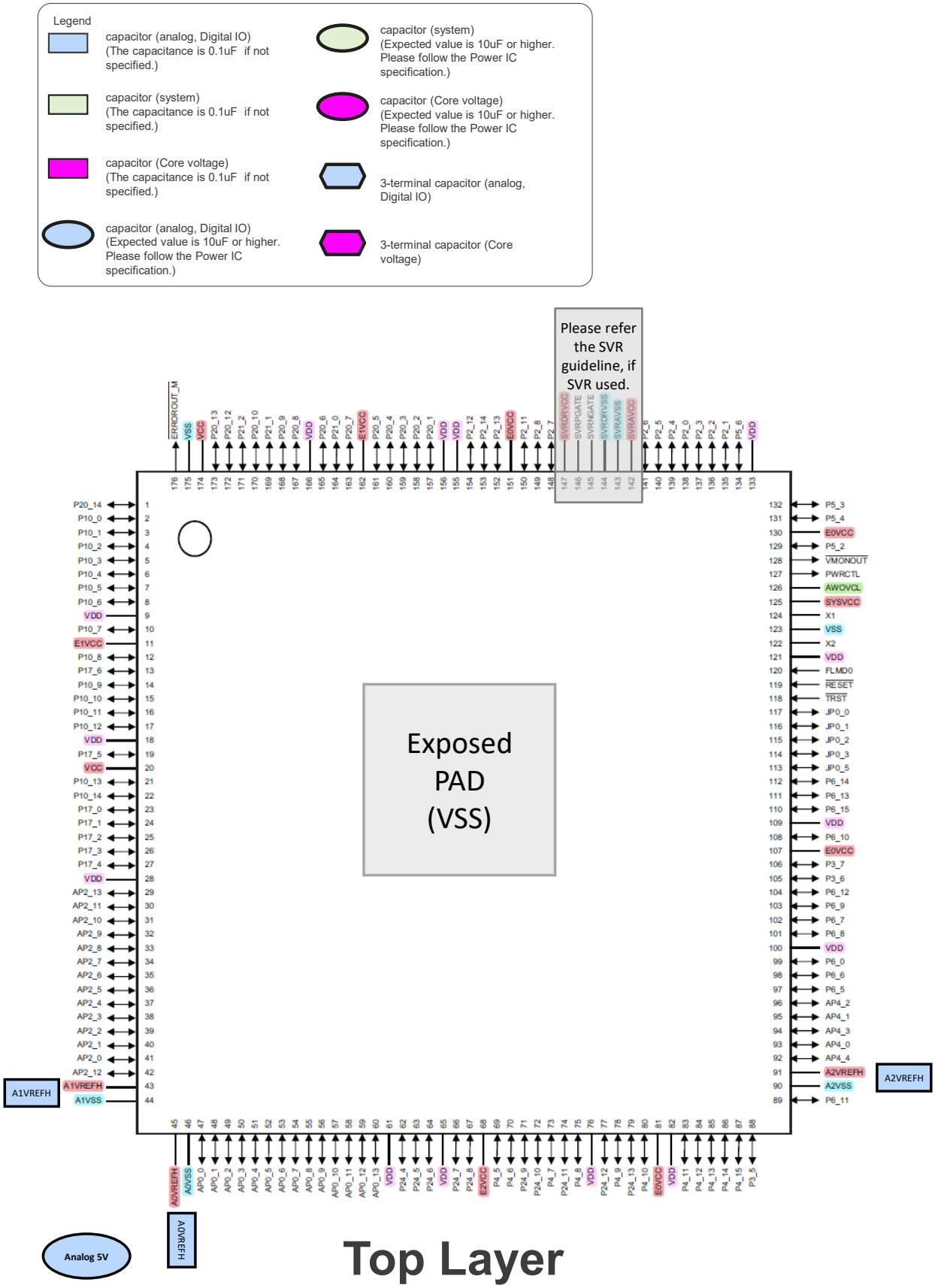


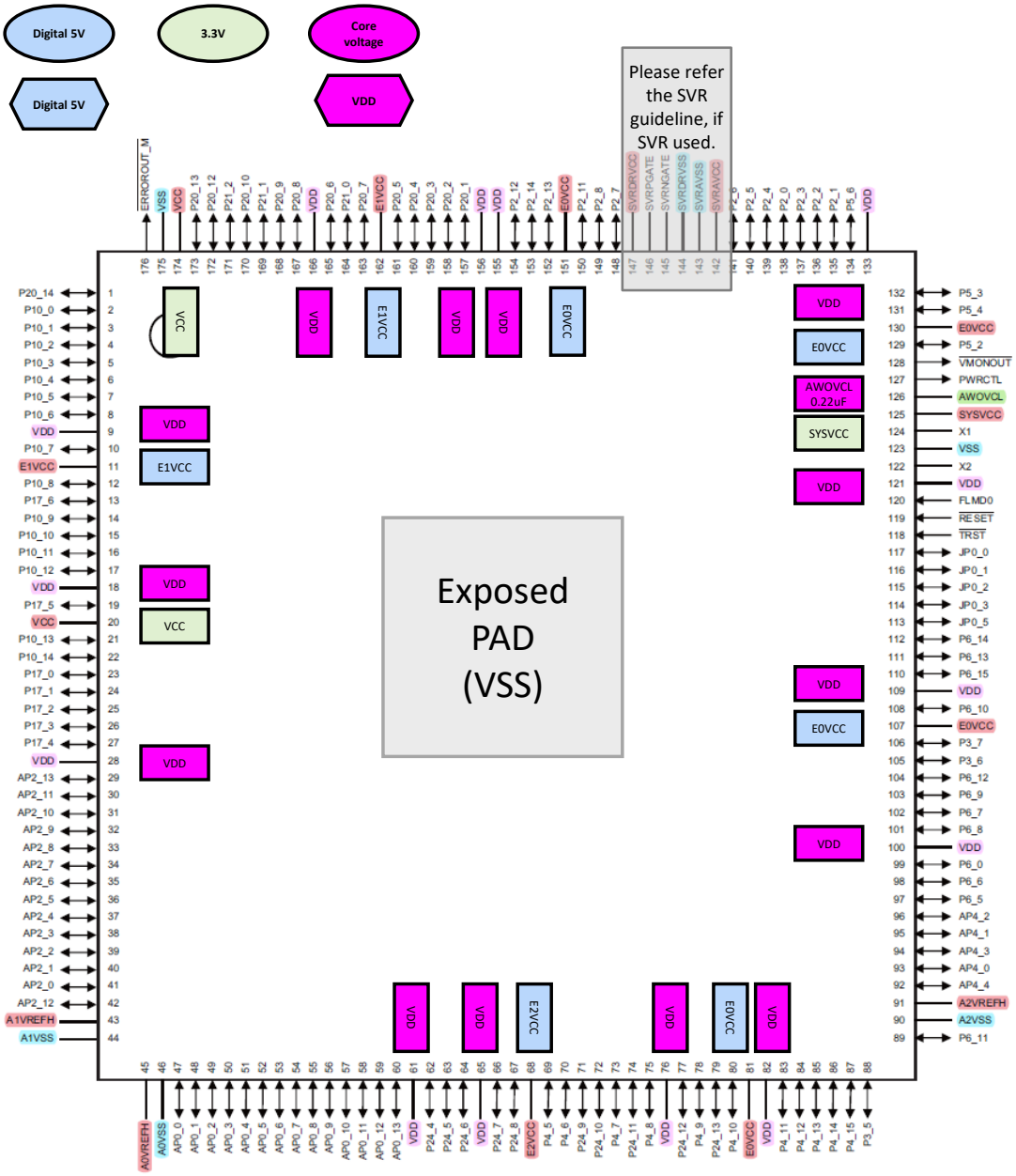
Top Layer



For examples of PCB board design, please refer to "3.3 Example capacitor placement for BGA292 package (U2A16/U2A8)".

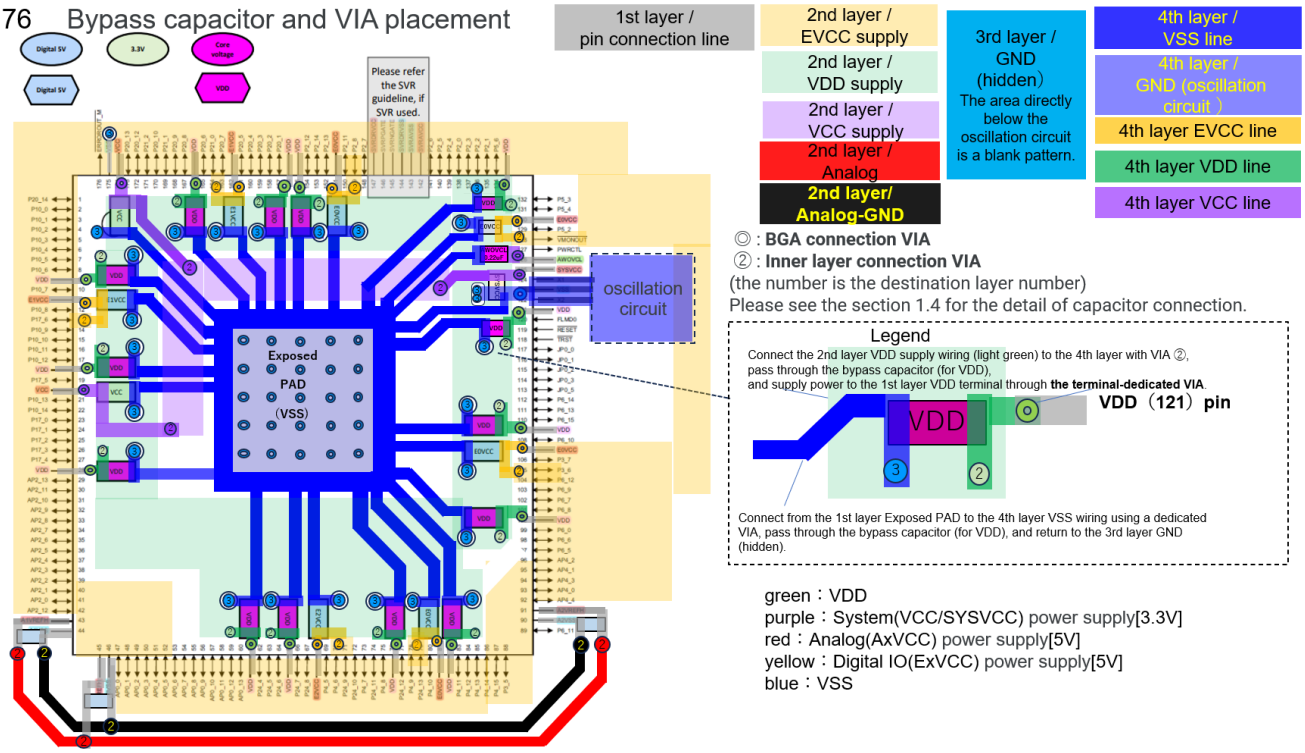
3.6 Example capacitor placement for HLQFP176 package (U2A6)





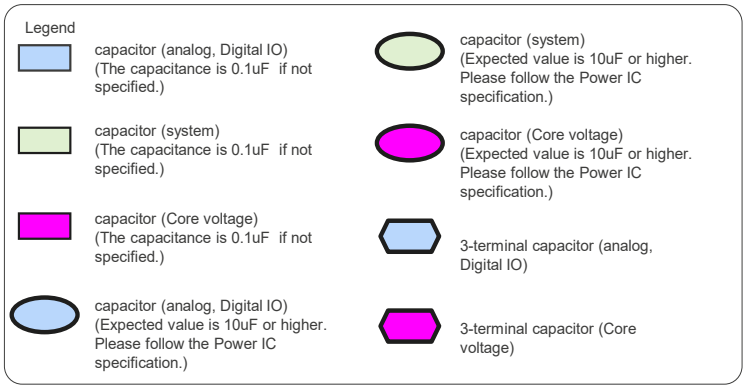
Bottom Layer

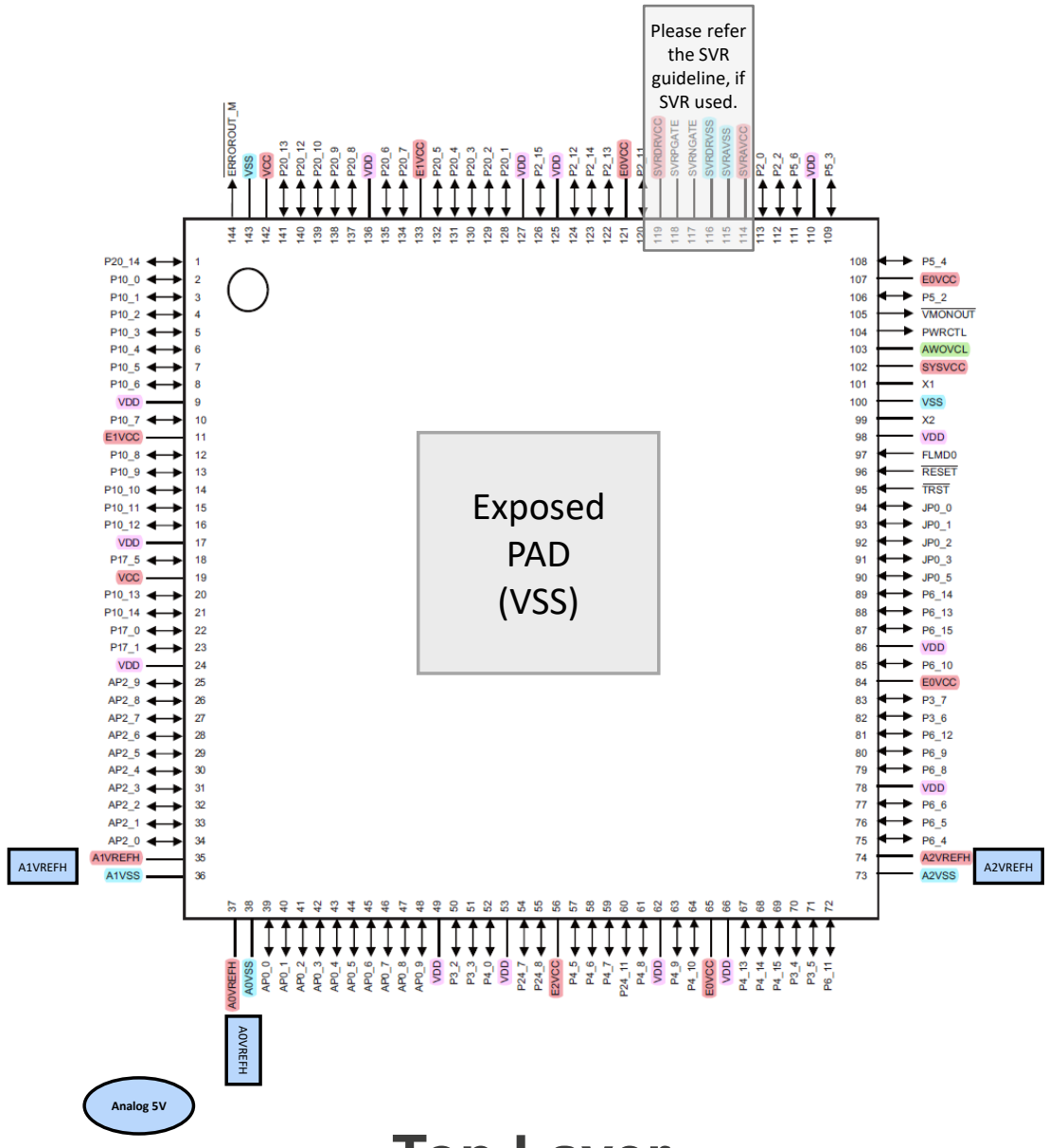
HLQFP176 Bypass capacitor and VIA placement



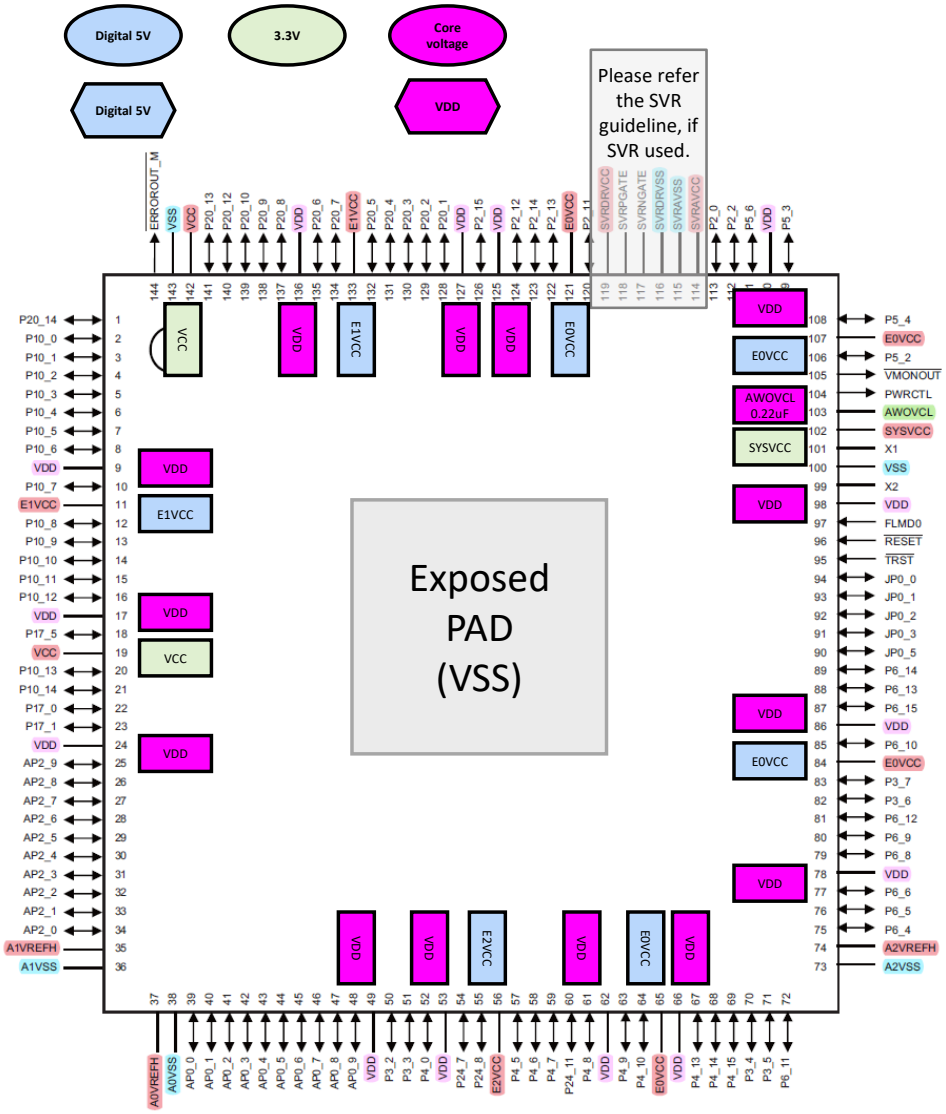
The 1st and 4th layers are displayed superimposed(Gray is the 1st layer, color is the 2nd layer, and 4th layer)

3.7 Example capacitor placement for HLQFP144 package (U2A6)





Top Layer



Bottom Layer

For examples of PCB board design, please refer to " 3.6 Example capacitor placement for HLQFP176 package (U2A6)".

4. Revision History

Rev.	Date	Description	
		Page	Summary
0.70	Mar.31.20	-	Initial version
1.00	Sep.30.20	all	Add U2A8
1.10	Jun.30.22	all	Add U2A6
1.20	Jan.31.24	Page1 Page3 Page4-7 Page4-10 Page13,14,17,18,21,22,24,26,29,31	Add a sentence about the purpose of this document Add “1.4 How to connect capacitor power supply/GND” Add capacitor number (for use in Chapter 3) Add reference text regarding capacitance value for VDD Add ferrite beads(FB1,FB2) Add examples of PCB board design

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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