RH850/U2A-EVA Group

CAN Reception Procedure (CAN FD Mode)

Summary

This application notes explains the procedure example for performing the CAN reception of automotive single-chip microcontroller RH850/U2A series for automobile (hereinafter called U2A).

Aim of this document and software is to provide supplemental information for the function on RH850/U2A. It is not intended to implement in the design for mass production.

There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2A-EVA Group

Target Integrated Development Environment

CS+(from RENESAS Electronics)

Version	:V8.07.00
Device File	:DR7F702300.DVF
	:DR7F702301.DVF
	:DR7F702302.DVF

Reference Document

RH850/U2A-EVA User's Manual: Hardware

For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

- RH850/U2A-EVA User's Manual (Rev.1.30): R01UH0864EJ0130

The register name "RSCFDnCFD" is omitted in this text.

Summary

1. Receive Function

The available functions when performing the CAN message reception are shown below. For the details on each process, refer to the following chapters.

2. Reception using Receive Buffer
3. Reception using Receive FIFO Buffer
4. Reception using Transmit/Receive FIFO Buffer

2. Reception using Receive Buffer

The receive buffer shared by all channels is available. The latest received data can be read since the stored message in the receive buffer with the same number is overwritten.

If it is received in the receive buffer, interrupt is not occurred.

When the storing process of the received message to the receive buffer starts, the receive bufferecomes "new message" (the RMNSu flag of the RMNDt register becomes "1"). Received data information can be read from the RMID register, RMPTR register, RMFDSTS register, and RMDFd register (d= 0 to 15). The maximum payload size that can be received in the receive buffer is up to 64 bytes. The receive FIFO or the transmit/receive FIFO is required to use for receiving the message exceeding 64 bytes.

Refer to “CAN Configuration Application Note” for the configuration setting to use the receive buffer.

Figure 2-1 shows the operation of the receive buffer.

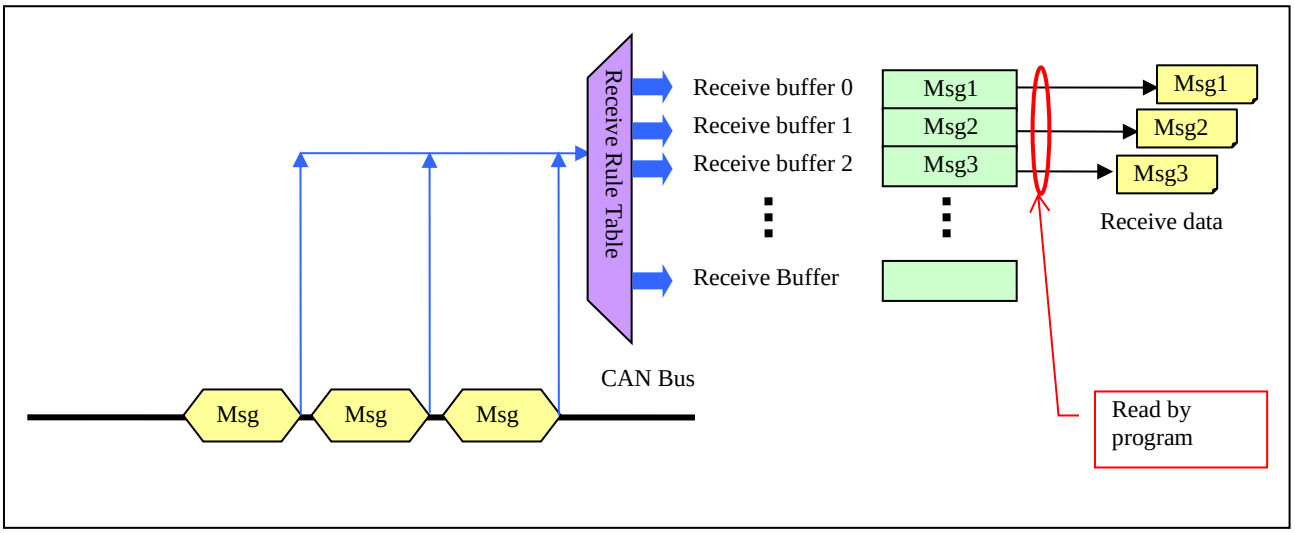
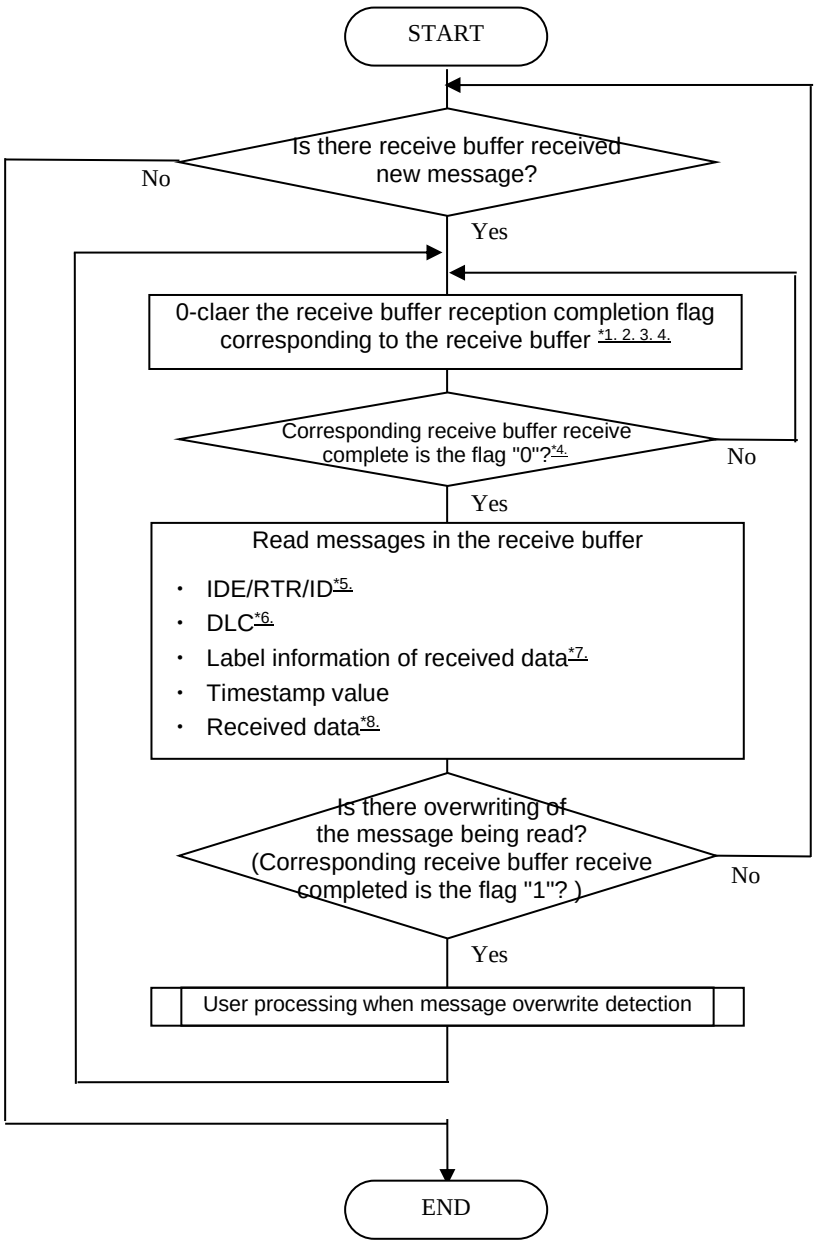


Figure 2-1 Receive Buffer Operation

2.1 Receive Buffer Read Procedure

Figure 2-2 shows the procedure for reading the receive buffer.



【Note】

1. Write “0” to RMNSu flag in the RMNDt register in global operation mode or global test mode.
2. Write “0” by the program when set “0” to the RMNSu flag.
3. When write "0" in the RMNSu flag, write "0" in the bit you want to set to "0" and "1" in the other bits by using the store instruction.
4. RMNSu flag cannot be “0” while storing the message. The storing message time depends on the stored payload size in the receive buffer.
5. Read b10 to b0 of the ID (the RMID [28:0] bits in the RMIDL register) when it is the standard ID. “0” can be read for b28 to b11.

6. When the DLC replacement is enabled (the DCE bit in the GCFG register is “1”, DRE bit is “1”) after filtering by the reception rule, the DLC (the GAFLDLC[3:0] bits in the GAFLP_j register) set value of receive rule table that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
7. After filtering by the receive rule, the set value of the label of the receive rule table (the GAFLPTR [15:0] bits in the GAFLP_j register) that matches the received message is stored.
8. If the DLC of the received message (the value of the RMDLC [3:0] bits in the RMPTR register) is less than the payload storage size of the receive buffer, the data byte (RMDFd register) for which no data is set can read “H'00”.

Figure 2-2 Receive Buffer Read Procedure

3. Reception using Receive FIFO Buffer

There are eight receive FIFO Buffers sharing to all channels. The messages for the number of buffers can be stored in each receive FIFO Buffer.

When the reception message is stored to the receive FIFO Buffer, the value of the corresponding message counter (the RFMC [7:0] bits in the RFSTS register) is incremented.

Received message can be read from the RFID register, RFPTR register, RFFDSTS register, and RFDFd register. The receive FIFO buffer can be read from the oldest message.

When the value of the message counter matches the buffer value of the FIFO buffer (the value set by the RFCCx register in RFDC [2:0] bits), the receive FIFO buffer becomes full (the RFFLL flag in the RFSTSx register is “1”).

When all messages are read from the receive FIFO buffer, the receive FIFO buffer becomes empty (the RFEMP flag in the RFSTSx register is “1”)

Refer to the “CAN Configuration Application Note” for configuration setting to use the receive FIFO buffer.

Figure3-1 shows the operation of the receive FIFO buffer.

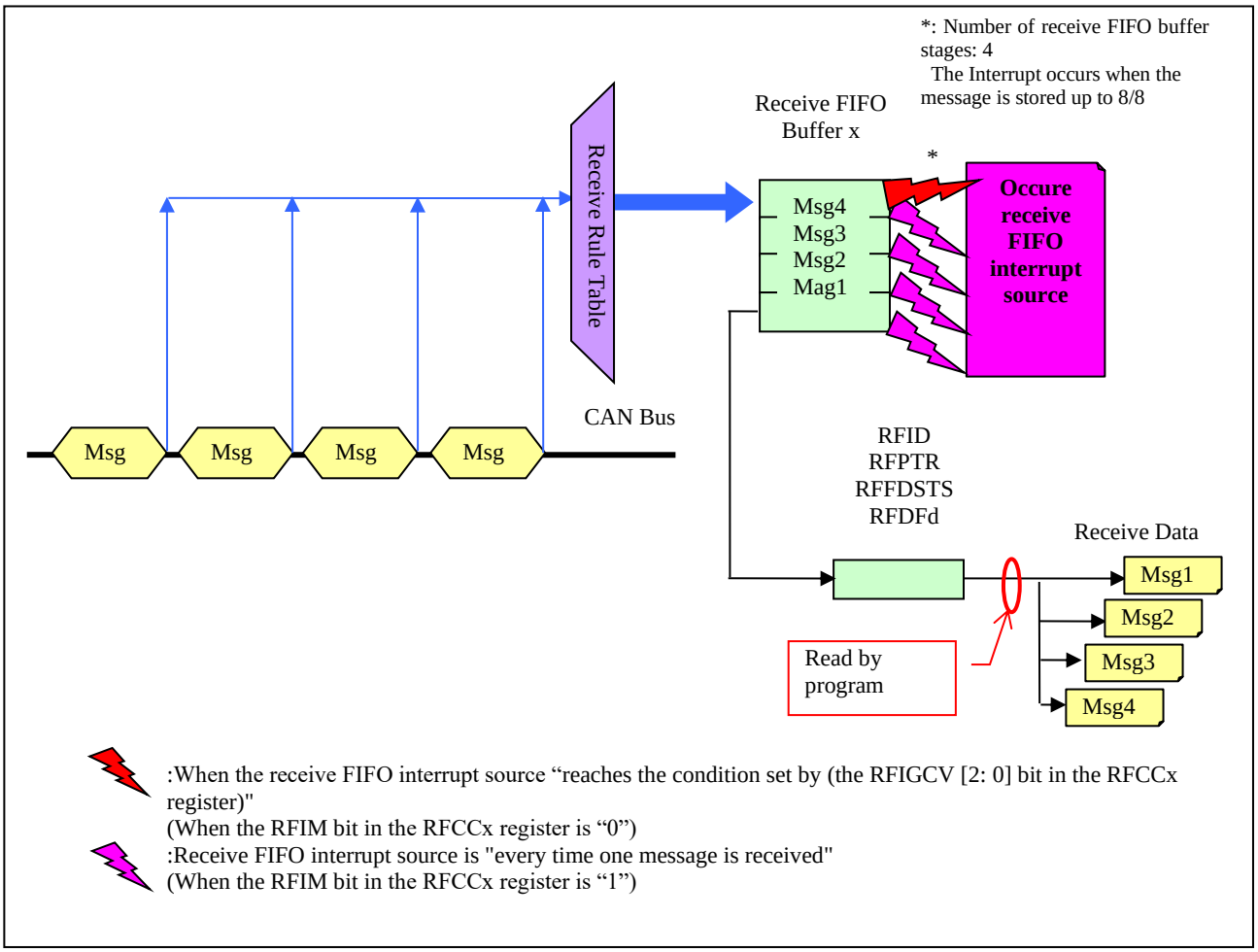
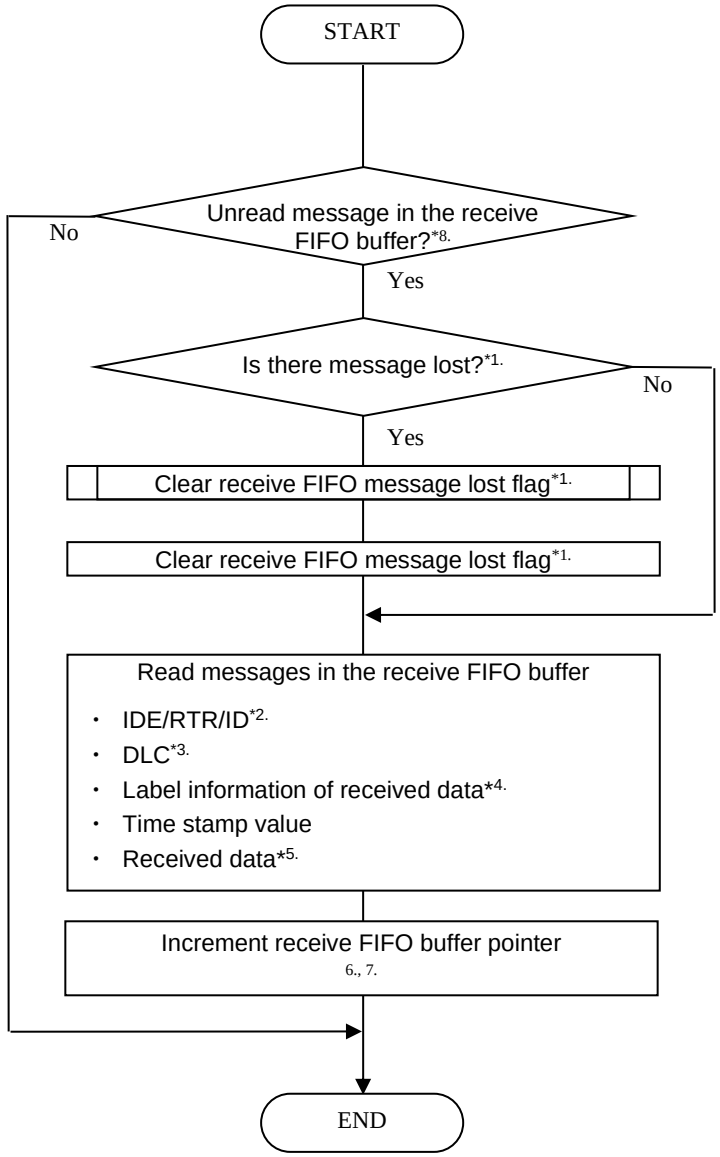


Figure3-1 Receive FIFO Buffer Operation

3.1 Receive FIFO Buffer Read Procedure

Figure 3-2 shows the procedure for reading the receive FIFO buffer, and Figure3-3 and Figure3-4 show the procedure for enabling and disabling the use of the receive FIFO buffer.

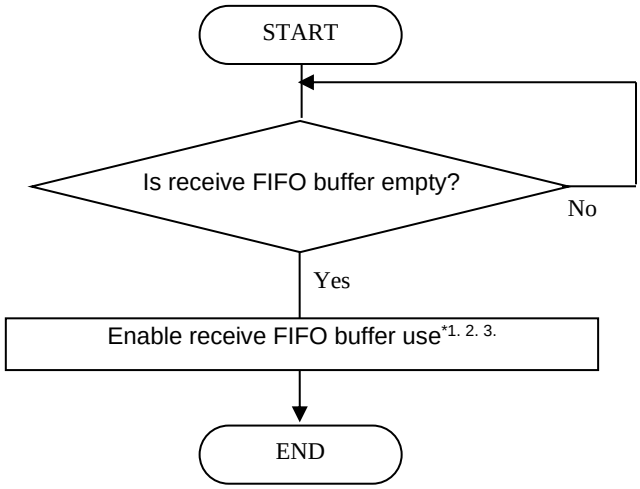


【Note】

1. If the FIFO message lost interrupt is enabled, execute in the global error interrupt processing.
2. For standard ID, read b10-b0 of ID (the RFID [28: 0] bits in the RFID register). b28 to b11 can read “0”.
3. If the DLC replacement is enabled (the DCE bit in the GCFG register is “1”, DRE bit is “1”) after filtering by the reception rule, the DLC (the GAFLDLC[3:0] bits in the GAFLP_j register) set value of receive rule table that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
4. After filtering by the receive rule, the set value of the label of the receive rule table (the GAFLPTR [15: 0] bits in the GAFLP_j register) that matches the received message is stored.
5. If the DLC of the received message (the value of the RFDLC [3:0] bits in the RFPTR register) is less than the payload storage size of the receive FIFO buffer, "H'00" can be read for the data byte (RFDFd register) for which no data is set.

6. After reading the message in the receive FIFO buffer (RFID register, RFPTR register, RFDFd register), increment the pointer (write "H'FF" to the RFPC [7:0] bits in the RFPCTRx register).
7. Increment the pointer when use the receive FIFO buffer (the RFE bit in the RFCCx register is “1”) and there is the unread message in the receive FIFO buffer (the RFEMP flag in the RFSTSx register is “0”).
8. When reading all the unread messages in the receive FIFO buffer, read until the buffer is empty by the loop sentence, etc.

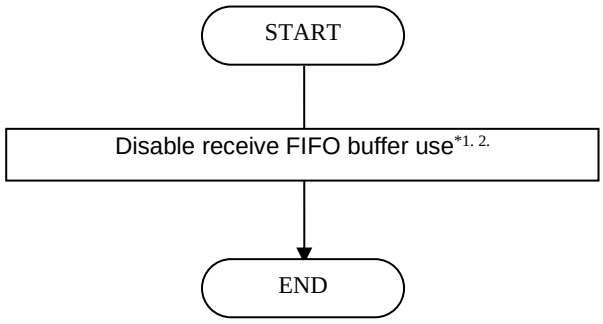
Figure 3-2 Receive FIFO Buffer Read Procedure (Unused Interrupt)



【Note】

1. Rewrite to enable/disable the receive FIFO buffer (the RFE bit in the RFCCx register) in the global operation mode or global test mode.
2. Perform the configuration settings for using the receive FIFO buffer, and then enable the receive FIFO buffer use (the RFE bit is "1").
3. If the number of receive FIFO buffers is set to “0” (“B’000” in the RFDC [2:0] bits in the RFCCx register), do not enable the receive FIFO buffer use.

Figure3-3 Receive FIFO Buffer Use Enable Procedure



【Note】

1. Rewrite to enable/disable the receive FIFO buffer (the RFE bit in the RFCCx register) in the global operation mode or global test mode.
2. Even if the receive FIFO buffer use is disabled (the RFE bit is “0”) while the interrupt request is occurred (the RFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFIF flag) is not automatically set to “0”. Set "0" to the interrupt request flag by the program.

Figure3-4 Receive FIFO Buffer Use Disable Procedure

3.2 Receive FIFO Interrupt Processing

3.2.1 Receive FIFO Interrupt Processing

If the receive FIFO interrupt is enabled, the receive FIFO interrupt is occurred when the conditions selected by the RFIM bit setting in the RFCCx register are satisfied.

Even if the receive FIFO buffer use is disabled (the RFE bit is “0”) while the interrupt request is occurred (the RFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFIF flag) is not automatically set to “0”. Set "0" to the interrupt request flag by the program.

Whether to enable or disable receive FIFO interrupts can be set for each receive FIFO buffer using the RFIE bit in the RFCCx register. The sources of receive FIFO interrupts are shown below.

The receive FIFO interrupt request is occured when the condition set by the RFIGCV [2: 0] bits in the RFCCx register is reached (the RFIM bit in the RFCCx register is "0").

RFIGCV[2:0] bits settings

- When the message is stored up to 1/8 in the receive FIFO buffer*1
- When the message is stored up to 2/8 in the receive FIFO buffer
- When the message is stored up to 3/8 in the receive FIFO buffer*1
- When the message is stored up to 4/8 in the receive FIFO buffer
- When the message is stored up to 5/8 in the receive FIFO buffer*1
- When the message is stored up to 6/8 in the receive FIFO buffer
- When the message is stored up to 7/8 in the receive FIFO buffer*1
- When the receive FIFO buffer is full

— Receive FIFO interrupt request occurs when every message reception is completed (the RFIM bits in RFCCx register is “1”)

【Note】 1. Do not set if the number of receive FIFO buffers is set to 4 messages (the RFDC [2: 0] bits in the RFCCx register is set to "B'001").

3.2.2 Receive FIFO Full Interrupt Processing

If the FIFO full interrupt is enabled (the RFFIE bits in the RFCCx register is “1”), the receive full interrupt is occurred when the receive FIFO buffer is full.

Even if the receive FIFO buffer is disabled (the RFE bit is “0”) while the interrupt request is occurred (the RFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFIF flag) is not automatically set to “0”. Set "0" to the interrupt request flag by the program.

3.2.3 Global Error Interrupt Processing

If the FIFO message lost interrupt is enabled, the global error interrupt is occurred when the message lost in the receive FIFO buffer is detected.

The interrupt enable/disable can be set to entire module in common by GCTR register.

4. Reception using Transmit/Receive FIFO Buffer

The transmit/receive FIFO buffer can be used in receive mode, transmit mode, or gate way mode (only receive mode is described in this chapter).

There is three transmit/receive FIFO buffer per channels. transmit/receive FIFO Buffer set to the receive mode can store the messages for the number of buffers same as the receive FIFO buffer.

When the received message is stored to the transmit/receive FIFO buffer set to receive mode, the value of the corresponding message counter (the CFMC [7: 0] bits in the CFSTSk register) is incremented.

The received messages can be read from the CFID register, CFPTR register, CFFDCTST register, and CFDFd register.

The transmit/receive FIFO buffer can be read from the oldest message.

When the value of the message counter matches the buffer value of the transmit/receive FIFO buffer (the value set in the CFDC [2:0] bits in the CFCCk register), the transmit/receive FIFO buffer becomes full (the CFFLL flag in the CFSTSk register is “1”).

When all messages are read from the transmit/receive FIFO buffer, the transmit/receive FIFO buffer becomes empty (the CFEMP flag in the CFSTSk register is “1”).

For the configuration settings for using the transmit/receive FIFO buffer, refer to "CAN Configuration Application Note".

Figure 4-1 shows the receive operation of the transmit/receive FIFO buffer

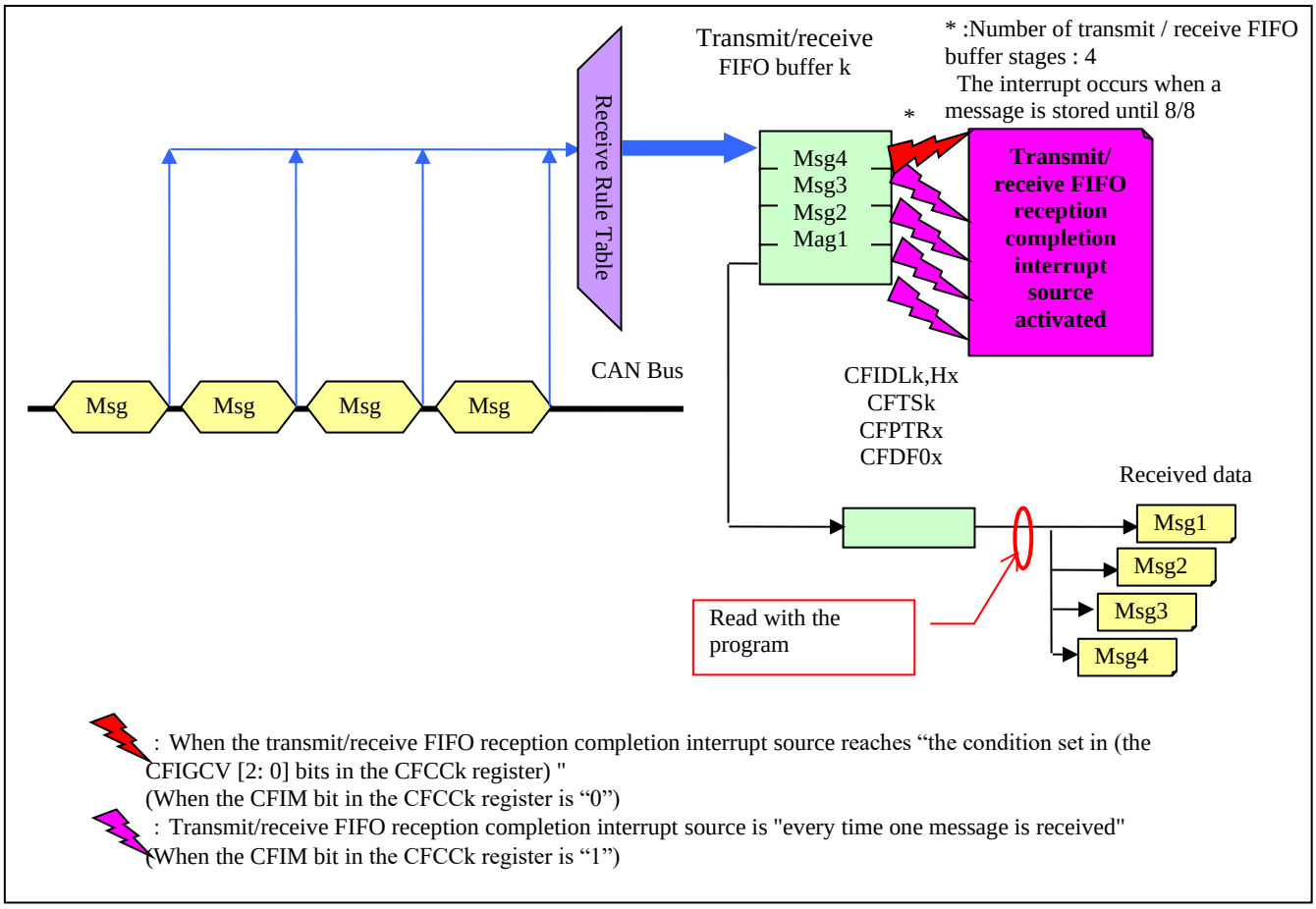
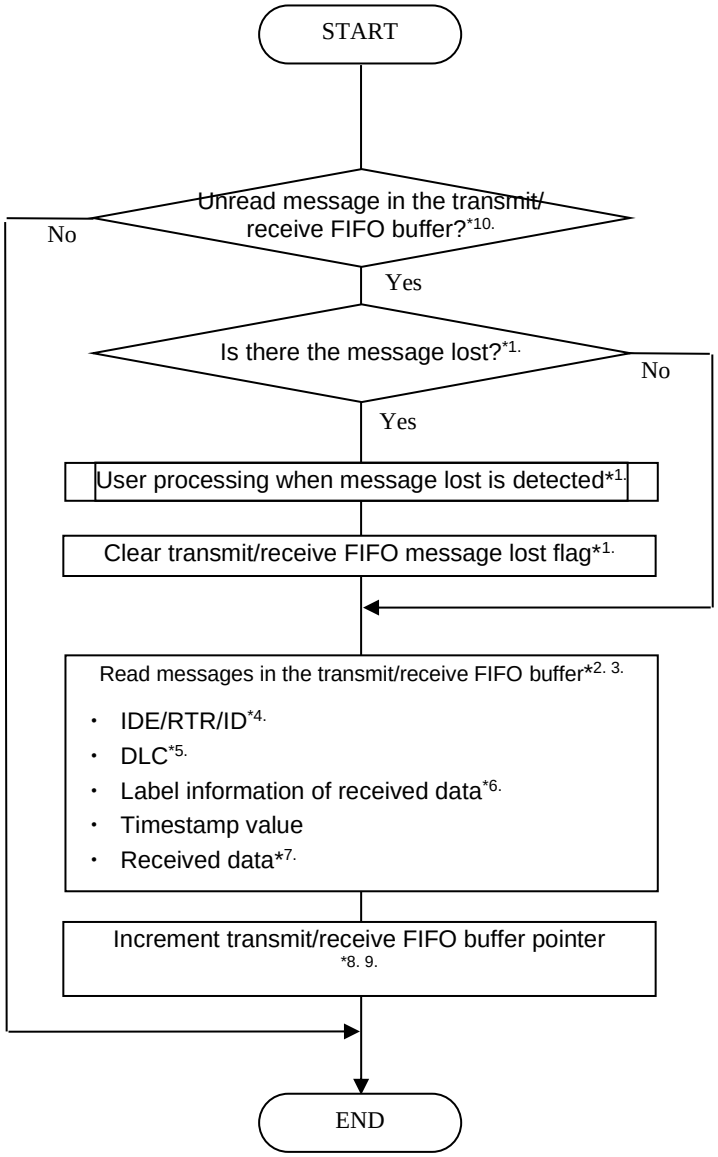


Figure 4-1 Transmit/Receive FIFO Buffer Operation (Receive mode)

4.1 Transmit/Receive FIFO Buffer Read Procedure

Figure 4-2 shows the procedure for reading the transmit/receive FIFO buffer, and Figure 4-3 and Figure 4-4 show the procedure for enabling and disabling the use of the transmit/receive FIFO buffer

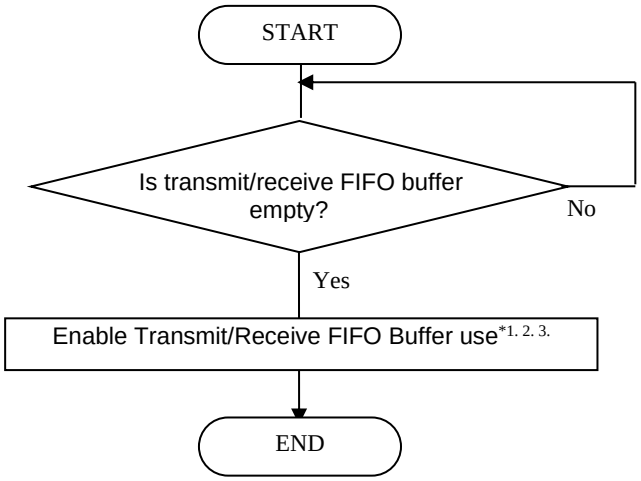


【Note】

1. If the FIFO message lost interrupt is enabled, execute it in the global error interrupt processing.
2. The transmit/receive FIFO buffer (CFID register, CFPTR register, CFDFd) can be read only in the receive mode (the CFM [1:0] bits in the CFCCk register is “B’00”).
3. In the receive mode, enabling or disabling the storage of transmission history data (the THLEN bit in the CFIDk register) is invalid.
4. For standard ID, read b10 to b0 of ID (the CFID [28:0] bits in the CFIDk register). b28 to b11 can read “0”.
5. If DLC replacement is enabled after filtering by the reception rule (the DCE bit in the GCFG register is “1”, the DRE bit is “1”), the DLC set value in the reception rule table (the GAFLDLC bit in the GAFLP_j register) that matches the received message is stored. Otherwise, the DLC value of the received message is stored.

6. After filtering by the reception rule, the set value of the reception rule table label (the GAFLPTR [15:0] bits in the GAFLP_j register) that matches the received message is stored.
7. If the DLC of the received message (the value of the CFDLC [3:0] bits in the CFPTRk register) is less than the payload storage size of the transmit/receive FIFO buffer, the data byte (CFDFd register) which is not set the data can read “H’00”.
8. After reading the messages in the transmit/receive FIFO buffer (the CFID register, CFPTR register, CFDFd register), increment the pointer (write "H'FF" to the CFPC [7:0] bits in the CFPCTRk register).
9. Increment the pointer when the transmit/receive FIFO buffer is used (the CFE bit in the CFCCk register is “1”) and there is unread message in the transmit/receive FIFO buffer (the CFEMP flag in the CFSTSk register is “0”).
10. When reading all the unread messages in the transmit/receive FIFO buffer, use a loop statement or the like to read until the buffer is empty.

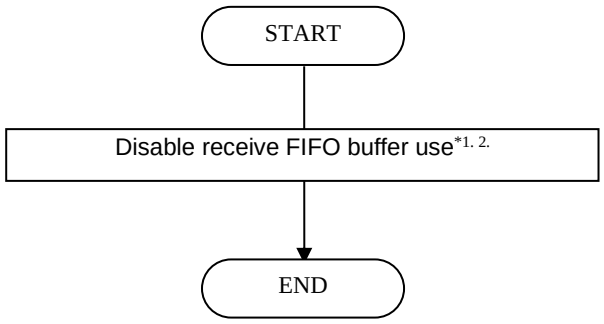
Figure 4-2 Read Procedure (Receive mode) of Transmit/receive FIFO Buffer (no interrupt used)



【Note】

1. Rewrite to enable/disable the receive FIFO buffer (the CFE bit in the CFCCx register) in the global operation mode or global test mode during using the receive mode.
2. Perform the configuration settings for using the transmit/receive FIFO buffer, and then enable the transmit/receive FIFO buffer use (the CFE bit is "1").
3. If the number of transmit/receive FIFO buffers is set to “0” (“B’000” in the CFDC [2:0] bits in the CFCCx register), do not enable the transmit/receive FIFO buffer use.

Figure 4-3 Transmit/Receive FIFO Buffer Use Enable Procedure



【Note】 1. Rewrite to enable/disable the transmit/receive FIFO buffer (the CFE bit in the CFCCx register) in the global operation mode or global test mode during using the receive mode.

2. Even if the transit/receive FIFO buffer use is disabled (the CFE bit is “0”) while the interrupt request is occurred (the CFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFRXIF flag) is not automatically set to “0”. Set "0" to the interrupt request flag by the program.

Figure 4-4 Transmit/Receive FIFO Buffer Use Disable Procedure

4.2 Transmit/Receive FIFO Buffer (Receive Mode) Interrupt Processing

4.2.1 Transmit/Receive FIFO Reception Completion Interrupt Processing

If the transmit/receive FIFO interrupt is enabled, the transmit/receive FIFO interrupt is occurred when the condition selected in the CFIM bit setting of the CFCCk register is satisfied.

Even if the use of the transmit/receive FIFO buffer is disabled (the CFE bit is “0”) while the interrupt request is occurred (the CFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFRXIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Whether to enable or disable transmit/receive FIFO interrupts can be set for each transmit/receive FIFO buffer using the CFRXIE bit in the CFCCk register.

The sources of transmit/receive FIFO interrupts in receive mode are shown below.

A transmit/receive FIFO interrupt request is occurred when the condition set by the CFIGCV [2: 0] bits in the CFCCk register is reached (the CFIM bit in the CFCCk register is "0").

RFIGCV[2:0] bits settings

- When the message is stored up to 1/8 in the transmit/receive FIFO buffer*1
- When the message is stored up to 2/8 in the transmit/receive FIFO buffer
- When the message is stored up to 3/8 in the transmit/receive FIFO buffer*1
- When the message is stored up to 4/8 in the transmit/receive FIFO buffer
- When the message is stored up to 5/8 in the transmit/receive FIFO buffer*1
- When the message is stored up to 6/8 in the transmit/receive FIFO buffer
- When the message is stored up to 7/8 in the transmit/receive FIFO buffer*1
- When the transmit/receive FIFO buffer is full
- Transmit/receive FIFO interrupt request occurs every time message reception is completed (the CFIM bit in CFCCk register is “1”)

【Note】 1. Do not set if the number of transmit/receive FIFO buffers is set to 4 messages (the CFDC [2: 0] bit in the CFCCk register is set to "B'001").

4.2.2 FIFO Full Interrupt Processing

If the FIFO full interrupt is enabled (the CFFIE bit in CFCCEk register), the transmit/receive full interrupt is occurred when the transmit/receive FIFO buffer is full.

Even if the use of the transmit/receive FIFO buffer is disabled (the CFE bit is “0”) while the interrupt request is occurred (the CFFIF flag in the CFSTSk register is “1”), the interrupt request flag (CFFIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program

4.2.3 Transmit/ Receive FIFO One-Frame Reception Interrupt Processing

If the transmit/receive FIFO one-frame reception interrupt is enabled (the CFOFRXIE bit in CFCCEk register), transmit/receive FIFO one-frame reception interrupt is occurred when the transmit/receive FIFO buffer received the message by one-frame reception.

Even if the use of the transmit/receive FIFO buffer is disabled (the CFE bit is “0”) while the interrupt request is occurred (the CFOFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFOFRXIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

4.2.4 Global Error Interrupt Processing

If the FIFO message lost interrupt is enabled, a global error interrupt is occurred when a message lost in the transmit/receive FIFO buffer is detected. If the FIFO message overwrite interrupt is enabled, the global error interrupt is occurred when the message overwrite of the transmit/receive FIFO buffer is detected.

Whether to enable or disable the FIFO message lost interrupt can be set in common for the entire module with the MEIE bit in the GCTR register. Also, whether the FIFO message lost interrupt enable/disable can be set to the entire module in common by the GCTR register.

5. CAN-related Interrupt Source

Refer to “CAN Configuration Application Note” for the CAN-related Interrupt.

6. Processing Flow Precautions

Refer to “CAN Configuration Application Note” for the CAN-related Interrupt.

7. Appendix

7.1 Operation when Receive Buffer is Completed and Receive (Transmit/receive) FIFO Buffer is Full

Table 7-1 shows the operation when the message to be stored is received when the receive buffer reception is completed, and the receive FIFO buffer, the transmit/receive FIFO buffer (reception mode) are full.

Table 7-1 Operation when Receive Buffer is Completed and Receive (Transmit/receive) FIFO Buffer is Full

FIFO/Buffer	When the next message is received*1	Occurred Interrupt request
Receive Buffer	Overwrite	Global Error Interrupt (CAN-FD message payload overwrite Interrupt)
Receive FIFO Buffer	Discard	Global error interrupt (Message lost in receive FIFO buffer)
Transmit/Receive FIFO Buffer (receive mode)	Overwrite to oldest buffer, and increment pointer. When CFCCEk.CFMOWM=1 is set.	Global Error Interrupt (Transmit/Receive FIFO message overwrite)
	Discard When CFCCEk.CFMOWM=0 is set.	Global Error Interrupt (Message lost in transmit/receive FIFO buffer)

【Note】 1. Overwrite: The next message is overwritten in the receive buffer
Discard: The next message is discarded (not stored in FIFO) and the message is lost.

7.2 Receive Rule Table

The receive rule table is the table with rules for filtering received messages.

The selected messages are stored in the specified buffer by data processing using the receive rule table.

Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function. For details on how to set the receive rule table, refer to "CAN Configuration Application Note".

The functions performed during data processing of received message according to the receive rule are shown below.

・Comparison of IDE / RTR / ID by IDE mask / RTR mask / ID mask

・Determination of receive rule target message (message sent by other node / own node) (when mirror function is enabled)

・DLC check (when DLC check is enabled)

・DLC replacement (when DLC check and DCL replacement are enabled)

・Storage FIFO / buffer selection

・Addition of receive rule label

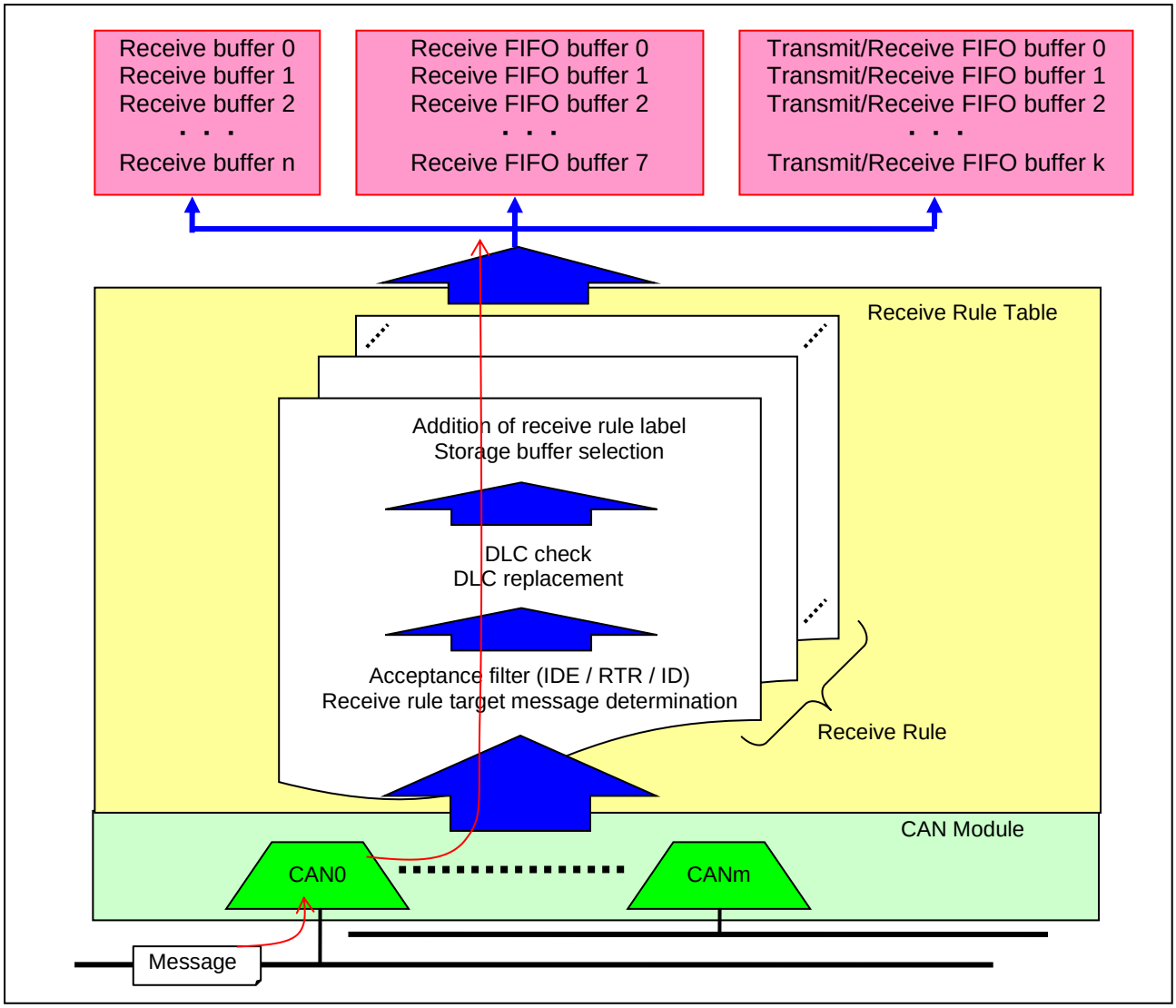


Figure 7-1 Filtering Image by receive rule table

Revision History

Rev.	Data	Description	
		Page	Summary
1.10	2022.01.20	-	Released English version of r01an4892jj0110

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

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