RH850/U2A

Estimation and Calculation of Chip Operating Temperature

Summary

This application note describes how chip operating temperature is estimated and calculated in RH850/U2A.

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1. Power Consumption of the LSI

Pd, the total power consumption of this LSI, can be calculated by the following Formula 1.1.

$$Pd = P_{ISOVDD} + P_{VCC} + P_{SYSVCC} + P_{LVDVCC} + P_{ADC} + P_{IO} + P_{SVR} + P_{EMUVCC} + P_{DVCC} + P_{ERAMVCC} + \\ + P_{EMUVDD} + P_{DVDD} + P_{ERAMVDD} + P_{GBETH} \quad \text{... Formula 1.1}$$

P_{ISOVDD}: Power consumption of ISOVDD

Pvcc: Power consumption of VCC

P_{SYSVCC}: Power consumption of SYSVCC

P_{LVDVCC}: Power consumption of LVDVCC

P_{ADC}: Power consumption of the AD convertor (power consumption of A0VCC, A0VREFH, A1VCC, A1VREFH, A2VCC, and A2VREFH)

$P_{IO} = P_{IO}const + P_{IOINJ} + P_{IODO}$

$P_{IO}const$: Constant power consumption of I/O buffers (power consumption of E0VCC, E1VCC, and E2VCC)

P_{IOINJ}: Power injected to I/O buffers

P_{IODO}: Power output from I/O buffers (AC operation)

P_{SVR}: Power consumption of SVR (Switching Voltage Regulator)

P_{EMUVCC}: Power consumption of EMUVCC

P_{DVCC}: Power consumption of DVCC

$P_{ERAMVCC}$: Power consumption of ERAMVCC

P_{EMUVDD}: Power consumption of EMUVDD

P_{DVDD}: Power consumption of DVDD

$P_{ERAMVDD}$: Power consumption of ERAMVDD

P_{GBETH}: Power consumption of Gigabit Ethernet (GETH0BVCC, GETH0RVCC, GETH0PVCC)

1.1 Power Consumption of ISOVDD

Power consumption of ISOVDD (P_{ISOVDD}), can be calculated by the following Formula 1.2.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{ISOVDD}, or contact our sales office for calculations under your conditions of use.

$$P_{ISOVDD} = I_{ISOVDD} \times ISOVDD \quad \text{... Formula 1.2}$$

I_{ISOVDD}: ISOVDD current (A)

ISOVDD: ISOVDD voltage (V)

1.2 Power Consumption of VCC

Power consumption of VCC (P_{VCC}), can be calculated by the following Formula 1.3.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{VCC}, or contact our sales office for calculations under your conditions of use.

$$Pvcc = I_{VCC} \times VCC \quad \text{... Formula 1.3}$$

1.3 Power Consumption of SYSVCC

Power consumption of SYSVCC (P_{SYSVCC}), can be calculated by the following Formula 1.4.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{SYSVCC}, or contact our sales office for calculations under your conditions of use.

$$P_{SYSVCC} = I_{SYSVCC} \times SYSVCC \quad \text{... Formula 1.4}$$

1.4 Power Consumption of LVDVCC

Power consumption of LVDVCC (P_{LVDVCC}), can be calculated by the following Formula 1.5.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{LVDS}, or contact our sales office for calculations under your conditions of use.

$$P_{LVDVCC} = I_{LVDS} \times LVDVCC \quad \text{... Formula 1.5}$$

1.5 Power Consumption of ADC

Power consumption of the AD convertor of this LSI (P_{ADC}), can be calculated by the following Formula 1.6.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{ADCn}, $I_{ADCnREF}$, or contact our sales office for calculations under your conditions of use.

$$P_{ADC} = P_{ADCJ0} + P_{ADCJ1} + P_{ADCJ2} \quad \text{... Formula 1.6}$$

$P_{ADCJn} = I_{ADCn} \times A_{nVCC} + I_{ADCnREF} \times A_{nVREFH(n=0\sim2)}$: Power consumption of SAR-AD module

1.6 Power Consumption of I/O Buffers

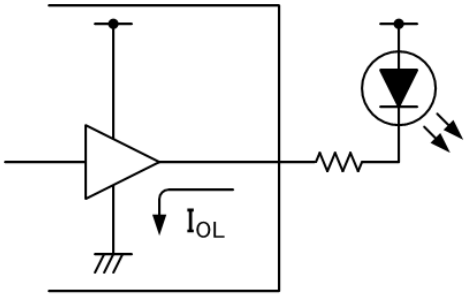
Add the constant power consumption when a direct current flows through input, output, or input/output pins.

Example 1: When LED operates (when a constant current flows)

$P_{IOCONST} = V_O \times I_{OL} \times A \times Buffer$

A: Ratio at which LED turns ON

Buffer: Number of input/output/bidirectional buffers



1.7 Power Injected to I/O Buffers

Power injected to I/O buffers of this LSI (P_{IOINJ}), can be calculated by the following Formula 1.7.

$$P_{IOINJ} = \{Pinjdp \times Ninjdp + Pinjdm \times Ninjdm + Pinjap \times Ninjap + Pinjam \times Ninjam\} \quad \text{... Formula 1.7}$$

Pinjdp: Power injected to each pin (digital pin; positive current injection)

Ninjdp: Number of pins currents are injected to (digital pin; positive current injection)

Pinjdm: Power injected to each pin (digital pin; negative current injection)

Ninjdm: Number of pins currents are injected to (digital pin; negative current injection)

Pinjap: Power injected to each pin (analog pin; positive current injection)

Ninjap: Number of pins currents are injected to (analog pin; positive current injection)

Pinjam: Power injected to each pin (analog pin; negative current injection)

Ninjam: Number of pins currents are injected to (analog pin; negative current injection)

1.8 Power Output from I/O Buffers (AC Operation)

Power output from I/O buffers of this LSI (AC operation) (P_{IODO}), can be calculated by the following Formula 1.8.

$$P_{IODO} = \Sigma(fo \times CL \times V^2) \quad \text{... Formula 1.8}$$

CL: Load capacitance

fo: Output frequency

V: Voltage of I/O buffers

1.9 Power Cunsumption of SVR converter

Power consumption of SVR converter (P_{SVR}), can be calculated by the following Formula 1.9.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{SVR}, I_{SVRA}, or contact our sales office for calculations under your conditions of use.

$$P_{SVR} = I_{SVR} \times SYSVCC + I_{SVRA} \times SVRAVCC + P_{SVRDR} \quad \text{... Formula 1.9}$$

$$P_{SVRDR} = f_{SVRSW} \times SVRDRVCC^2 \times (C_{iss\_}PMOSFET + C_{iss\_}NMOSFET)$$

f_{SVRSW} :SVR switching frequency

Ciss_PMOSFET: SVR external capacitor of Pch MOSFET

Ciss_NMOSFET: SVR external capacitor of Nch MOSFET

1.10 Power Consumption of EMUVCC

Power consumption of EMUVCC (P_{EMUVCC}), can be calculated by the following Formula 1.10.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{EMUVCC}, or contact our sales office for calculations under your conditions of use.

$$P_{EMUVCC} = I_{EMUVCC} \times EMUVCCC \quad \text{... Formula 1.10}$$

1.11 Power Consumption of DVCC

Power consumption of DVCC (P_{DVCC}), can be calculated by the following Formula 1.11.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{DVCC}, or contact our sales office for calculations under your conditions of use.

$$P_{DVCC} = I_{DVCC} \times DVCC \quad \text{... Formula 1.11}$$

1.12 Power Consumption of ERAMVCC

Power consumption of ERAMVCC ($P_{ERAMVCC}$), can be calculated by the following Formula 1.12.

See **RH850/U2A-EVA Group User's Manual: Hardware** for $I_{ERAMVCC}$, or contact our sales office for calculations under your conditions of use.

$$P_{ERAMVCC} = I_{ERAMVCC} \times ERAMVCC \quad \text{... Formula 1.12}$$

1.13 Power Consumption of EMUVDD

Power consumption of EMUVDD (P_{EMUVDD}), can be calculated by the following Formula 1.13.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{EMUVDD}, or contact our sales office for calculations under your conditions of use.

$$P_{EMUVDD} = I_{EMUVDD} \times EMUVDD \quad \text{... Formula 1.13}$$

1.14 Power Consumption of DVDD

Power consumption of DVDD (P_{DVDD}), can be calculated by the following Formula 1.14.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{DVDD}, or contact our sales office for calculations under your conditions of use.

$$P_{DVDD} = I_{DVDD} \times DVDD \quad \text{... Formula 1.14}$$

1.15 Power Consumption of ERAMVDD

Power consumption of ERAMVDD ($P_{ERAMVDD}$), can be calculated by the following Formula 1.15.

See **RH850/U2A-EVA Group User's Manual: Hardware** for $I_{ERAMVDD}$, or contact our sales office for calculations under your conditions of use.

$$P_{ERAMVDD} = I_{ERAMVDD} \times ERAMVDD \quad \text{... Formula 1.15}$$

1.16 Power Consumption of Gigabit Ethernet

Power consumption of Gigabit Ethernet (P_{GBETH}), can be calculated by the following Formula 1.16.

See **RH850/U2A-EVA Group User's Manual: Hardware** for I_{GBETH}, Rin or contact our sales office for calculations under your conditions of use.

$$P_{GBETH} = I_{GBETH} \times GETH0BVCC + \frac{|V_{OD}|^2}{R_{IN}} \quad \text{... Formula 1.16}$$

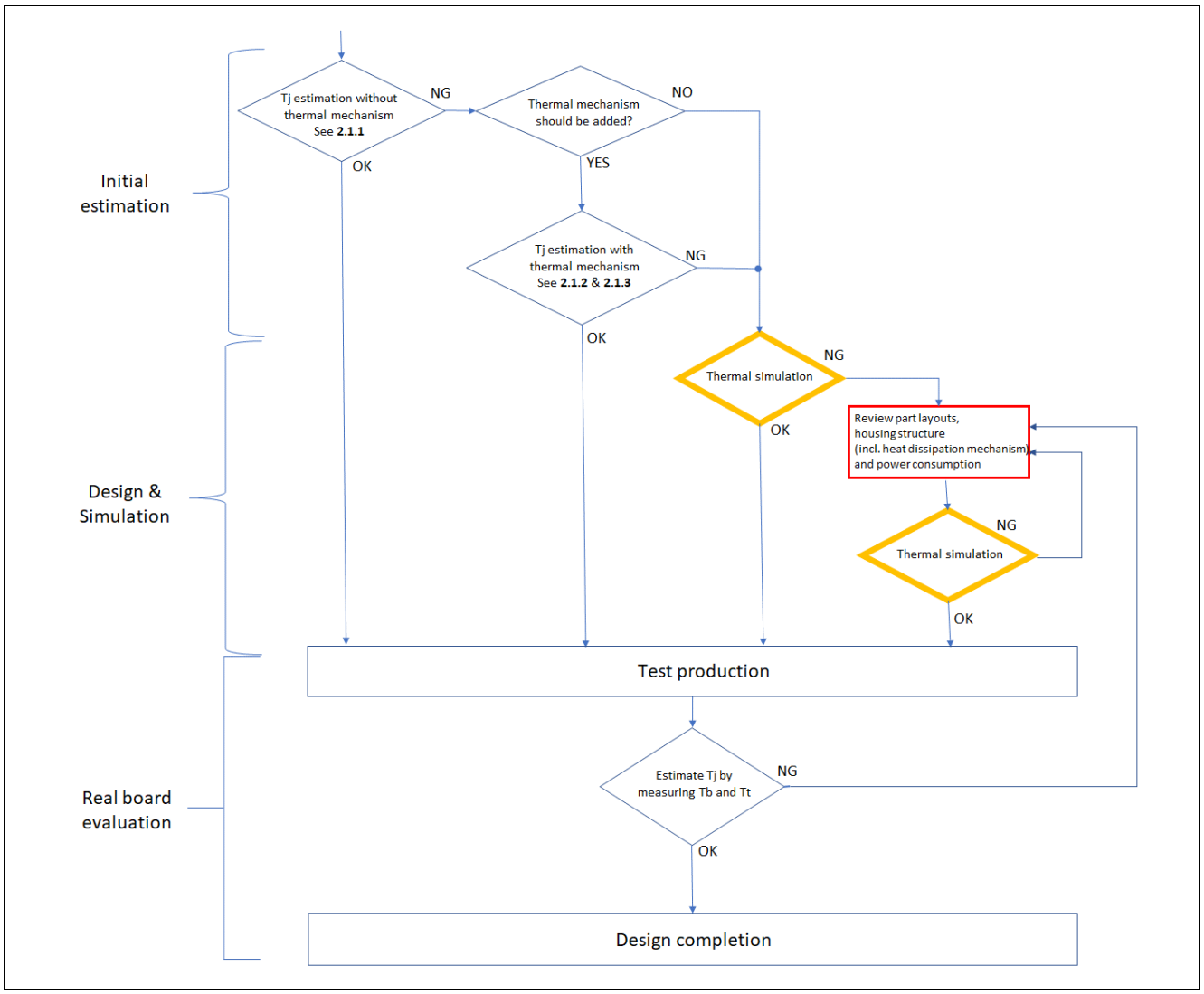
V_{OD} : Output Differential Voltage of opposing device

Rin : Receiver differential input impedance

2. Chip Temperature (Tj) Estimation (Thermal Design Guide)

When existing products enable you to calculate board temperature Tb and package surface temperature Tt (See **2.4.2** for definition) in the early development stage, estimate chip temperature (Tj) with values of Ψjb and Ψjt (for actual values, see **RH850/U2A-EVA Group User's Manual: Hardware**). This is the most accurate way for initial estimation of Tj. When Tb or Tt cannot be estimated, use θja (for actual values, see **RH850/U2A-EVA Group User's Manual: Hardware**) to estimate Tj. When the estimated Tj is around Tjmax (for actual values, see **RH850/U2A-EVA Group User's Manual: Hardware**), add heat dissipation mechanism or perform thermal simulation to obtain more accurate Tj.

Review part layouts, housing structure (including heat dissipation mechanism), and power consumption if necessary. Measure Tb or Tt with an evaluation board even when thermal simulation reveals there will be enough margins. Make sure that Tj is equal to or less than Tjmax by estimating Tj with Ψjb and Ψjt in conjunction with the measured values of Tb, Tt and power consumption.



2.1 Initial Estimation

2.1.1 Tj Estimation Without Heat Dissipation Mechanism

Estimate Tj with Formula 2.1 when Tb can be estimated from existing products, or estimate Tj with Formula 2.2 in which Tt is used when Tb cannot be estimated. Estimate Tj by using Formula 2.3 when neither of Tb nor Tt can be estimated. Apply XYΨjb, XYΨjt, and XYθja in **RH850/U2A-EVA Group User's Manual: Hardware**, which are most suitable for your assumed board. When the estimated Tj is around Tjmax, add heat dissipation mechanism or perform thermal simulation to obtain more accurate Tj.

(1) When Tj is estimated from Tb:

$$Tj = Tb + XY\Psi jb \times Pd \quad \text{... Formula 2.1}$$

(2) When Tj is estimated from Tt:

$$Tj = Tt + XY\Psi jt \times Pd \quad \text{... Formula 2.2}$$

(3) When Tj is estimated from Ta:

$$Tj = Ta + XY\theta ja \times Pd \quad \text{... Formula 2.3}$$

Note: See **2.1.3** for definition of each symbol. The value of Ta varies largely according to the measurement point where Ta is measured, which can lead to inaccurate Tj estimation. Therefore, we recommend you obtain Tb/Tt data and estimate Tj based on obtained Tb/Tt whenever possible.

2.1.2 Tj Estimation When Only Top Side Cooling is Applied

Estimate Tj with an assumed thermal resistor network model of θja in Figure 1 when only top side cooling is applied. Vertical heat dissipation from the junction can be simulated under conditions that the ECU peripheral temperature (Ta) is the same. Formula 2.4 represents the relationships of Ta and Tj, as shown in Figure 1. When θca can be estimated, Tj estimation by using Ta is possible. When θca cannot be estimated, perform Tj estimation by estimating Tt and using Formula 2.5. θca, which changes according to your operating environment, must be calculated by each user.

$$Tj = (\theta ca + \theta jc) \times Pt + Ta = (\theta ca + \theta jc) \times \left(1 - \frac{\Psi jb}{\theta jb}\right) \times Pd + Ta \ldots \text{ Formula 2.4}$$

$$Tj = \theta jc \times Pt + Tt = \theta jc \times \left(1 - \frac{\Psi jb}{\theta jb}\right) \times Pd + Tt \ldots \text{ Formula 2.5}$$

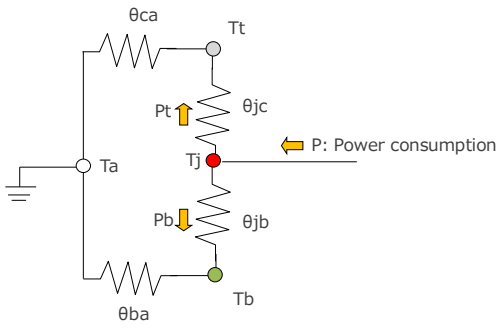


Figure 1. θja Thermal Resistor Network Model

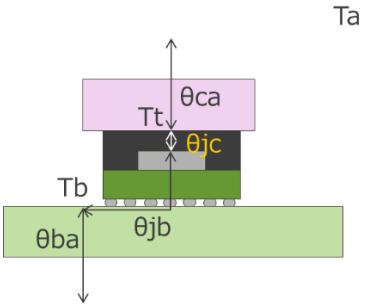


Figure 2. Cross-Sectional Image of Thermal Resistor Network

Estimate Tj with Formula 2.6 when Tt can be estimated from existing products, or estimate Tj with Formula 2.7 when θca can be estimated. Apply XYΨjb and XYθjb in **RH850/U2A-EVA Group User's Manual: Hardware**, which are most suitable for your assumed board. When the estimated Tj is around Tjmax, add heat dissipation mechanism or perform thermal simulation to obtain more accurate Tj.

(1) When Tt can be estimated:

$$Tj = \theta jc \times \left(1 - \frac{XY\Psi jb}{XY\theta jb}\right) \times Pd + Tt \ldots \text{Formula 2.6}$$

(2) When θca can be estimated:

$$Tj = (\theta ca + \theta jc) \times \left(1 - \frac{XY\Psi jb}{XY\theta jb}\right) \times Pd + Ta \ldots \text{ Formula 2.7}$$

Note: See **2.1.3** for definition of each symbol.

2.1.3 Tj Estimation When Both of Top and Bottom Side Cooling Are Applied/When Only Bottom Side Cooling Is Applied

Estimate Tj with an assumed thermal resistor network model of θja in Figure 3 when both of top and bottom side cooling are or only bottom side cooling is applied. Vertical heat dissipation from the junction can be simulated under conditions that the ECU peripheral temperature (Ta) is the same. Formula 2.8 represents the relationships of Ta and Tj, as shown in Figure 3. When θca can be estimated, Tj estimation by using Ta is possible. When θca cannot be estimated, perform Tj estimation by estimating Tt and using Formula 2.9. θca, which changes according to your operating environment, must be calculated by each user.

$$Tj = (\theta ca + \theta jc) \times Pt + Ta = (\theta ca + \theta jc) \times \left(1 - \frac{\Psi jmb}{\theta jcbot}\right) \times Pd + Ta \ldots \text{ Formula 2.8}$$

$$Tj = \theta jc \times Pt + Tt = \theta jc \times \left(1 - \frac{\Psi jmb}{\theta jcbot}\right) \times Pd + Tt \ldots \text{ Formula 2.9}$$

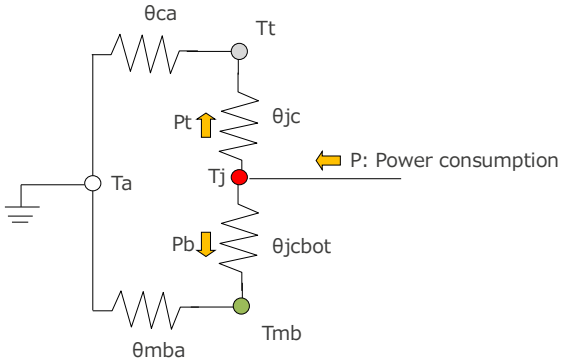


Figure 3. θja Thermal Resistor Network Model

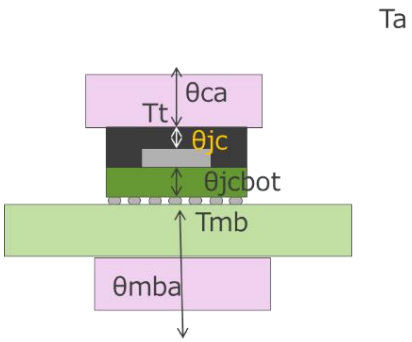


Figure 4. Cross-Sectional Image of Thermal Resistor Network

Estimate Tj with Formula 2.10 when Tt can be estimated from existing products, or estimate Tj with Formula 2.11 when θca can be estimated. Apply XYΨjmb in **RH850/U2A-EVA Group User's Manual: Hardware** which are most suitable for your assumed board. When the estimated Tj is around Tjmax, perform thermal simulation to obtain more accurate Tj.

(1) When Tt can be estimated:

$$Tj = \theta jc \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times Pd + Tt \ldots \text{Formula 2.10}$$

(2) When θca can be estimated:

$$Tj = (\theta ca + \theta jc) \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times Pd + Ta \ldots \text{Formula 2.11}$$

Tj: LSI chip junction temperature

Ta: Peripheral temperature of the LSI package

Tb: Temperature in **2.4.2 Measurement Point**

Tt: Temperature in **2.4.2 Measurement Point**

Tmb: Package center temperature in the surface of the board L1

Pd: Power consumption of the LSI calculated by Formula 1.1

Pt: Power flowing to the top side of the package

Pb: Power flowing to the bottom side of the package

θca: Thermal resistance between Tt and Ta (must be calculated by each user)

θba: Thermal resistance between Tb and Ta (must be calculated by each user)

θjb: Thermal resistance of the LSI package (not use in thermal estimation. Use XY θ jb which is appropriate for your assumed board.)

θmba: Thermal resistance between Tmb and Ta (must be calculated by each user)

Ψjb: Thermal characteristics of the LSI package (not use in thermal estimation. Use XY Ψjb which is appropriate for your assumed board.)

Ψjmb: Thermal characteristics of the LSI package (not use in thermal estimation. Use XY Ψjmb which is appropriate for your assumed board.)

θjc: Thermal resistance of the LSI package (See the following part of User's Manual.) Note

θjcbot: Thermal resistance of the LSI package (See the following part of User's Manual.) Note

XYθja: Thermal resistance of the LSI package (See the following part of User's Manual.) Note

XYθjb: Thermal resistance of the LSI package (See the following part of User's Manual.) Note

XYΨjb: Thermal characteristics of the LSI package (See the following part of User's Manual.) Note

XYΨjt: Thermal characteristics of the LSI package (See the following part of User's Manual.) Note

XYΨjmb: Thermal characteristics of the LSI package (See the following part of User's Manual.) Note

Note: See **RH850/U2A-EVA Group User's Manual: Hardware**, **Thermal Characteristics Parameter**.

X: Number of board layers

Y: Board size

For assumed board size, see **2.4.4 Assumed Board**.

2.2 Thermal Simulation

To more accurately estimate temperature, perform thermal fluid simulation (Computational Fluid Dynamics: CFD). We can provide a package model for FloTHERM (DELPHI model). Contact our sales office for more details.

2.3 Real Board Evaluation (Tj Evaluation with Evaluation Board)

2.3.1 Tj Estimation Without Heat Dissipation Mechanism

Estimate Tj with Formula 2.12 by measuring Tb and power consumption, or estimate Tj with Formula 2.13 by measuring Tt and power consumption. Apply the most appropriate values in **RH850/U2A-EVA Group User's Manual: Hardware** for XYΨjt, XYΨjb and XYTb_inc for your evaluation board. (The following formulas do not contain measurement errors, which should be included when you estimate Tj.)

(1) When Tj is estimated from Tb:

$$Tj = Tb\_typ + XY\Psi jb \times Pdtyp + (XY\Psi jb + XYTb\_inc) \times (Pd\_offset + Pd\_vothers) \quad \text{... Formula 2.12}$$

(2) When Tj is estimated from Tt:

$$Tj = Tt\_typ + XY\psi jt \times (Pdtyp + Pd\_offset + Pd\_vothers) \quad \text{... Formula 2.13}$$

$$Pd\_offset = Vm \times Id\_offset + I0 \times (Vm\text{-}V0) + Vm \times (dI/dV) \times (Vm\text{-}V0) \quad \text{... Formula 2.14}$$

Note 1. Pd_offset can be calculated as follows when the worst power is calculated by a power calculation tool:

$$Pd\_offset = Pd\_max - Pdtyp$$

Note 2. See **2.3.3** for definition of each symbol.

2.3.2 Tj Estimation When Only Top Side Cooling is Applied

When only top side cooling is applied: Assumed conditions are a case where the top side of the package is connected through a thermal sheet (1 mm thickness, 1W/mK) as large as mold resin to a metal plate (electrogalvanized steel with 1 mm thickness) as large as the board.

Measure Tb and power consumption and estimate Tj with Formula 2.15, or measure Tt and power consumption and estimate Tj with Formula 2.16. Apply the most appropriate values in **RH850/U2A-EVA Group User's Manual: Hardware** for XYΨjb and XYTb_inc and XYθjb for your evaluation board. (The following formulas do not contain measurement errors, which should be included when you estimate Tj.)

(1) When Tj is estimated from Tb:

$$Tj = Tb\_typ + XY\Psi jb \times Pdtyp + (XY\Psi jb + XYTb\_inc) \times (Pd\_offset + Pd\_vothers) \quad \text{... Formula 2.15}$$

(2) When Tj is estimated from Tt:

$$Tj = Tt\_typ + \theta jc \times \left(1 - \frac{XY\Psi jb}{XY\theta jb}\right) \times (Pdtyp + Pd\_offset + Pd\_vothers) \quad \text{... Formula 2.16}$$

$$Pd\_offset = Vm \times Id\_offset + I0 \times (Vm\text{-}V0) + Vm \times (dI/dV) \times (Vm\text{-}V0) \quad \text{... Formula 2.17}$$

Note 1. Pd_offset can be calculated as follows when the worst power is calculated by a power calculation tool:

$$Pd\_offset = Pd\_max - Pdtyp$$

Note 2. See **2.3.3** for definition of each symbol.

2.3.3 Tj Estimation When Both of Top and Bottom Side Cooling Are Applied/When Only Bottom Side Cooling Is Applied

When both of top and bottom side cooling are applied or only bottom side cooling is applied: Assumed conditions are a case where the top and bottom sides of the package are connected through a thermal sheet (1 mm thickness, 1W/mK) as large as mold resin to a metal plate (electrogalvanized steel with 1 mm thickness) as large as the board.

Estimate Tj with Formula 2.18 by measuring Tt and power consumption. Apply the most appropriate value in **RH850/U2A-EVA Group User's Manual: Hardware** for XYΨjmb for your evaluation board. (The following formulas do not contain measurement errors, which should be included when you estimate Tj.)

$$Tj = Tt\_typ + \theta jc \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times Pdtyp + \theta jc \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times (Pd\_offset + Pd\_vothers) \quad \text{... Formula 2.18}$$

$$Pd\_offset = Vm \times Id\_offset + I0 \times (Vm\text{-}V0) + Vm \times (dI/dV) \times (Vm\text{-}V0) \quad \text{... Formula 2.19}$$

Note 1: Pd_offset can be calculated as follows when the worst power is calculated by a power calculation tool.

$$Pd\_offset = Pd\_max - Pdtyp$$

Tj: LSI chip junction temperature

Tb_typ: Actual measurement values of Tb when applications are operated by real ECUs

Tt_typ: Actual measurement values of Tt when applications are operated by real ECUs

Pdtyp: Actual measurement values of VDD when applications are operated by real ECUs

Pd_max: Worst VDD calculated by a power calculation tool

Pd_offset: Difference between Pdtyp and power consumption of corner samples

Pd_vothers: Power consumption of power supply except VDD (e.g. AnVCC or LVDVCC)

Id_offset: Difference between I0 and worst VDD calculated by a power calculation tool

dI/dV: VDD dependency coefficient of IDD

Vm: Max VDD voltage (max voltage under conditions of use by each user)

V0: Measured VDD voltage

I0: Measured VDD current

θjc: Thermal resistance of the LSI package (See the following part of User's Manual.) Note 2

θjcbot: Thermal characteristics of the LSI package (See the following part of User's Manual.) Note 2

XYθjb: Thermal resistance of the LSI package (See the following part of User's Manual.) Note 2

XYΨjb: Thermal characteristics of the LSI package (See the following part of User's Manual.) Note 2

XYΨjt: Thermal characteristics of the LSI package (See the following part of User's Manual.) Note 2

XYΨjmb: Thermal characteristics of the LSI package (See the following part of User's Manual.) Note 2

XYTb_inc: Power consumption dependency of Tb (See the following part of User's Manual.) Note 2

Note 2: See **RH850/U2A-EVA User's Manual: Hardware**, **Thermal Characteristics Parameter**.

When Tb_0 is the assumed Tb where the MCU generates 0 W of heat, or Tb_1 where the MCU generates 1 W of heat,

$$XYTb\_inc = Tb\_1 - Tb\_0$$

X: Number of board layers

Y: Board size

For assumed board size, see **2.4.4 Assumed Board**.

2.4 Notes on Tb/Tt Measurement

2.4.1 Measurement Using Thermocouple

Be careful when you select a thermocouple you use and connect it to the measurement target for accurately measuring temperature. Follow the instructions below:

- Use a thermocouple with as small a wire diameter as possible to prevent heat dissipation (recommended size: equal to or less than 100 µm in diameter).

- It is preferable to use a K-type thermocouple (A T-type one radiates more heat, which may lead to a lower measured temperature).

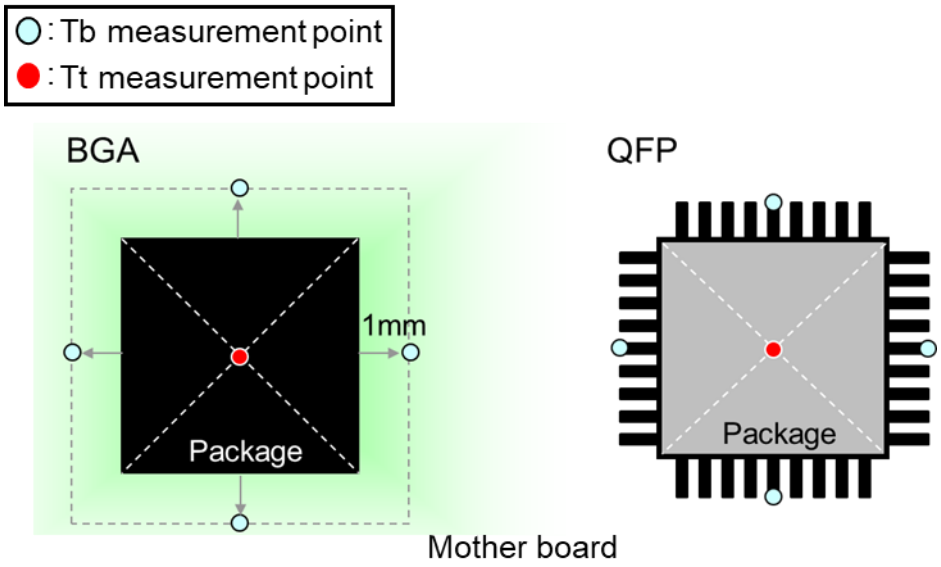
- It is recommended that heat-resistant Kapton tape or hear-resistant material be used to fasten thermocouples.

- Fasten thermocouples tightly to the measurement target (An interspace can lead to measurement errors).

2.4.2 Measurement Point

BGA: Check if the temperature reaches saturation, and measure Tb on the board wiring 1 mm outward from the midpoint on each side of the package. When temperature distribution exists due to influences of peripheral parts, use the average value of 4 measurement points as Tb. Tt is temperature measured at the center top surface of the package.

QFP: Check if the temperature reaches saturation, and measure Tb on the midpoint of lead footprint on each side of the package. When temperature distribution exists due to influences of peripheral parts, use the average value of 4 measurement points as Tb. Tt is temperature measured at the center top surface of the package.



2.4.3 Measurement Using Thermography (Thermo Camera)

Set emissivity of the measurement target to obtain proper temperature values. Emissivity of the board surface is about 0.8 or 0.9, but that of the metal surface typically will be smaller (Measuring the metal surface with 0.8 or 0.9 emissivity can lead to a lower temperature measurement). When the emissivity is unclear, perform surface finishing by blackbody spray and apply its emissivity, which enable correct temperature measurement.

Note that it is impossible to obtain an accurate measurement result when there is any object (even a transparent acrylic plate) between thermography and the measurement target (Thermography will measure the temperature of the acrylic plate in this case).

To measure temperature by thermography may be difficult depending on how the measurement target is placed. However, we recommend the measurement by thermography be used with thermocouples because it is an effective way to know temperature distribution.

2.4.4 Assumed Board

JESD51-9 Compliant Board (4 layers)

	Board size (mm)		Area (mm2)
	X	Y	
Board size	101.5	114.5	11621.75
Remaining copper rate		Conductor thickness	
50 – 95 – 95 – 50%		70 – 35 – 35 – 70 µm	

L board (4 layers)

	Board size (mm)		Area (mm2)
	X	Y	
Board size	90	160	14400
Remaining copper rate		Conductor thickness	
30 – 80 – 80 – 30%		35 – 35 – 35 – 35 µm	

3. Reference

See the following web site for the overview of package thermal characteristics and electrical characteristics:

https://www.renesas.com/us/en/support/technical-resources/packaging/characteristic.html

Revision History

Rev.	Issued Date	Page	Description
0.70	May.21.2020	—	New Release
1.00	Sep.30.2020	7	Modify the wrong description in 1.16 Gigabit Ethernet
		9-15	Modify the number of fomular
		9	Add XY XYΨjb,XYΨjt,XY θja
		10	θba -> θca, add XY XYΨjb,XY θjb
		11	Delete XY θjcbot
		12	Modify the description for θjb,Ψjb,Ψjmb
		13	Add XY XYΨjt,XYΨjb,XYTb_inc Delete the description for XYΨjt
		14	Add XY XYΨjb,XYTb_inc Add XY θjb
		15	Add XY XYΨjmb Modify the description for Id_offset

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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