RH850/F1Kx, RH850/F1K Series

Hardware Design Guide

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Introduction

This application note is intended to provide RH850/F1Kx, RH850/F1K series specific information and recommendations on the device usage. It should be used in conjunction with the corresponding RH850/F1Kx, RH850/F1K series user manual (includes the electrical characteristics).

Target Device

RH850/F1Kx Series

- RH850/F1KM Group
  - RH850/F1KM-S1
    - 100pin
    - 80pin
    - 64pin
    - 48pin
  - RH850/F1KM-S2
    - 176pin
    - 144pin
    - 100pin
  - RH850/F1KM-S4
    - 272pin
    - 233pin
    - 176pin
    - 144pin
    - 100pin
- RH850/F1KH Group
  - RH850/F1KH-D8
    - 324pin
    - 233pin
    - 176pin
- RH850/F1K Series
  - RH850/F1K Group
    - 176pin
    - 144pin
    - 100pin

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1. Power Supply

The internal circuits are separated into two independent power domains, the Always-On area (AWO area) and the Isolated area (ISO area). The power supply of the Always-On area (AWO area) is always on in all operating modes and stand-by modes. The power supply of the Isolated area (ISO area) can be turned off to reduce the overall power consumption depending on the type of stand-by mode. For each power domain, a dedicated on-chip voltage regulator generates the internal supply voltage.

1.1 Power Supply Overview of RH850/F1KM-S1

1.1.1 Power Supply Pin Overview of RH850/F1KM-S1

The devices of the RH850/F1KM-S1 have the following power supply pins:

- Power supply voltage REGVCC for the on-chip voltage regulators. The output voltage of the voltage regulators is supplied to the digital circuits in each power domain.
- Power supply voltage EVCC for I/O ports.
- Power supply voltage A0VREF for the A/D converters and the separated I/O ports.

Table 1: RH850/F1KM-S1 Power supply pin overview

Device	Power Supply Pins
RH850/F1KM-S1 (100pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS
RH850/F1KM-S1 (64pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS
RH850/F1KM-S1 (48pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS

Note: The pins AWOVCL and ISOVCL are available on all devices to connect external stabilization capacitors. Do not use AWOVCL and ISOVCL as power source of other devices.

1.1.2 Power Supply Pin Configuration of RH850/F1KM-S1

The following shows power supply pin configuration. Do not open any power and GND terminals even if those are internally connected.

- The EVCC supply pins are internally connected.
- The EVSS pins are internally connected.
- AWOVSS and ISOVSS are internally connected.
- Others are not internally connected.

1.1.3 Power Supply Pin Architecture of RH850/F1KM-S1

The RH850/F1KM-S1 supports different power supply architectures. The power supply architecture depends on the application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1KM-S1:

- REGVCC = EVCC = VPOC to 5.5V
- A0VREF = 3.0V to 5.5V
- AWOVSS = ISOVSS = EVSS = A0VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

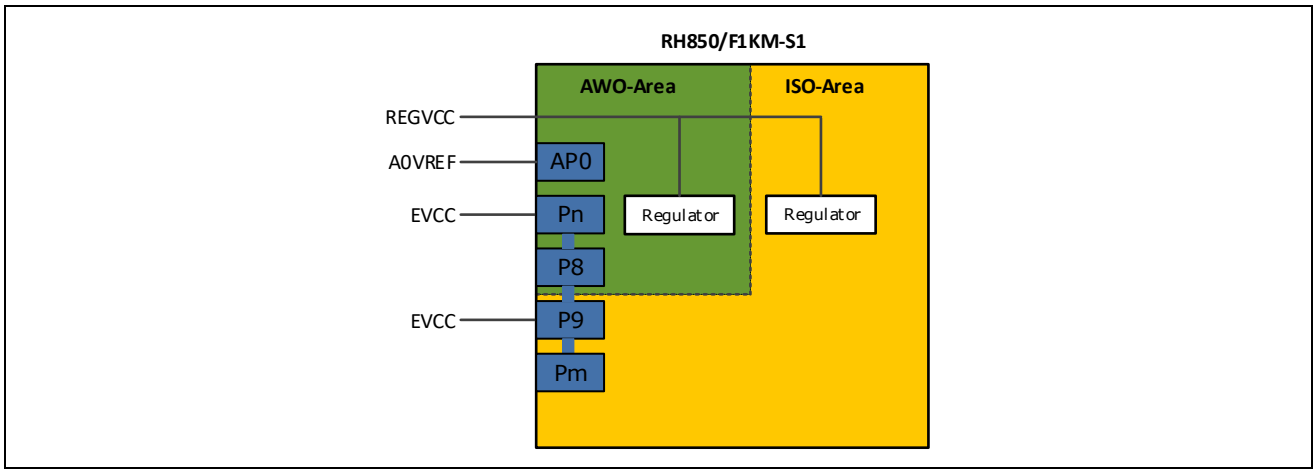


Figure 1: RH850/F1KM-S1 Power supply architecture

Table 2: RH850/F1KM-S1 Overview of power supply architecture cases

Case	Supply Voltage			Permission
	REGVCC	EVCC	A0VREF	
Case 1	5V	5V	5V	Operation permitted
Case 2	5V	5V	3.3V	Operation permitted
Case 3	5V	3.3V	*	Operation not permitted
Case 4	3.3V	5V	*	Operation not permitted
Case 5	3.3V	3.3V	5V	Operation permitted
Case 6	3.3V	3.3V	3.3V	Operation permitted

Note: * means “don’t care”.

Table 3: RH850/F1KM-S1 Power supply architecture with single supply 5V

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 4: RH850/F1KM-S1 Power supply architecture with mixed supply 5V & 3.3V

Case 2 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 5: RH850/F1KM-S1 Power supply architecture with mixed supply 5V & 3.3V

Case 3 and Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC ≠ EVCC EVCC = 3.3V or 5V A0VREF = Don't care
Port Function	–
Limitation	Common condition REGVCC = EVCC not met
→	**Operation not permitted**

Table 6: RH850/F1KM-S1 Power supply architecture with mixed supply 5V & 3.3V

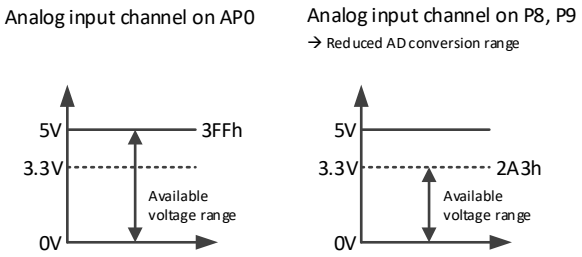
Case 5 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 7: RH850/F1KM-S1 Power supply architecture with single supply 3.3V

Case 6 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

1.1.4 Power Supply Timing of RH850/F1KM-S1

The RH850/F1KM-S1 has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms. Satisfy the spec of voltage slope by using power IC with enable control or by using power IC which starts output over VPOC. The following shows an example of configuration between RH850/F1KM-S1 and PMIC.

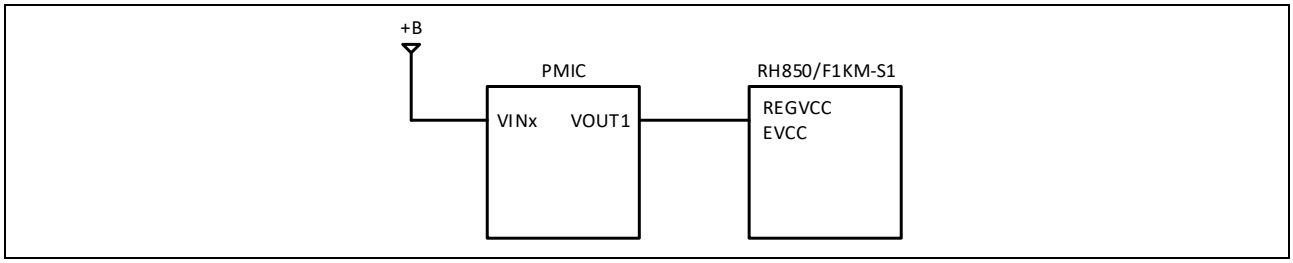


Figure 2: Recommended REGVCC power configuration for RH850/F1KM-S1

The voltage range which has to be kept voltage slope is as follows. There is no voltage slope limitation at the case other than below condition. For detail, see the following figure.

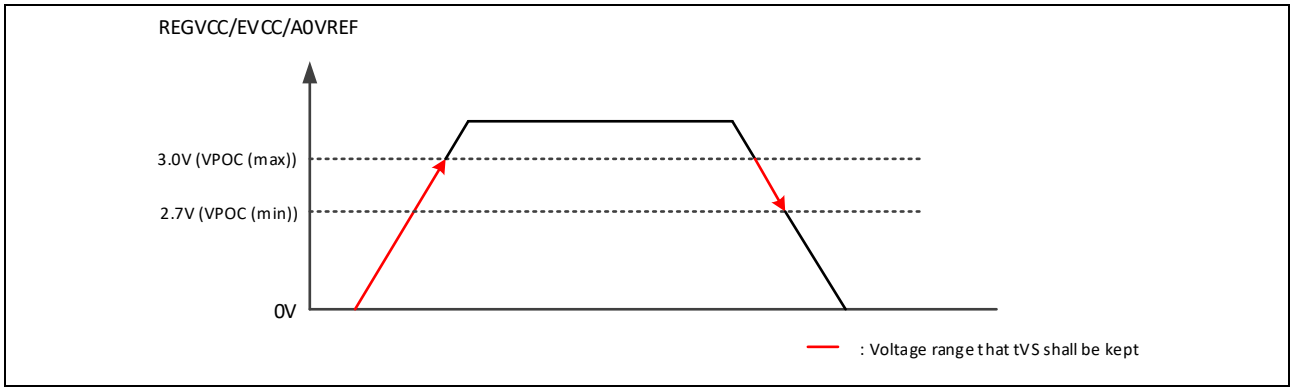


Figure 3: The voltage range which has to be kept voltage slope for RH850/F1KM-S1

Note: When the power source rises again, keep the spec of “REGVCC minimum width (t_{W_POC})“, which is specified in the Section 47C.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

For details on the electrical characteristics, please refer to Section 47C, Electrical Characteristics of RH850/F1KM-S1 of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

a) When $\overline{\text{RESET}}$ terminal is used

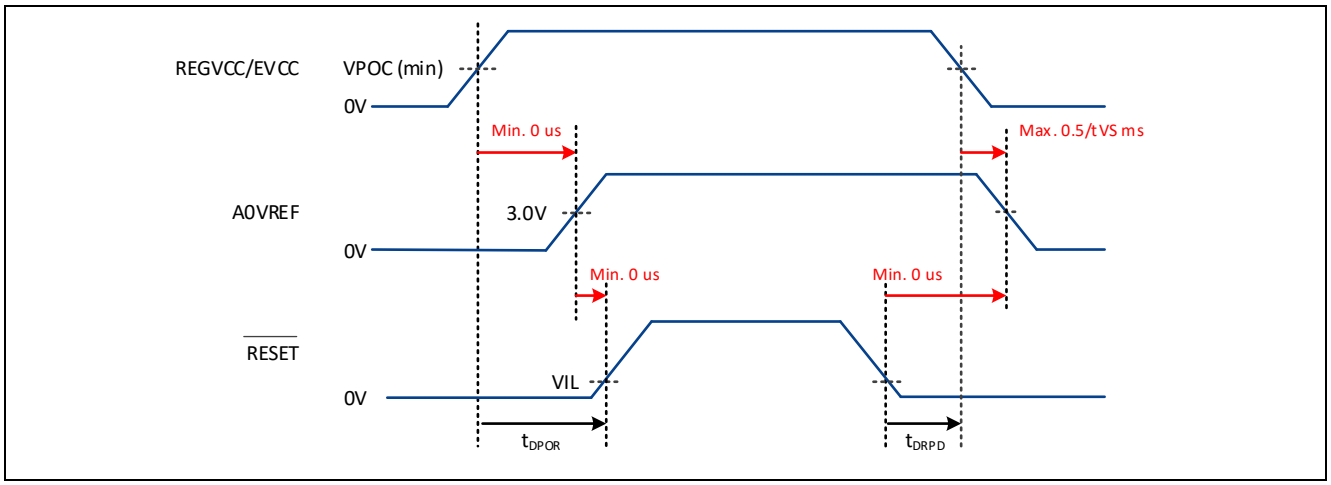


Figure 4: RH850/F1KM-S1 Power up/down timing

b) When $\overline{\text{RESET}}$ terminal is not used

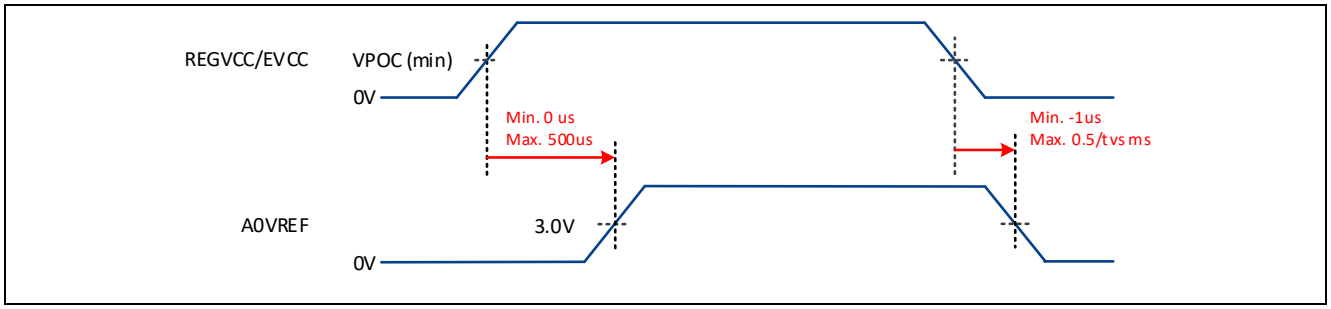


Figure 5: RH850/F1KM-S1 Power up/down timing

Note. For the spec of t_{DPOR}, t_{DRPD} and t_{VS}, please refer to Section 47C.4.5.3, Power Up/Down Timing of the RH850/F1KH, RH850/F1KM Hardware User's Manual.

1.2 Power Supply Overview of RH850/F1KM-S2

1.2.1 Power Supply Pin Overview of RH850/F1KM-S2

The devices of the RH850/F1KM-S2 have the following power supply pins:

- Power supply voltage REGVCC for the on-chip voltage regulators. The output voltage of the voltage regulators is supplied to the digital circuits in each power domain.
- Power supply voltages EVCC and BVCC (depending on device pin count) for the I/O ports.
- Power supply voltages A0VREF and A1VREF (depending on the device pin count) for the A/D converters and the separated I/O ports.

Table 8: RH850/F1KM-S2 Power supply pin overview

Device	Power Supply Pins
RH850/F1KM-S2 (176pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KM-S2 (144pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KM-S2 (100pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS

Note: The pins AWOVCL and ISOVCL are available on all devices to connect external stabilization capacitors. Do not use AWOVCL and ISOVCL as power source of other devices.

1.2.2 Power Supply Pin Configuration of RH850/F1KM-S2

The following shows power supply pin configuration. Do not open any power and GND terminals even if those are internally connected.

- The EVCC supply pins are internally connected.
- The BVCC supply pins are internally connected (when available on the device).
- The EVSS pins are internally connected.
- The BVSS pins are internally connected (when available on the device).
- AWOVSS and ISOVSS are internally connected.
- Others are not internally connected.

1.2.3 Power Supply Pin Architecture of RH850/F1KM-S2

The RH850/F1KM-S2 supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1KM-S2 device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1KM-S2:

- REGVCC = EVCC = VPOC to 5.5V
- BVCC = VPOC to REGVCC (when available on the device)
- A0VREF = 3.0V to 5.5V
- A1VREF = 3.0V to 5.5V (when available on the device)
- AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

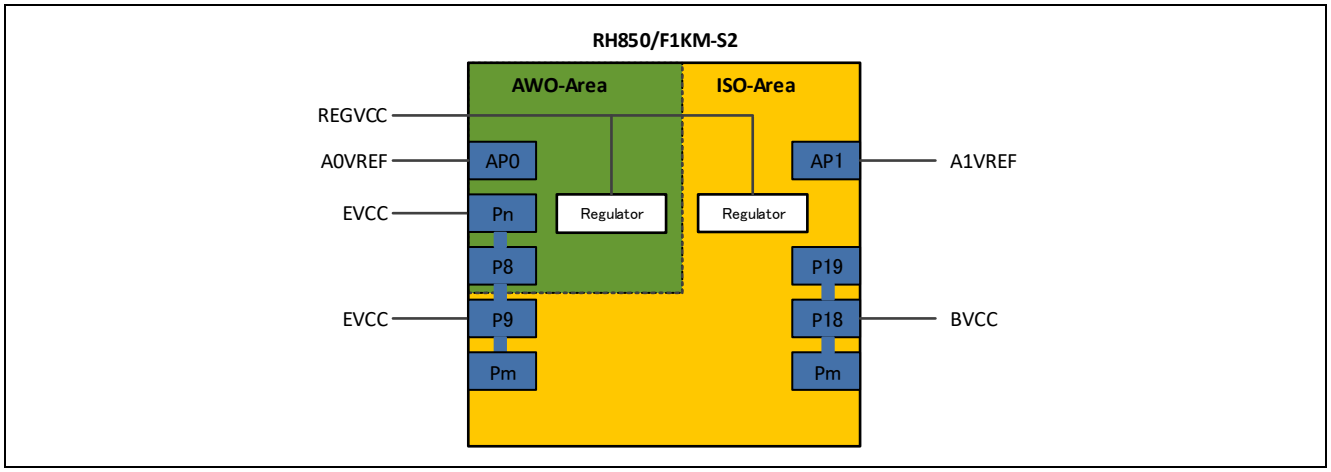


Figure 6: RH850/F1KM-S2 Power supply architecture

Note: The BVCC and A1VREF supply pin availability depends on the chosen device.

Table 9: RH850/F1KM-S2 Overview of power supply architecture cases

Case	Voltage					Permission
	REGVCC	EVCC	BVCC	A0VREF	A1VREF	
Case 1	5V	5V	5V	5V	5V	Operation permitted
Case 2	5V	5V	5V	5V	3.3V	Operation permitted
Case 3	5V	5V	5V	3.3V	5V	Operation permitted
Case 4	5V	5V	5V	3.3V	3.3V	Operation permitted
Case 5	5V	5V	3.3V	5V	5V	Operation permitted
Case 6	5V	5V	3.3V	5V	3.3V	Operation permitted
Case 7	5V	5V	3.3V	3.3V	5V	Operation permitted
Case 8	5V	5V	3.3V	3.3V	3.3V	Operation permitted
Case 9	5V	3.3V	*	*	*	Operation not permitted
Case 10	3.3V	5V	*	*	*	Operation not permitted
Case 11	3.3V	3.3V	5V	*	*	Operation not permitted
Case 12	3.3V	3.3V	3.3V	5V	5V	Operation permitted
Case 13	3.3V	3.3V	3.3V	5V	3.3V	Operation permitted
Case 14	3.3V	3.3V	3.3V	3.3V	5V	Operation permitted
Case 15	3.3V	3.3V	3.3V	3.3V	3.3V	Operation permitted

Note: * means “don’t care”.

Table 10: RH850/F1KM-S2 Power supply architecture with single supply 5V

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 11: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

Case 2 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 12: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 13: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 14: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

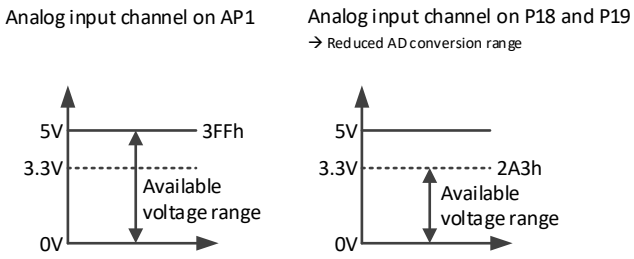
Case 5 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 15: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

Case 6 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 16: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

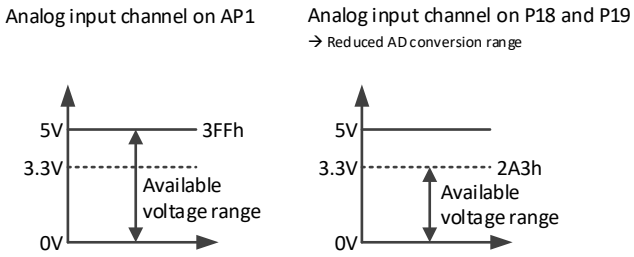
Case 7 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 17: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

Case 8 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 18: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

Case 9, Case 10 – Mixed Supply 5V & 3.3V	
Condition	REGVCC ≠ EVCC EVCC = 3.3V or 5V BVCC = Don't care A0VREF = Don't care A1VREF = Don't care
Port Function	-
Limitation	Common condition REGVCC = EVCC not met
→	**Operation not permitted**

Table 19: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

Case 11 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 5V A0VREF = Don't care A1VREF = Don't care
Port Function	-
Limitation	Common condition REGVCC ≥ BVCC not met
→	**Operation not permitted**

Table 20: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

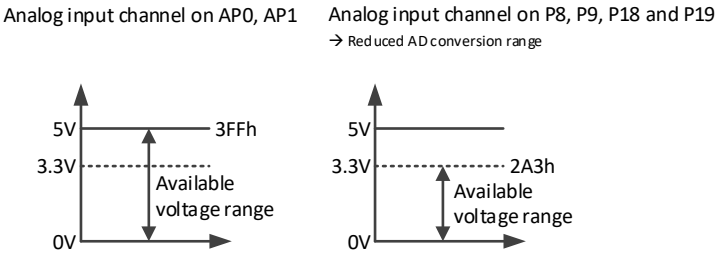
Case 12 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 21: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

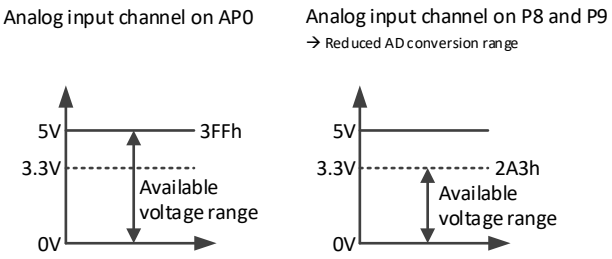
Case 13 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 22: RH850/F1KM-S2 Power supply architecture with mixed supply 5V & 3.3V

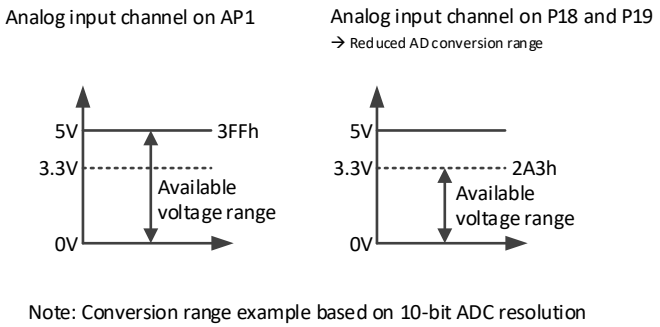
Case 14 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 23: RH850/F1KM-S2 Power supply architecture with single supply 3.3V

Case 15 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

1.2.4 Power Supply Timing of RH850/F1KM-S2

The RH850/F1KM-S2 has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms. Satisfy the spec of voltage slope by using power IC with enable control or by using power IC which starts output over VPOC. The following shows an example of configuration between RH850/F1KM-S2 and PMIC.

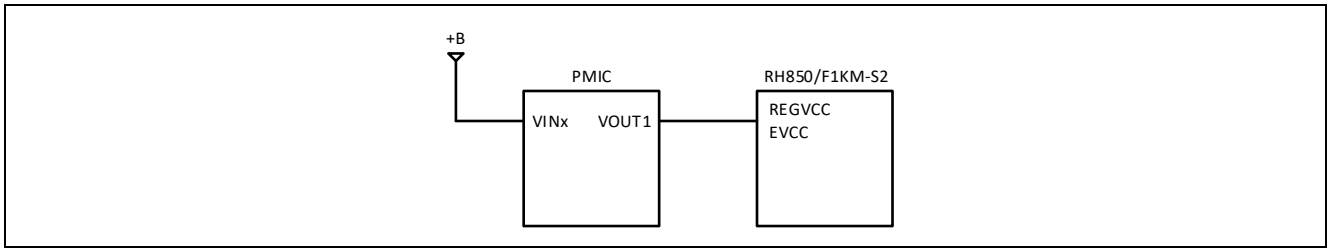


Figure 7: Recommended REGVCC power configuration for RH850/F1KM-S2

The voltage range which has to be kept voltage slope is as follows. There is no voltage slope limitation at the case other than below condition. For detail, see the following figure.

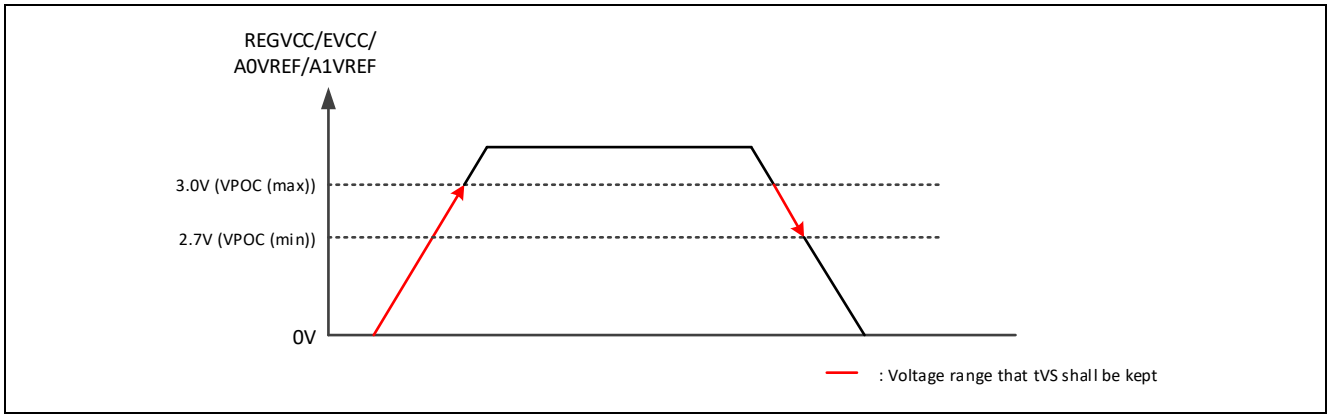


Figure 8: The voltage range which has to be kept voltage slope for RH850/F1KM-S2

Note: When the power source rises again, keep the spec of “REGVCC minimum width (tw_POC)“, which is specified in the Section 47B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

For details on the electrical characteristics, please refer to Section 47B, Electrical Characteristics of RH850/F1KM-S4, RH850/F1KM-S2 of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

a) When RESET terminal is used

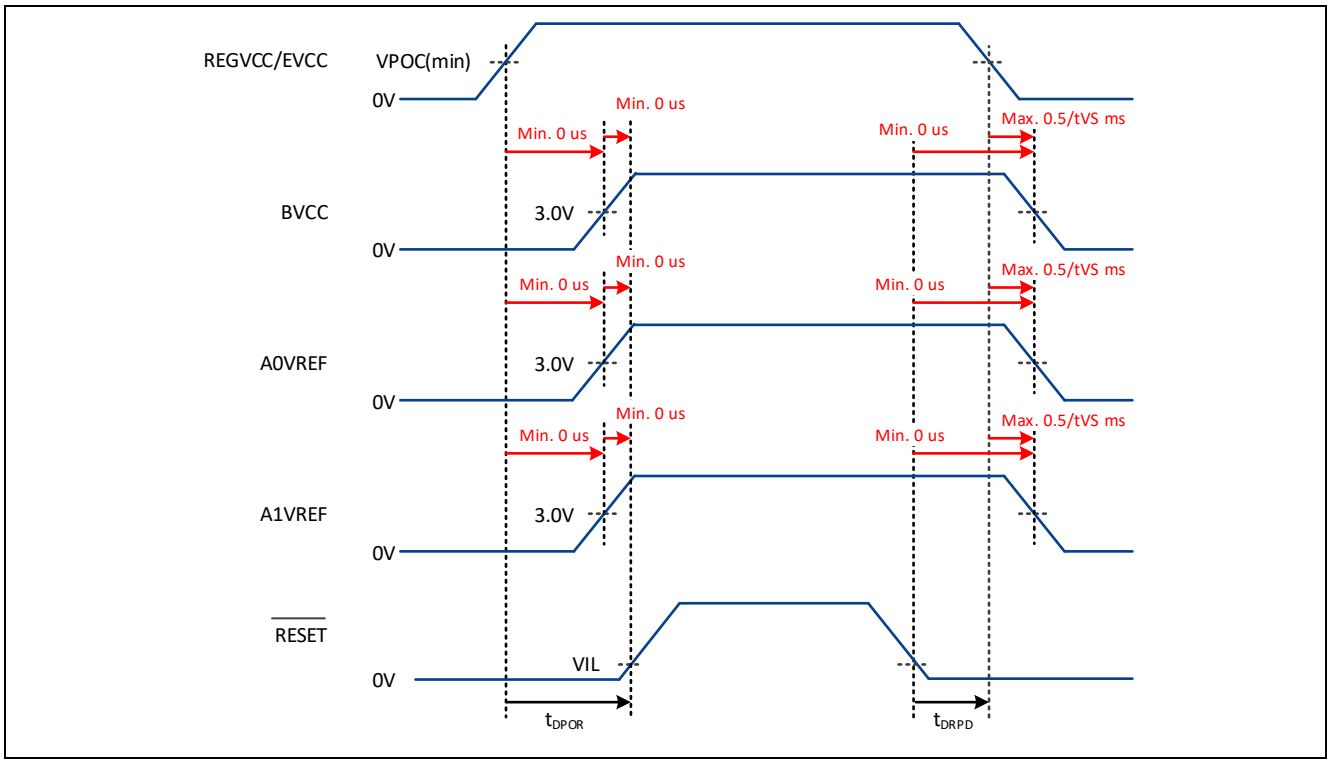


Figure 9: RH850/F1KM-S2 Power up/down timing

b) When RESET terminal is not used

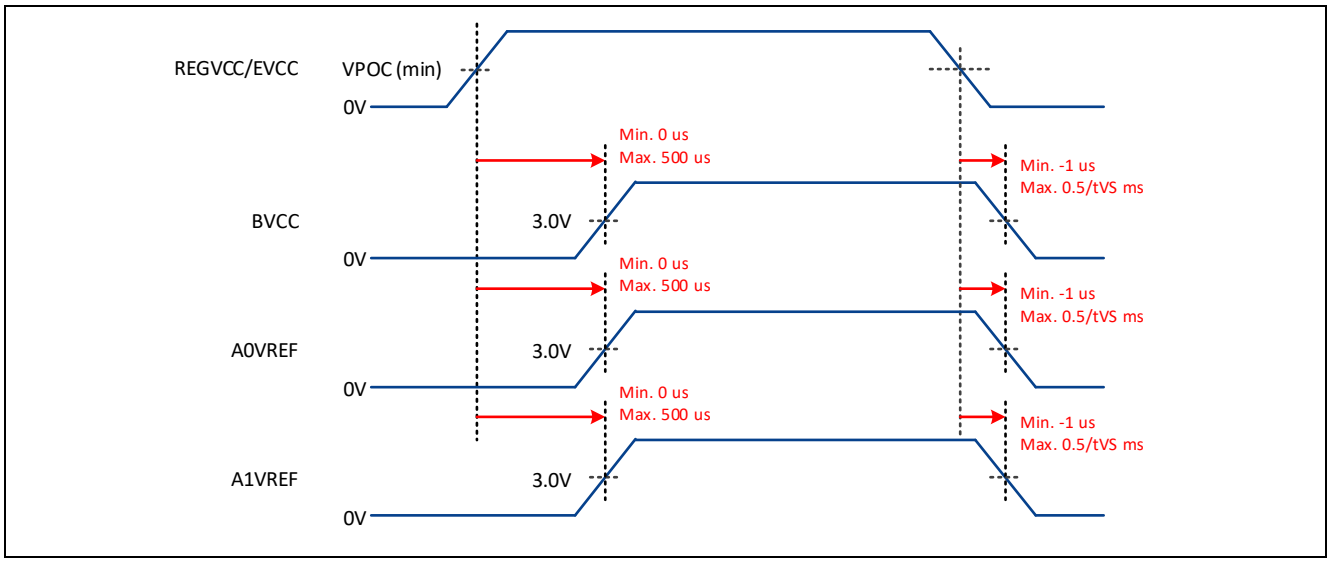


Figure 10: RH850/F1KM-S2 Power up/down timing

Note: For the spec of t_{DPOR}, t_{DRPD} and t_{VS}, please refer to Section 47B.4.5.3, Power Up/Down Timing of the RH850/F1KH, RH850/F1KM Hardware User's Manual.

1.3 Power Supply Overview of RH850/F1KM-S4

1.3.1 Power Supply Pin Overview of RH850/F1KM-S4

The devices of the RH850/F1KM-S4 have the following power supply pins:

- Power supply voltage REGVCC for the on-chip voltage regulators. The output voltage of the voltage regulators is supplied to the digital circuits in each power domain.
- Power supply voltages EVCC and BVCC (depending on device pin count) for the I/O ports.
- Power supply voltages A0VREF and A1VREF (depending on the device pin count) for the A/D converters and the separated I/O ports.

Table 24: RH850/F1KM-S4 Power supply pin overview

Device	Power Supply Pins
RH850/F1KM-S4 (272pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KM-S4 (233pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KM-S4 (176pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KM-S4 (144pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KM-S4 (100pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS

Note: The pins AWOVCL and ISOVCL are available on all devices to connect external stabilization capacitors. Do not use AWOVCL and ISOVCL as power source of other devices.

1.3.2 Power Supply Pin Configuration of RH850/F1KM-S4

The following shows power supply pin configuration. Do not open any power and GND terminals even if those are internally connected.

- The EVCC supply pins are internally connected.
- The BVCC supply pins are internally connected (when available on the device).
- The EVSS pins are internally connected.
- The BVSS pins are internally connected (when available on the device).
- AWOVSS and ISOVSS are internally connected.
- Others are not internally connected.

1.3.3 Power Supply Pin Architecture of RH850/F1KM-S4

The RH850/F1KM-S4 supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1KM-S4 device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1KM-S4:

- REGVCC = EVCC = VPOC to 5.5V
- BVCC = VPOC to REGVCC (when available on the device)
- A0VREF = 3.0V to 5.5V
- A1VREF = 3.0V to 5.5V (when available on the device)
- AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

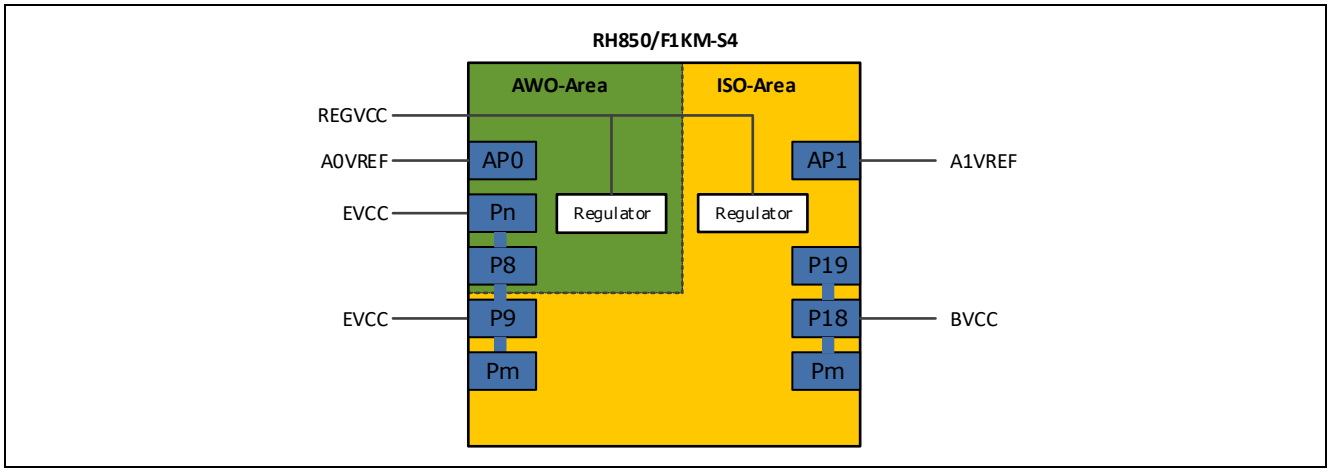


Figure 11: RH850/F1KM-S4 Power supply architecture

Note: The BVCC and A1VREF supply pin availability depends on the chosen device.

Table 25: RH850/F1KM-S4 Overview of power supply architecture cases

Case	Voltage					Permission
	REGVCC	EVCC	BVCC	A0VREF	A1VREF	
Case 1	5V	5V	5V	5V	5V	Operation permitted
Case 2	5V	5V	5V	5V	3.3V	Operation permitted
Case 3	5V	5V	5V	3.3V	5V	Operation permitted
Case 4	5V	5V	5V	3.3V	3.3V	Operation permitted
Case 5	5V	5V	3.3V	5V	5V	Operation permitted
Case 6	5V	5V	3.3V	5V	3.3V	Operation permitted
Case 7	5V	5V	3.3V	3.3V	5V	Operation permitted
Case 8	5V	5V	3.3V	3.3V	3.3V	Operation permitted
Case 9	5V	3.3V	*	*	*	Operation not permitted
Case 10	3.3V	5V	*	*	*	Operation not permitted
Case 11	3.3V	3.3V	5V	*	*	Operation not permitted
Case 12	3.3V	3.3V	3.3V	5V	5V	Operation permitted
Case 13	3.3V	3.3V	3.3V	5V	3.3V	Operation permitted
Case 14	3.3V	3.3V	3.3V	3.3V	5V	Operation permitted
Case 15	3.3V	3.3V	3.3V	3.3V	3.3V	Operation permitted

Note: * means “don’t care”.

Table 26: RH850/F1KM-S4 Power supply architecture with single supply 5V

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 27: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

Case 2 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 28: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 29: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 30: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

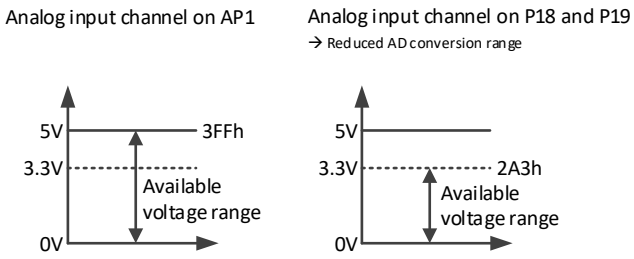
Case 5 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 31: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

Case 6 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 32: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

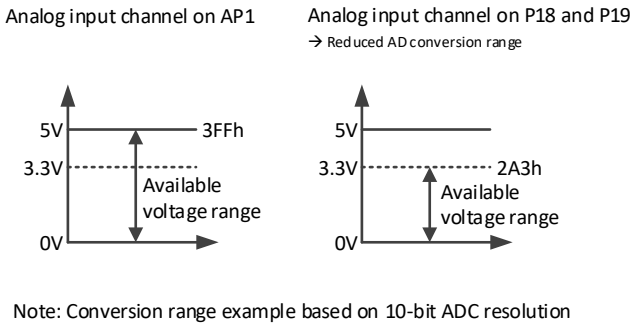
Case 7 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 33: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

Case 8 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 34: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

Case 9, Case 10 – Mixed Supply 5V & 3.3V	
Condition	REGVCC ≠ EVCC EVCC = 3.3V or 5V BVCC = don't care A0VREF = don't care A1VREF = don't care
Port Function	-
Limitation	Common condition REGVCC = EVCC not met
→	**Operation not permitted**

Table 35: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

Case 11 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 5V A0VREF = don't care A1VREF = don't care
Port Function	-
Limitation	Common condition REGVCC ≥ BVCC not met
→	**Operation not permitted**

Table 36: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

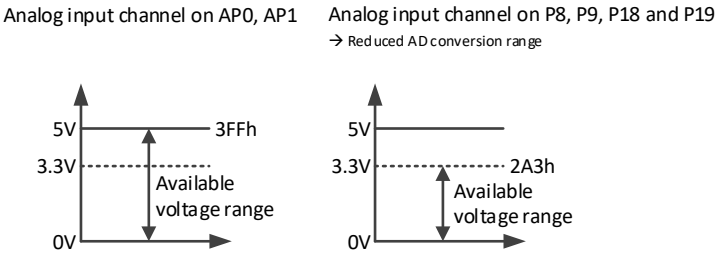
Case 12 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 37: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

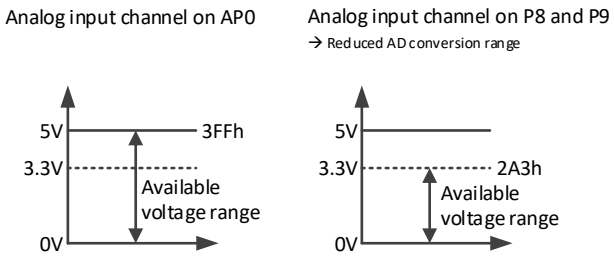
Case 13 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 38: RH850/F1KM-S4 Power supply architecture with mixed supply 5V & 3.3V

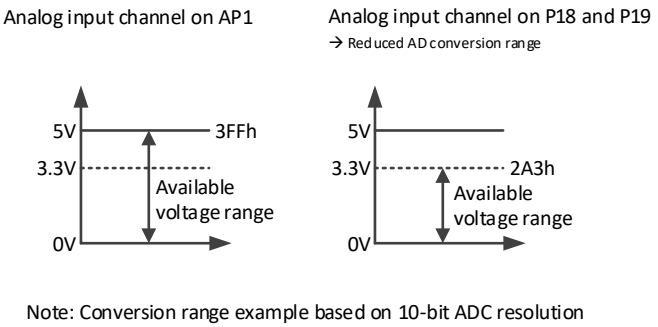
Case 14 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 39: RH850/F1KM-S4 Power supply architecture with single supply 3.3V

Case 15 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

1.3.4 Power Supply Timing of RH850/F1KM-S4

The RH850/F1KM-S4 has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms. Satisfy the spec of voltage slope by using power IC with enable control or by using power IC which starts output over VPOC. The following shows an example of configuration between RH850/F1KM-S4 and PMIC.

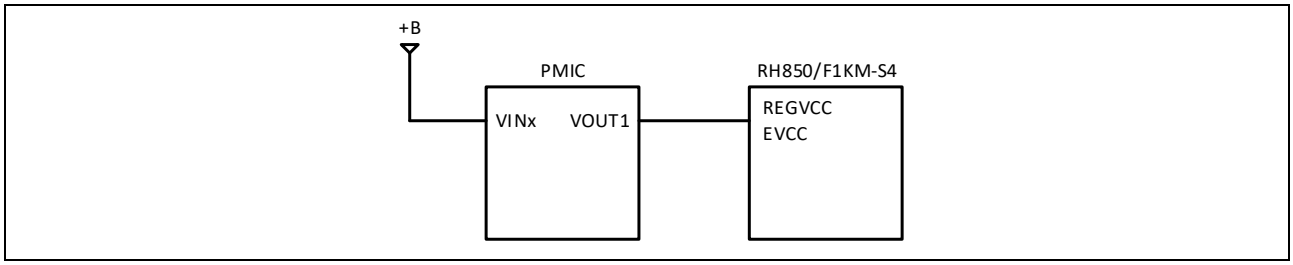


Figure 12: Recommended REGVCC power configuration for RH850/F1KM-S4

The voltage range which has to be kept voltage slope is as follows. There is no voltage slope limitation at the case other than below condition. For detail, see the following figure.

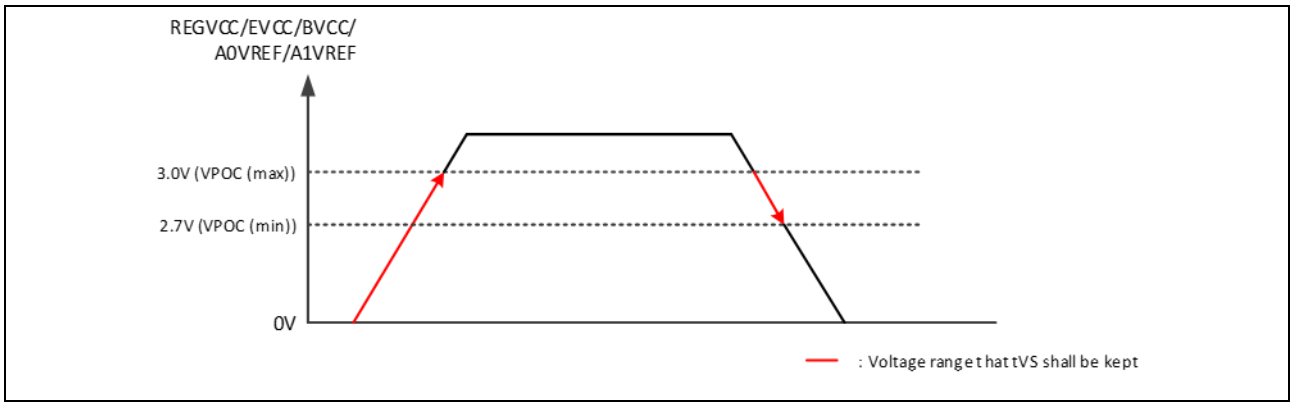


Figure 13: The voltage range which has to be kept voltage slope for RH850/F1KM-S4

Note: When the power source rises again, keep the spec of “REGVCC minimum width (t_{W_POC})“, which is specified in the Section 47B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

For details on the electrical characteristics, please refer to Section 47B, Electrical Characteristics of RH850/F1KM-S4, RH850/F1KM-S2 of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

a) When $\overline{\text{RESET}}$ terminal is used

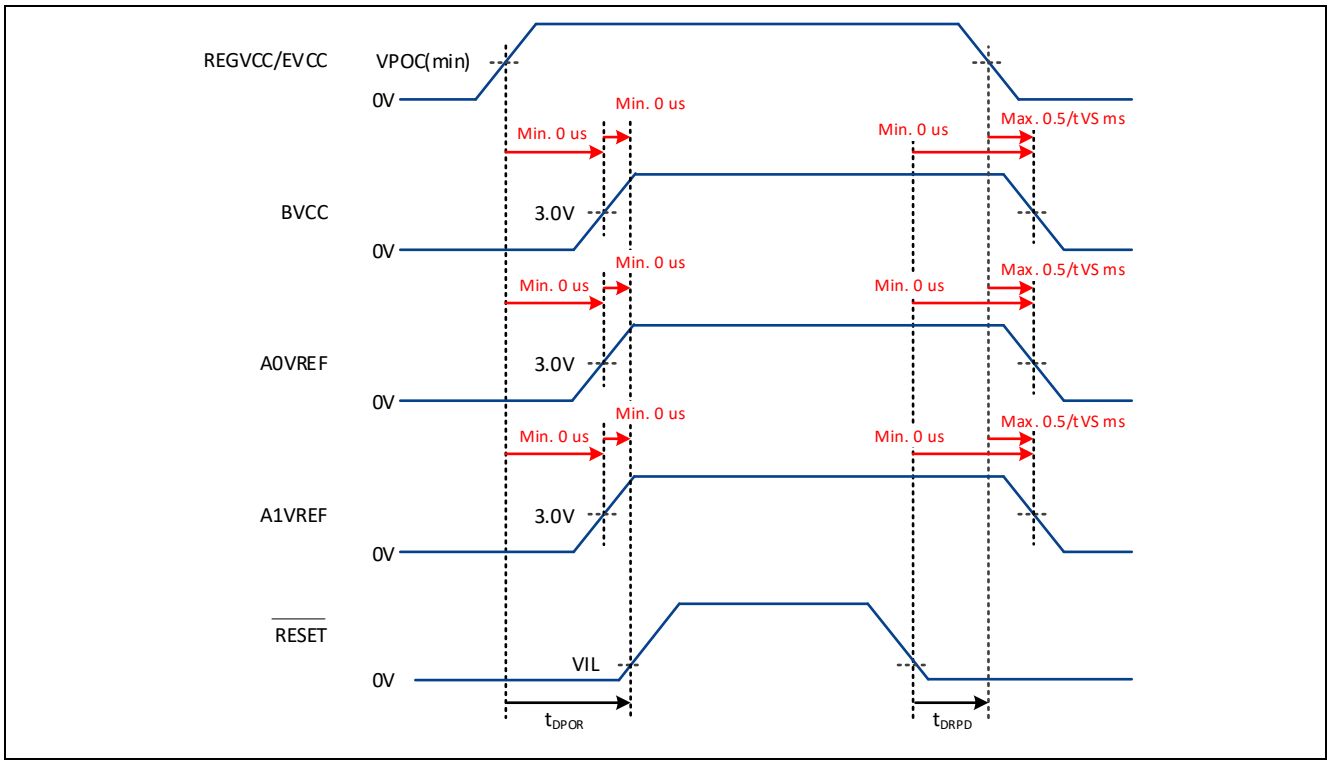


Figure 14: RH850/F1KM-S4 Power up/down timing

b) When $\overline{\text{RESET}}$ terminal is not used

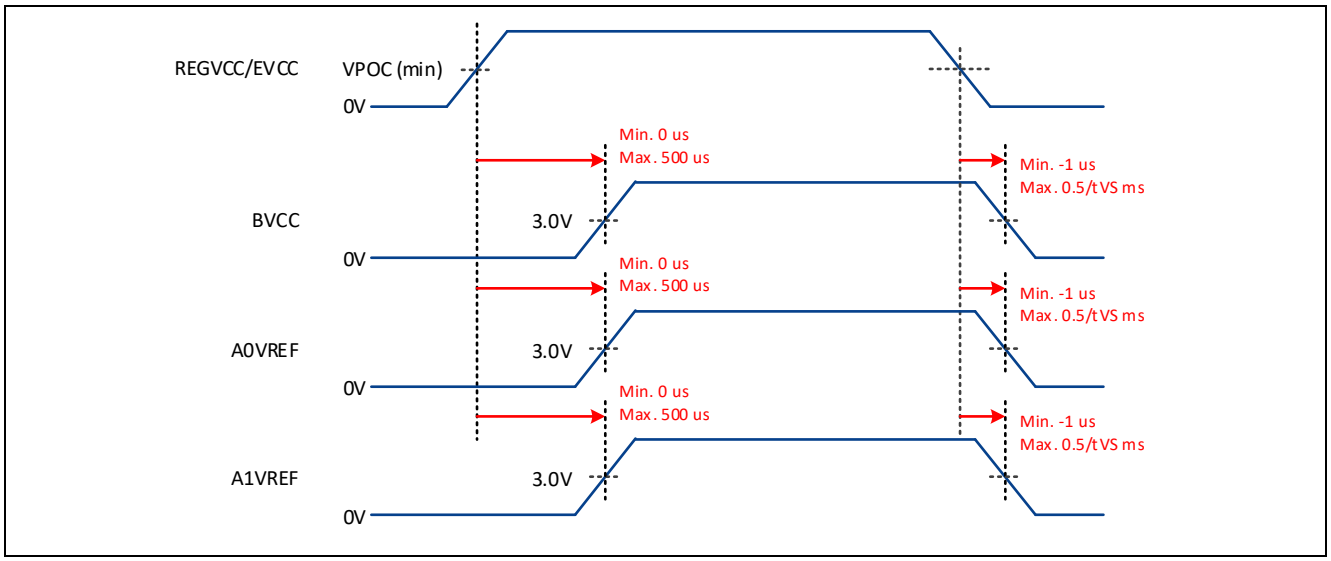


Figure 15: RH850/F1KM-S4 Power up/down timing

Note: For the spec of t_{DPOR}, t_{DRPD} and t_{VS}, please refer to Section 47B.4.5.3, Power Up/Down Timing of the RH850/F1KH, RH850/F1KM Hardware User's Manual.

1.4 Power Supply Overview of RH850/F1KH-D8

1.4.1 Power Supply Pin Overview of RH850/F1KH-D8

The devices of the RH850/F1KH-D8 have the following power supply pins:

- Power supply voltage REG0VCC and REG1VCC for the on-chip voltage regulators. The output voltage of the voltage regulators is supplied to the digital circuits in each power domain.
- Power supply voltages EVCC and BVCC for the I/O ports.
- Power supply voltages A0VREF and A1VREF for the A/D converters and the separated I/O ports.

Table 40: RH850/F1HM-D8 Power supply pin overview

Device	Power Supply Pins
RH850/F1KH-D8 (324pin)	REG0VCC, REG1VCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KH-D8 (233pin)	REG0VCC, REG1VCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1KH-D8 (176pin)	REG0VCC, REG1VCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS BVCC, BVSS A0VREF, A0VSS A1VREF, A1VSS

Note: The pins AWOVCL and ISOVCL are available on all devices to connect external stabilization capacitors. Do not use AWOVCL and ISOVCL as power source of other devices.

1.4.2 Power Supply Pin Configuration of RH850/F1KH-D8

The following shows power supply pin configuration. Do not open any power and GND terminals even if those are internally connected.

- The EVCC supply pins are internally connected.
- The BVCC supply pins are internally connected.
- The EVSS pins are internally connected.
- The BVSS pins are internally connected.
- AWOVSS and ISOVSS are internally connected.
- Others are not internally connected.

1.4.3 Power Supply Pin Architecture of RH850/F1KH-D8

The RH850/F1KH-D8 supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1KH-D8 device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1KH-D8:

REG0VCC = EVCC = VPOC to 5.5V

REG1VCC = VPOC to 3.6V

REG1VCC ≤ REG0VCC

BVCC = VPOC to REG0VCC

A0VREF = 3.0V to 5.5V

A1VREF = 3.0V to 5.5V

AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

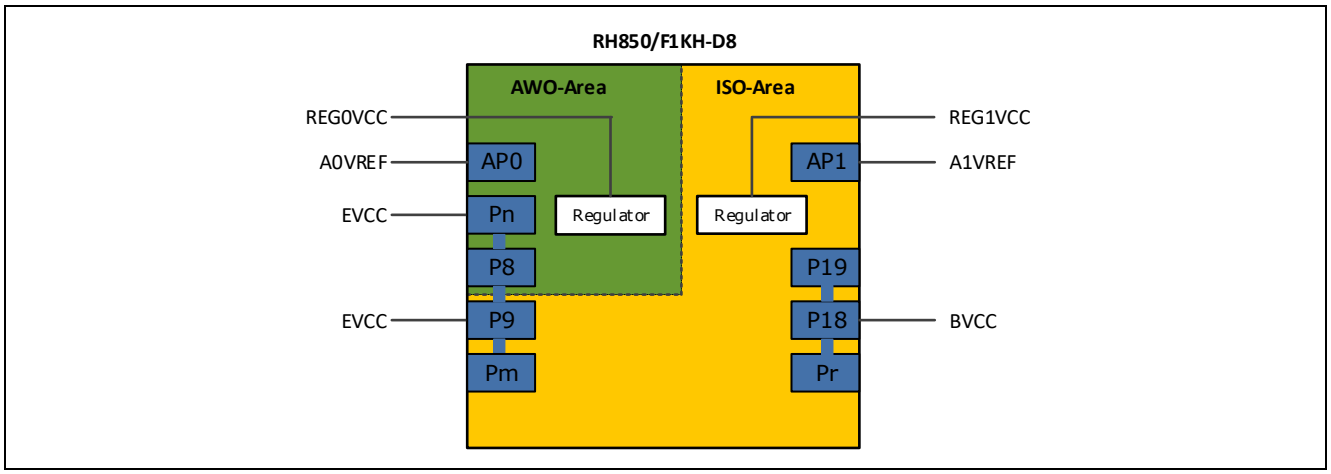


Figure 16: RH850/F1KH-D8 Power supply architecture

Table 41: RH850/F1KH-D8 Overview of power supply architecture cases

Case	Voltage						Permission
	REG0VCC	REG1VCC	EVCC	BVCC	A0VREF	A1VREF	
Case 1	5V	5V	*	*	*	*	Operation not permitted
Case 2	5V	3.3V	5V	5V	5V	5V	Operation permitted
Case 3	5V	3.3V	5V	5V	5V	3.3V	Operation permitted
Case 4	5V	3.3V	5V	5V	3.3V	5V	Operation permitted
Case 5	5V	3.3V	5V	5V	3.3V	3.3V	Operation permitted
Case 6	5V	3.3V	5V	3.3V	5V	5V	Operation permitted
Case 7	5V	3.3V	5V	3.3V	5V	3.3V	Operation permitted
Case 8	5V	3.3V	5V	3.3V	3.3V	5V	Operation permitted
Case 9	5V	3.3V	5V	3.3V	3.3V	3.3V	Operation permitted
Case 10	5V	3.3V	3.3V	*	*	*	Operation not permitted
Case 11	3.3V	5V	*	*	*	*	Operation not permitted
Case 12	3.3V	3.3V	5V	*	*	*	Operation not permitted
Case 13	3.3V	3.3V	3.3V	5V	*	*	Operation not permitted
Case 14	3.3V	3.3V	3.3V	3.3V	5V	5V	Operation permitted
Case 15	3.3V	3.3V	3.3V	3.3V	5V	3.3V	Operation permitted
Case 16	3.3V	3.3V	3.3V	3.3V	3.3V	5V	Operation permitted
Case 17	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	Operation permitted

Note: * means “don’t care”.

Table 42: RH850/F1KH-D8 Power supply architecture with single supply 5V

Case 1 – Single Supply 5V	
Condition	REG0VCC = 5V REG1VCC = 5V EVCC = don’t care BVCC = don’t care A0VREF = don’t care A1VREF = don’t care
Port Function	-
Limitation	Common condition of REG1VCC (REG1VCC ≤ 3.6V) not met
→	**Operation not permitted**

Table 43: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 2 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 44: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 45: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 4 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 46: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 5 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 47: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

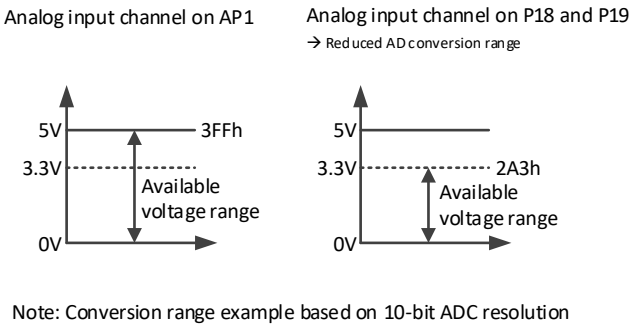
Case 6 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 48: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 7 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 49: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

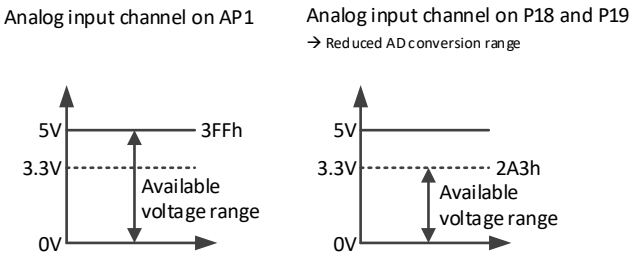
Case 8 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 3.3V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 50: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 9 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 5V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 51: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 10 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 5V REG1VCC = 3.3V EVCC = 3.3V BVCC = don’t care A0VREF = don’t care A1VREF = don’t care
Port Function	-
Limitation	Common condition REG0VCC = EVCC not met
→	**Operation not permitted**

Table 52: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 11 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 3.3V REG1VCC = 5V EVCC = don’t care BVCC = don’t care A0VREF = don’t care A1VREF = don’t care
Port Function	-
Limitation	Common condition of REG1VCC (REG1VCC ≤ 3.6V) not met
→	**Operation not permitted**

Table 53: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 12 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 3.3V REG1VCC = 3.3V EVCC = 5V BVCC = don't care A0VREF = don't care A1VREF = don't care
Port Function	-
Limitation	Common condition REG0VCC = EVCC not met
→	**Operation not permitted**

Table 54: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

Case 13 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 3.3V REG1VCC = 3.3V EVCC = 3.3V BVCC = 5V A0VREF = don't care A1VREF = don't care
Port Function	-
Limitation	Common condition REG0VCC ≥ BVCC not met
→	**Operation not permitted**

Table 55: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

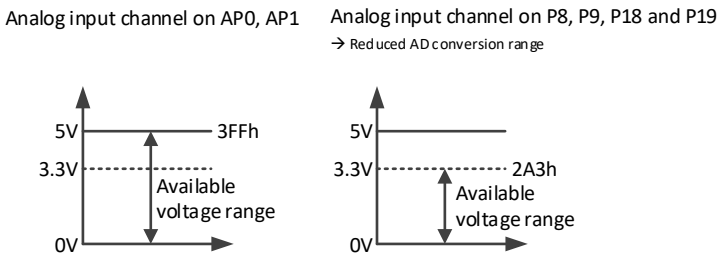
Case 14 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 3.3V REG1VCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Table 56: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

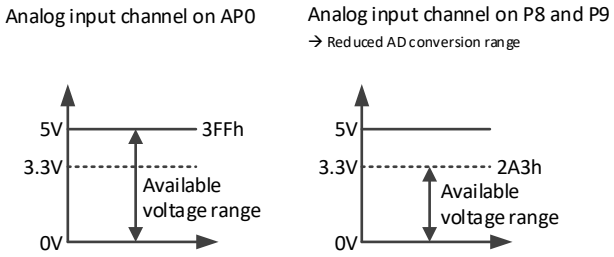
Case 15 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 3.3V REG1VCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 57: RH850/F1KH-D8 Power supply architecture with mixed supply 5V & 3.3V

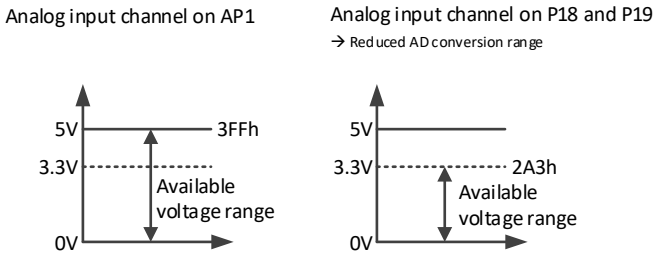
Case 16 – Mixed Supply 5V & 3.3V	
Condition	REG0VCC = 3.3V REG1VCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Table 58: RH850/F1KH-D8 Power supply architecture with single supply 3.3V

Case 17 – Single Supply 3.3V	
Condition	REG0VCC = 3.3V REG1VCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

1.4.4 Power Supply Timing of RH850/F1KH-D8

The RH850/F1KH-D8 has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms. Satisfy the spec of voltage slope by using power IC with enable control or by using power IC which starts output over VPOC. The following shows an example of configuration between RH850/F1KH-D8 and PMIC.

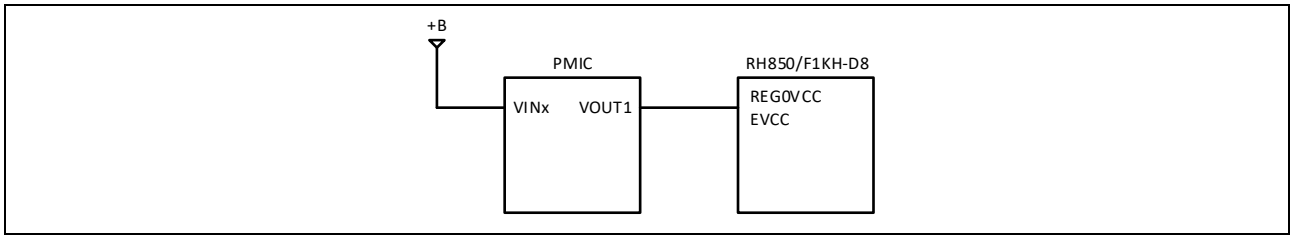


Figure 17: Recommended REG0VCC power configuration for RH850/F1KH-D8

The voltage range which has to be kept voltage slope is as follows. There is no voltage slope limitation at the case other than below condition. For detail, see the following figure.

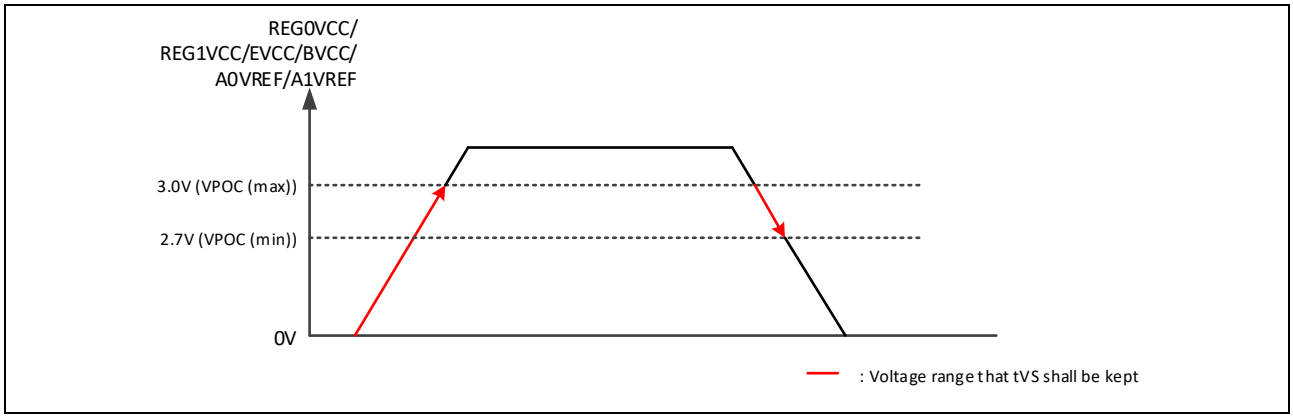


Figure 18: The voltage range which has to be kept voltage slope for RH850/F1KH-D8

Note: When the power source rises again, keep the spec of “REGVCC minimum width (t_{W_POC})“, which is specified in the Section 47A.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

For details on the electrical characteristics, please refer to Section 47A, Electrical Characteristics of RH850/F1KH-D8 of the RH850/F1KH, RH850/F1KM Hardware User’s Manual.

a) When $\overline{\text{RESET}}$ terminal is used

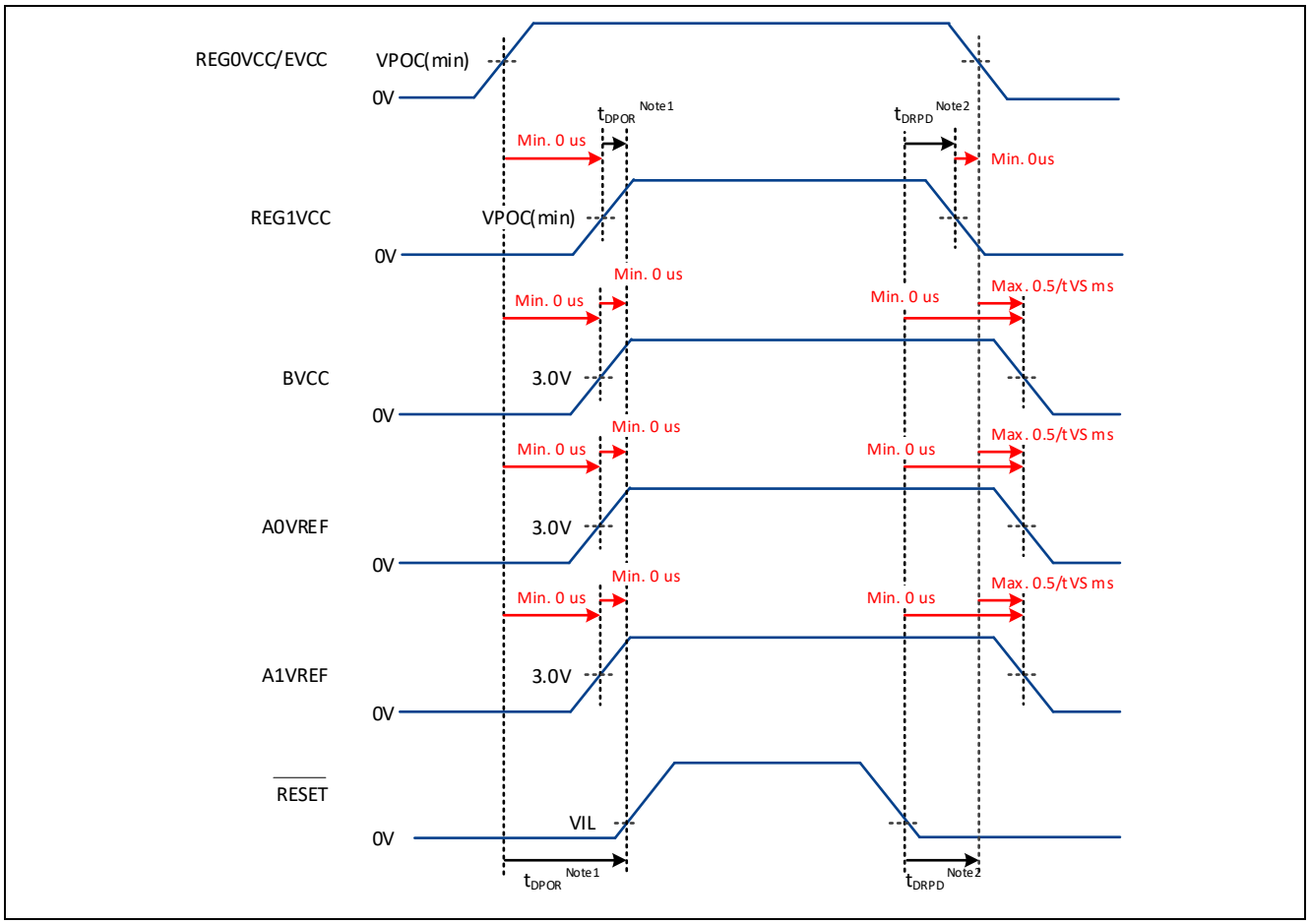


Figure 19: RH850/F1KH-D8 Power up/down timing

Note 1. Both t_{DPOR} timing should be kept.
Note 2. Both t_{DRPD} timing should be kept.
Note 3. For the spec of t_{DPOR}, t_{DRPD} and t_{VS}, please refer to Section 47A.4.5.3, Power Up/Down Timing of the RH850/F1KH, RH850/F1KM Hardware User's Manual.

b) When $\overline{\text{RESET}}$ terminal is not used

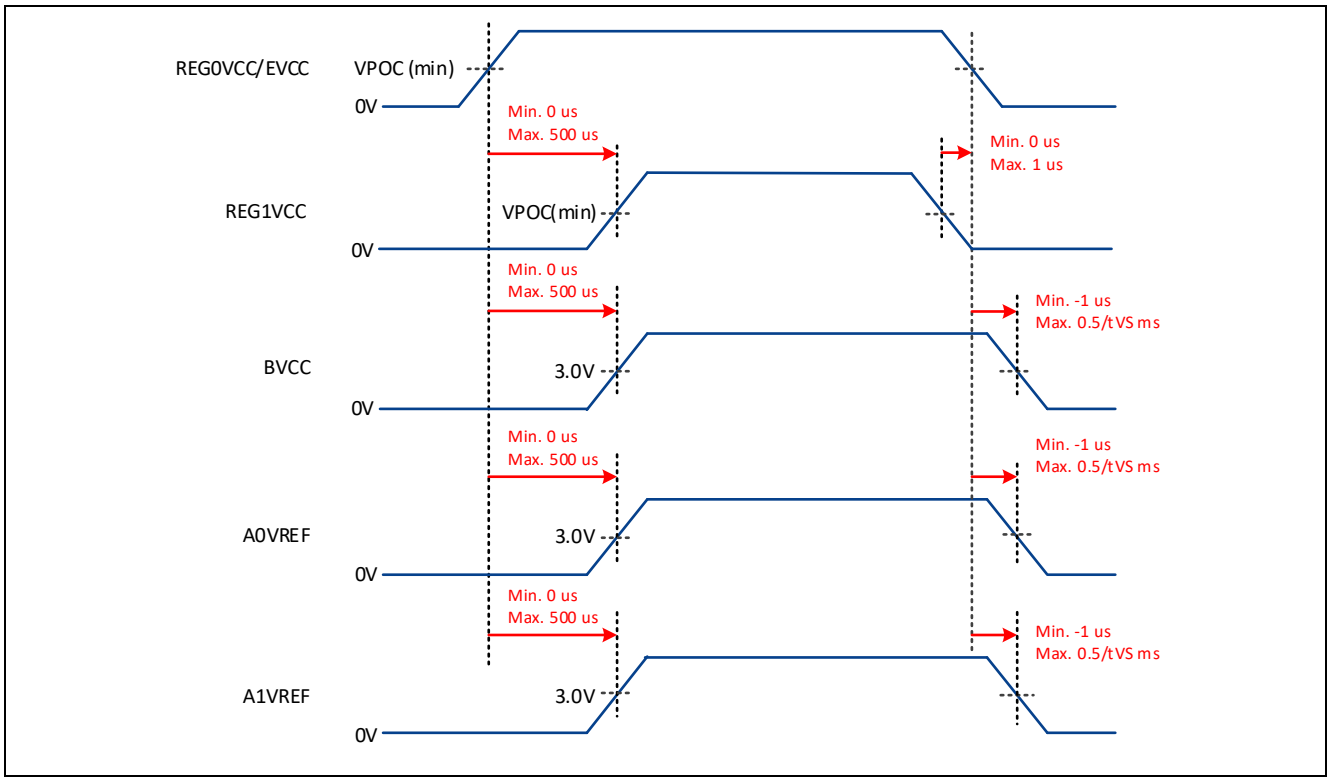


Figure 20: RH850/F1KH-D8 Power up/down timing

Note: tVS is the timing of the voltage slope

1.5 Power Supply Overview of RH850/F1K

1.5.1 Power Supply Pin Overview of RH850/F1K

The devices of the RH850/F1K have the following power supply pins:

- Power supply voltage REGVCC for the on-chip voltage regulators. The output voltage of the voltage regulators is supplied to the digital circuits in each power domain.
- Power supply voltage EVCC for the I/O ports.
- Power supply voltages A0VREF and A1VREF (depending on the device pin count) for the A/D converters and the separated I/O ports.

Table 59: RH850/F1K Power supply pin overview

Device	Power Supply Pins
RH850/F1K (176pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1K (144pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS A1VREF, A1VSS
RH850/F1K (100pin)	REGVCC AWOVCL[Note], AWOVSS ISOVCL[Note], ISOVSS EVCC, EVSS A0VREF, A0VSS

Note: The pins AWOVCL and ISOVCL are available on all devices to connect external stabilization capacitors. Do not use AWOVCL and ISOVCL as power source of other devices.

1.5.2 Power Supply Pin Configuration of RH850/F1K

The following shows power supply pin configuration. Do not open any power and GND terminals even if those are internally connected.

- The EVCC supply pins are internally connected.
- The EVSS pins are internally connected.
- AWOVSS and ISOVSS are internally connected.
- Others are not internally connected.

1.5.3 Power Supply Pin Architecture of RH850/F1K

The RH850/F1K supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1K device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1K:

- REGVCC = EVCC = VPOC to 5.5V
- A0VREF = 3.0V to 5.5V
- A1VREF = 3.0V to 5.5V (when available on the device)
- AWOVSS = ISOVSS = EVSS = A0VSS = A1VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

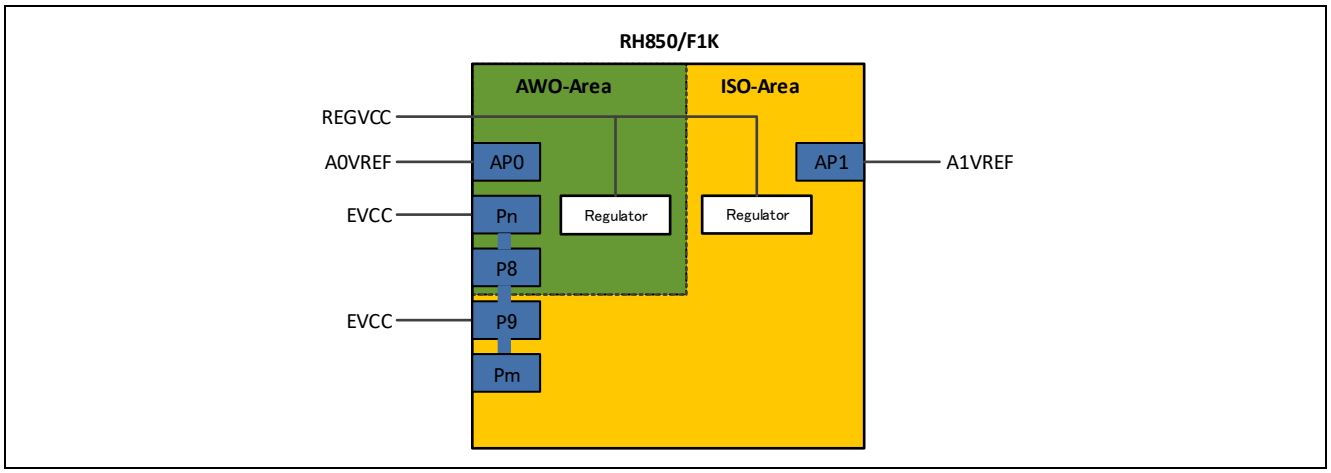


Figure 21: RH850/F1K Power supply architecture

Note: The A1VREF supply pin availability depends on the chosen device.

Table 60: RH850/F1K Overview of power supply architecture cases

Case	Voltage				Permission
	REGVCC	EVCC	A0VREF	A1VREF	
Case 1	5V	5V	5V	5V	Operation permitted
Case 2	5V	5V	5V	3.3V	Operation permitted
Case 3	5V	5V	3.3V	5V	Operation permitted
Case 4	5V	5V	3.3V	3.3V	Operation permitted
Case 5	5V	3.3V	*	*	Operation not permitted
Case 6	3.3V	5V	*	*	Operation not permitted
Case 7	3.3V	3.3V	5V	5V	Operation permitted
Case 8	3.3V	3.3V	5V	3.3V	Operation permitted
Case 9	3.3V	3.3V	3.3V	5V	Operation permitted
Case 10	3.3V	3.3V	3.3V	3.3V	Operation permitted

Note: * means “don’t care”.

Table 61: RH850/F1K Power supply architecture with single supply 5V

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 62: RH850/F1K Power supply architecture with mixed supply 5V & 3.3V

Case 2 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P18
→	Operation permitted

Table 63: RH850/F1K Power supply architecture with mixed supply 5V & 3.3V

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 64: RH850/F1K Power supply architecture with mixed supply 5V & 3.3V

Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group. AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V. When analog input terminal is over 3.3V, do not include the input into an AD scan group.
Limitation	Analog port function limitation applies to P8, P9 and P18
→	Operation permitted

Table 65: RH850/F1K Power supply architecture with mixed supply 5V & 3.3V

Case 5, Case 6 – Mixed Supply 5V & 3.3V	
Condition	REGVCC ≠ EVCC EVCC = 3.3V or 5V A0VREF = don't care A1VREF = don't care
Port Function	-
Limitation	Common condition REGVCC = EVCC not met
→	**Operation not permitted**

Table 66: RH850/F1K Power supply architecture with mixed supply 5V & 3.3V

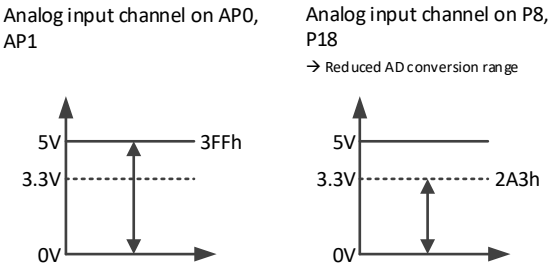
Case 7 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9 and P18
→	Operation permitted

Table 67: RH850/F1K Power supply architecture with mixed supply 5V & 3.3V

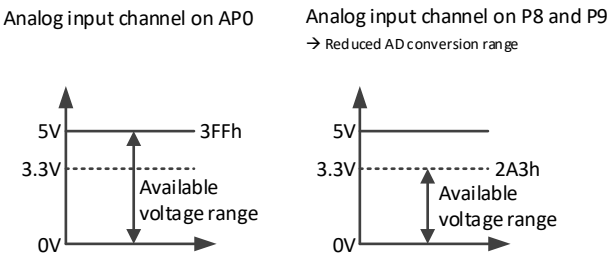
Case 8 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 5V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8 and P9
→	Operation permitted

Table 68: RH850/F1K Power supply architecture with mixed supply 5V & 3.3V

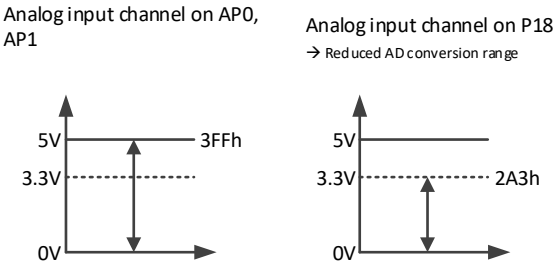
Case 9 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 3.3V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P18
→	Operation permitted

Table 69: RH850/F1K Power supply architecture with single supply 3.3V

Case 10 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

1.5.4 Power Supply Timing of RH850/F1K

The RH850/F1K has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms. Satisfy the spec of voltage slope by using power IC with enable control or by using power IC which starts output over VPOC. The following shows an example of configuration between RH850/F1K and PMIC.

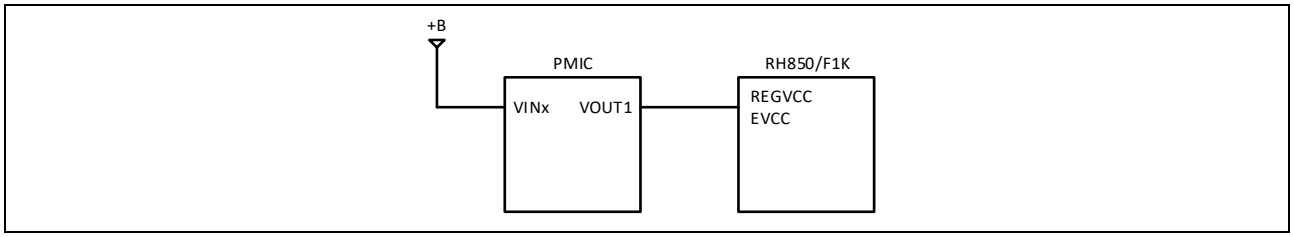


Figure 22: Recommended REGVCC power configuration for RH850/F1K

The voltage range which has to be kept voltage slope is as follows. There is no voltage slope limitation at the case other than below condition. For detail, see the following figure.

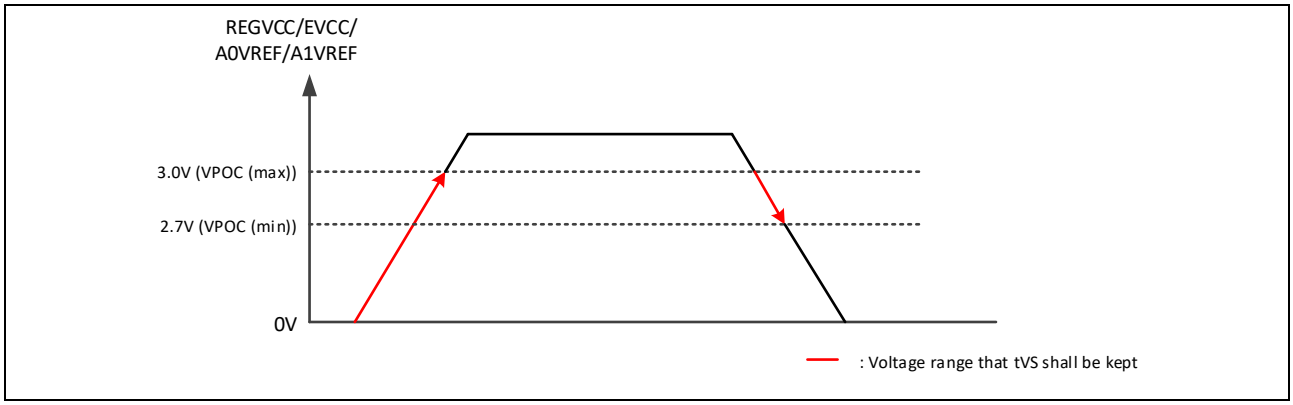


Figure 23: The voltage range which has to be kept voltage slope for RH850/F1K

Note: When the power source rises again, keep the spec of “REGVCC minimum width (t_{W_POC})“ that is specified in the Section 40.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics of the RH850/F1K Hardware User’s Manual.

For details on the electrical characteristics, please refer to the Electrical Characteristics of the RH850/F1K Hardware User’s Manual.

a) When $\overline{\text{RESET}}$ terminal is used

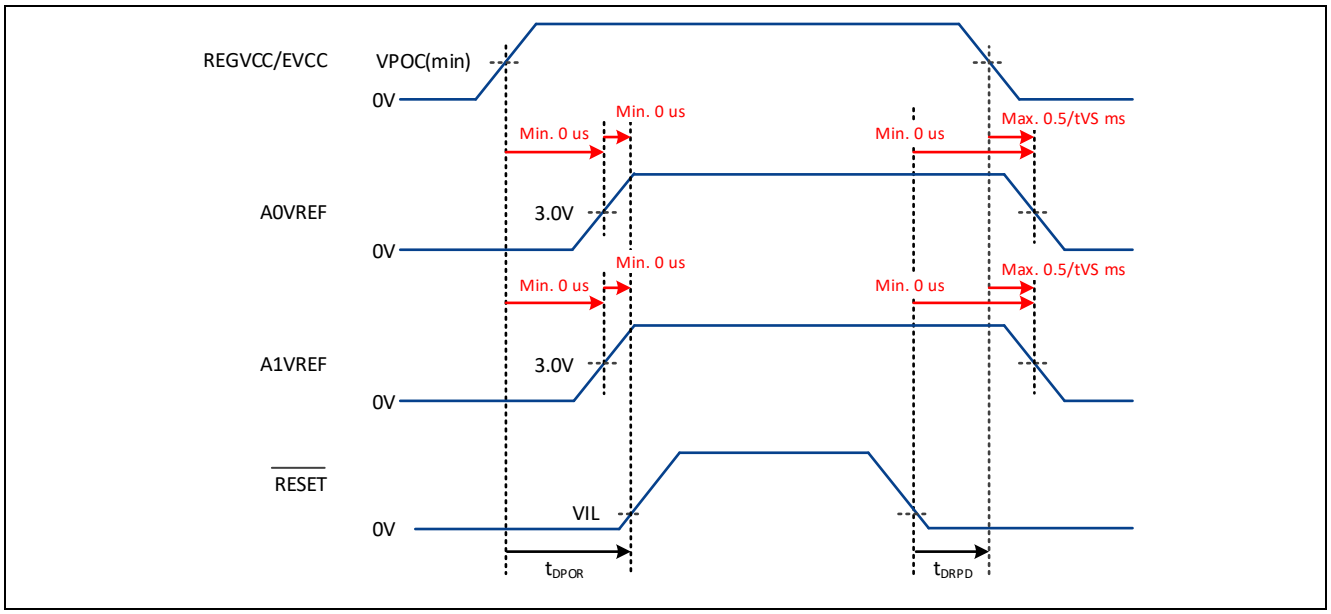


Figure 24: RH850/F1K Power up/down timing

b) When $\overline{\text{RESET}}$ terminal is not used

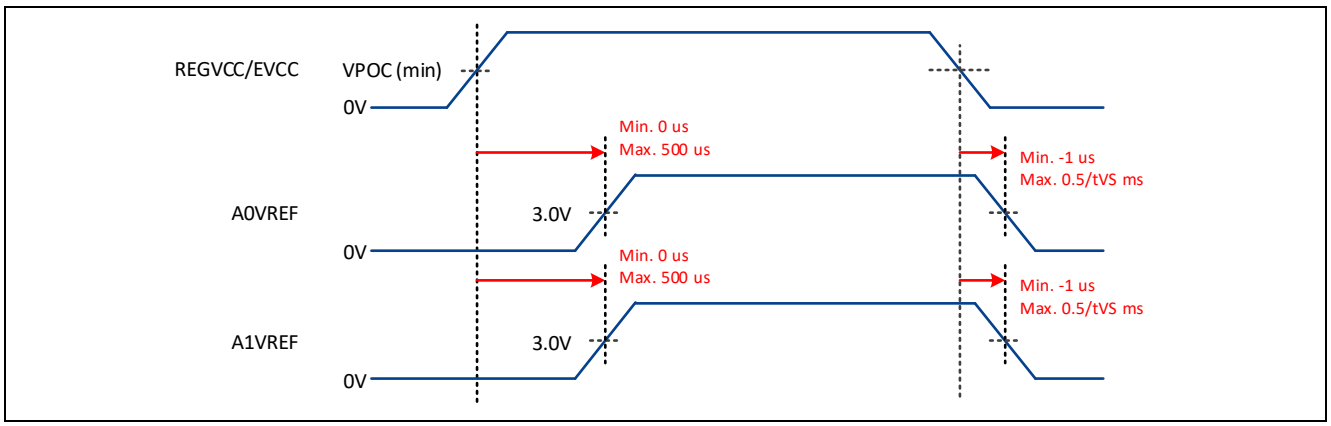


Figure 25: RH850/F1K Power up/down timing

Note: For the spec of t_{DPOR}, t_{DRPD} and t_{VS}, please refer to the Section 40.8.2 Power Up/Down Timing of the RH850/F1K Hardware User's Manual.

1.6 Principle Capacitor Placement at REGVCC of RH850/F1Kx, RH850/F1K Series

It should be considered to add an additional capacitor to the REGVCC pin and to use a close component placement to the supply pin in order to optimize the EMI noise behavior especially during the program and erase operation.

The following recommendations shall be considered for the capacitor placement of the additional capacitor for EMI optimization especially during the program and erase operation at the REGVCC pin:

- Capacitor: 4.7µF or larger
- Pin: REGVCC (F1KH-D8: REG0VCC, REG1VCC)
- Layout/distance: Capacitor within 10mm from mounting pad

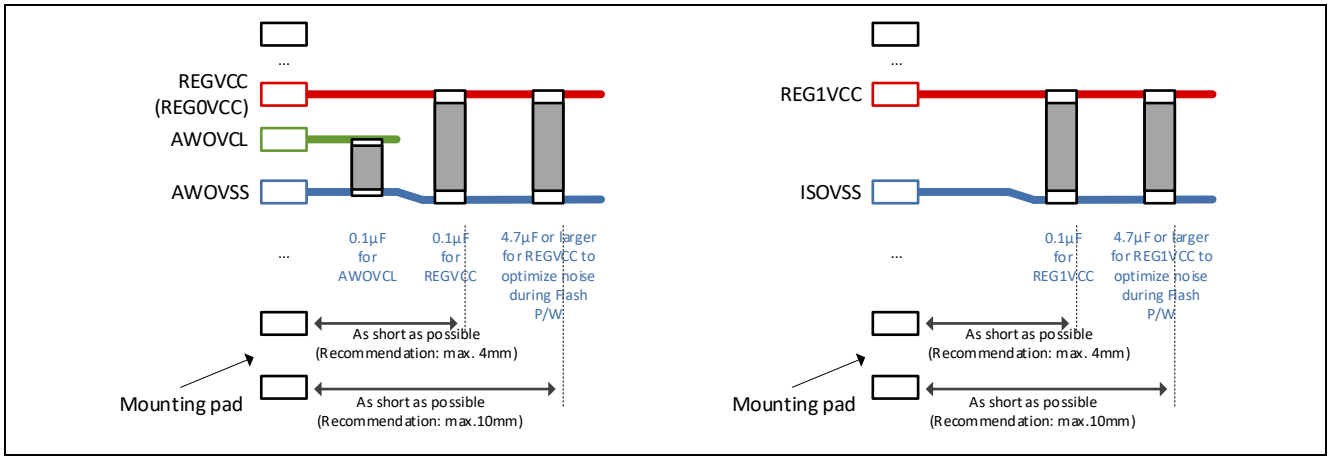


Figure 26: Principle capacitor placement at REGVCC for EMI

2. Minimum External Components

The RH850/F1Kx series requires a certain number of external connections and components for a proper operation in normal operating mode. The components are shown in different categories depending on the device operation and the use case.

2.1 Minimum External Components of RH850/F1KM-S1

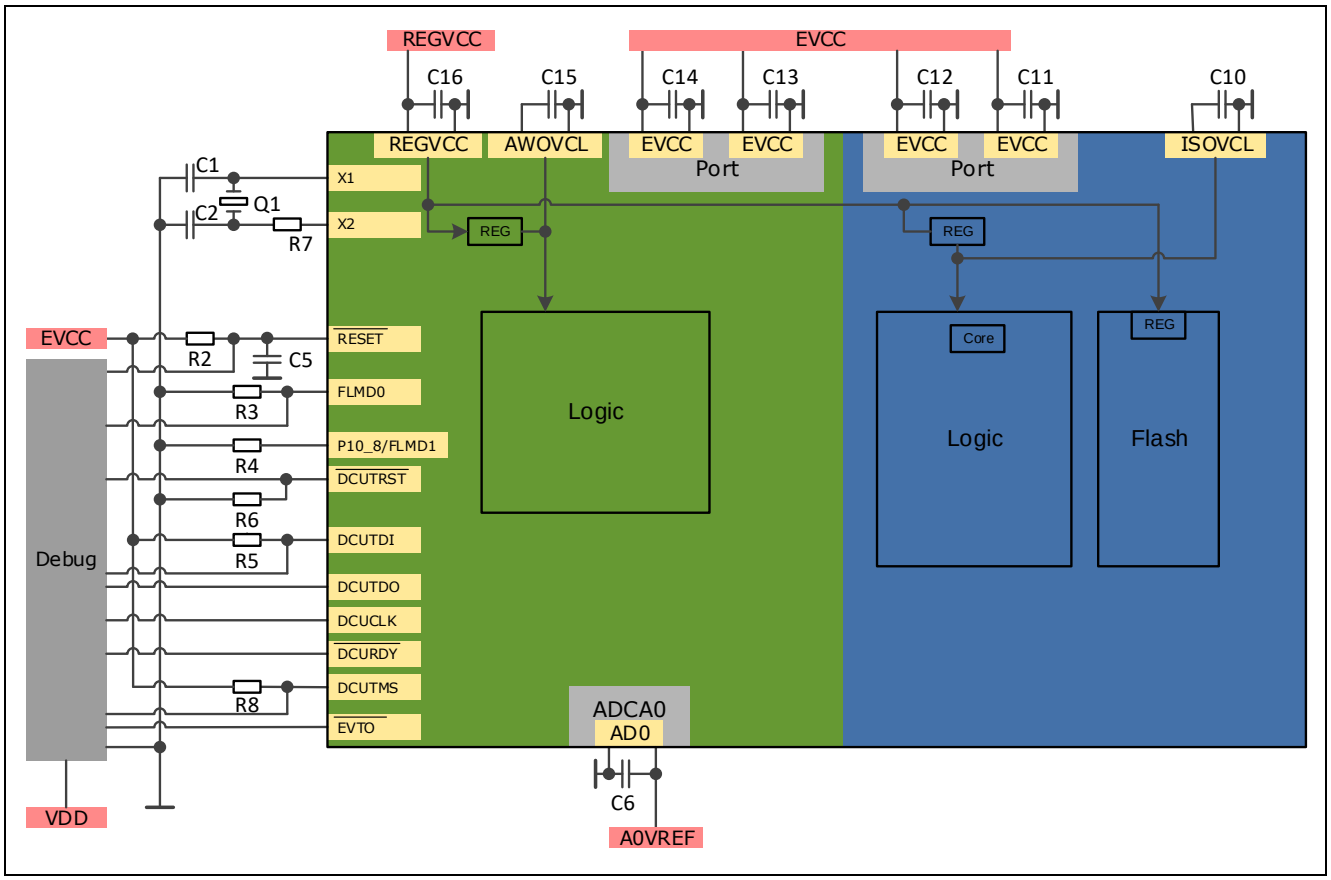


Figure 27: Minimum external components of RH850/F1KM-S1 in normal operating mode

Note: The debug interface connections shown covers Nexus, LPD (1 pin) and LPD (4 pins). For details of the single debug connection, see Chapter 8, Development Tool Interface for the corresponding debug interface. For details of other external components, see their related chapters.

Table 70: Minimum external components of RH850/F1KM-S1 (100pin)

Component	Value			Category
	Min.	Typ.	Max.	
Q1	Note1		Note1	Typical
R2	1kΩ Note 3		10kΩ Note 3	Required
R3	86kΩNote 6			Required
R4	-	10kΩNote 5	-	Typical
R5	1kΩ Note 8		10kΩ Note 8	Typical
R6	10kΩNote 9	-	100kΩNote 9	Required
R7	-	Note 1	-	Typical
R8	-	OptionalNote 10	-	Typical
C1, C2	-	Note 1	-	Typical
C5	-	Note 3	-	Recommended
C6, C11, C12, C13, C14, C16	-	100nFNote 2	-	Recommended
C10, C15	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required

Notes 1. See Chapter 3.1.1, Main Oscillator for details.

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the electrical characteristics (described in the RH850/F1Kx hardware user's manual).

3. See Chapter 4.2.1, Minimum RESET Circuit for details.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS can be applied. But in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (ex. E1 emulator) is not able to apply a high ('1') signal.

8. See Chapters 8, Development Tool Interface and 9, Test Tool Interface for details.

9. See Chapters 4.3.2, JP0_4/ $\overline{\text{DCUTRST}}$, 4.4.1, Recommended Connection of Unused Pins and 8, Development Tool Interface for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See Chapter 8, Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

General guideline and recommendation to improve the electromagnetic interference:

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of typ. 4.7µF or larger in parallel to the capacitor C11 at REGVCC. The value and PCB placement of the parallel capacitor depends on the application requirements.

2.2 Minimum External Components of RH850/F1KM-S2

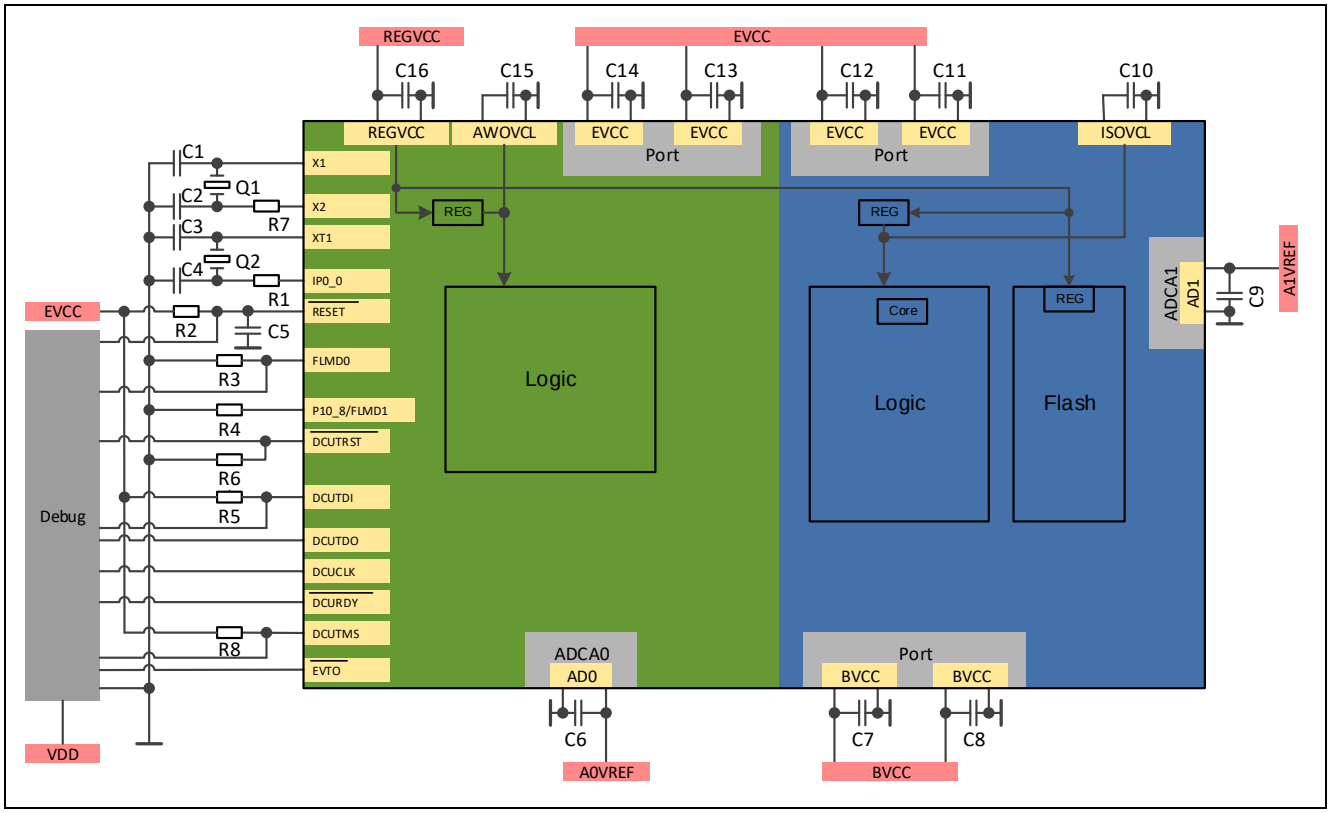


Figure 28: Minimum external components of RH850/F1KM-S2 in normal operating mode

Note: The debug interface connections shown covers Nexus, LPD (1 pin) and LPD (4 pins). For details of the single debug connection, see Chapter 8, Development Tool Interface for the corresponding debug interface. For details of other external components, see their related chapters.

Table 71: Minimum external components for RH850/F1KM-S2 (176pin)

Component	Value			Category
	Min.	Typ.	Max.	
Q1	Note1		Note1	Typical
Q2	-	Note1	-	Typical
R1	-	Note 1	-	Typical
R2	1kΩ Note 3		10kΩ Note 3	Required
R3	86kΩNote 6			Required
R4	-	10kΩNote 5	-	Typical
R5	1kΩ Note 8		10kΩ Note 8	Typical
R6	10kΩNote 9	-	100kΩNote 9	Required
R7	-	Note 1	-	Typical
R8	-	OptionalNote 10	-	Typical
C1, C2	-	Note 1	-	Typical
C3, C4	-	Note 1	-	Typical
C5	-	Note 3	-	Recommended
C6, C7, C8, C9, C11, C12, C13, C14, C16	-	100nFNote 2	-	Recommended
C10, C15	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required

Notes 1. See Chapters 3.1.1, Main Oscillator and 3.1.2, Sub Oscillator for details.

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the electrical characteristics (described in the RH850/F1Kx hardware user's manual).

3. See Chapter 4.2.1, Minimum RESET Circuit for details.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS can be applied. But in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (ex. E1 emulator) is not able to apply a high ('1') signal.

8. See Chapters 8, Development Tool Interface and 9, Test Tool Interface for details.

9. See Chapters 4.3.2, JP0_4/ $\overline{\text{DCUTRST}}$, 4.4.3, Recommended Connection of Unused Pins and 8, Development Tool Interface for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See Chapter 8, Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

General guideline and recommendation to improve the electromagnetic interference:

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of typ. 4.7µF or larger in parallel to the capacitor C16 at REGVCC. The value and PCB placement of the parallel capacitor depends on the application requirements.

2.3 Minimum External Components of RH850/F1KM-S4

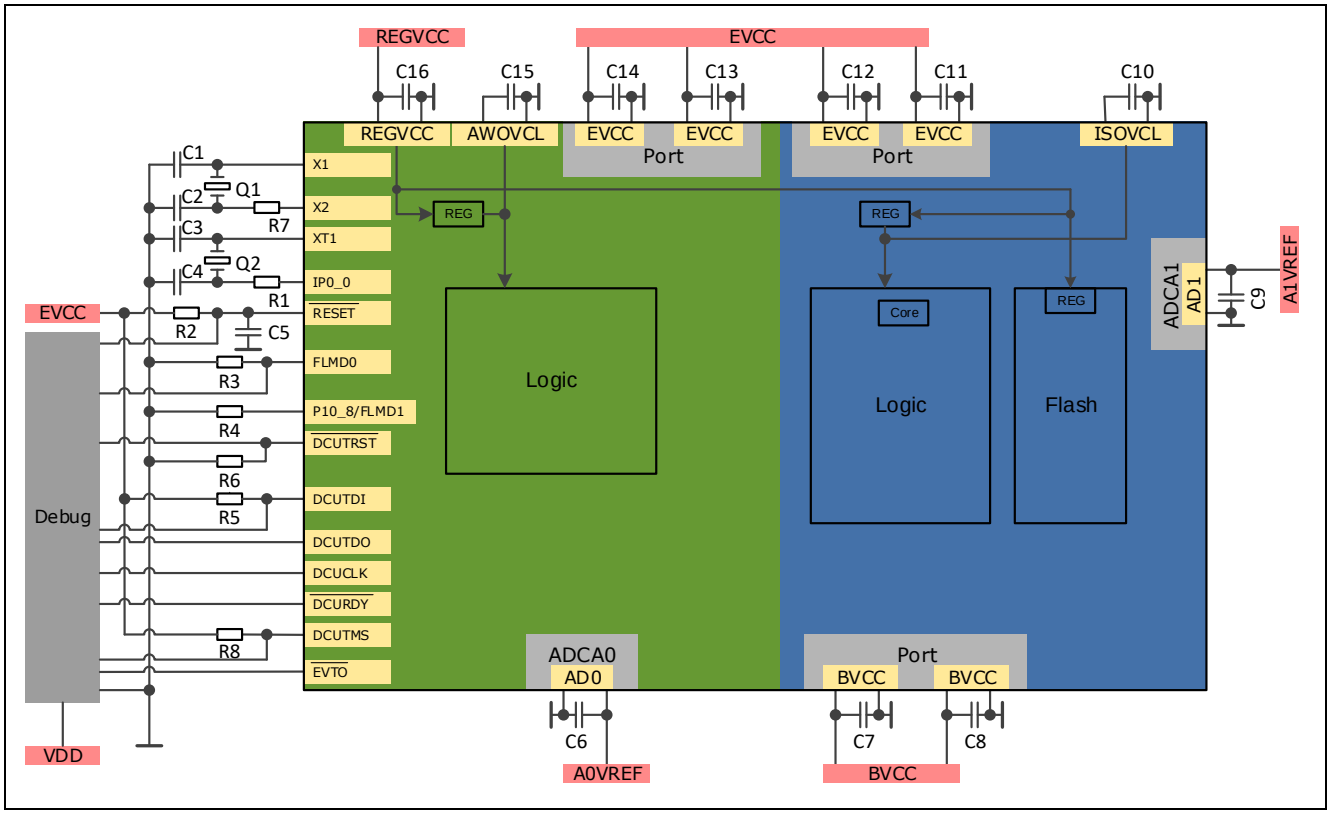


Figure 29: Minimum external components of RH850/F1KM-S4 in normal operating mode

Note: The debug interface connections shown covers Nexus, LPD (1 pin) and LPD (4 pins). For details of the single debug connection, see Chapter 8, Development Tool Interface for the corresponding debug interface. For details of other external components, see their related chapters.

Table 72: Minimum external components for RH850/F1KM-S4 (272pin)

Component	Value			Category
	Min.	Typ.	Max.	
Q1	Note1		Note1	Typical
Q2	-	Note1	-	Typical
R1	-	Note 1	-	Typical
R2	1kΩ Note 3		10kΩ Note 3	Required
R3	86kΩNote 6			Required
R4	-	10kΩNote 5	-	Typical
R5	1kΩ Note 8		10kΩ Note 8	Typical
R6	10kΩNote 9	-	100kΩNote 9	Required
R7	-	Note 1	-	Typical
R8	-	OptionalNote 10	-	Typical
C1, C2	-	Note 1	-	Typical
C3, C4	-	Note 1	-	Typical
C5	-	Note 3	-	Recommended
C6, C7, C8, C9, C11, C12, C13, C14, C16	-	100nFNote 2	-	Recommended
C10, C15	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required

Notes 1. See Chapters 3.1.1, Main Oscillator and 3.1.2, Sub Oscillator for details.

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the electrical characteristics (described in the RH850/F1Kx hardware user's manual).

3. See Chapter 4.2.1, Minimum RESET Circuit for details.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS can be applied. But in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (ex. E1 emulator) is not able to apply a high ('1') signal.

8. See Chapters 8, Development Tool Interface and 9, Test Tool Interface for details.

9. See Chapters 4.3.2, JP0_4/ $\overline{\text{DCUTRST}}$, 4.4.3, Recommended Connection of Unused Pins and 8, Development Tool Interface for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See Chapter 8, Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

General guideline and recommendation to improve the electromagnetic interference:

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of typ. 4.7µF or larger in parallel to the capacitor C16 at REGVCC. The value and PCB placement of the parallel capacitor depends on the application requirements.

2.4 Minimum External Components of RH850/F1KH-D8

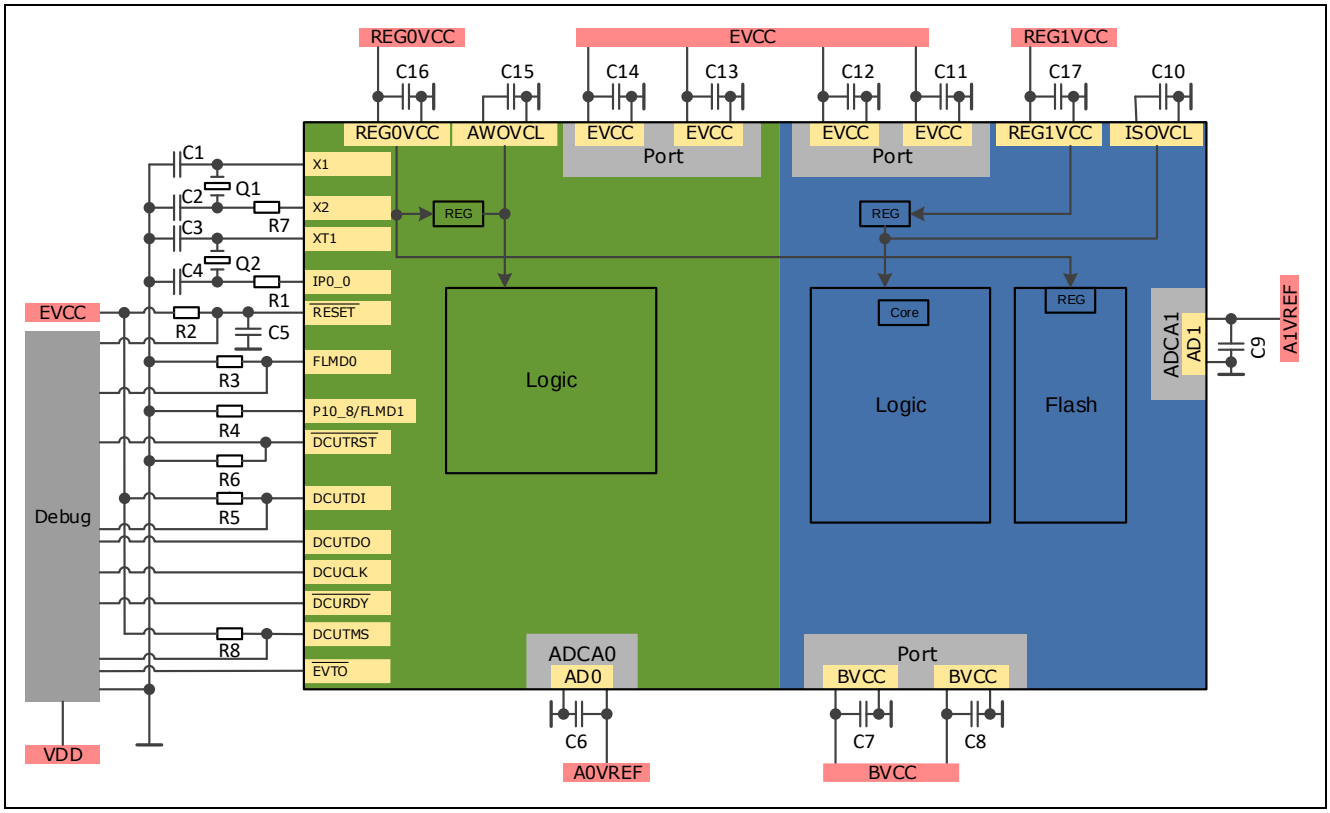


Figure 30: Minimum external components of RH850/F1KH-D8 in normal operating mode

Note: The debug interface connections shown covers Nexus, LPD (1 pin) and LPD (4 pins). For details of the single debug connection, see Chapter 8, Development Tool Interface for the corresponding debug interface. For details of other external components, see their related chapters.

Table 73: Minimum external components for RH850/F1KH-D8 (324pin)

Component	Value			Category
	Min.	Typ.	Max.	
Q1	Note1		Note1	Typical
Q2	-	Note1	-	Typical
R1	-	Note 1	-	Typical
R2	1kΩ Note 3		10kΩ Note 3	Required
R3	86kΩNote 6			Required
R4	-	10kΩNote 5	-	Typical
R5	1kΩ Note 8		10kΩ Note 8	Typical
R6	10kΩNote 9	-	100kΩNote 9	Required
R7	-	Note 1	-	Typical
R8	-	OptionalNote 10	-	Typical
C1, C2	-	Note 1	-	Typical
C3, C4	-	Note 1	-	Typical
C5	-	Note 3	-	Recommended
C6, C7, C8, C9, C11, C12, C13, C14, C16, C17	-	100nFNote 2	-	Recommended
C10, C15	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required

Notes 1. See Chapters 3.1.1, Main Oscillator and 3.1.2, Sub Oscillator for details.

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the electrical characteristics (described in the RH850/F1Kx hardware user's manual).

3. See Chapter 4.2.1, Minimum RESET Circuit for details.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS can be applied. But in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (ex. E1 emulator) is not able to apply a high ('1') signal.

8. See Chapters 8, Development Tool Interface and 9, Test Tool Interface for details.

9. See Chapters 4.3.2, JP0_4/ $\overline{\text{DCUTRST}}$, 4.4.4, Recommended Connection of Unused Pins and 8, Development Tool Interface for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See Chapters 8, Development and 9, Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

General guideline and recommendation to improve the electromagnetic interference:

In order to improve the electromagnetic interference and susceptibility it is recommended to add capacitors of typ. 4.7µF or larger in parallel to the capacitors C16 at REG0VCC and C17 at REG1VCC. The value and PCB placement of the parallel capacitor depends on the application requirements.

2.5 Minimum External Components of RH850/F1K

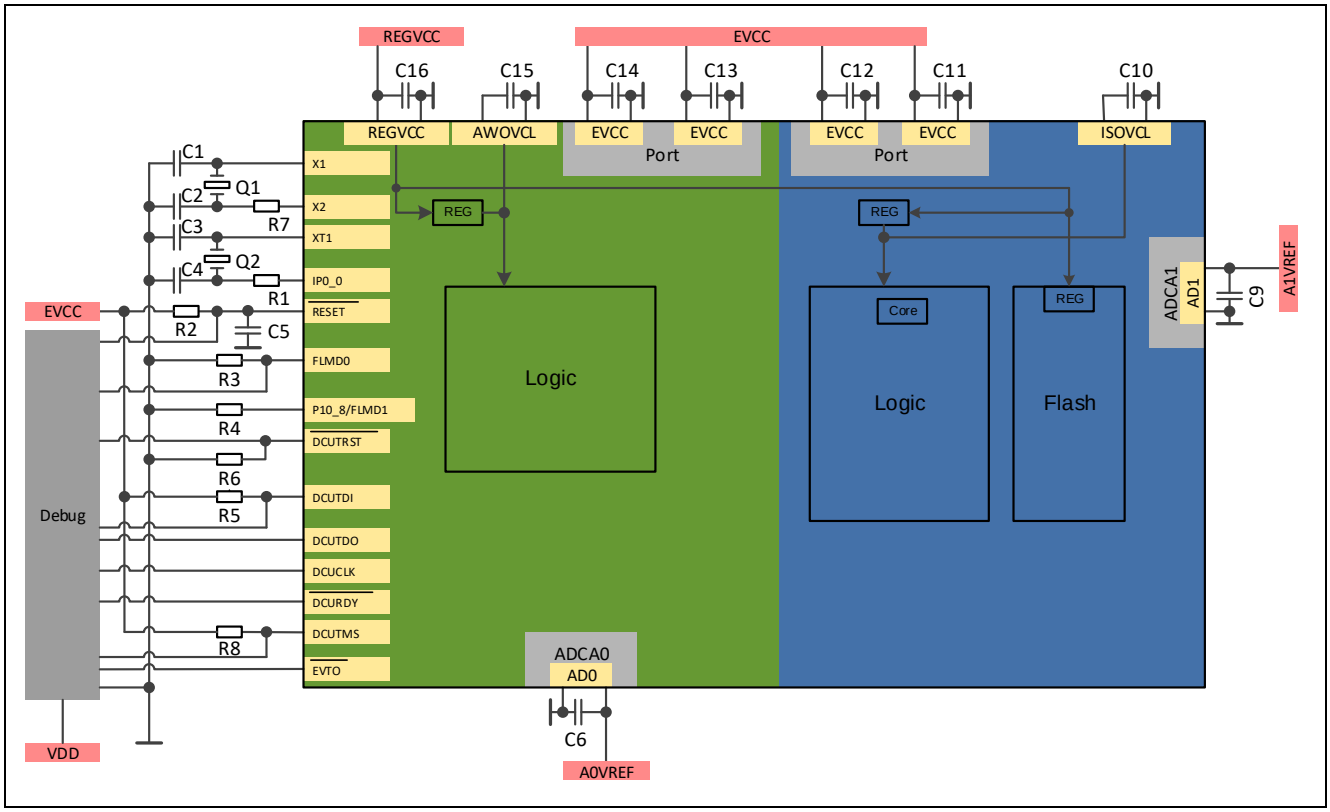


Figure 31: Minimum external components of RH850/F1K in normal operating mode

Note: The debug interface connections shown covers Nexus, LPD (1 pin) and LPD (4 pins). For details of the single debug connection, see Chapter 8, Development Tool Interface for the corresponding debug interface. For details of other external components, see their related chapters.

Table 74: Minimum external components for RH850/F1K (176pin)

Component	Value			Category
	Min.	Typ.	Max.	
Q1	Note1		Note1	Typical
Q2	-	Note1	-	Typical
R1	-	Note 1	-	Typical
R2	1kΩ Note 3		10kΩ Note 3	Required
R3	86kΩNote 6			Required
R4	-	10kΩNote 5	-	Typical
R5	1kΩ Note 8		10kΩ Note 8	Typical
R6	10kΩNote 9	-	100kΩNote 9	Required
R7	-	Note 1	-	Typical
R8	-	OptionalNote 10	-	Typical
C1, C2	-	Note 1	-	Typical
C3, C4	-	Note 1	-	Typical
C5	-	Note 3	-	Recommended
C6, C9, C11, C12, C13, C14, C16	-	100nFNote 2	-	Recommended
C10, C15	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required

Notes 1. See Chapters 3.1.1, Main Oscillator and 3.1.2, Sub Oscillator for details.

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the electrical characteristics (described in the RH850/F1K hardware user's manual).

3. See Chapter 4.2.1, Minimum RESET Circuit for details.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS can be applied. But in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (ex. E1 emulator) is not able to apply a high ('1') signal.

8. See Chapters 8, Development Tool Interface and 9, Test Tool Interface for details.

9. See Chapters 4.3.2, JP0_4/ $\overline{\text{DCUTRST}}$, 4.4.3, Recommended Connection of Unused Pins and 8, Development Tool Interface for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See Chapter 8, Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

General guideline and recommendation to improve the electromagnetic interference:

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of typ. 4.7µF or larger in parallel to the capacitor C16 at REGVCC. The value and PCB placement of the parallel capacitor depends on the application requirements.

3. Oscillator

3.1 Recommended Oscillator Circuit

3.1.1 Main Oscillator

A crystal or ceramic resonator can be connected to the main clock input pins as shown below.

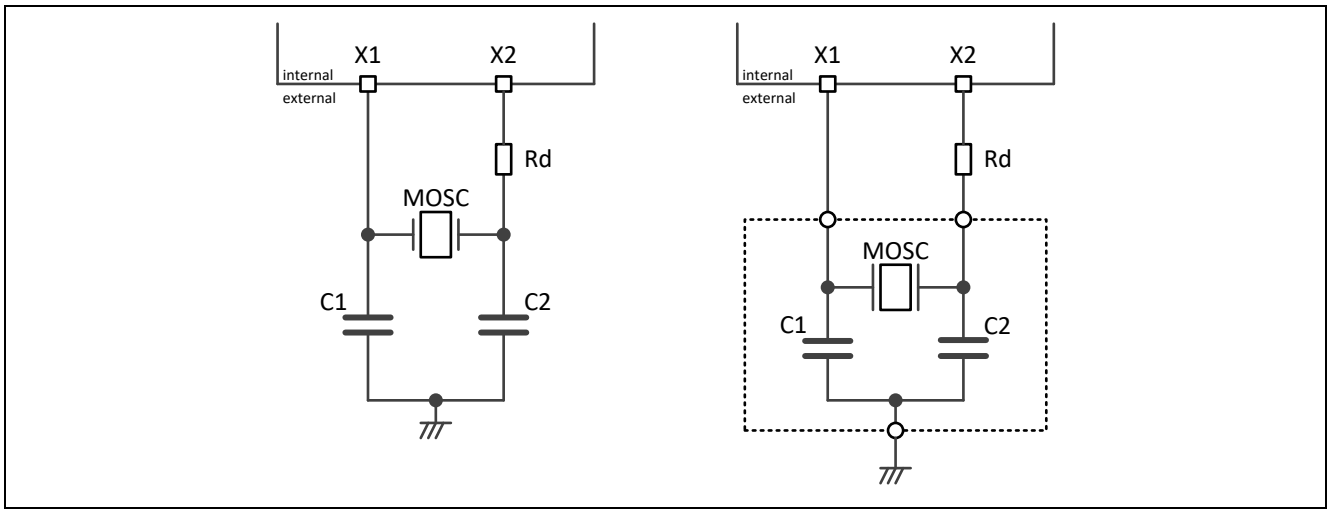


Figure 32: Recommended main oscillator circuit

General guidance values of the main oscillator circuit:

Table 75: Guidance values of the main oscillator circuit

Component	Value
MOSC	RH850/F1Kx: 8MHz, 16MHz, 20MHz, 24MHz RH850/F1K: 16MHz, 20MHz, 24MHz
C1	10pF
C2	10pF
Rd	0Ω

Caution

Values of C1, C2, Rd and amplification gain selection controlled by MOSCC.MOSCAMPSEL[1:0] depend on the use of ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

3.1.2 Sub Oscillator

A crystal resonator can be connected to the sub clock input pins as shown below.

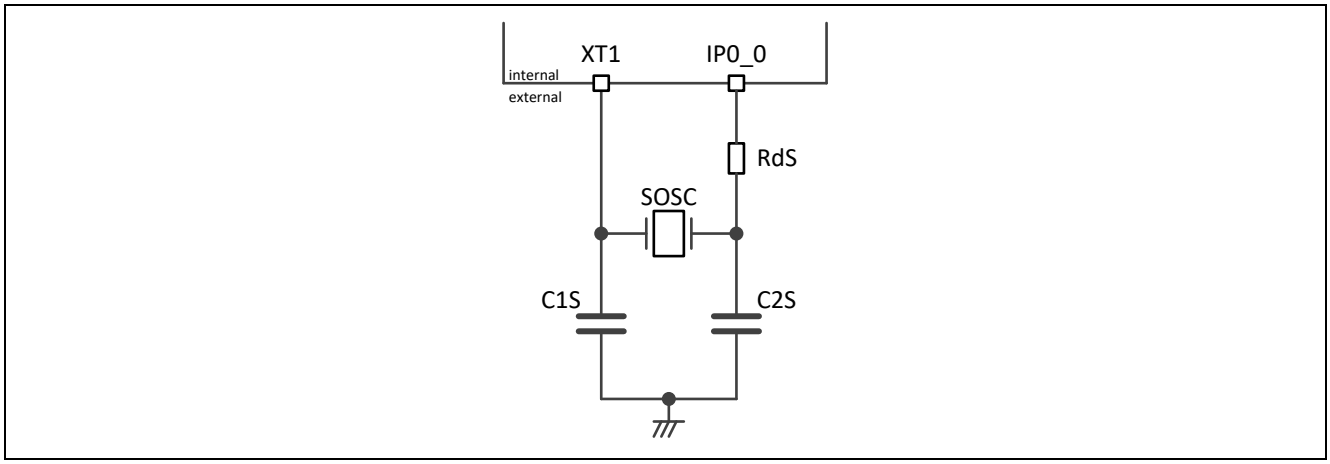


Figure 33: Recommended sub oscillator circuit

General guidance values of the sub oscillator circuit:

Table 76: Guidance values of the sub oscillator circuit

Component	Value
SOSC	32.768kHz
C1S	12pF
C2S	12pF
RdS	100kΩ

Caution

Values of C1S, C2S and RdS depend on the crystal resonator used and must be specified in cooperation with a crystal resonator manufacturer.

3.2 Recommended Oscillator Layout

General guidance for PCB layout:

- Keep the wiring length as short as possible
- Do not cross the wiring with other signal lines
- Do not route this circuit close to a signal line with high fluctuating current flow
- Always make the ground point of the oscillator capacitor the same potential as AWOVSS
- Do not ground the capacitor to a ground pattern with high current flow
- Do not tap signals from the oscillator

4. Device Pins

4.1 X1

4.1.1 Direct Clock Supply to X1

A clock waveform from an external clock source can be used as clock supply to the X1 pin of the microcontroller. The device has to be configured by software (register MOSCM) appropriately for the direct clock input. In this case, set the MOSCM bit of the MOSCM register to 1 before clock input to X1 pin is applied.

The configuration by software has to be done when the main oscillator is stopped and before the direct clock is supplied to X1. These conditions have to be considered when the system is designed.

For the electrical characteristics of the X1 clock input signal, please refer to Sections 47A.3.2, Oscillator Characteristics, 47B.3.2, Oscillator Characteristics or 47C.3.2, Oscillator Characteristics of the RH850/F1KH, RH850/F1KM Hardware User's Manual respectively the Section 40.5 Oscillator Characteristics of the RH850/F1K Hardware User's Manual.

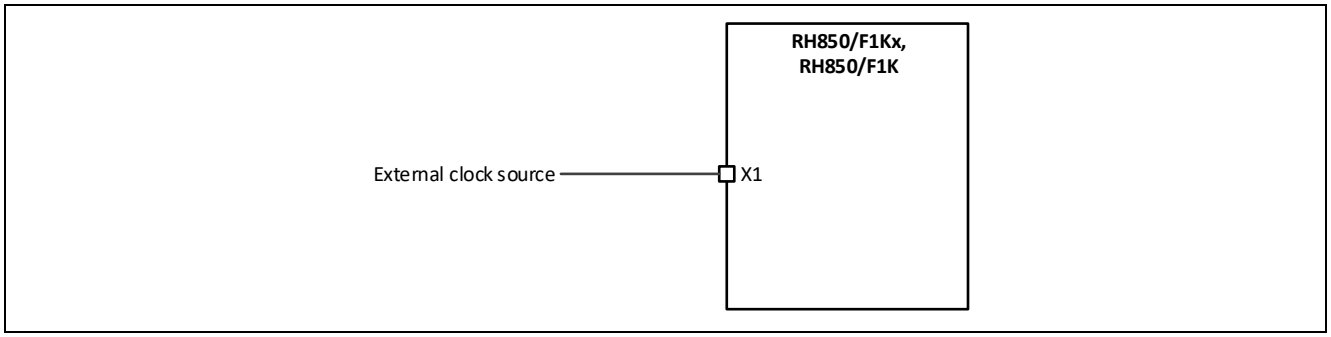


Figure 34: Direct clock supply to X1 (MOSC)

In order to improve the electromagnetic interference and susceptibility it is recommended to add an external filter circuit based on the application requirements.

4.2 RESET

4.2.1 Minimum RESET Circuit

The RH850/F1Kx, RH850/F1K series has an on-chip Power-on Clear (POC) circuit. Therefore, a specific external RESET circuit is not required, and the minimum requirement of the RESET circuit is a resistor to EVCC for start-up of the device. The resistor should be dimensioned large enough to allow a RESET signal generated by development tool or flash programmer to control the $\overline{\text{RESET}}$ pin.

In addition, a capacitor should be added as protection against surges.

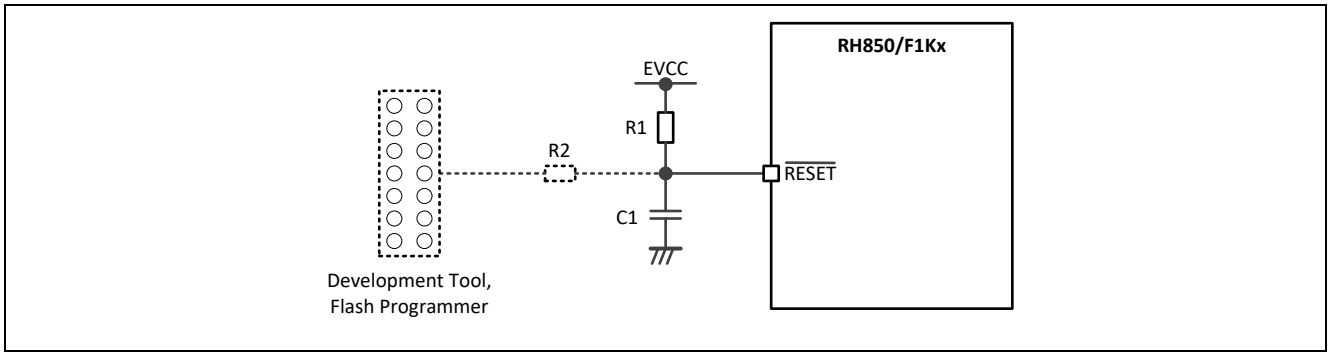


Figure 35: Minimum RESET circuit

General guidance values of the minimum RESET circuit:

Table 77: Guidance values for the minimum RESET circuit

Component	Value
R1	1 to 10kΩ
R2	100Ω
C1	1 to 10nF

The series resistor R2 is optional to suppress external signals from EMC point of view and depends on the application requirements.

The capacitor C1 can be adopted to a different value when the AC specification of the $\overline{\text{RESET}}$ timing, the AC specification of the flash programmer setup timing and the EMC requirements of the ECU are fulfilled.

4.2.2 RESET Input Characteristics

The RESET is passed through an internal analog noise filter to prevent erroneous resets due to spikes.

The following figure shows the timing when an external reset is performed. It explains the effect of the noise elimination.

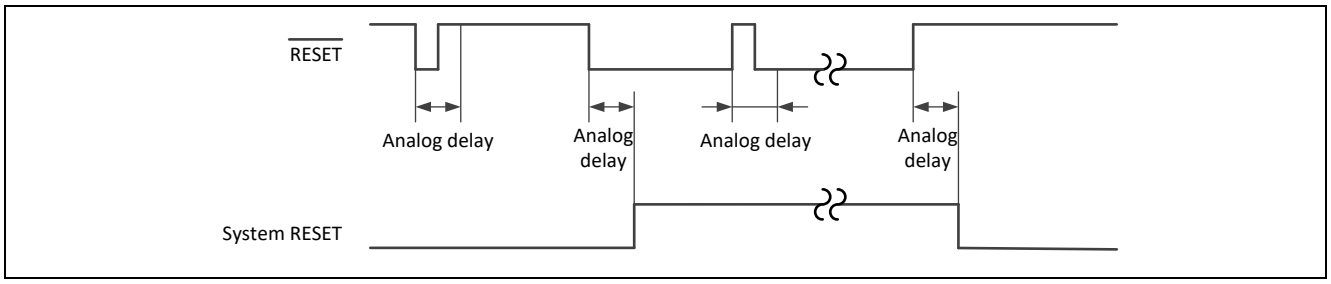


Figure 36: External RESET timing

The analog filter generates the analog delay. The filter regards pulses up to a certain width as noise and suppresses them.

For the minimum RESET pulse width and the minimum RESET pulse rejection, please refer to Sections 47A.5.1, $\overline{\text{RESET}}$ Timing, 47B.5.1, $\overline{\text{RESET}}$ Timing or 47C.5.1, $\overline{\text{RESET}}$ Timing of the RH850/F1KH, RH850/F1KM Hardware User's Manual respectively the Section 40.12 $\overline{\text{RESET}}$ Timing of the RH850/F1K Hardware User's Manual.

4.3 General Purpose I/O

4.3.1 RESET State of General Purpose I/P

During RESET state, all general-purpose I/O pins are in input mode with high-Z behavior except the pins JP0_4/ $\overline{\text{DCUTRST}}$ and P8_6/ $\overline{\text{RESETOUT}}$.

4.3.2 JP0_4/ $\overline{\text{DCUTRST}}$

During power-on or when $\overline{\text{RESET}}$ is at low level the pin JP0_4 should not be driven externally to high-level. Therefore, JP0_4/ $\overline{\text{DCUTRST}}$ has to be connected in all device operation modes to EVSS via a resistor.

4.3.3 P8_6/ $\overline{\text{RESETOUT}}$

When the $\overline{\text{RESETOUT}}$ signal is selected for the P8_6 pin the output on the pin is at low level during a reset and after release from the reset state depending on the option byte setting (OPBT0[9] register).

For further details, please refer to Sections 2A.11.1.1, P8_6: $\overline{\text{RESETOUT}}$, 2B.11.1.1, P8_6: $\overline{\text{RESETOUT}}$ and 2C.11.1.1 P8_6: $\overline{\text{RESETOUT}}$ of the RH850/F1KH, RH850/F1KM Hardware User's Manual.

For further details, please refer to the Section 2.11.1.1, P8_6: $\overline{\text{RESETOUT}}$ of the RH850/F1K Hardware User's Manual.

4.3.4 Analog Filter Function

Depending on the alternative port functionality selected, some input signals of the device pins are passed through an analog filter - respectively analog delay stage - to remove noise and glitches from the input signal.

The detection level of the filtered input signal depends on the high-level/low-level input voltage of the port input buffer and its supported electrical characteristics.

After passing the external signal through an analog filter to eliminate noise and spikes, the event detection evaluates the level or any level change, i.e. an edge, of the signal and generates an output accordingly.

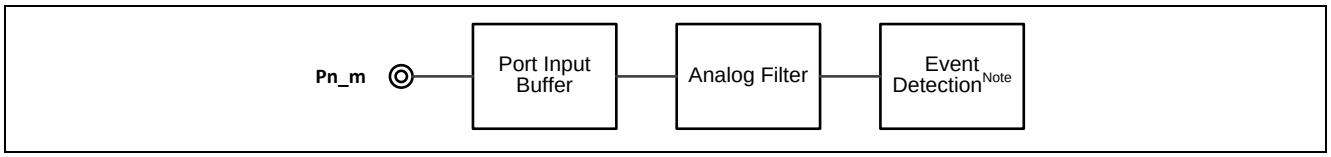


Figure 37: Analog filter function

Note: The event detection implementation depends on the analog filter type.

The input detection level as well as the pulse rejection of the analog filters are specified in the corresponding pin characteristics and peripheral chapters in the electrical characteristics of the RH850/F1KH, RH850/F1KM Hardware User's Manual respectively the electrical characteristics of the RH850/F1K Hardware User's Manual.

4.3.5 Port and Pin Behavior during Low Power Mode

During the low power modes, different states apply for the ports and pins of the RH850/F1Kx, RH850/F1K series. The states depend on the chosen low-power mode and may not have the same behavior for pins used as GPIO and used as alternative functions.

The following overview provides a summary of the pin behavior during low-power modes:

Table 78: Port and pin behavior during low power mode

	Always-On area (AWO area)		Isolated area (ISO area)	
	Pins used as GPIO	Pins used as alternative functions	Pins used as GPIO	Pins used as alternative functions
RUN Mode (HALT State)	Functional	Functional	Functional	Functional
STOP Mode	Kept	Functional	Kept	Functional
DeepSTOP Mode	Kept	Functional	I/O hold	I/O hold
Cyclic RUN Mode	Functional	Functional	Functional	Functional
Cyclic STOP Mode	Kept	Functional	Kept	Functional

Functional	Functional

Kept	State before entering the mode is kept

I/O hold	State before entering the mode is kept (with I/O hold).
	Internal logics are initialized after wake-up.
	
	I/O hold function for Isolated area (ISO area)
	• During the DeepSTOP mode, the state of the pins on the Isolated area (ISO area) can be held automatically. Thus, its input and/or output remain in the same state as before entering I/O buffer hold state. No external or internal signal can change its state until the I/O buffer hold state is terminated.
	• The I/O buffers in DeepSTOP mode are changing into I/O buffer hold state by default.
	• After the wake-up from DeepSTOP mode the I/O buffer hold state is terminated in the following steps:
	  ○ 1. Re-configure the peripheral or port function
	  ○ 2. Release I/O hold state by setting IOHOLD.IOHOLD = 0

4.4 Recommended Connection of Unused Pins

4.4.1 Recommended Connection of Unused Pins for RH850/F1KM-S1

Table 79: Recommended connection of unused pins for RH850/F1KM-S1

Pin	Recommended Connection of Unused Pin
A0VREF	Connect to EVCC
A0VSS	Connect to EVSS
$\overline{\text{RESET}}$	Connect to EVCC via a resistor
X1	Connect to AWOVSS via a resistor
X2	Leave open
P0 P8 (excluding P8_6) P9	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P8_6	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2, P10_6 and P10_8)	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10_1 P10_2 P10_6 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note2
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note1	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Connect to EVCC via a resistor $\overline{\text{DCUTRST}}$ (JP0_4): Connect to EVSS via a resistor Note2 $\overline{\text{DCURDY}}$ /LPDCLKOUT (JP0_5): Leave open

Notes 1. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, see Chapter 8, Development Tool Interface.

2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1KM-S1, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

4.4.2 Recommended Connection of Unused Pins for RH850/F1KM-S2

Table 80: Recommended connection of unused pins for RH850/F1KM-S2

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF[Note1]	**[144pin and 176pin]** Connect to EVCC or BVCC **[100pin]** Connect to EVCC
A0VSS, A1VSS[Note1]	**[144pin and 176pin]** Connect to EVSS or BVSS **[100pin]** Connect to EVSS
$\overline{\text{RESET}}$	**[144pin and 176pin]** Connect to EVCC or BVCC via a resistor **[100pin]** Connect to EVCC via a resistor
X1	Connect to AWOVSS via a resistor
X2	Leave open
XT1	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or connected to AWOVSS (bit 0 of IPIBC0 = 0)
IP0_0/XT2	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or leave open (IPIBC0.0 bit = 0)
P0 P1 P2 P8 (excluding P8_6) P9 P20	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P8_6	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2, P10_6 and P10_8) P11 P12 P18	**[144pin and 176pin]** Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVCC or BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open **[100pin]** Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
P10_1 P10_2 P10_6 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note3
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note2	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Connect to EVCC via a resistor $\overline{\text{DCUTRST}}$ (JP0_4): Connect to EVSS via a resistor Note3 $\overline{\text{DCURDY}}$ /LPDCLKOUT (JP0_5): Leave open $\overline{\text{EVTO}}$ (JP0_6): Leave open Note1

Notes
1. The pin availability depends on the selected device.
2. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, see Chapter 8, Development Tool Interface.
3. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
4. XT1 = IP0_0 (XT2) = REGVCC or AWOVSS should be set.

   XT1 is connected to IP0_0 (XT2) through an internal resistor. Therefore, it is necessary to maintain an equal voltage level in order not to generate a current path.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1KM-S2, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

4.4.3 Recommended Connection of Unused Pins for RH850/F1KM-S4

Table 81: Recommended connection of unused pins for RH850/F1KM-S4

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF[Note1]	**[144pin, 176pin, 233pin and 272pin]** Connect to EVCC or BVCC **[100pin]** Connect to EVCC
A0VSS, A1VSS[Note1]	**[144pin, 176pin, 233pin and 272pin]** Connect to EVSS or BVSS **[100pin]** Connect to EVSS
$\overline{\text{RESET}}$	**[144pin, 176pin, 233pin and 272pin]** Connect to EVCC or BVCC via a resistor **[100pin]** Connect to EVCC via a resistor
X1	Connect to AWOVSS via a resistor
X2	Leave open
XT1	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or connected to AWOVSS (bit 0 of IPIBC0 = 0)
IP0_0/XT2	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or leave open (IPIBC0.0 bit = 0)
P0 P1 P2 P3 P8 (excluding P8_6) P9 P20	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P8_6	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2, P10_6 and P10_8) P11 P12 P13 P18 P19 P21 P22	**[144pin, 176pin, 233pin and 272pin]** Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVCC or BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open **[100pin]** Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
P10_1 P10_2 P10_6 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note3
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note2	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Connect to EVCC via a resistor $\overline{\text{DCUTRST}}$ (JP0_4): Connect to EVSS via a resistor Note3 $\overline{\text{DCURDY}}$ /LPDCLKOUT (JP0_5): Leave open $\overline{\text{EVTO}}$ (JP0_6): Leave open Note1

Notes
1. The pin availability depends on the selected device.
2. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, see Chapter 8, Development Tool Interface.
3. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
4. XT1 = IP0_0 (XT2) = REGVCC or AWOVSS should be set.

   XT1 is connected to IP0_0 (XT2) through an internal resistor. Therefore, it is necessary to maintain an equal voltage level in order not to generate a current path.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1KM-S4, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

4.4.4 Recommended Connection of Unused Pins for RH850/F1KH-D8

Table 82: Recommended connection of unused pins for RH850/F1KH-D8

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF	Connect to EVCC or BVCC
A0VSS, A1VSS	Connect to EVSS or BVSS
$\overline{\text{RESET}}$	Connect to EVCC or BVCC via a resistor
X1	Connect to AWOVSS via a resistor
X2	Leave open
XT1	Connect to REGnVCC or AWOVSS via a resistor[Note3] (bit 0 of IPIBC0 = 1) or connected to AWOVSS (bit 0 of IPIBC0 = 0)
IP0_0/XT2	Connect to REGnVCC or AWOVSS via a resistor[Note3] (bit 0 of IPIBC0 = 1) or leave open (IPIBC0.0 bit = 0)
P0 P1 P2 P3 P8 (excluding P8_6) P9 P20 P23	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P8_6	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2, P10_6 and P10_8) P11 P12 P13 P18 P19 P21 P22 P24	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVCC or BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10_1 P10_2 P10_6 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note2
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note1	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Connect to EVCC via a resistor $\overline{\text{DCUTRST}}$ (JP0_4): Connect to EVSS via a resistor Note1 $\overline{\text{DCURDY}}$ /LPDCLKOUT (JP0_5): Leave open $\overline{\text{EVTO}}$ (JP0_6): Leave open

Notes
1. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, see Chapter 8, Development Tool Interface.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. XT1 = IP0_0 (XT2) = REGVCC or AWOVSS should be set.

   XT1 is connected to IP0_0 (XT2) through an internal resistor. Therefore, it is necessary to maintain an equal voltage level in order not to generate a current path.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1KH-D8, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

4.4.5 Recommended Connection of Unused Pins for RH850/F1K

Table 83: Recommended connection of unused pins for RH850/F1K

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF[Note1]	Connect to EVCC
A0VSS, A1VSS[Note1]	Connect to EVSS
$\overline{\text{RESET}}$	Connect to EVCC via a resistor
X1	Connect to AWOVSS via a resistor
X2	Leave open
XT1	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or connected to AWOVSS (bit 0 of IPIBC0 = 0)
IP0_0/XT2	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or leave open (IPIBC0.0 bit = 0)
P0 P1 P2 P8 (excluding P8_6) P9 P20	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P8_6	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2, P10_6 and P10_8) P11 P12 P18	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10_1 P10_2 P10_6 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note3
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note2	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Connect to EVCC via a resistor $\overline{\text{DCUTRST}}$ (JP0_4): Connect to EVSS via a resistor Note3 $\overline{\text{DCURDY}}$ /LPDCLKOUT (JP0_5): Leave open $\overline{\text{EVTO}}$ (JP0_6): Leave open Note1

Notes
1. The pin availability depends on the selected device.
2. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, see Chapter 8, Development Tool Interface.
3. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
4. XT1 = IP0_0 (XT2) = REGVCC or AWOVSS should be set.

   XT1 is connected to IP0_0 (XT2) through an internal resistor. Therefore, it is necessary to maintain an equal voltage level in order not to generate a current path.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1K, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

4.5 Injected Current

The RH850/F1Kx, RH850/F1K series has different electrical characteristics for the injected current depending on the pin group and device pins of the different package variants.

When a current is applied to the protection diodes of the device, the current that exceeds the limit of the microcontroller will increase or decrease the supply voltage or GND level of the device. In such a case, the system should be configured that the voltage at a pin is within the operation voltage range (-0.8V to 6.0V).

Please evaluate and confirm the influence caused by:

- the change of current on many ports at the same time
- impact to the operation by external noise

The protection diodes on the device differ from normal switching diodes and are not aimed as level-shifter of DC input signals. Therefore, do not apply a sudden stress like a rush current to the protection diodes.

The value of R1, R2 and C depends on the usage condition and has to be defined based on application requirements. Especially, in case of sensors the conversion accuracy of analog input signal depends on the scan period and impedance of the sensors.

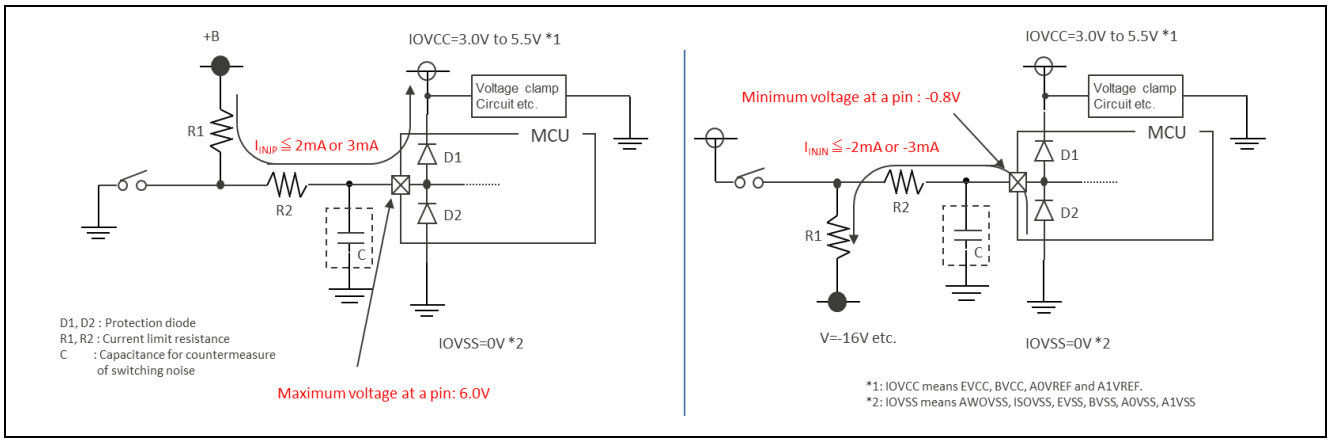


Figure 38: Mechanism of injection current

For details, please refer to Sections 47A.4.4, Injection Currents, 47B.4.4, Injection Currents or 47C.4.4, Injection Currents of the RH850/F1KH, RH850/F1KM Hardware User's Manual.

For details, please refer to Section 40.27 Injection Currents of the RH850/F1K Hardware User's Manual.

5. SENT Interface (RH850/F1Kx Series only)

The SENT module supports the SPC (Short PWM Code) extension of the J2716 specification that introduces a bi-directional and synchronous communication. The SPC extension can be enabled by software (by RSENTnCC.SPCE bit).

When the SPC extension is used an external transistor is required in order to pull-down the RX line to initiate a SENT message transmission. In the RH850/F1Kx series this is realized by controlling an external transistor connected to the RSENTnSPCO pin. The polarity of the RSENTnSPCO pin can be configured by software (by RSENTnCC.SOPC bit).

6. AD-Converter

6.1 Conversion time

The ADC conversion time consists of a number of timing parameters, which are summed-up to get the conversion timing depending on the application.

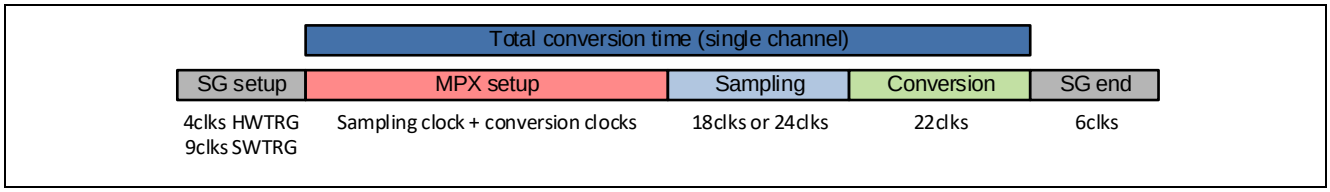


Figure 39: ADC conversion time

Notes:
1. SG - Scan Group
2. MPX - External multiplexer
3. HWTRG - Hardware trigger
4. SWTRG - Software trigger

The setting of the ADC clock and the sampling time results in the following conversion timing:

Table 84: ADC conversion time overview

ADCLK [MHz]	Sampling time [clks]	MPX Setup time [µs]	Sampling time [µs]	Conversion time [µs]	Total conversion time (excluding MPX) [µs]	Total conversion time (including MPX) [µs]
40	24	1.15	0.60	0.55	1.15	2.30
32	18	1.25	0.56	0.69	1.25	2.50
32	24	1.44	0.75	0.69	1.44	2.88
24	18	1.67	0.75	0.92	1.67	3.33
24	24	1.92	1.00	0.92	1.92	3.83
8	18	5.00	2.25	2.75	5.00	10.00
8	24	5.75	3.00	2.75	5.75	11.50

Note: The sampling time is set by the ADCAnSMPCR.SMPT [7:0] bits.

6.2 External Multiplexer Wait Time

The analog input stabilization time can be defined for each physical channel of the ADC by register settings (registers ADCAnMPXSTBTSELR0 to 4, ADCAnMPXSTBTR0 to 7) when an external analog multiplexer is used.

For details, please refer to Section 38, A/D Converter (ADCA) of the RH850/F1KH, RH850/F1KM Hardware User's Manual or Section 31, A/D Converter (ADCA) of the RH850/F1K Hardware User's Manual.

6.3 Equivalent Input Circuit

The A/D-converters have different options for the input with track & hold path or direct path only. Please refer to Section 38.1.1, Number of Units and Channels of the RH850/F1KH, RH850/F1KM Hardware User's Manual or Section 31.1.1, Number of Units and Channels of the RH850/F1K Hardware User's Manual, which A/D-converter is supported by the chosen device.

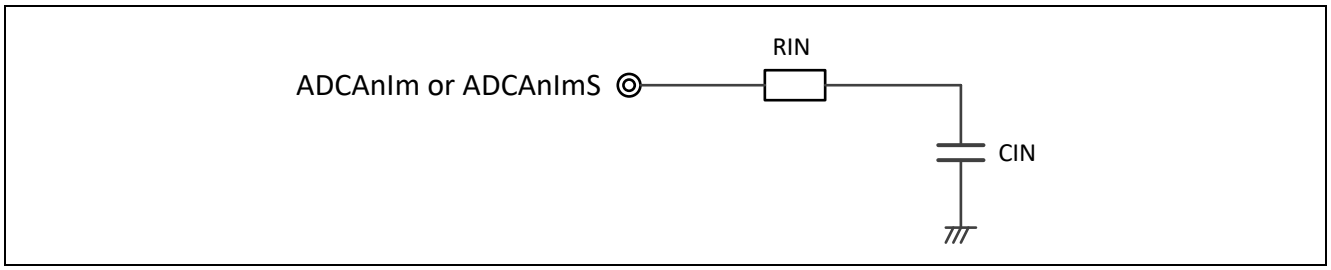


Figure 40: ADC equivalent input circuit

About the value of RIN and CIN for each device, please refer to Sections 47A.6.1, Equivalent Circuit of the Analog Input Block, 47B.6.1, Equivalent Circuit of the Analog Input Block or 47C.6.1, Equivalent Circuit of the Analog Input Block of the RH850/F1KH, RH850/F1KM Hardware User's Manual.

About the value of RIN and CIN for each device, please refer to Sections 40.26.1 of the Analog Input Block of the RH850/F1K Hardware User's Manual.

6.4 External Circuit on ADC Input

To preserve the accuracy of the A/D-converter, it is recommended that analog input pins have a low impedance. Therefore, placing a capacitor at the analog input pin can provide an effective result. This capacitor contributes to noise filtering on the analog input pin. A basic filter can be realized by using a series resistor with a capacitor on the input pin (RC-filter).

The filter at the input pins should be designed considering the dynamic characteristics of the input signal, the equivalent input impedance of the ADC itself and the injected current specification of the analog input pins.

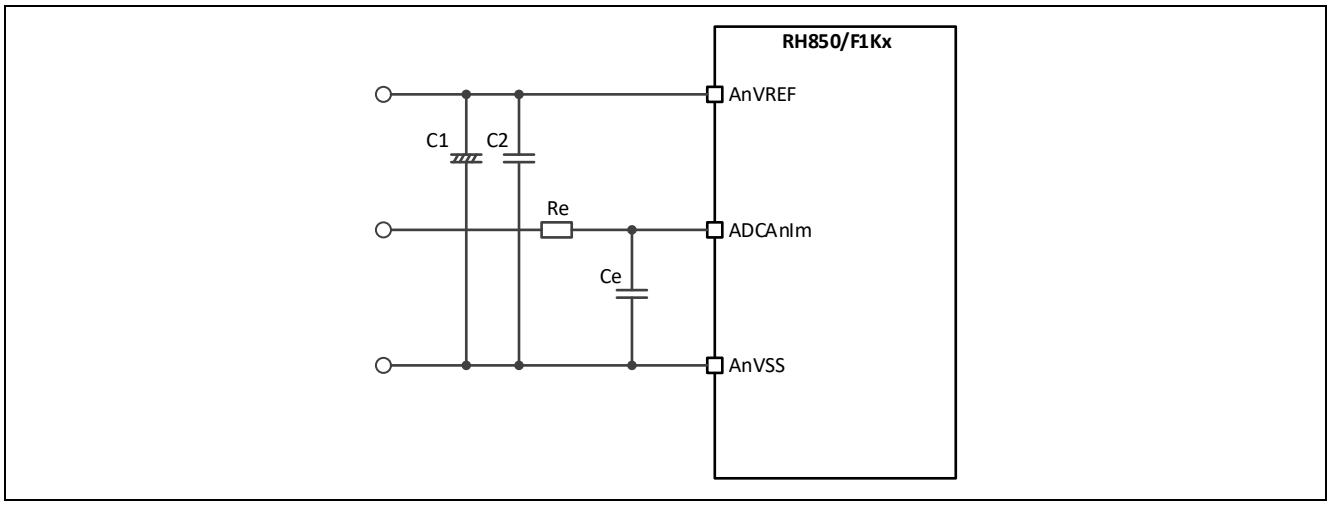


Figure 41: ADC external circuit on analog input

Note: For details about suffix “m” and “n”, please refer to Section 38.1.1, Number of Units and Channels of the RH850/F1KH, RH850/F1KM Hardware User’s Manual or Section 31.1.1, Number of Units and Channels of the RH850/F1K Hardware User’s Manual.

General guidance values of the basic external ADC input circuit:

Table 85: Basic external ADC input circuit

Component	Value
C1	4.7µF or larger
C2	10nF to 100nF
Ce	5nF to 10nF
Re	0 to 1kΩ

The values of the resistors and capacitors depend on the application requirements.

The capacitor (C2) placed close to the supply pin AnVREF helps to improve the resistance against electromagnetic disturbance.

In order to improve the accuracy of the ADC it is recommended to add a capacitor (C1) of minimum 4.7µF in parallel to the capacitor C2 at AnVREF. The value and PCB placement of the parallel capacitor depends on the application requirements.

As guideline for the calculation of the external capacitor at the analog input pin the formula based on the internal equivalent capacitance and the ADC resolution of the corresponding AD-converter channel can be used. In this case, sampling error based on charge-sharing between Ce and CIN will be roughly 1 LSB at the start timing of sampling.

$$Ce = CIN \times 2^{ADCresolution}$$

Ce: External capacitor at the analog input pin

CIN: Equivalent input capacitance

ADCresolution: AD-converter resolution for RH850/F1Kx or RH850/F1K, either 12-bit or 10-bit resolution

6.5 Formulas for sampling error

Sampling error is error to which “Errors (Sampling error 1) which depend on input leakage current of analog pin” and “Errors (Sampling error 2) which depend on conversion cycles with charge sharing” were added.

$$Sampling\ error\ = Sampling\ error\ 1 + Sampling\ error\ 2$$

The external circuit of the A/D pin indicates below about the factor (sampling error 1 and sampling error 2) which becomes sampling error.

a) Errors (Sampling error 1) which depend on input leakage current of analog pin

The error depends on the input leakage current (ILeak) of analog pin and external resistance (Re) and occurs. The error which depends on the input leakage current is given by the formula of the following.

$$Sampling\ error\ 1\ (LSB) = Re \times ILeak \times \frac{2^{ADCresolution}}{V_{avrefh}}$$

Vavrefh: AnVREF voltage

ADCresolution: AD-converter resolution for RH850/F1Kx, either 12-bit or 10-bit resolution

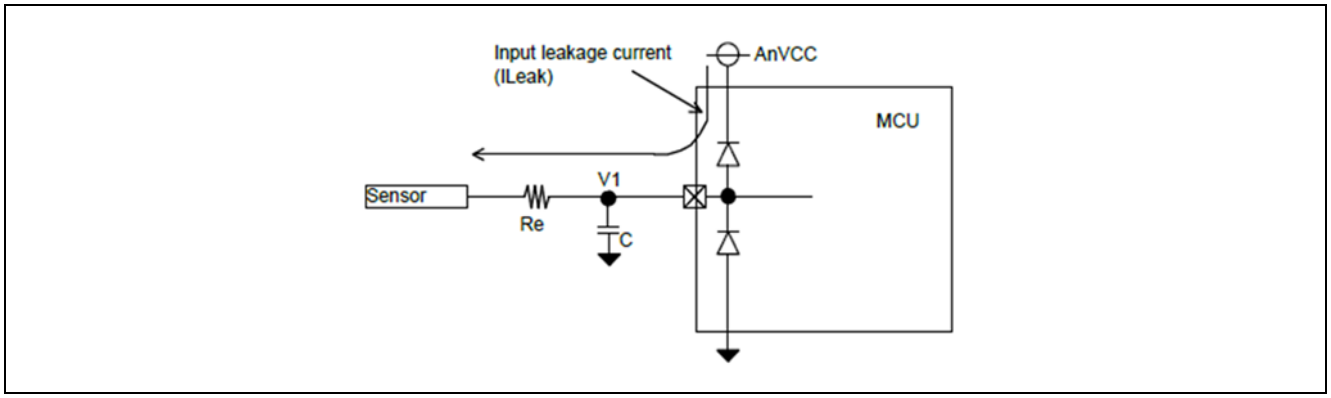


Figure 42: Schematic for sampling error 1 formula

b) Errors (Sampling error 2) which depend on conversion cycles with charge sharing

A formula for errors in sampled values due to the external circuit of the A/D converter is given below. These errors will depend on the input circuit and conversion cycle. The formula given below for the errors is simplified for the calculation of sampling error based on internal stray capacitance, amplifier offset, resistance of the signal source, and conversion cycle. This formula can also be used to calculate the effects of the signal source resistance and conversion cycle on these errors.

The formula gives the error of analog input 2 as shown in the figure below when A/D conversion is performed in the order of analog input 1 then 2.

$$Sampling\ error\ 2\ (LSB) = \left[\left(\frac{(V1-V2)\times CIN1}{Ce+CIN1} + \frac{|V_{vfaerr}|\times CIN2}{Ce+CIN2}\right)\times\frac{1}{1-e^{-T1/(Re\times Ce)}} + \left(\frac{1}{T1}\times C1\times V3\times Re\right)\right]\times\frac{2^{ADCresolution}}{V_{avrefh}}$$

Item	Symbol	Condition	Reference	Unit
Common capacitance of the final stage of channel multiplexer	CIN1	ADCJ0Im	2.2	pF
		ADCJ1Im	2.2	pF
Common capacitance of the final stage of the amplifier	CIN2	ADCJ0Im	11.5	pF
		ADCJ1Im	9.4	pF
External capacitor on analog input pin	Ce		Depends on customer's environment	uF
Signal source impedance	Re			kΩ
Conversions cycle of analog Input pins	T1			ms
AnVREF voltage	Vavrefh			V
Potential difference between V1 and V2	V2-V1			V
Offset voltage of the amplifier	Vvfaerr		50	mV
Parasitic capacitance in the channel multiplexer	C1		2	pF
|AnVCC voltage / 2.5 - measured pin voltage (V2)|	V3		Depends on customer's environment	V
AD-converter resolution, either 12-bit or 10-bit resolution	ADCresolution		12 or 10	-

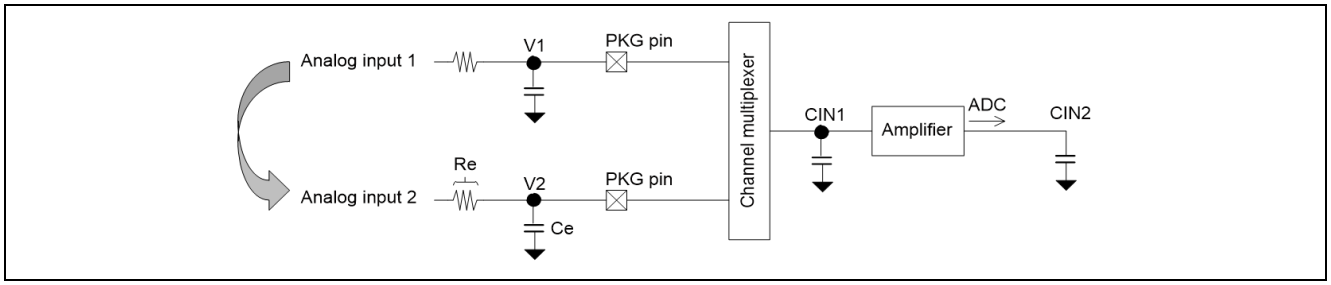


Figure 43: Schematic for sampling error 2 formula

7. Device Operation Modes

The RH850/F1Kx series and RH850/F1K series support the following operation modes that are used for normal operation, debugging, flash programming and test by using boundary scan.

Table 86: Device operation mode overview

FLMD0	P10_8 (FLMD1)	P10_1 (MODE0)	P10_2 (MODE1)	P10_6 (MODE2)	Operation Mode
0	X	X	X	X	Normal operating mode
1	0	X	X	X	Flash programming mode
1	1	0	1	X	Boundary scan mode
1	1	1	1	1	User boot mode
Other than the above					Setting prohibited

Note: x – Don’t care

Table 87: Device operation mode description

Operation Mode	Mode Description
Normal operating mode	Mode used for the execution of application software and during debugging. When FLMD0 is pulled-up to high-level during operation in this mode, writing to the code flash memory by self-programming is enabled.
Flash programming mode	Mode used during the flash memory program/erase of the device.
Boundary scan mode	Mode used for boundary scan test.
User boot mode	Mode used for the execution of application software and during debugging, where the base address is fixed and the transition to stand-by modes is not supported.

The related pins have to be configured accordingly on the PCB in order to define and support the required operation modes.

Caution

To change the operating mode, restart from power-on clear reset (remove the power supply once and apply it again). For details, please refer to Sections 6, Operating Mode, 9A.1.1, Reset Sources and 9BC.1.1, Reset Sources of the RH850/F1KH, RH850/F1KM Hardware User’s Manual or Sections 6, Operating Mode and 9.1.1, Reset Sources of the RH850/F1K Hardware User’s Manual.

8. Development Tool Interface

The description of the development tool interface in this chapter assumes that the normal operating mode of the MCU is used. When the user boot mode shall be used the configuration of the pins FLMD0, P10_8/FLMD1, P10_1/MODE0, P10_2/MODE1 and P10_6/MODE2 has to be set accordingly.

8.1 Debug Interface Connection

For the debugging environment, the following interface connections are supported:

- Low pin debug interface (1 pin) - hereinafter called "LPD (1 pin)"
- Low pin debug interface (4 pins) - hereinafter called "LPD (4 pins)"
- Nexus interface
    - The Nexus interface is only supported by 3rd party development tools.

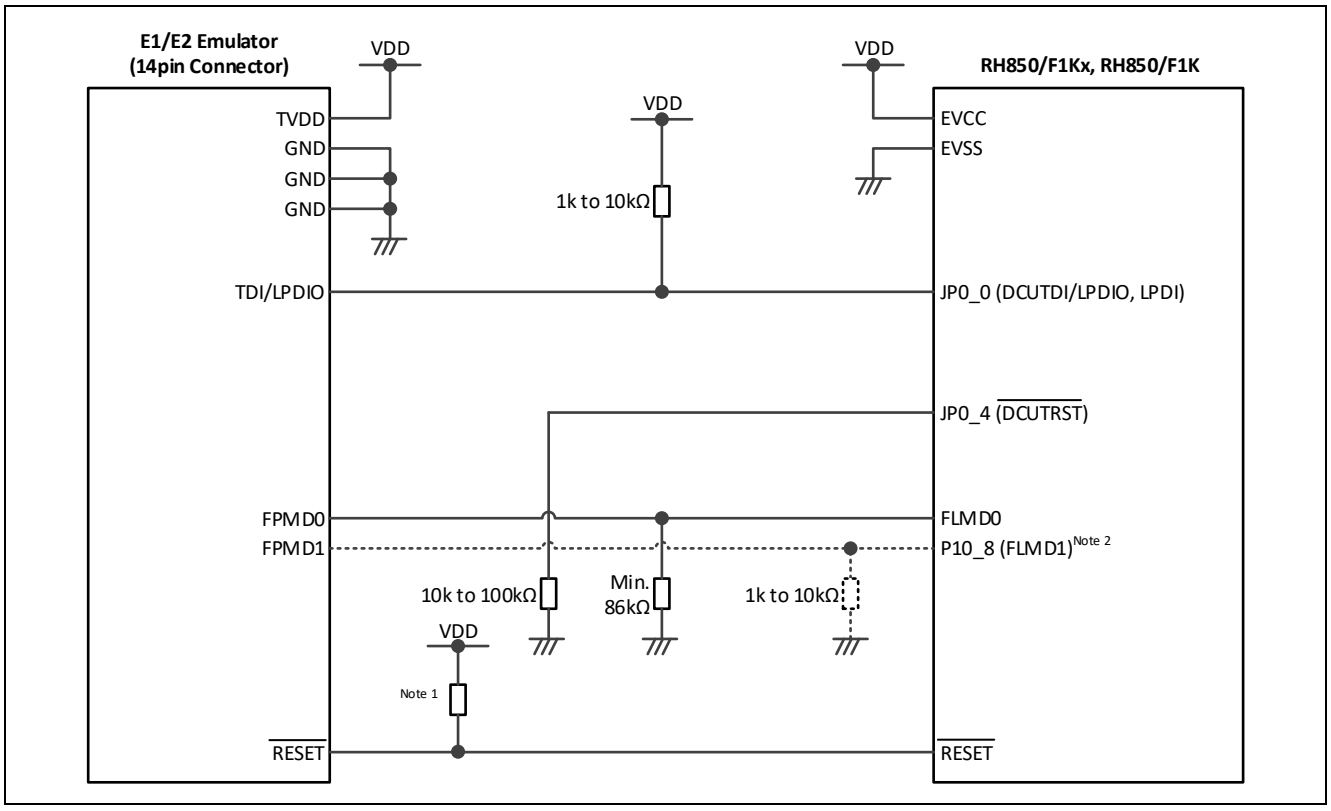


Figure 44: LPD (1 pin) connection

Notes:
1. The maximum sink current of the $\overline{\text{RESET}}$ terminal of the E1/E2 emulator is 2mA. The external pull-up circuit of the $\overline{\text{RESET}}$ pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.
2. Design the circuit in the way that the FLMD1 pin must be at the low level during serial programming. During programming (using the RFP), it outputs a low level on FPMD1 to place the device in the serial programming mode.

   If necessary, connect FPMD1 and FLMD1.

When the LPD (1 pin) mode is used, the port of the JP0 port group is automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDIO input/output
- JP0_1: General-purpose I/O
- JP0_2: General-purpose I/O
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: General-purpose I/O
- JP0_6: General-purpose I/O (depending on device)

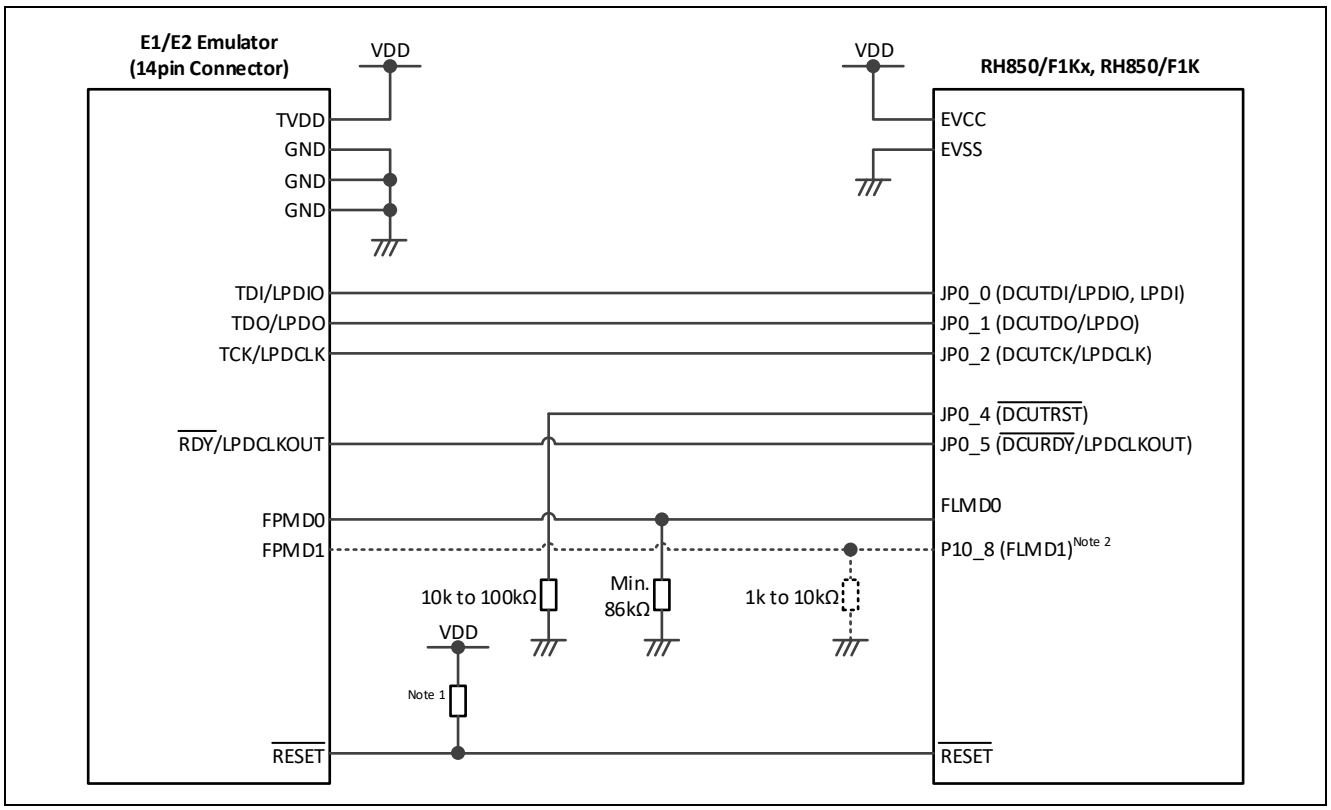


Figure 45: LPD (4 pins) connection

Notes:

1. The maximum sink current of the $\overline{\text{RESET}}$ terminal of the E1/E2 emulator is 2mA. The external pull-up circuit of the $\overline{\text{RESET}}$ pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.
2. Design the circuit in the way that the FLMD1 pin must be at the low level during serial programming. During programming (using the RFP), it outputs a low level on FPMD1 to place the device in the serial programming mode.

   If necessary, connect FPMD1 and FLMD1.

When the LPD (4 pins) mode is used, the ports of the JP0 port group are automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDI input
- JP0_1: LPDO output
- JP0_2: LPDCLK input
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: LPDCLKOUT output
- JP0_6: General-purpose I/O (depending on device)

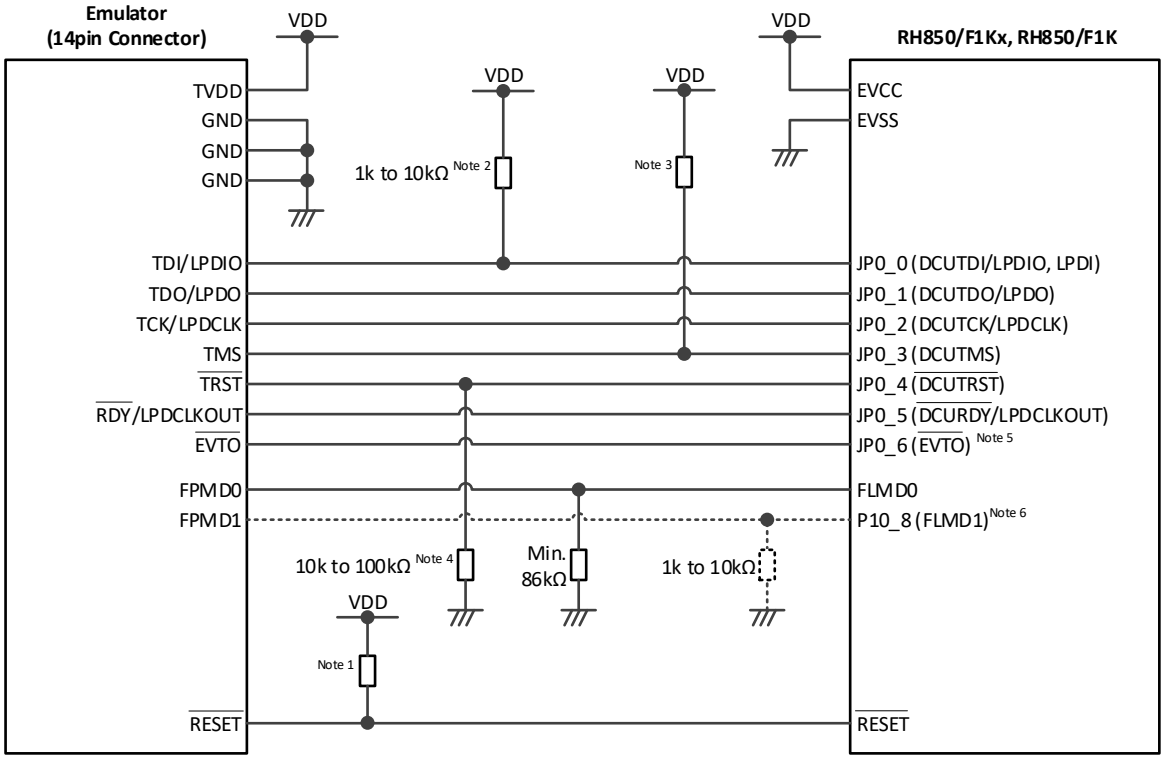


Figure 46: Nexus, LPD (4 pins) and LPD (1 pin) connection

Notes:

1. The maximum sink current of the $\overline{\text{RESET}}$ terminal of the E1/E2 emulator is 2mA. The external pull-up circuit of the $\overline{\text{RESET}}$ pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.
2. The resistor is optional when the LPD (4 pins) mode is used
3. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
4. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
5. Depending on the device.
6. Design the circuit in the way that the FLMD1 pin must be at the low level during serial programming. During programming (using the RFP), it outputs a low level on FPMD1 to place the device in the serial programming mode.
   If necessary, connect FPMD1 and FLMD1.

When the Nexus debug mode is used, the ports of the JP0 port group are automatically switched to the debug interface mode.

- JP0_0: DCUTDI input
- JP0_1: DCUTDO output
- JP0_2: DCUTCK input
- JP0_3: DCUTMS input
- JP0_4: $\overline{\text{DCUTRST}}$ input
- JP0_5: $\overline{\text{DCURDY}}$ output
- JP0_6: $\overline{\text{EVTO}}$ (depending on device)

The debug interface signal connection of the E1/E2 interface is given in the table below:

Table 88: Debug interface signal connection

E1/E2 Interface Connector	E1/E2 Interface Signal	Device Pin
1	LPDCLK/(DCUTCK)	JP0_2
2	GND	EVSS
3	($\overline{\text{DCUTRST}}$)	JP0_4
4	FPMD0/FLMD0	FLMD0
5	LPDO/(DCUTDO)	JP0_1
6	FPMD1	FLMD1
7	LPDI/LPDIO/(DCUTDI)	JP0_0
8	TVDD	EVCC
9	(DCUTMS)	JP0_3
10	($\overline{\text{EVTO}}$)	JP0_6 Note 2
11	LPDCLKOUT/($\overline{\text{DCURDY}}$)	JP0_5
12	GND	EVSS
13	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
14	GND	EVSS

Notes: 1. The Nexus interface signals marked with (*text*) are supported by 3rd party development tools and not by E1/E2 emulator.

2. Depending on the device.

8.2 Flash Programming Interface

For the programming environment PG-FPx, the following connections are supported:

- Single-wire asynchronous flash programming interface
- Two-wire asynchronous flash programming interface
- Synchronous flash programming interface

For the programming environment combination of E1/E2 emulator and RFP, the following connections are supported:

- Single-wire asynchronous flash programming interface
- Two-wire asynchronous flash programming interface

Table 89: Basic flash programming connection

Flash Programming Interface	Function	Device Pins
1-wire UART	RxD/TxD	JP0_0
2-wire UART	RxD	JP0_0
	TxD	JP0_1
CSI	SI	JP0_0
	SO	JP0_1
	SCK	JP0_2

8.2.1 Flash Programming by PG-FPx

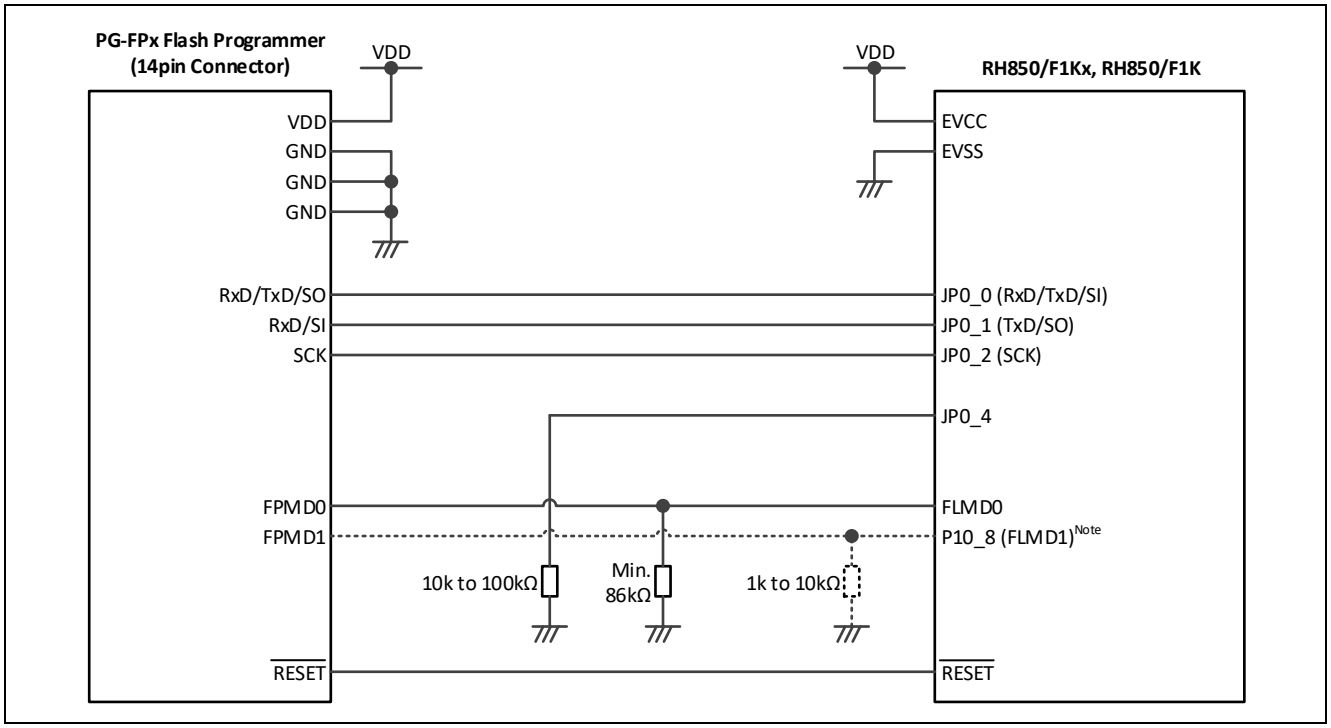


Figure 47: PG-FPx flash programming interface connection

Note: Design the circuit in the way that the FLMD1 pin must be at the low level during serial programming. During programming, it outputs a low level on FPMD1 to place the device in the serial programming mode.

If necessary, connect FPMD1 and FLMD1.

The flash programming signal connection of the PG-FPx interface is given in the table below:

Table 90: PG-FPx Flash programming signal connection

PG-FPx Interface Connector	PG-FPx Signal	Device Pin
1	SCK	JP0_2
2	GND	EVSS
3	-	-
4	FPMD0	FLMD0
5	SI/RxD	JP0_1
6	FPMD1	FLMD1
7	SO/TxD	JP0_0
8	VDD	EVCC
9	-	-
10	-	-
11	-	-
12	GND	EVSS
13	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
14	-	-

8.2.2 Flash Programming by E1/E2 Emulator and RFP

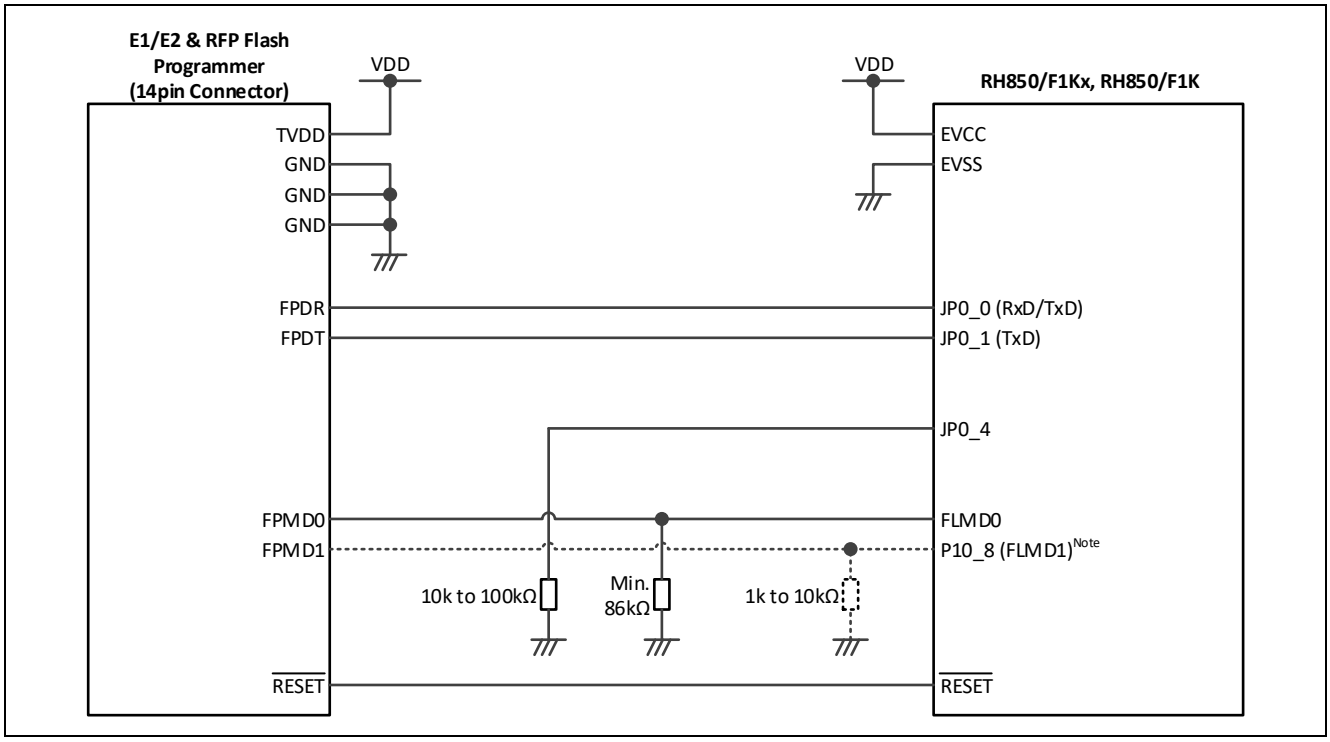


Figure 48: E1/E2 flash programming interface connection

Note: Design the circuit in the way that the FLMD1 pin must be at the low level during serial programming. During programming (using the RFP), it outputs a low level on FPMD1 to place the device in the serial programming mode.

If necessary, connect FPMD1 and FLMD1.

The flash programming signal connection of the E1/E2 interface is given in the table below:

Table 91: E1/E2 Flash programming signal connection

E1/E2 Interface Connector	E1/E2 Signal	Device Pin
1	-	-
2	GND	EVSS
3	-	-
4	FPMD0	FLMD0
5	FPDT	JP0_1
6	FPMD1	FLMD1
7	FPDR	JP0_0
8	TVDD	EVCC
9	-	-
10	-	-
11	-	-
12	GND	EVSS
13	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
14	GND	EVSS

8.3 Combined Debug and Flash Programming Interface Connection

The following figure describes the combined connections for debugging and flash programming, supporting

- Low pin debug interface (1 pin) - hereinafter called "LPD (1 pin)"
- Low pin debug interface (4 pins) - hereinafter called "LPD (4 pins)"
- Nexus interface
- Single-wire asynchronous flash programming interface with PG-FPx or E1/E2 & RFP
- Two-wire asynchronous flash programming interface with PG-FPx or E1/E2 & RFP
- Synchronous flash programming interface with PG-FPx

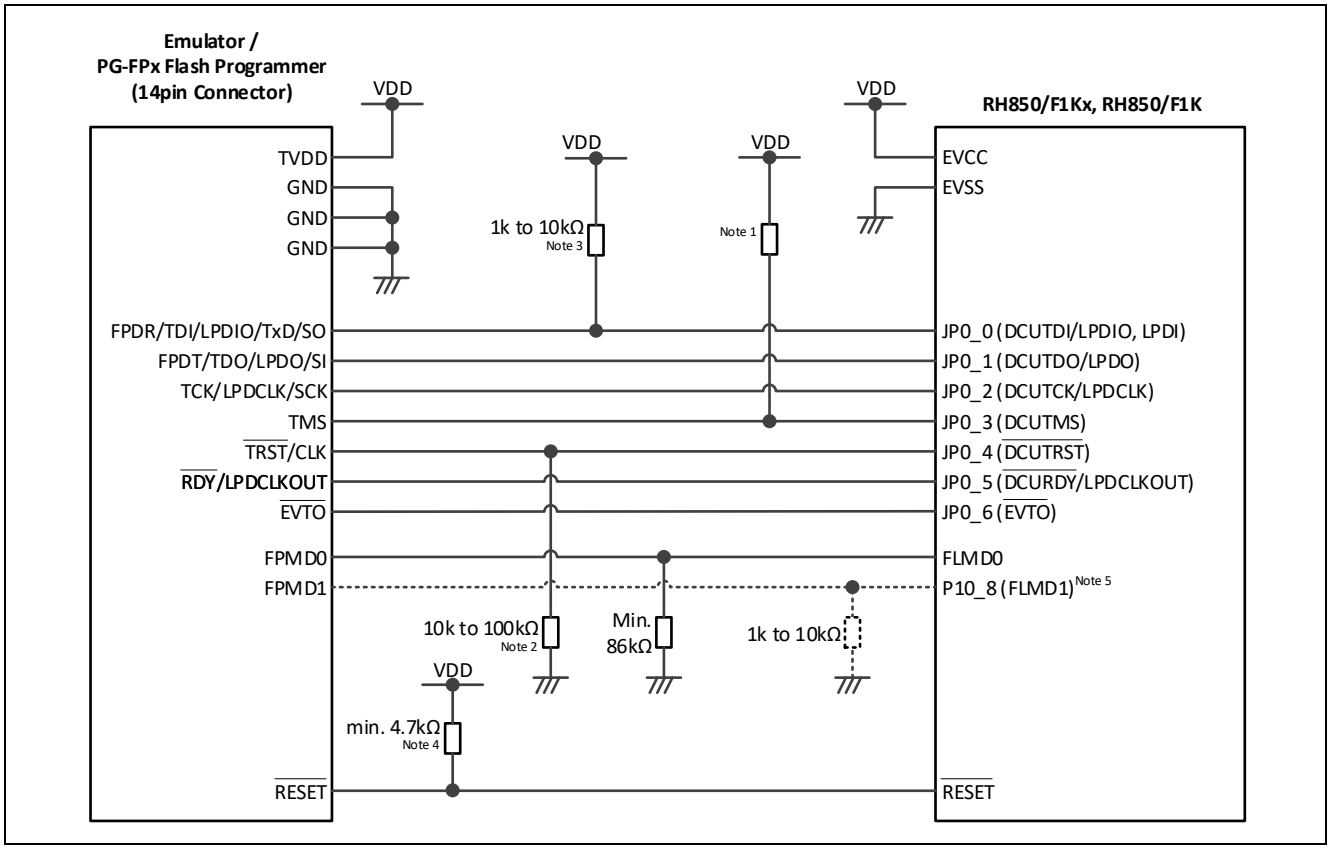


Figure 49: Combined debug and flash programming interface connections

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the LPD (4 pins) mode is used
4. The maximum sink current of the $\overline{\text{RESET}}$ terminal of the E1/E2 emulator is 2mA. The external pull-up circuit of the $\overline{\text{RESET}}$ pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

5. Design the circuit in the way that the FLMD1 pin must be at the low level during serial programming. During programming (using the RFP), it outputs a low level on FPMD1 to place the device in the serial programming mode.
   If necessary, connect FPMD1 and FLMD1.

8.4 Debug Considerations when Hot Plug-in is used

When it is planned to use the hot plug-in function for debugging the following topics should be considered.

$\overline{\text{RESET}}$ pin

When the hot plug-in will be used it is recommended to consider the installation of a capacitor between the reset signal and GND in order to suppress a noise. In this case, the time constant of the reset circuit shall be adjusted that the time elapsing before the signal reaches 80% of the high level from the low level is within 900 µs.

Power source monitoring

When the hot plug-in function will be used it is recommended to configure the external circuit of the power source monitoring at pin 8 (TVDD) of the E1/E2 emulator connector with a ferrite bead or inductor. This additional ferrite bead or inductor is recommended to avoid a momentary drop in the power-supply voltage on the user system that could lead to a reset of the microcontroller.

This effect can be reduced as shown in Figure 22 by placing a ferrite bead (or inductor) L1 and an additional capacitor C1 near the TVDD line of the connector for the E1/E2 emulator.

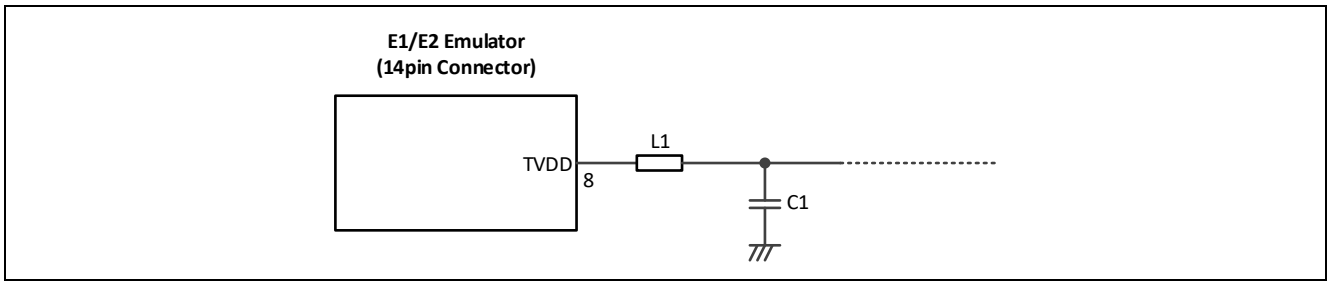


Figure 50: Circuit configuration for hot plug-in

Note: This measure might not eliminate completely the voltage drop.

General guidance for the additional external components for the power source monitoring during hot plug-in:

Table 92: Basic component value for hot plug-in

Component	Value
C1	10 to 47µF, ESR < 4Ω
L1	10 to 22µH

The value of the capacitor C1 and the inductor/ferrite bead L1 depends on the application requirements.

9. Test Tool Interface

The boundary scan test is compliant with IEEE Standard 1149.1 and certain boundary scan instructions are supported.

When the boundary scan mode shall be used, several connections have to be done between boundary scan test tool and the device. Especially the boundary scan mode selection pins have to be considered from application point of view as these pins are normally used for application related functions.

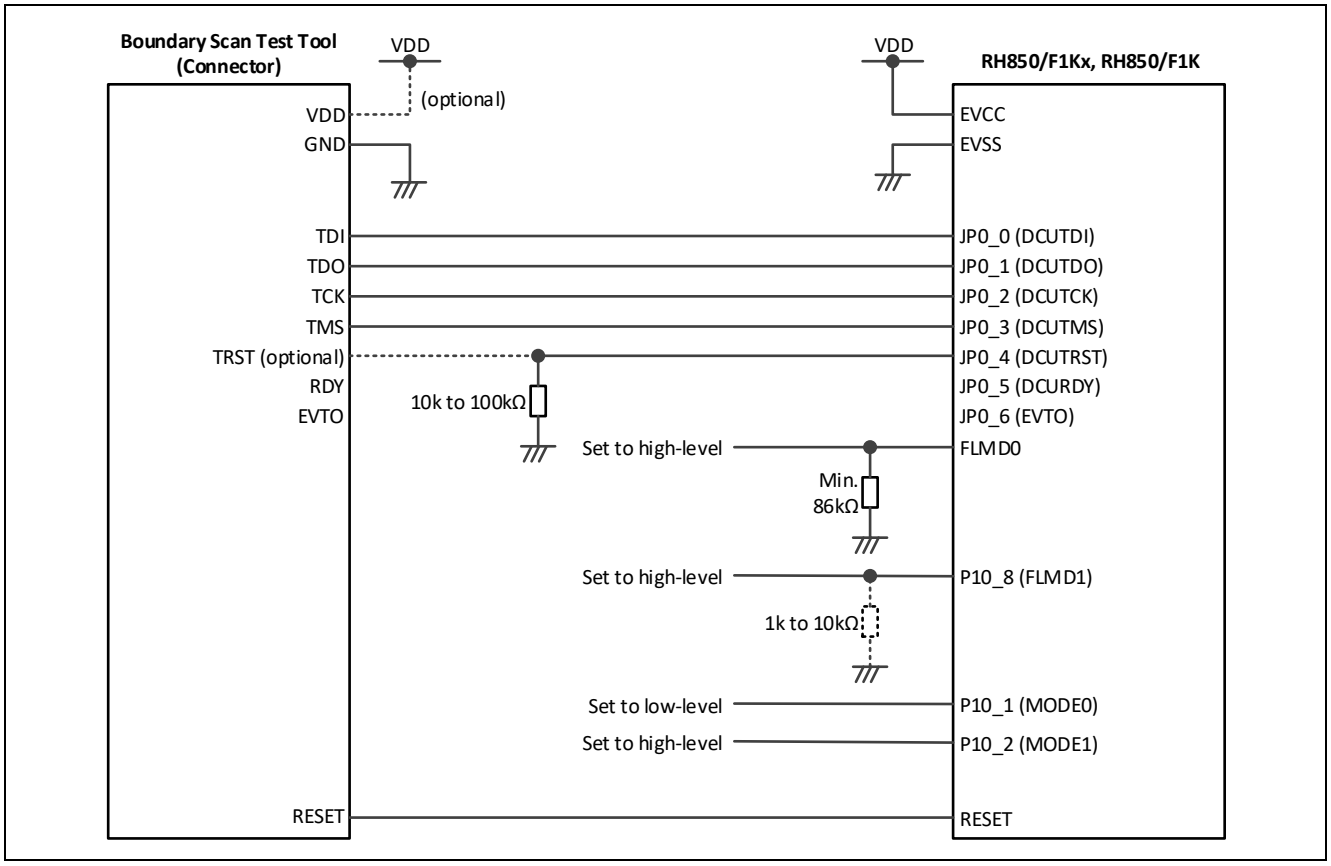


Figure 51: Boundary scan connection of RH850/F1Kx and RH850/F1K series

Notes 1. During boundary scan mode the level of the following pins must be fixed: P10_1: Low, P10_2: High, P10_8: High

2. The pin availability of JP0_6/ $\overline{\text{EVTO}}$ depends on the selected device.

In case of the digital I/O pins shared with an analog buffer the boundary scan function only applies to the general I/O function:

- ADCA0: AP0, P8 and P9
- ADCA1: AP1, P18 and P19 (availability depending on the device)

10. Differences to RH850/F1L/M/H, RH850/F1Kx and RH850/F1K

This chapter provides an overview about the differences between the RH850/F1KM, RH850/F1KH, RH850/F1x and RH850/F1K.

For details about device related differences, please refer to the application note “F1Kx Migration Information” (R01AN2917EDxxxx).

11. Reference Documents

Item	Document No.	Document Title
1	R01UH0684EJxxxx	Preliminary User's Manual Hardware RH850/F1KH, RH850/F1KM (including electrical characteristics)
2	R20UT3985EJxxxx	E1/E20 Emulator, E2 Emulator Additional Document for User's Manual (Notes on Connection of RH850/F1KH and RH850/F1KM)
3	R01AN2917EDxxxx	Application Note "F1KM Migration Information"
4	R01UH0562EJxxxx	User's Manual Hardware RH850/F1K (including electrical characteristics)
5	R20UT3431EJxxxx	E1/E20 Emulator, E2 Emulator Additional Document for User's Manual (Notes on Connection of RH850/F1K)
6	R20UT4469EJxxxx	PG-FP6 Flash Memory Programmer User's Manual

12. Abbreviations

ADC	A/D-converter
HSOSC	internal High-speed Oscillator
HWTRG	Hardware Trigger
MOSC	Main Oscillator
MPX	Multiplexer
SG	Scan Group
SOSC	Sub Oscillator
SWTRG	Software Trigger

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Revision History

Rev.	Date	Description	
		Section	**Summary**
0.50	2017-04-25	-	Initial version
0.90	2017-07-11	-	Typing error correction
		-	Description of RH850/F1KH-D8 added to related chapters
		-	Change of some chapter titles due to Renesas internal rules
		4.1	Added description about electromagnetic interference and susceptibility
		4.3.5	Changed “HALT Mode” to “HALT State”
		5	Reference of RH850 SENT application note added
		6.4	RH850/F1KH description added to Notes
		7	• Corrected device operation mode overview table • Caution added
		8.1	Some device naming corrected to RH850/F1KM-S1
		8.3	Some device naming corrected to RH850/F1KM-S4
		11	Added document reference of RH850 SENT application note
1.00	2019-04-26	-	• Typing error correction • Target device/product reference adjusted to updated product line-up • Removal of some chapters and title headers • Aligned some keywords • Improved information of reference (chapter etc.)
		1.1.1	Added description of note
		1.1.2	Added connection information
		1.1.3	• Modified figure • Described all power supply cases
		1.1.4	• Added figure of recommended power configuration • Added voltage range which has to be kept voltage slope • Modified power up/down timing • Some keywords aligned
		1.3.1	Added description of note
		1.3.2	Added connection information
		1.3.3	• Modified figure • Described all power supply cases
		1.3.4	• Added figure of recommended power configuration • Added voltage range which has to be kept voltage slope • Modified power up/down timing • Some keywords aligned
		1.4.1	Added description of note
		1.4.2	Added connection information
		1.4.3	• Modified figure • Described all power supply cases
		1.4.4	• Added figure of recommended power configuration • Added voltage range which has to be kept voltage slope • Modified power up/down timing • Some keywords aligned
		1.5	• Changed capacitor value • Modified figure for capacitor placement
		2.1	• Changed capacitor value • Modified contents of the table and notes
		2.3	• Changed capacitor value • Modified contents of the table and notes

		2.4	• Changed capacitor value • Modified contents of the table and notes • Modified the power source of Flash
		3	Added information of gain setting in the caution
		4.3.5	Modified the contents of the table
		4.5	Added detailed information about injected current
		6.1	Modified the number of clocks on the figure of ADC conversion time
		6.3	Removed RIN and CIN values for ADC equivalent circuit, and added reference information
		6.4	• Modified note • Modified contents of external components • Added guidance for formula of charge-sharing
		6.5	Added information regarding sampling error
		8	• Merged connection information of each device to one section • Removed “Debug and Flash Programming Interface Connection when the internal HSOSC is used as Clock Supply” • Modified FLMD0 resistance value • Modified LPDIO resistance value
		9	Modified FLMD0 resistance value
		10	Deleted contents and referred F1KM Migration Guide
1.10	2019-08-08	-	• Typing error correction • Description of RH850/F1K series added to related chapters • Document references updated to cover RH850/F1Kx and RH850/F1K documentation
		1.4.4	Modified Figure 14 and Figure 15
		2.1	Capacitor and resistor re-numbered
		3.1.1	Updated MOSC table to include RH850/F1Kx and RH850/F1K
		3.2	Reference of “PCB-Design for Improved EMC” removed
		4.1.1	Adjusted description to be synchronized with RH850/F1Kx and RH850/F1K HW UM
		4.2.1	Reference of “PCB-Design for Improved EMC” removed
		5	• Chapter title updated • Reference of application note removed
		8.1	• Note added at P10_8 (FLMD1) for clarification and understanding • Removed pull-up resistance on JP0_0/TDI/LPDIO/LPDI at LPD4 as it is only required for LPD1 • Caution about P10_8/FLMD1 removed • Target connector name on Figure 40 modified
		8.2	PG-FP5 replaced by PG-FPx
		8.2.1	• Note added at P10_8 (FLMD1) for clarification and understanding • Caution about P10_8/FLMD1 removed • PG-FP5 replaced by PG-FPx
		8.2.2	• Note added at P10_8 (FLMD1) for clarification and understanding • PG-FP5 replaced by PG-FPx
		8.3	• Target connector name on Figure 43 modified
		11	• Reference of SENT application note removed • Reference of “PCB-Design for Improved EMC” removed • RH850/F1K hardware manual added • E1/E2 emulator add-on manual for F1K added • PG-FP6 flash programmer manual added

1.20	2021-02-03	-	• Typing error correction • New template applied • Description of RH850/F1KM-S2 group added to related chapters

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external $\overline{\text{RESET}}$ pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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