RH850/F1K Series

Hardware Design Guide

R01AN2911EJ0100
Rev. 1.00
Aug 04, 2016

Introduction

This application note is intended to provide RH850/F1K series specific information and recommendations on the device usage. It should be used in conjunction with the corresponding RH850/F1K series user manual (includes the electrical characteristics).

Target Device

RH850/F1K Group

- RH850/F1K ECO Line
  - 176 pin
  - 144 pin
- RH850/F1K ADVANCED line
  - 176 pin
  - 144 pin
  - 100 pin
- RH850/F1K PREMIUM Line
  - 176 pin
  - 144 pin
  - 100 pin

Table of Contents

Table of Figures

Table of Tables

1. Power Supply

1.1 Power Supply Overview of RH850/F1K Group

1.1.1 Power Supply Pin Overview of RH850/F1K Group

The devices of the RH850/F1K group have the following power supply pins.

Table 1 Power supply pin overview

Device	Power Supply Pins
RH850/F1K (176pin)	REGVCC EVCC, EVSS AnVREF, AnVSS (n = 0, 1)
RH850/F1K (144pin)	REGVCC EVCC, EVSS AnVREF, AnVSS (n = 0, 1)
RH850/F1K (100pin)	REGVCC EVCC, EVSS A0VREF, A0VSS

The pins AWOVCL, AWOVSS and ISOVCL, ISOVSS are available on all devices to connect external capacitors.

1.1.2 Power Supply Pin Configuration of RH850/F1K Group

Depending on the device, the following power supply pin configuration applies:

The EVCC supply pins are internally connected.

1.1.3 Power Supply Pin Architecture of RH850/F1K Group

The RH850/F1K group supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1K group device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1K group:

- REGVCC = EVCC = VPOC to 5.5V
- A0VREF = 3.0V to 5.5V
- A1VREF = 3.0V to 5.5V
- AWOVSS = ISOVSS = EVSS = A0VSS = A1VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

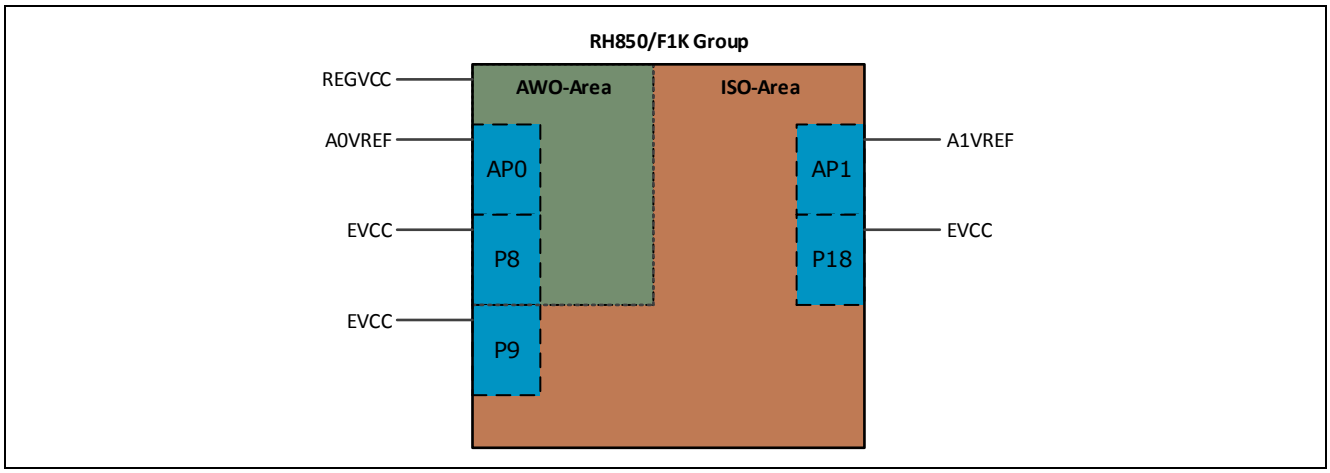


Figure 1 RH850/F1K Power supply architecture

Table 2 Power supply architecture RH850/F1K with single supply 5V

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 3 Power supply architecture RH850/F1K with single supply 3.3V

Case 2 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Table 4 Power supply architecture RH850/F1K with mixed supply 5V & 3.3V

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	Common condition REGVCC = EVCC not met
→	**Operation not permitted**

Table 5 Power supply architecture RH850/F1K with mixed supply 5V & 3.3V

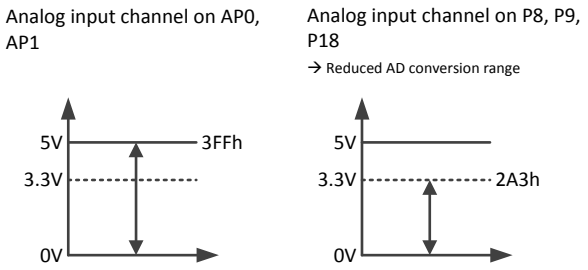
Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9 and P18
→	Operation permitted

Table 6 Power supply architecture RH850/F1K with mixed supply 5V & 3.3V

Case 5 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with digital function only P9 – Port usable with digital function only AP1 – Port usable with analog or digital function P18 – Port usable with digital function only
Limitation	No limitation applies to P8, P9 and P18 when these ports are used as digital port only.
→	Operation permitted

Table 7 Power supply architecture RH850/F1K with mixed supply 5V & 3.3V

Case 6 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V
Limitation	Analog port function limitation applies to P8, P9 and P18.
→	Operation permitted

1.1.4 Power Supply Timing of RH850/F1K Group

The RH850/F1K group has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms.

For details on the electrical characteristics, please refer to the corresponding device RH850/F1K hardware user's manual.

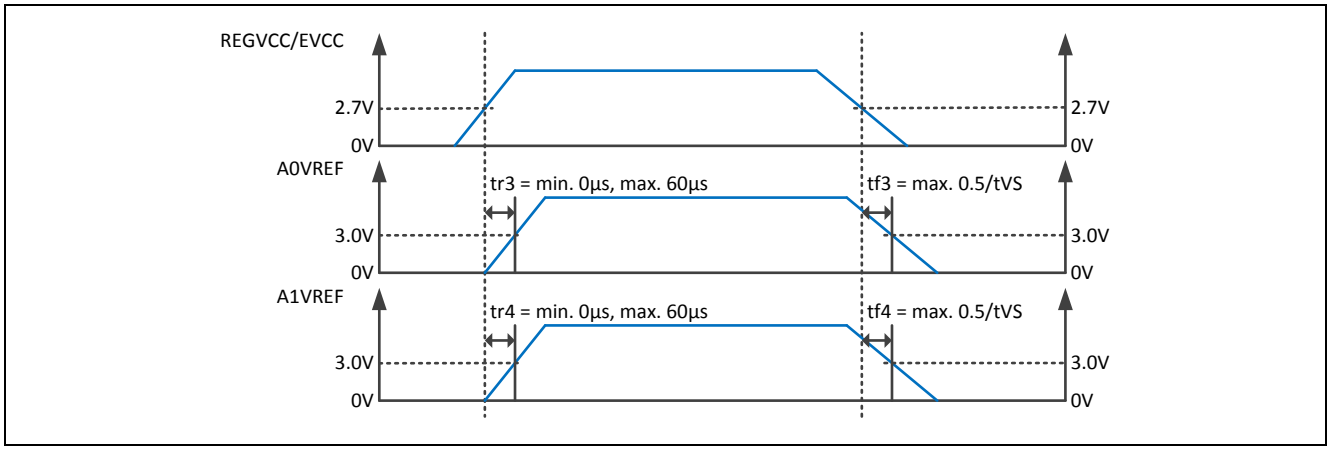


Figure 2 RH850/F1K Power up/down timing

Note: tVS is the timing of the voltage slope

1.2 Principle Capacitor Placement at REGVCC of RH850/F1K Group

When the data flash of the RH850/F1K group will be used in the application it should be considered to add an additional capacitor to the REGVCC pin and to use a close component placement to the supply pin in order to optimize the EMI noise behavior during the program and erase operation of the data flash.

The following recommendations shall be considered for the capacitor placement of the additional capacitor for EMI optimization during data flash operation at the REGVCC pin:

- Capacitor: 4.7µF to 10µF
- Pin: REGVCC
- Layout/distance: Capacitor within 10mm from mounting pad

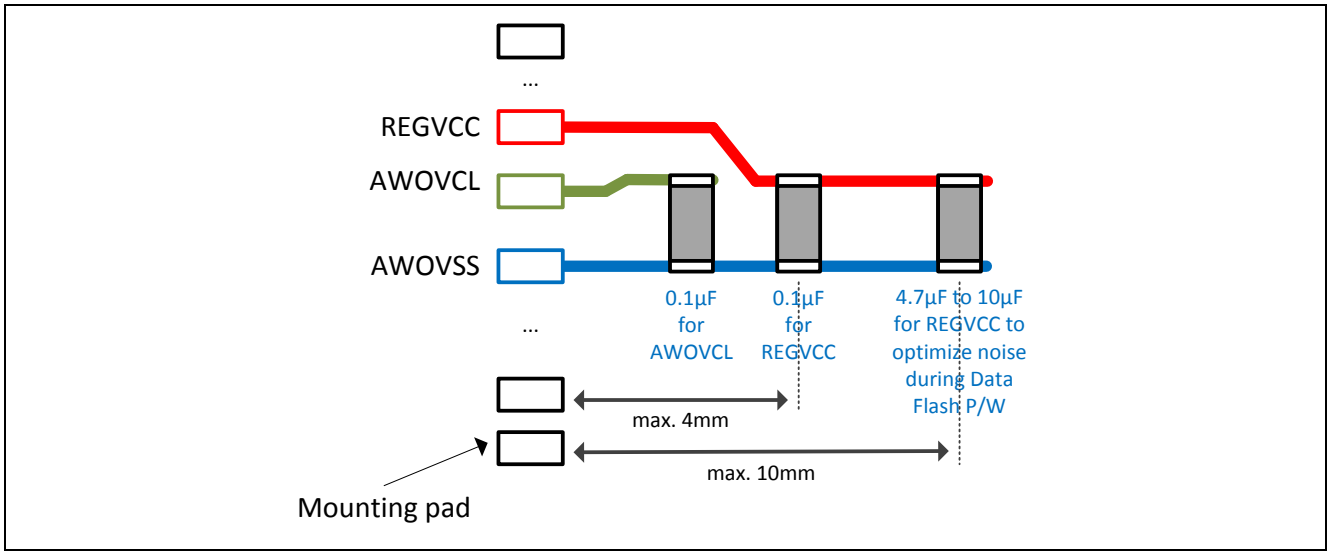


Figure 3 Principle capacitor placement at REGVCC for EMI at data flash operation

2. Minimum External Components

The RH850/F1K series requires a certain number of external connections and components for a proper operation in normal operation mode. The components are shown in different categories depending on the device operation and the use case.

2.1 Minimum External Components of RH850/F1K Group

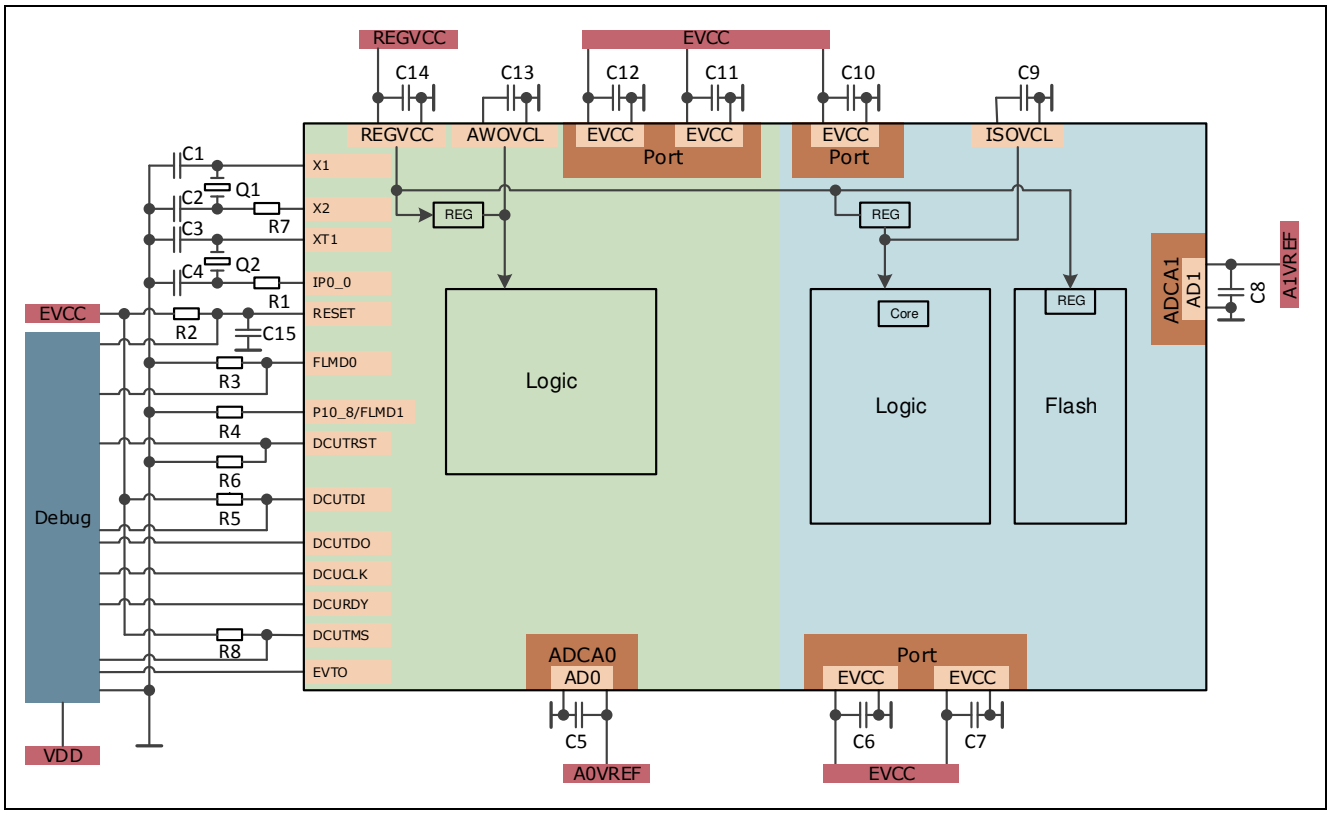


Figure 4 Minimum external components for RH850/F1K (176pin) for normal operation mode

Note: The debug interface connections shown covers Nexus, LPD 1pin and LPD 4pin. For details of the single debug connection, please refer to the corresponding debug interface connection chapter. For details of other external components, refer to their related chapters.

Table 8 Minimum external components for RH850/F1K (176pin)

Component	Value			Category
	Min.	Typ.	Max.	
Q1	16MHz	-	24MHz	Typical
Q2	-	32.768kHz	-	Typical
R1	-	100kΩ[Note 1]	-	Typical
R2	1kΩ[Note 3]	4.7kΩ[Note 3]	6.6kΩ[Note 3]	Required
R3	86kΩ[Note 6]	100kΩ[Note 7]	105kΩ[Note 6]	Required
R4	-	10kΩ[Note 5, 7]	-	Typical
R5	-	1k to 4.7kΩ[Note 4, 7, 8]	-	Typical
R6	10kΩ[Note 9]	-	100kΩ[Note 9]	Required
R7	-	0Ω[Note 1]	-	Typical
R8	-	Optional[Note 10]	-	Typical
C1, C2	-	10pF[Note 1]	-	Typical
C3, C4	-	12pF[Note 1]	-	Typical
C5, C6, C7, C8, C10, C11, C12, C14	-	100nF[Note 2]	-	Recommended
C9, C13	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required
C15	-	1nF to 10nF[Note 3]	-	Recommended

Notes 1. The shown values for reference only.
The final values must be evaluated (with the resonator manufacturer).

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the electrical characteristics (described in the RH850/F1K hardware user's manual).

3. See chapter RESET for details.

4. For values much smaller than the typical values, the connected devices might not be able to apply a low level to the signal. Additionally higher currents will flow through the resistor / device.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS *can* be applied. *But* in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (E1) is not able to apply a high ('1') signal.

7. For values much higher than the typical value, the required signal timings might not be achieved due to the weaker currents. Additionally environmental effects (e.g. moisture and dirt) might generate other weak currents and therefore influence the signal.

8. See chapter Development and Test Tool Interface for details.

9. See chapter JP0_4/_DCUTRST and chapter Recommended Connection of Unused Pins for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See chapter Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of typ. 4.7µF to 10µF in parallel to the capacitor C15 at REGVCC. The value and PCB placement of the parallel capacitor depends on the application requirements.

3. Oscillator

3.1 Recommended Oscillator Circuit

3.1.1 Main Oscillator

A crystal or ceramic resonator can be connected to the main clock input pins as shown below.

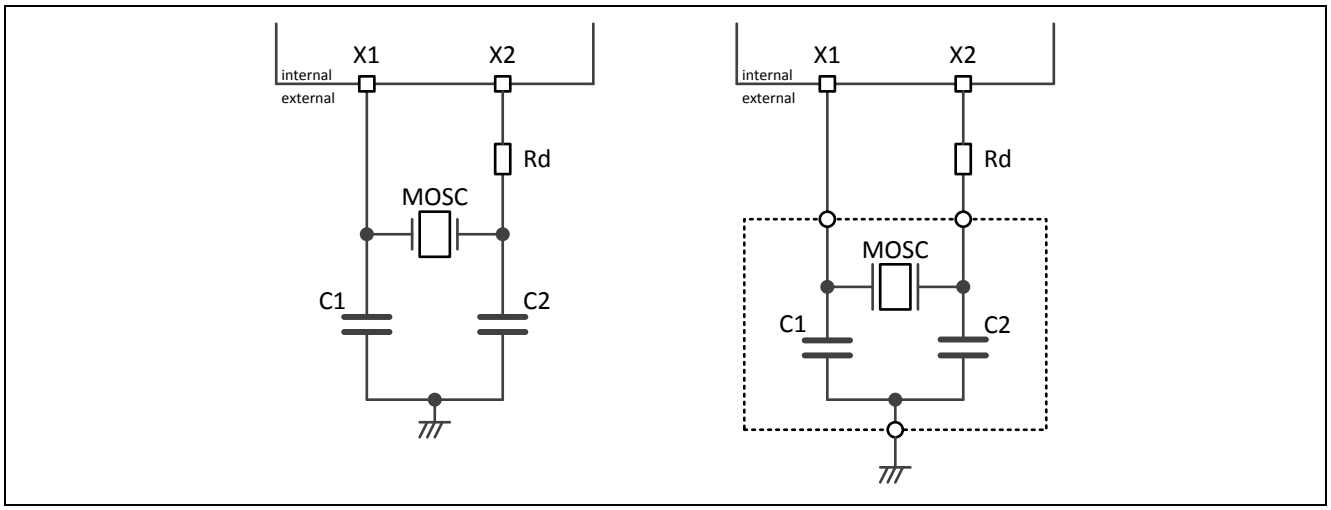


Figure 5 Recommended main oscillator circuit

General guidance values of the main oscillator circuit:

Table 9 Guidance values of the main oscillator circuit

Component	Value
MOSC	16MHz, 20MHz, 24MHz
C1	10pF
C2	10pF
Rd	0Ω

Caution

Values of C1, C2 and Rd depend on the use of ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

3.1.2 Sub Oscillator

A crystal resonator can be connected to the sub clock input pins as shown below.

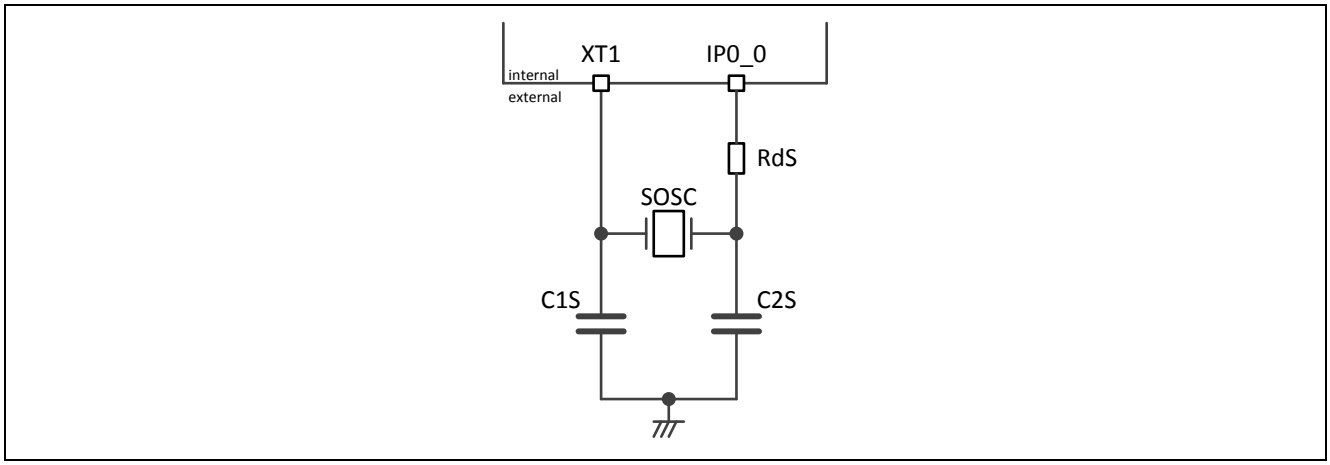


Figure 6 Recommended sub oscillator circuit

General guidance values of the sub oscillator circuit:

Table 10 Guidance values of the sub oscillator circuit

Component	Value
SOSC	32.768kHz
C1S	12pF
C2S	12pF
RdS	100kΩ

Caution

Values of C1S, C2S and RdS depend on the crystal resonator used and must be specified in cooperation with a crystal resonator manufacturer.

3.2 Recommended Oscillator Layout

General guidance for PCB layout:

- Keep the wiring length as short as possible
- Do not cross the wiring with other signal lines
- Do not route this circuit close to a signal line with high fluctuating current flow
- Always make the ground point of the oscillator capacitor the same potential as AWOVSS
- Do not ground the capacitor to a ground pattern with high current flow
- Do not tap signals from the oscillator

For further layout, related recommendations please refer to the application note “PCB-Design for Improved EMC” (R01AN0733EDxxxx).

4. Device Pins

4.1 RESET

4.1.1 Minimum RESET Circuit

The RH850/F1K series has an on-chip Power-on Clear (POC) circuit. Therefore, a specific external RESET circuit is not required and the minimum requirement of the RESET circuit is a resistor to EVCC for start-up of the device. The resistor should be dimensioned large enough to allow a RESET signal generated by development tool or flash programmer to control the RESET pin.

In addition, a capacitor should be added as protection against surges.

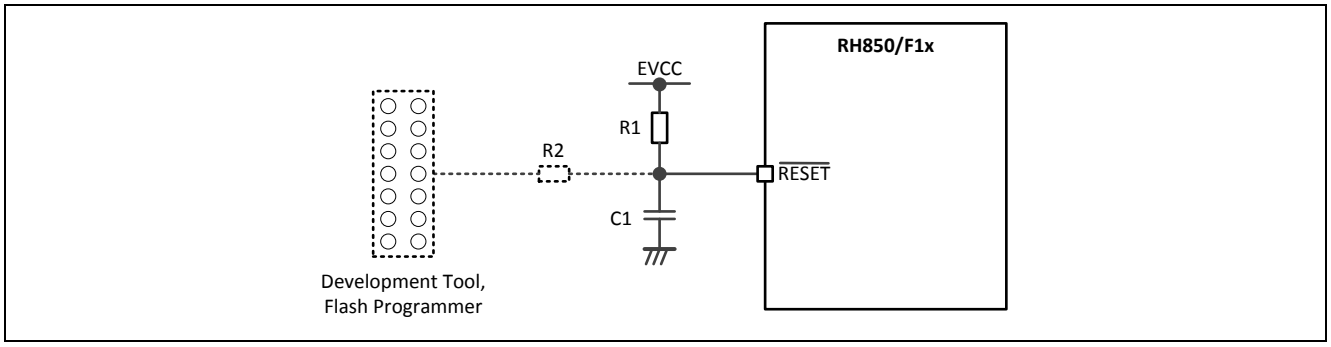


Figure 7 Minimum RESET circuit

General guidance values of the minimum RESET circuit:

Table 11 Guidance values for the minimum RESET circuit

Component	Value
R1	1 to 10kΩ
R2	100Ω
C1	1 to 10nF

The series resistor R2 is optional to suppress external signals from EMC point of view and depends on the application requirements.

The capacitor C1 can be adopted to a different value when the AC specification of the RESET (terminal) timing, the AC specification of the serial programmer setup timing and the EMC requirements of the ECU are fulfilled.

For further layout, related recommendations please refer to the application note “PCB-Design for Improved EMC” (R01AN0733EDxxxx).

4.1.2 RESET Input Characteristics

The RESET is passed through an internal analog noise filter to prevent erroneous resets due to spikes.

The following figure shows the timing when an external reset is performed. It explains the effect of the noise elimination.

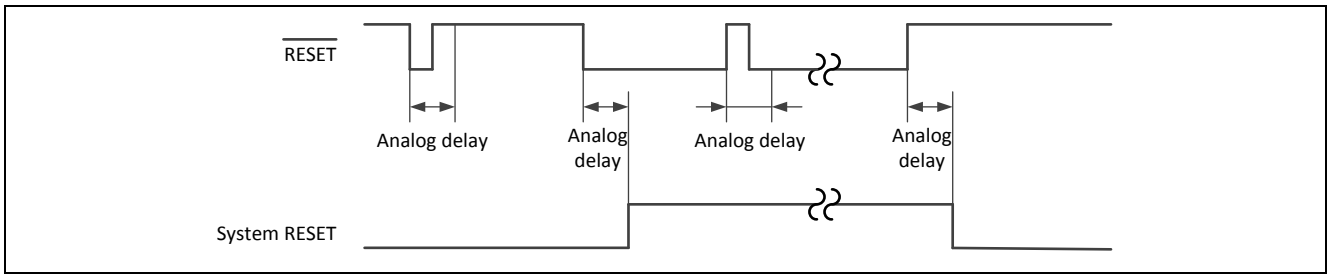


Figure 8 External RESET timing

The analog filter generates the analog delay. The filter regards pulses up to a certain width as noise and suppresses them.

For the minimum RESET pulse width and the minimum RESET pulse rejection, refer to the electrical characteristics described in the RH850/F1K hardware user's manual.

4.2 General Purpose I/O

4.2.1 RESET State of General Purpose I/O

During RESET state, all general-purpose I/O pins are in input mode with high-Z behavior except the pin P8_6/_RESETOUT.

4.2.2 JP0_4/_DCUTRST

During power-on, RESET the pin JP0_4 should not be driven externally to high-level. Therefore, JP0_4/_DCUTRST has to be connected in all device operation modes to EVSS via a resistor.

4.2.3 P8_6/_RESETOUT/NMI/CSIH0CSS4/PWGA38O/RTCAOUT/ADCA0I8S

When the _RESETOUT signal is selected for the P8_6 pin the output on the pin is at low level during a reset and after release from the reset state depending on the option byte setting (OPBT0[9] register).

P8_6 with alternate function

When P8_6 shall be used with an alternate function (e.g. NMI/CSIH0CSS4/PWGA38O/RTCAOUT, etc.), it has to be considered that the pin P8_6 is on low level after a Power-on RESET or any other device RESET source until it is released by the application software.

P8_6 and RESETOUT function

The pin P8_6 has an emulated RESETOUT function as default function. By this function, this pin can drive an output to low-level during and after reset, e.g. to reset an external ASIC. In addition, that RESETOUT function can be disabled that the pin P8_6 behaves like other pins with high-z during RESET state.

For further details, please refer to the chapter “P8_6: RESETOUT” of the RH850/F1K hardware user’s manual.

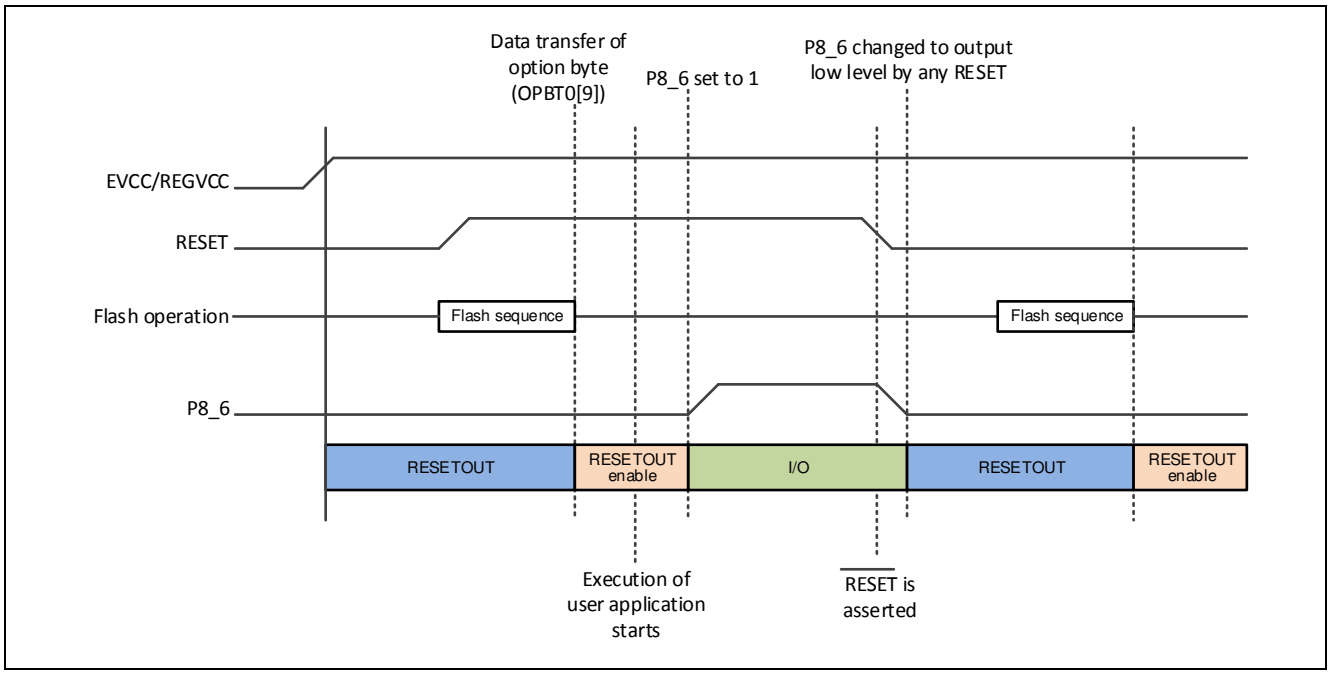


Figure 9 RESETOUT pin behavior at OPBT0[9] = 1

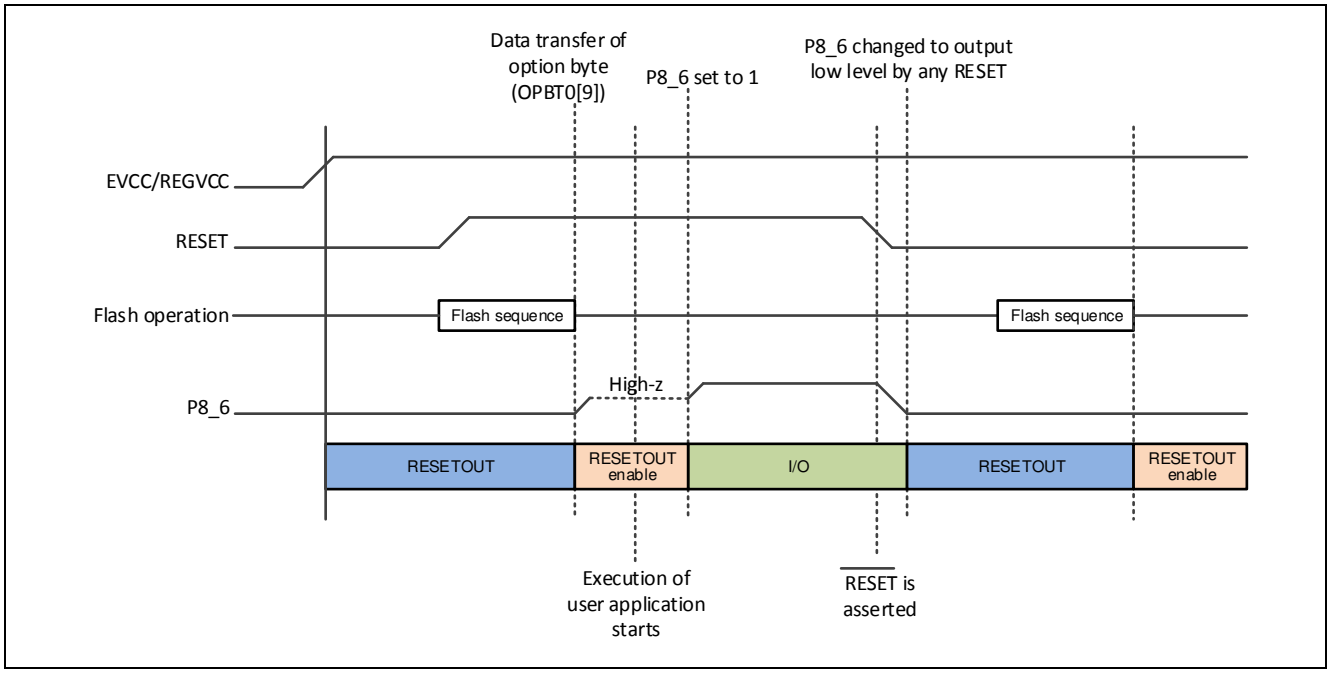


Figure 10 RESETOUT pin behavior at OPBT0[9] = 0

Caution

Until being disabled by register settings, the pin P8_6 drives an output low-level or high-z after any kind of reset. To avoid a data collision, the outside circuit connected to the P8_6 pin must not drive high-level.

4.2.4 Analog Filter Function

Depending on the alternative port functionality selected, some input signals of the device pins are passed through an analog filter - respectively analog delay stage - to remove noise and glitches from the input signal.

The detection level of the filtered input signal depends on the high-level/low-level input voltage of the port input buffer and its supported electrical characteristics.

After passing the external signal through an analog filter to eliminate noise and spikes, the event detection evaluates the level or any level change, i.e. an edge, of the signal and generates an output accordingly.

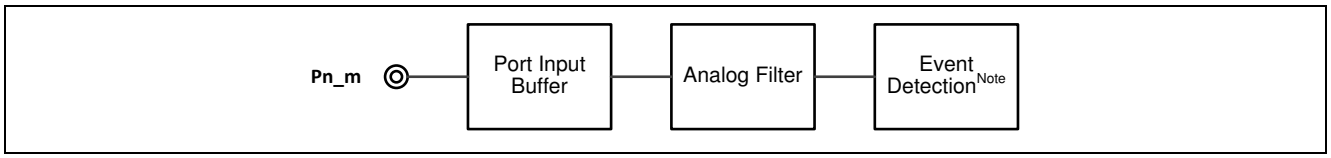


Figure 11 Analog Filter Function

Note: The event detection implementation depends on the analog filter type.

The input detection level as well as the pulse rejection of the analog filters are specified in the corresponding pin characteristics and peripheral chapters in the electrical characteristics of the RH850/F1K hardware user's manual.

4.2.5 Behavior during Low Power Mode

During the low power modes, different states apply for the ports and pins of the RH850/F1K series. The states depend on the chosen low-power mode and may not have the same behavior for ports and pins.

- Port means that a pin works as a general-purpose input/output pin.
- Pin denotes the physical pin. Every pin is denoted by a unique pin number.

The following overview provides a summary of the port and pin behavior during low-power modes:

Table 12 Behavior during low power mode

	Always-on Area		Isolated Area	
	Ports	**Pins**	**Ports**	**Pins**
HALT Mode				
STOP Mode				
DEEP STOP Mode				
Cyclic RUN Mode				
Cyclic STOP Mode				

	Functional

	State before entering the mode is kept

	The ports are not powered and therefore not functional
	
	I/O hold function for isolated area
	• During the DEEP STOP mode, the state of the port pins on the isolated area can be held automatically. Thus, its input and/or output remain in the same state as before entering I/O buffer hold state. No external or internal signal can change its state until the I/O buffer hold state is terminated.
	• The I/O buffers in DEEP STOP mode are changing into I/O buffer hold state by default.
	• After the wake-up from DEEP STOP mode the I/O buffer hold state is terminated in the following steps:
	  ○ 1. Re-configure the peripheral or port function
	  ○ 2. Release I/O hold state by setting IOHOLD.IOHOLD = 0

4.3 Recommended Connection of unused Pins

4.3.1 Recommended Connection of unused Pins for RH850/F1K Group

Table 13 Recommended Connection of unused Pins for RH850/F1K Group

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF	Connect to EVCC
A0VSS, A1VSS	Connect to EVSS
RESET	Connect to EVCC via a resistor
X1	Connect to AWOVSS via a resistor
X2	Leave open
XT1	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or connected to AWOVSS (bit 0 of IPIBC0 = 0)
IP0_0/XT2	Connect to REGVCC or AWOVSS via a resistor[Note4] (bit 0 of IPIBC0 = 1) or leave open (IPIBC0.0 bit = 0)
P0 P1 P2 P8 (excluding P8_6) P9 P20	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC of EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P8_6	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2, P10_6 and P10_8) P11 P12 P18	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC of EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10_1 P10_2 P10_6 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note3
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note2	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Connect to EVCC via a resistor _DCUTRST (JP0_4): Connect to EVSS via a resistor Note3 _DCURDY/LPDCLKOUT (JP0_5): Leave open _EVTO (JP0_6): Leave open Note1

Notes
1. The pin availability depends on the selected device.
2. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, please refer to the chapter Debug Interface Connection.
3. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
4. XT1 = IP0_0 (XT2) = REGVCC or AWOVSS should be set.

   XT1 is connected to IP0_0 (XT2) through an internal resistor. Therefore, it is necessary to maintain an equal voltage level in order not to generate a current path.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1K-2 group, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

4.4 Pin Assignment Differences

The pin assignment of the RH850/F1K (176pin), RH850/F1L (176pin) and the RH850/F1M (176pin) shows some hardware related differences as described in the table below.

Table 14 Basic pin assignment differences

RH850/F1K-2 (176pin) Pin Assignment	RH850/F1L (176pin) Pin Assignment	RH850/F1M (176pin) Pin Assignment
EVCC	BVCC	BVCC
EVSS	BVSS	BVSS
P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / CSIH0SSI / DPO	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / CSIH0SSI / DPO / RESETOUT	P0_0 / TAUD0I2 / TAUD0O2 / RLIN20RX / CAN0TX / PWGA10O / CSIH0SSI / DPO / RESETOUT
P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S / RESETOUT	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S	P8_6 / NMI / CSIH0CSS4 / PWGA38O / RTCA0OUT / ADCA0I8S
P8_5 / TAUJ0I3 / TAUJ0O3 / NMI / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S	P8_5 / TAUJ0I3 / TAUJ0O3 / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S	P8_5 / TAUJ0I3 / TAUJ0O3 / CSIH0CSS3 / INTP9 / PWGA37O / ADCA0I7S
P8_7 / CSIH3CSS0 / PWGA39O / ADCA0SEL0 / RTCA0OUT / ADCA0I14S	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0I14S	P8_7 / CSIH3CSS0 / PWGA39O / ADCA0I14S
P9_5 / CSIH0CSS6 / PWGA34O / TAUJ1I1 / TAUJ1O1 / ADCA0I12S	P9_5 / CSIH0CSS6 / PWGA34O / TAUJ1I1 / TAUJ1O1 / ADCA0I12S	ISOVCL
P9_6 / CSIH0CSS7 / PWGA35O / ADCA0I13S	P9_6 / CSIH0CSS7 / PWGA35O / ADCA0I13S	ISOVSS
P0_8/ RLIN21TX / DPIN6 / CSIH0CSS6 / CSIH1SSI / TAUB0I2 / TAUB0O2 / CAN3TX	P0_8/ RLIN21TX / DPIN6 / CSIH1SSI / TAUB0I2 / TAUB0O2 / CAN3TX	P0_8 / RLIN21TX / DPIN6 / CSIH0CSS6 / CSIH1SSI / TAUB0I2 / TAUB0O2 / CAN3TX
P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX	P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / ADCA0I10S	P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S
P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
P11_1 / CSIH2SSI / RLIN20RX / CSIH0CSS7 / PWGA26O / TAUB0I13 / TAUB0O13	P11_1 / CSIH2SSI / RLIN20RX / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9	P11_1 / CSIH2SSI / FLXA0TXDA / RLIN20RX / CSIH0CSS7 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9

Note: The pin assignment differences due to functional differences (e.g. number of peripheral channels) are not described in the table above and have to be verified based on the pin assignment of the corresponding products.

4.5 Injected Current

The RH850/F1K series has different electrical characteristics for the injected current depending on the pin group and device pins of the different package variants.

For details, please refer to the electrical characteristics of the related RH850/F1K hardware user's manual.

5. A/D-Converter

5.1 Conversion Time

The ADC conversion time consists of a number of timing parameters, which are summed-up to get the conversion timing depending on the application.

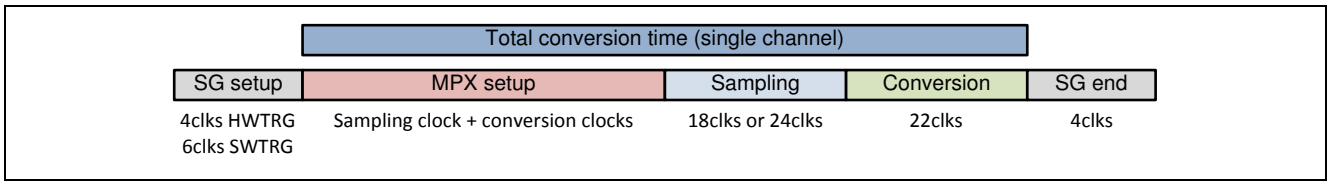


Figure 12 ADC conversion time

Notes:
1. SG - Scan Group
2. MPX - External multiplexer
3. HWTRG - Hardware trigger
4. SWTRG - Software trigger

The setting of the ADC clock and the sampling time results in the following conversion timing:

Table 15 ADC conversion time overview

ADCLK [MHz]	Sampling time [clks]	MPX Setup time [µs]	Sampling time [µs]	Conversion time [µs]	Total conversion time (excluding MPX) [µs]	Total conversion time (including MPX) [µs]
40	24	1.15	0.60	0.55	1.15	2.30
32	18	1.25	0.56	0.69	1.25	2.50
32	24	1.44	0.75	0.69	1.44	2.88
24	18	1.67	0.75	0.92	1.67	3.33
24	24	1.92	1.00	0.92	1.92	3.83
8	18	5.00	2.25	2.75	5.00	10.00
8	24	5.75	3.00	2.75	5.75	11.50

Note: The sampling time is set by the ADCAnSMPCR.SMPT [7:0] bits.

5.2 External Multiplexer Wait Time

When an external multiplexer is used to extend the number of analogue input channels, a fixed wait time/set-up time of one conversion time has to be taken into account.

5.3 Equivalent Input Circuit

The A/D-converters have different options for the input with track & hold path or direct path only. Please refer to the user's manual, which A/D-converter is supported by the chosen device.

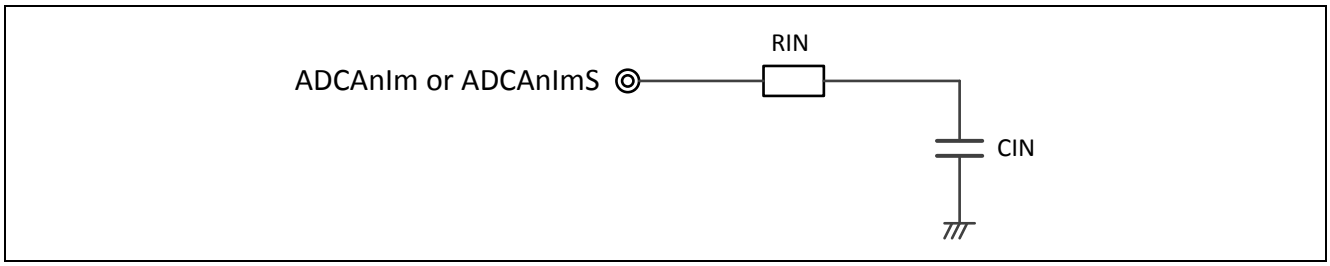


Figure 13 ADC equivalent input circuit

Table 16 Equivalent input circuit of ADCA0

ADCA0			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA0I0 to ADCA0I5	Channel T&H is not used	3.9	2.1
ADCA0I0 to ADCA0I5	Channel T&H is used	14.0	1.8
ADCA0I6 to ADCA0I15		3.9	2.1
ADCA0I0S to ADCA0I3S, ADCA0I5S to ADCA0I16S		5.0	8.6
ADCA0I4S, ADCA0I17S to ADCA0I19S		5.4	8.6

Table 17 Equivalent input circuit of ADCA1

ADCA1			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA1I0 to ADCA1I15		3.6	1.8
ADCA1I0S to ADCA1I17S		4.7	4.5

Caution

These specifications are not tested during outgoing inspection. Therefore, RIN and CIN are reference values only and not guaranteed. In addition, these values are specified as maximum values.

5.4 External Circuit on ADC Input

To preserve the accuracy of the A/D-converter, it is recommended that analog input pins have a low impedance. Therefore placing a capacitor at the analog input pin can provide an effective result. This capacitor contributes to noise filtering on the analog input pin. A basic filter can be realized by using a series resistor with a capacitor on the input pin (RC-filter).

The filter at the input pins should be designed taking into account the dynamic characteristics of the input signal, the equivalent input impedance of the ADC itself and the injected current specification of the analog input pins.

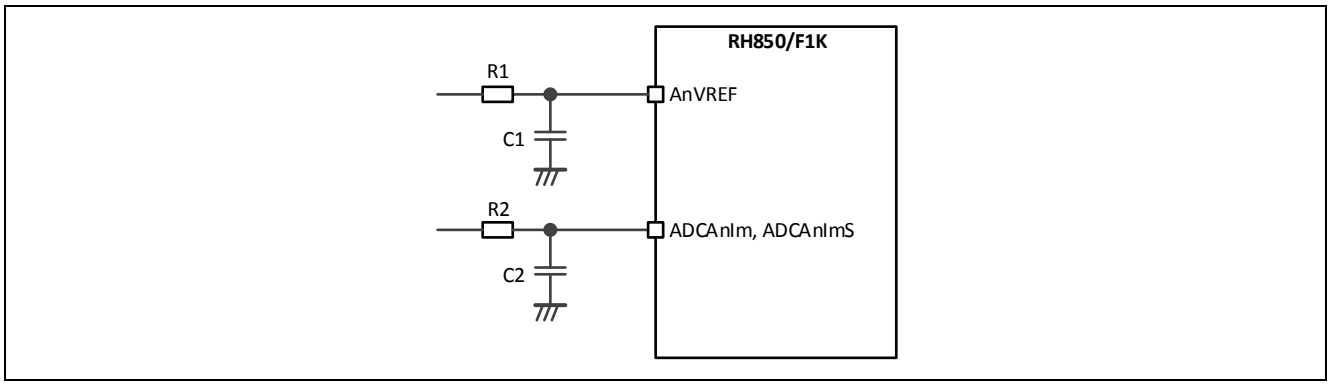


Figure 14 ADC external circuit on analog input

Note: RH850/F1K Group (max. device configuration) n = 0, m = 0 to 15, 0S to 19S
n = 1, m = 0 to 15, 0S to 7S

General guidance values of the basic external ADC input circuit:

Table 18 Basic external ADC input circuit

Component	Value
R1	2.2 to 6.8Ω
R2	10kΩ
C1	100nF
C2	10nF

The values of the resistor and capacitor depend on the application requirements.

In order to improve the electromagnetic susceptibility it should be considered to add a series resistor (R1) to the supply line of AnVREF. The combination of series resistor and capacitor (C1) placed close to the supply pin AnVREF helps to improve the resistance against electromagnetic disturbance.

The resistor value influences the conversion accuracy and depends on the application requirements.

In order to improve the accuracy of the ADC it is recommended to add a capacitor of minimum 2µF (typical 4.7µF) in parallel to the capacitor C1 at AnVREF. The value and PCB placement of the parallel capacitor depends on the application requirements.

As guide line for the calculation of the external capacitor at the analog input pin the formula based on the internal equivalent capacitance and the ADC resolution of the corresponding AD-converter channel can be used:

$$Cexternal = CIN \times 2^{ADCresolution}$$

Cexternal:	External capacitor at the analog input pin
CIN:	Equivalent input capacitance
ADCresolution:	AD-converter resolution for RH850/F1K-2 either 12-bit or 10-bit resolution

6. Development and Test Tool Interface

The RH850/F1x series supports the following operation modes that are used for debugging, flash programming and test by using boundary scan.

Table 19 Operation mode overview

FLMD0	P10_8 (FLMD1)	P10_1 (MODE0)	P10_2 (MODE1)	Operation Mode
0	x	x	x	Normal operation mode
1	0	x	x	Flash programming mode
1	1	0	1	Boundary scan mode
1	1	1	1	User boot mode

Note: x – Don't care

Table 20 Operation mode description

Operating Mode	Mode Description
Normal operating mode	Mode used for the execution of application software and during debugging.
Flash programming mode	Mode used during the flash memory program/erase of the device.
Boundary scan mode	Mode used for boundary scan test
User boot mode	Mode used for the execution of application software and during debugging, where the base address is fixed and the transition to stand-by modes is not supported.

6.1 Development Tool Interface of RH850/F1K Group

The description of the development tool interface in this chapter assumes that the normal operating mode of the MCU is used. When the user boot mode shall be used the configuration of the pins FLMD0, P10_8/FLMD1, P10_1/MODE0, P10_2/MODE1 and P10_6/MODE2 has to be set accordingly.

6.1.1 Debug Interface Connection of RH850/F1K Group

For the debugging environment, the following interface connections are supported:

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
    - The Nexus interface is only supported by 3rd party development tools.

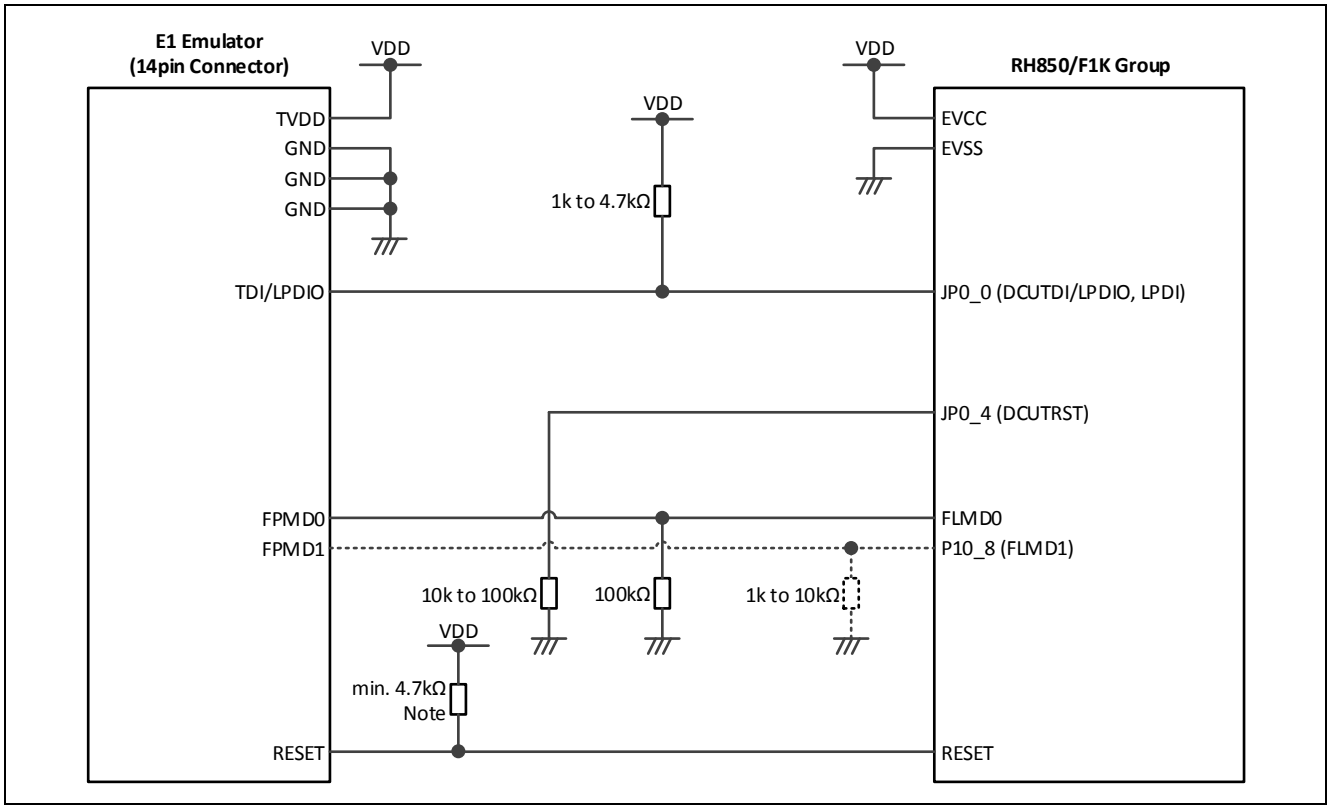


Figure 15 RH850/F1K 1pin Low-pin debug interface connection

Note: The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 1pin debug mode is used on the RH850/F1K group, the port of the JP0 port group is automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDIO input/output
- JP0_1: General-purpose I/O
- JP0_2: General-purpose I/O
- JP0_3: General-purpose I/O

- JP0_4: General-purpose I/O
- JP0_5: General-purpose I/O
- JP0_6: General-purpose I/O

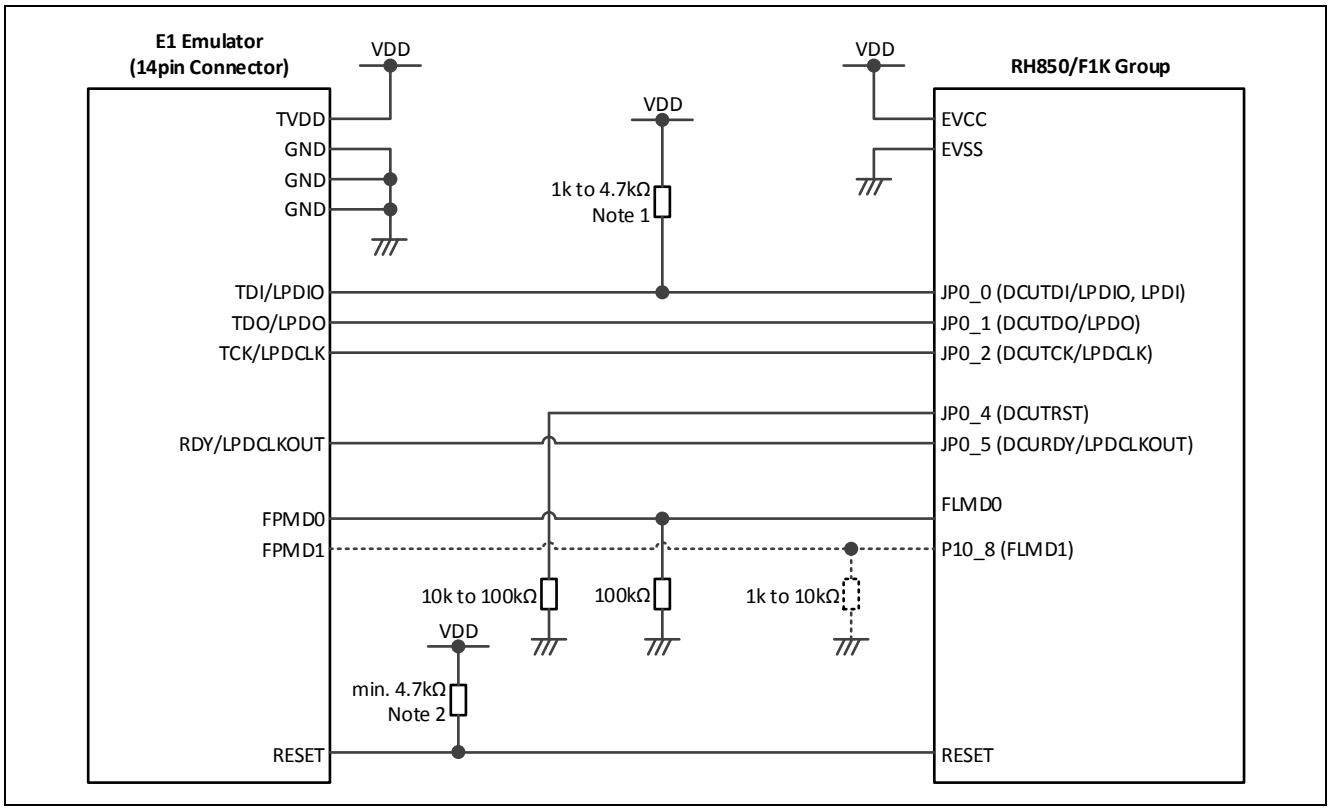


Figure 16 RH850/F1K 4pin Low-pin debug interface connection

Notes: 1. The resistor is optional in 4pin low-pin debug mode.

2. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 4pin debug mode is used on the RH850/F1K group, the ports of the JP0 port group are automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDI input
- JP0_1: LPDO output
- JP0_2: LPDCLK input
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: LPDCLKOUT output
- JP0_6: General-purpose I/O

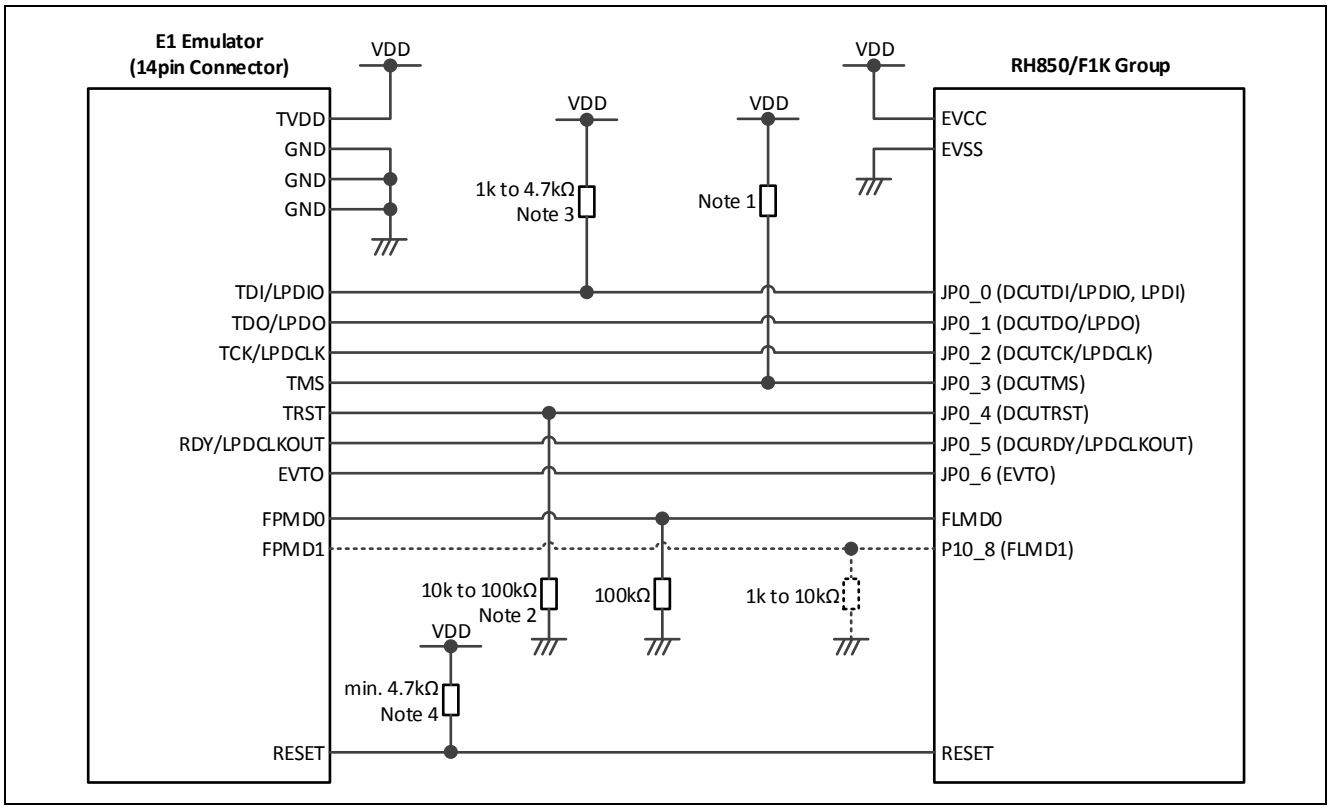


Figure 17 RH850/F1K Nexus, 4pin LPD and 1pin LPD debug interface connection

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the Nexus debug mode is used on the RH850/F1K group, the ports of the JP0 port group are automatically switched to the debug interface mode.

- JP0_0: DCUTDI input
- JP0_1: DCUTDO output
- JP0_2: DCUTCK input
- JP0_3: DCUTMS input
- JP0_4: DCUTRST input
- JP0_5: DCUTRDY output
- JP0_6: EVTO

The debug interface signal connection of the E1 interface is given in the table below:

Table 21 Debug interface signal connection of RH850/F1K

E1 Interface Connector	E1 Interface Signal	RH850/F1K Device Pin
1	LPDCLK/(DCUTCK)	JP0_2
2	GND	EVSS
3	(DCUTRST)	JP0_4
4	FPMD0/FLMD0	FLMD0
5	LPDO/(DCUTDO)	JP0_1
6	FPMD1	FLMD1
7	LPDI/LPDIO/(DCUTDI)	JP0_0
8	TVDD	EVCC
9	(DCUTMS)	JP0_3
10	(EVTO)	JP0_6
11	LPDCLKOUT/(DCURDY)	JP0_5
12	GND	EVSS
13	RESET	RESET
14	GND	EVSS

Note: The Nexus interface signals marked with (*text*) are supported by 3rd party development tools and not by E1 emulator.

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

6.1.2 Flash Programming Interface Connection of RH850/F1K Group

For the programming environment PG-FP5, the following connections are supported:

- Single-wire asynchronous flash programming interface
- Two-wire asynchronous flash programming interface
- Synchronous flash programming interface

For the programming environment combination of E1 emulator and RFP, the following connections are supported:

- Single-wire asynchronous flash programming interface
- Two-wire asynchronous flash programming interface

Table 22 Basic flash programming connection of RH850/F1K

Flash Programming Interface	Function	RH850/F1K Device Pins
1-wire UART	RxD/TxD	JP0_0
2-wire UART	RxD	JP0_0
	TxD	JP0_1
CSI	SI	JP0_0
	SO	JP0_1
	SCK	JP0_2

(a) **Flash Programming by PG-FP5**

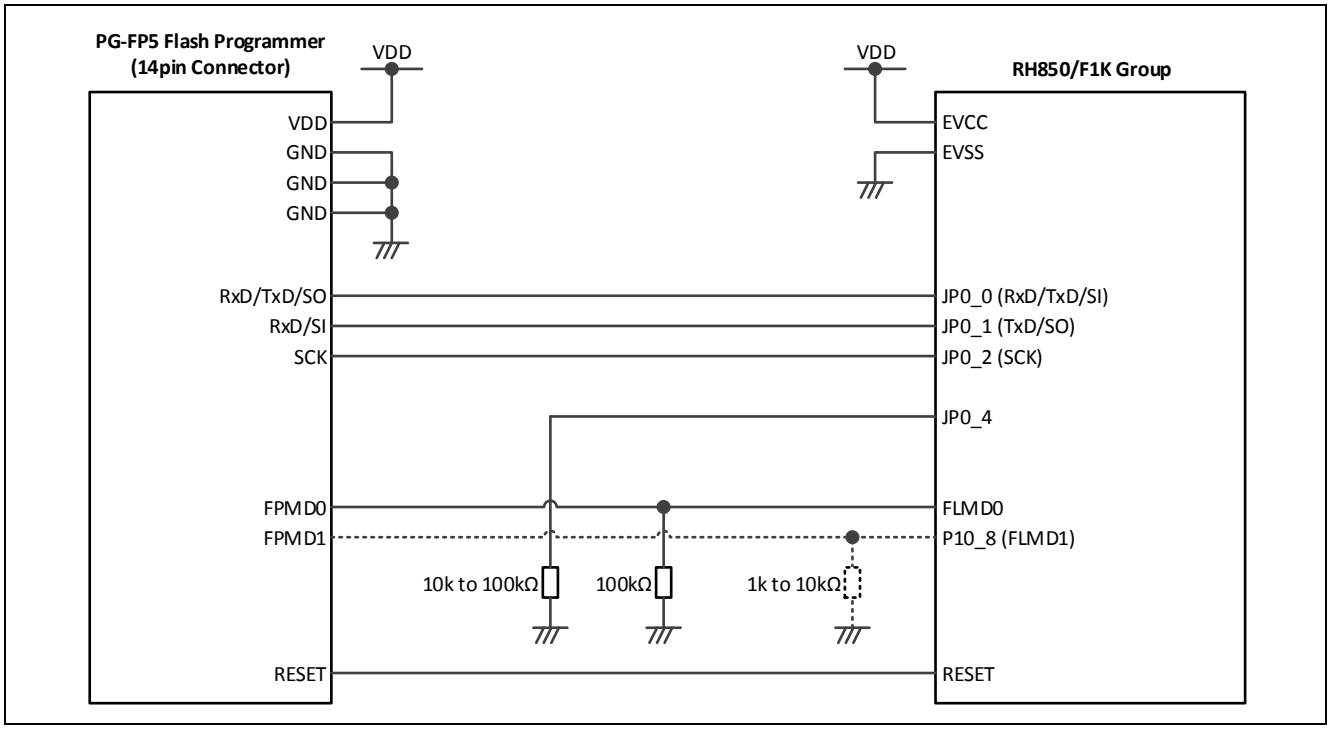


Figure 18 RH850/F1K PG-FP5 flash programming interface connection

The flash programming signal connection of the PG-FP5 interface is given in the table below:

Table 23 PG-FP5 Flash programming signal connection of RH850/F1K

PG-FP5 Interface Connector	PG-FP5 Signal	RH850/F1K Device Pin
1	SCK	JP0_2
2	GND	EVSS
3	-	-
4	FPMD0	FLMD0
5	SI/RxD	JP0_1
6	FPMD1	FLMD1
7	SO/TxD	JP0_0
8	VDD	EVCC
9	-	-
10	-	-
11	-	-
12	GND	EVSS
13	RESET	RESET
14	-	-

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

(b) **Flash Programming by E1 emulator and RFP**

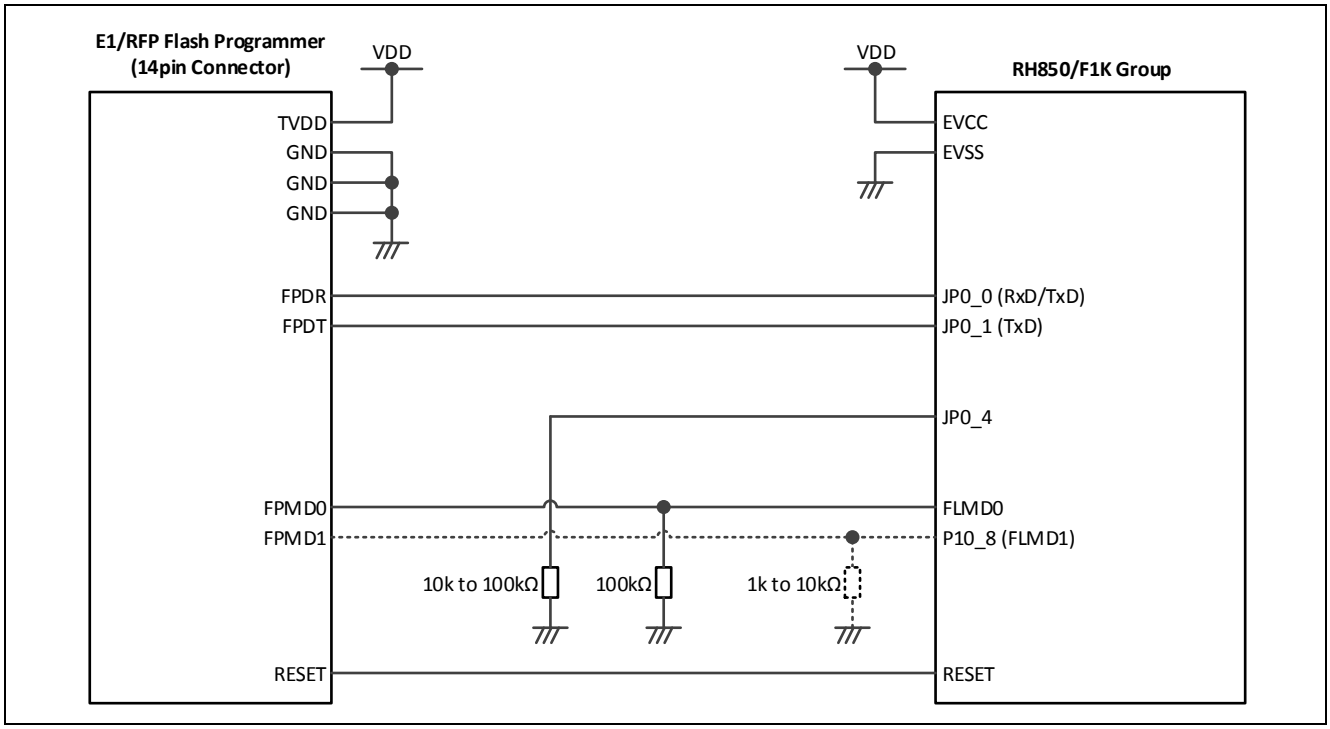


Figure 19 RH850/F1K E1 flash programming interface connection

The flash programming signal connection of the E1 interface is given in the table below:

Table 24 E1 Flash programming signal connection of RH850/F1K

E1 Interface Connector	E1 Signal	RH850/F1K Device Pin
1	-	-
2	GND	EVSS
3	-	-
4	FPMD0	FLMD0
5	FPDT	JP0_1
6	FPMD1	FLMD1
7	FPDR	JP0_0
8	TVDD	EVCC
9	-	-
10	-	-
11	-	-
12	GND	EVSS
13	RESET	RESET
14	GND	EVSS

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

6.1.3 Combined Debug and Flash Programming Interface Connection of RH850/F1K Group

The following figure describes the combined connections for debugging and flash programming of the RH850/F1K group, supporting

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
- Single-wire asynchronous flash programming interface with PG-FP5 or E1/RFP
- Two-wire asynchronous flash programming interface with PG-FP5 or E1/RFP
- Synchronous flash programming interface with PG-FP5

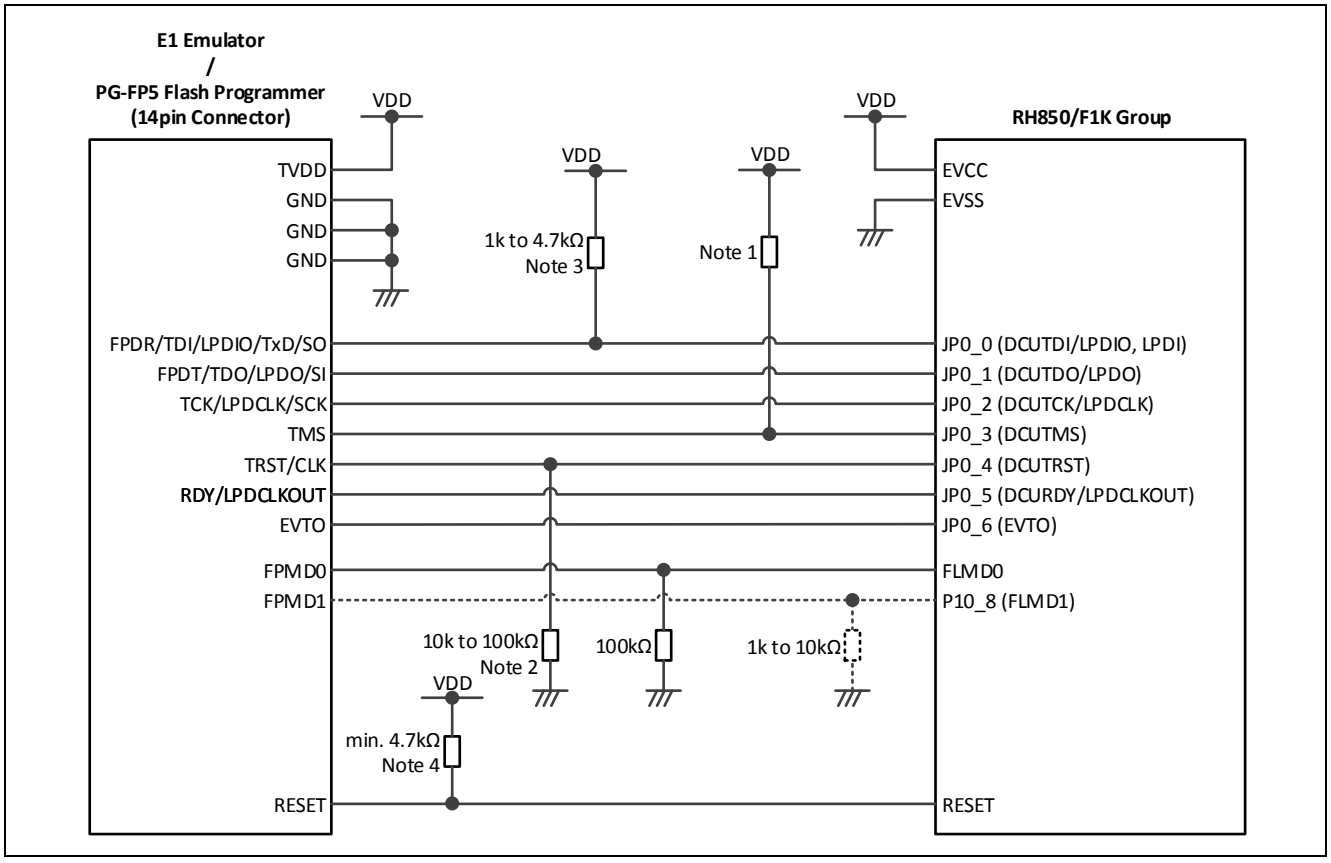


Figure 20 RH850/F1K Combined debug and flash programming interface connections

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

6.1.4 Debug and Flash Programming Interface Connection of RH850/F1K Group when the internal HSOSC is used as Clock Supply

When the devices of the RH850/F1K group are supply only with the internal high-speed oscillator (HSOSC) the following functions are supported

- 4pin Low-pin debug interface (4pin LPD)
- Synchronous flash programming interface with PG-FP5

The debugging by 1pin Low pin debug interface (1pin LPD) and the flash programming by UART interface is not supported when the internal HSOSC is used as clock supply.

The E1 emulator does not support the flash programming through CSI. A programmer that supports the CSI (e.g. PG-FP5) has to be used for flash programming.

When the debugging is started with a blank device the option byte to select the 4-pin LPD interface has to be set in advance by using the flash programmer PG-FP5 that supports the flash programming by CSI interface.

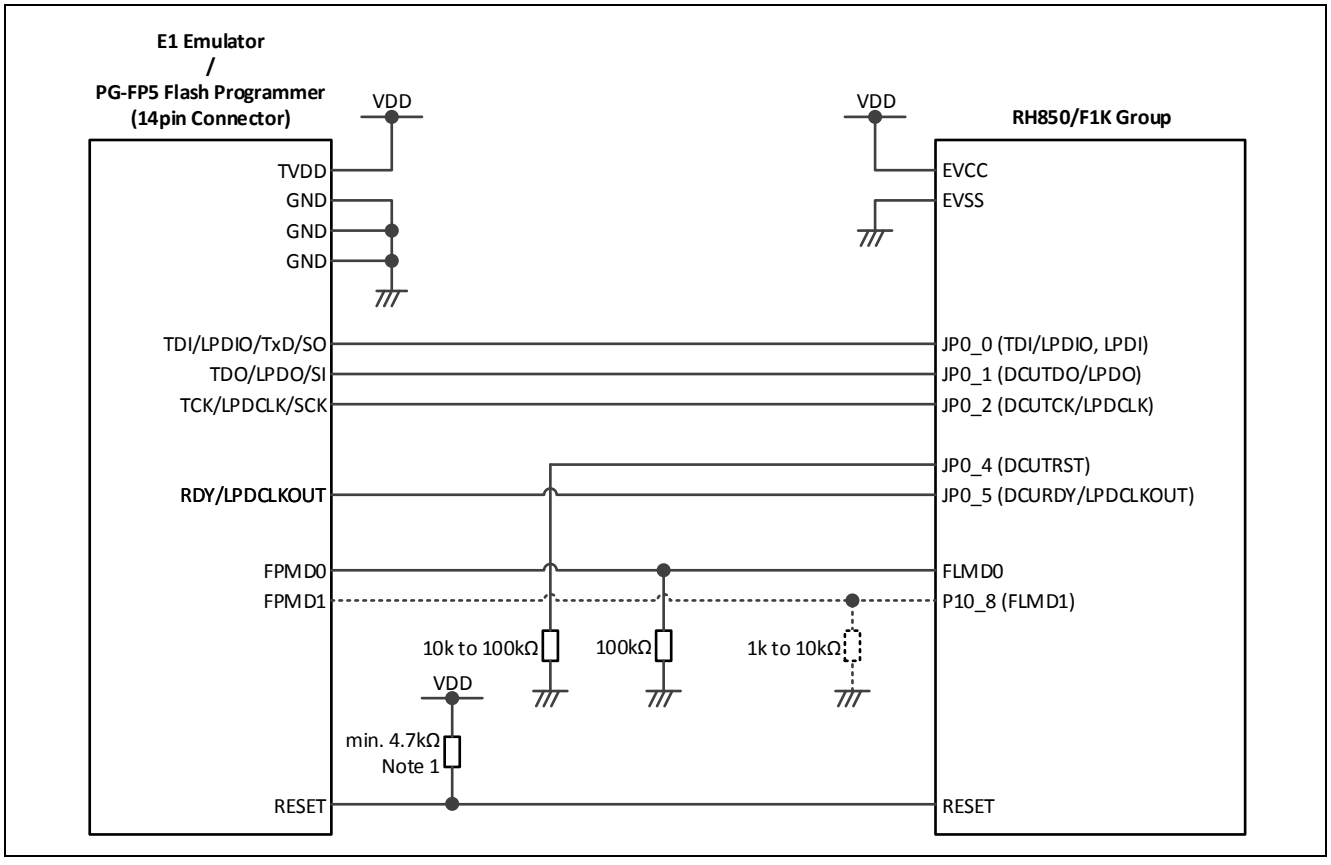


Figure 21 RH850/F1K Debug and flash programming interface connections when the HSOSC is used as clock supply

Notes: 1. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 4pin debug mode is used on the RH850/F1K group, the ports of the JP0 port group are automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDI input
- JP0_1: LPDO output
- JP0_2: LPDCLK input
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: LPDCLKOUT output
- JP0_6: General-purpose I/O

6.1.5 Debug Considerations when Hot Plug-in is used

When it is planned to use the hot plug-in function for debugging the following topics should be considered.

RESET pin

When the hot plug-in will be used it is recommended to consider the installation of a capacitor between the reset signal and GND in order to suppress a noise. In this case, the time constant of the reset circuit shall be adjusted that the time elapsing before the signal reaches 80% of the high level from the low level is within 900 µs.

Power source monitoring

When the hot plug-in function will be used it is recommended to configure the external circuit of the power source monitoring at pin 8 (TVDD) of the E1 emulator connector with a ferrite bead or inductor. This additional ferrite bead or inductor is recommended to avoid a momentary drop in the power-supply voltage on the user system that could lead to a reset of the microcontroller.

This effect can be reduced as shown in Figure 22 by placing a ferrite bead (or inductor) L1 and an additional capacitor C1 near the TVDD line of the connector for the E1 emulator.

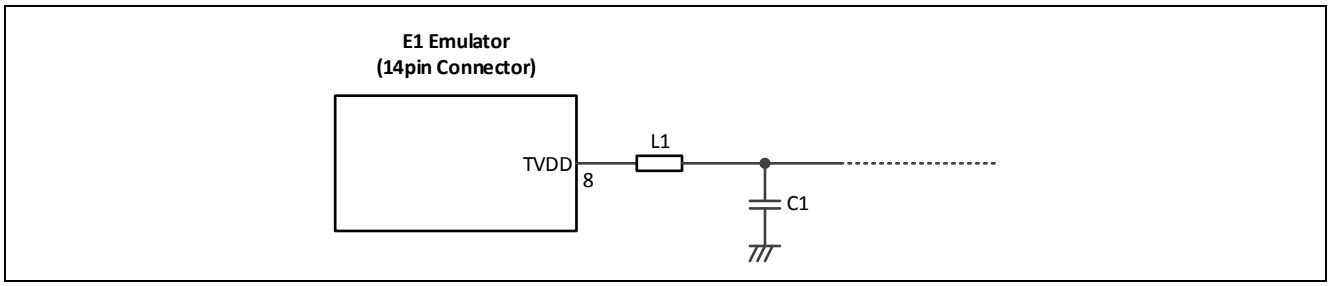


Figure 22 Circuit configuration for hot plug-in

Note: This measure might not eliminate completely the voltage drop.

General guidance for the additional external components for the power source monitoring during hot plug-in:

Component	Value
C1	10 to 47µF, ESR < 4Ω
L1	10 to 22uH

The value of the capacitor C1 and the inductor/ferrite bead L1 depends on the application requirements.

6.2 Boundary Scan Mode Interface of RH850/F1K Group

The boundary scan test is compliant with IEEE Standard 1149.1 and certain boundary scan instructions are supported.

When the boundary scan mode shall be used, several connections have to be done between boundary scan test tool and the device. Especially the boundary scan mode selection pins have to be considered from application point of view as these pins are normally used for application related functions.

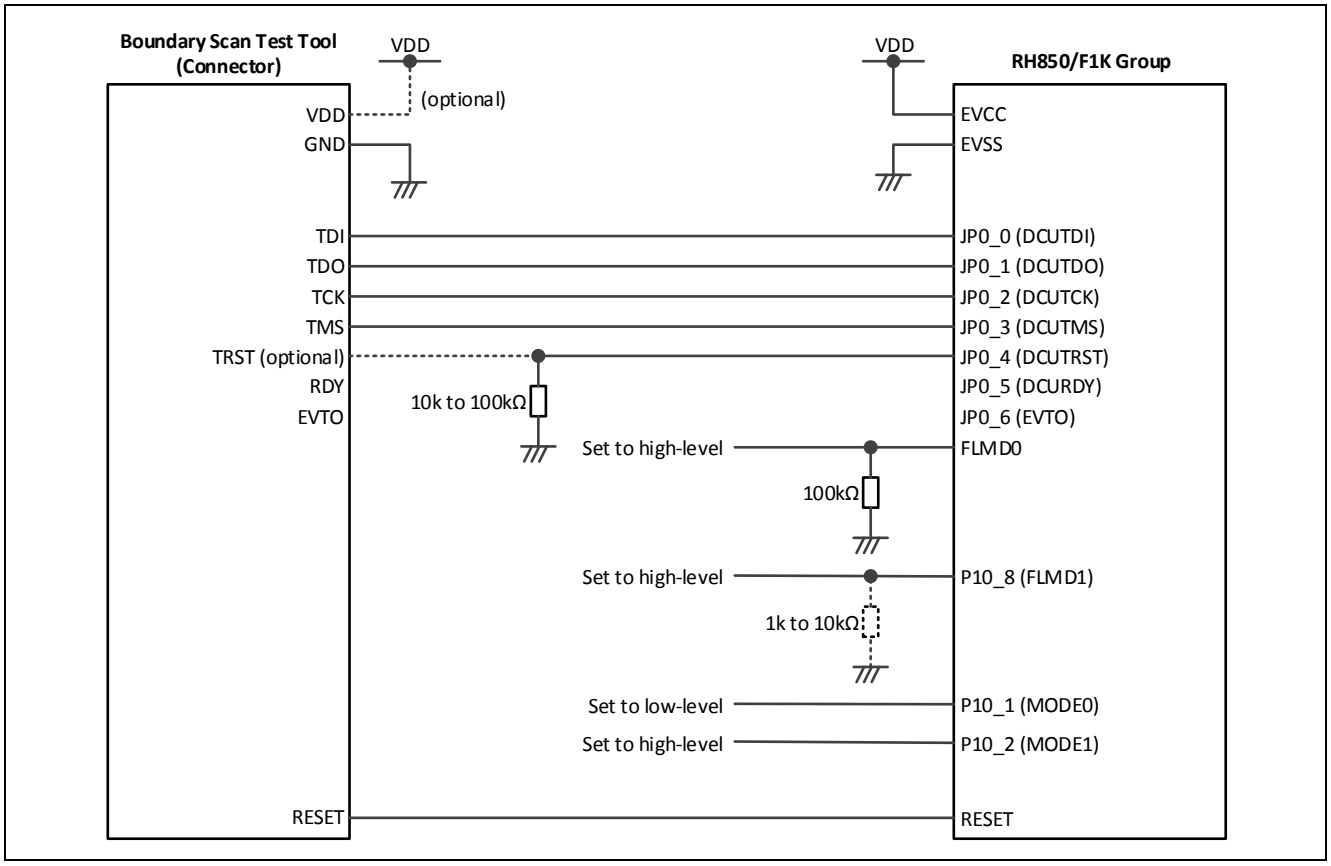


Figure 23 Boundary scan connection of RH850/F1K

Note: During boundary scan mode the level of the following pins must be fixed: P10_1: Low, P10_2: High, P10_8: High

In case of the digital I/O pins shared with an analog buffer the boundary scan function only applies to the general I/O function:

- ADCA0: AP0, P8 and P9
- ADCA1: AP1, P18

7. Reference Documents

Item	Document No.	Document Title
1	R01UH0562EJxxxx	Preliminary User's Manual Hardware RH850/F1K Group (including electrical characteristics)
2	R01TU0100EDxxxx	RH850/F1K Operating Precaution
3	R01AN0733EDxxxx	Application note "PCB-Design for Improved EMC"
4	R20UT3431EJxxxx	E1/E20 Emulator, Additional Document for User's Manual (Notes in Connection of RH850/F1K)

8. Abbreviations

ADC	A/D-converter
HSOSC	internal High-speed Oscillator
HWTRG	Hardware Trigger
MOSC	Main Oscillator
MPX	Multiplexer
SG	Scan Group
SOSC	Sub Oscillator
SWTRG	Software Trigger

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Revision History

Rev.	Date	Description	
		Section	Summary
0.10	2015-08-26	-	Initial version
0.50	2015-12-17	-	Typing error correction
		-	RH850/F1K Group name adjusted
		Target Device	RH850/F1K-100 ECO removed according to RH850/F1K Hardware user's manual
		3.1.1	MOSC value adjusted according to RH850/F1K Hardware user's manual
		4.3.1	Recommended connection of unused pins updated
		5.3	ADC equivalent input circuit values changed to tbd
		6.1	• Adjusted pull-down resistor value ofP10_8/FLMD1 from "4.7k to 10kΩ" to "1k to 10kΩ" • Description added that normal operating mode is assumed for the development tool interface
		6.1.1	Added EVTO / JP0_6 in table 21
		6.1.4	Description added regarding support of 1pin LPD and flash programming by UART
		6.1.5	Corrected component naming
		6.2	Adjusted pull-down resistor value ofP10_8/FLMD1 from "4.7k to 10kΩ" to "1k to 10kΩ"
		7	Reference document updated
1.00	2016-08-04	-	Typing error correction
		1.1.4	Figure of power up/down timing corrected
		2	Added "in normal operation mode" for easier understanding
		2.1	Adjusted minimum value of R3 to 86kΩ
		4.1.2	Added "and the minimum RESET pulse rejection" in reference to RH850/F1K hardware user's manual
		4.3	Adjusted Notes and corrected related Note for JP0, JP0_3 and JP0_4 in table
			Corrected description of X1
			Adjusted description for XT1 and IP0_0/XT2 and added Note 4
		5.3	ADC equivalent input circuit added

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 LanGao Rd., Putuo District, Shanghai, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 3.0