RH850 Series

R01AN6031EJ0100
Rev.1.0

Test Mode Procedure (CAN FD Mode)

Summary

This document describes an example procedure for testing the RS-CAN FD module using the RH850 series. For the setting of each register, refer to the notes described in the latest user's manual hardware edition.

Operation Confirmed Devices

This document applies to the RH850 series.

Please refer to Table 1-1 for the variables described in the text.

Table 1-1   Target Device and Variable

	Variable	Target Device		
		RH850/E2x	RH850/E1M-S2	RH850/P1M-E
RS-CAN FD channel number	m	0~4	0~3	0~2
Receive rule table registration register number	j	0~15	0~15	0~15
RAM test register number for CAN	r	0~63	0~63	0~63

The functions marked with ★ in the text are applicable when 2 channels or more are installed. CFD is omitted from the register names in the text.

Contents

1. Test Function

The RH850 series has the following test functions. By using these functions, it is possible to perform the self-diagnosis test for CAN communication using a CAN transceiver or MCU, and the self-diagnosis test for RAM. For details of each process, refer to the following chapters.

- Communication Test Function
  - ・Standard test mode
  - ・Listen-only mode
  - ・Self-test mode 0 (external loopback mode)
  - ・Self-test mode 1 (internal loopback mode)
  - ・Restricted operation mode (Only in CAN FD mode)

- Global Test
  - ・RAM test (read/write test)
  - ・Inter-channel communication test [CRC error test enabled]

2.   Communication Test Function

2.1   Standard Test Mode (CRC Test)

When the communication test mode is enabled (the CTME bit of the CmCTR register is "1"), the CRC value calculated based on the transmitted or received message can be read from the register where the CRC calculation data is stored. If the communication test mode is disabled (the CTME bit of the CmCTR register is "0"), the CRC calculation data can always be read as "0".

The registers that read the CRC operation data are as follows.
・Classical CAN frame: CRCREG [14: 0] bit of the CmERFL register
・CAN FD frame: CRCREG [20: 0] bit of the FDCRC register

By using the inter-channel communication test, communication between channels is possible inside the MCU, so by comparing the CRC calculation data of the transmitted channel with the CRC calculation data of the received channel, the CRC calculation circuit test of the MCU alone can be performed. For the inter-channel communication test, refer to "2.3.3 Inter-channel communication test".
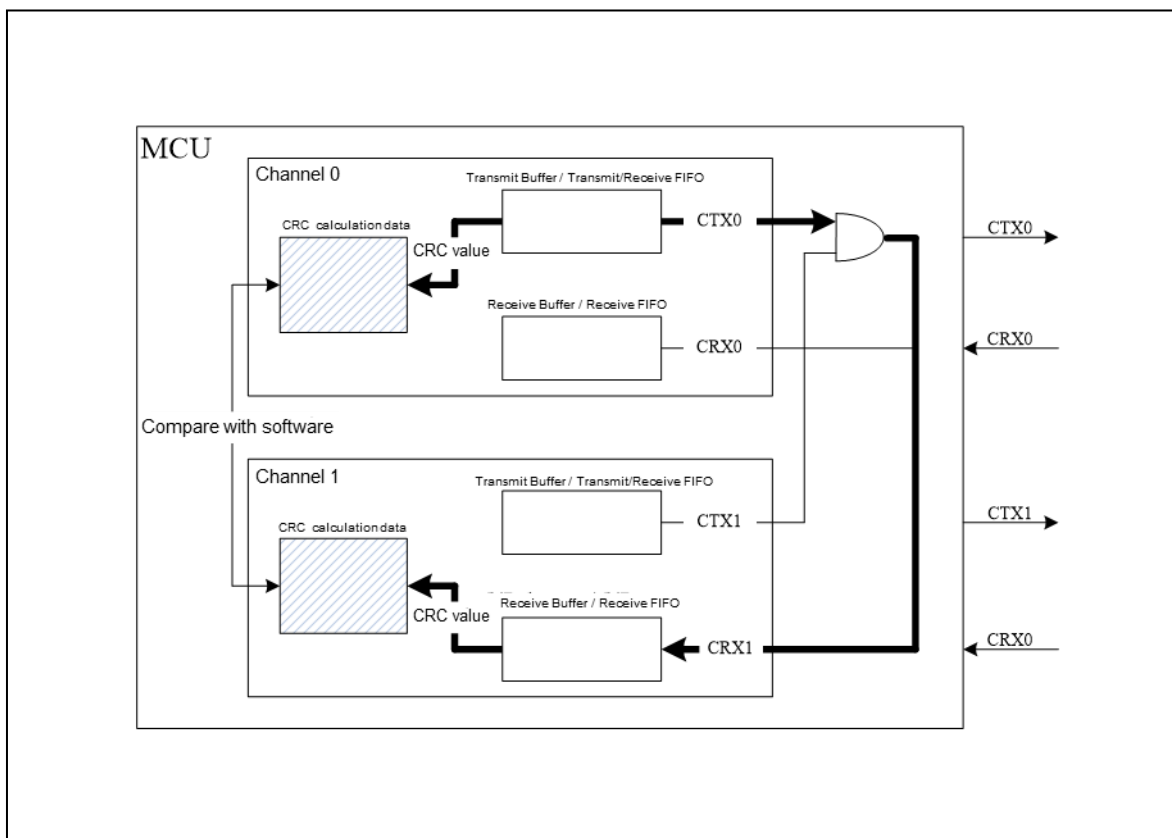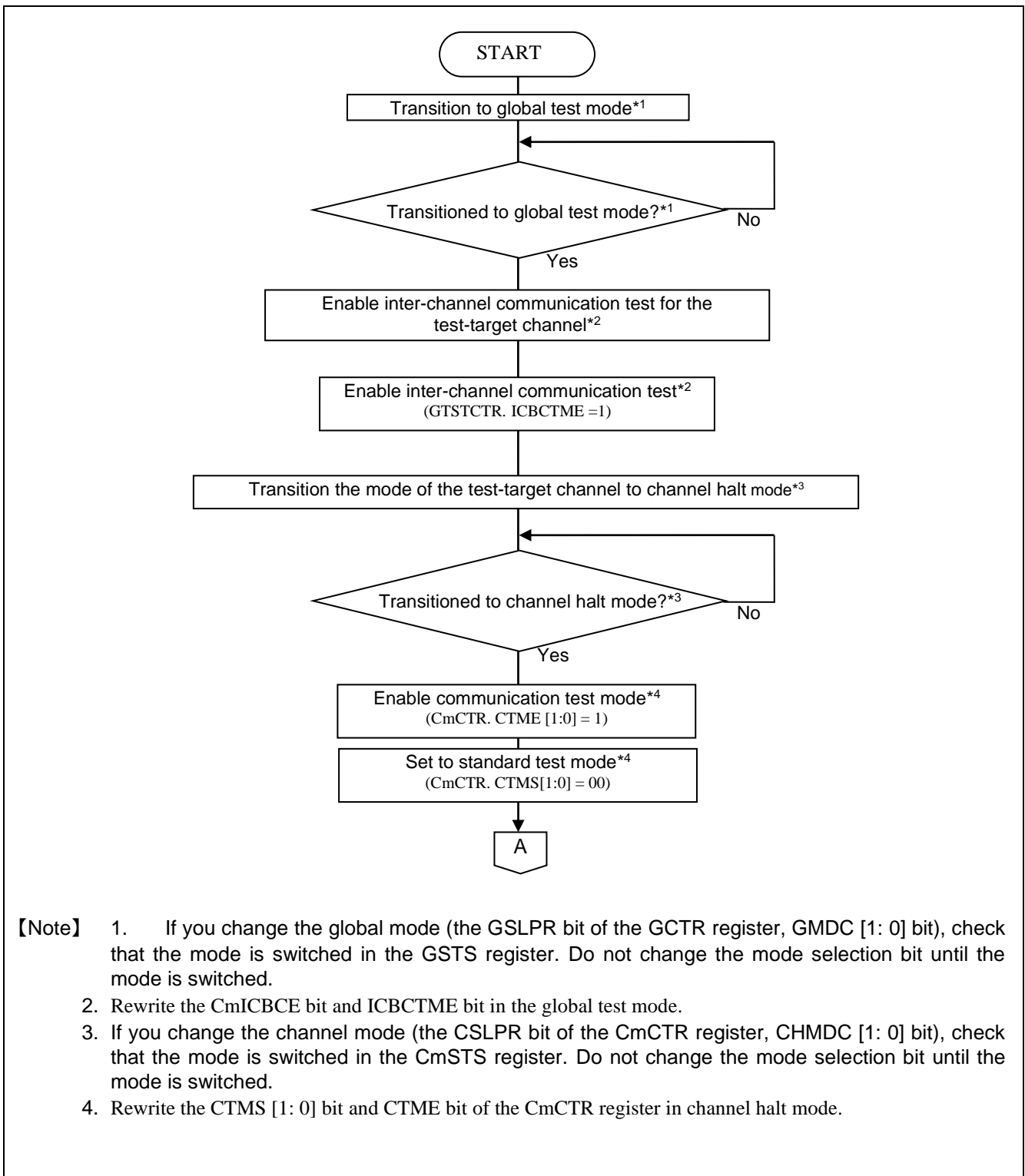
Figure 2-1 shows an image of the CRC test.



Figure 2-1   CRC Test Image (Between Channel 0 and 1)

2.1.1 Standard Test Mode Setting Procedure

Figure 2-2 to Figure 2-4 show the procedure for setting the standard test mode.

```
                              ( START )
                                  |
            +-------------------------------------------+
            |   Transition to global test mode*1        |
            +-------------------------------------------+
                                  |
                                  v
                   /-----------------------------\
                  <  Transitioned to global        >----> No
                   \  test mode?*1                 /
                    \-----------------------------/
                                  | Yes
            +-------------------------------------------+
            |  Enable inter-channel communication       |
            |  test for the test-target channel*2       |
            +-------------------------------------------+
                                  |
            +-------------------------------------------+
            |  Enable inter-channel communication       |
            |  test*2                                    |
            |  (GTSTCTR. ICBCTME =1)                     |
            +-------------------------------------------+
                                  |
            +-------------------------------------------+
            | Transition the mode of the test-target    |
            | channel to channel halt mode*3            |
            +-------------------------------------------+
                                  |
                                  v
                   /-----------------------------\
                  <  Transitioned to channel       >----> No
                   \  halt mode?*3                 /
                    \-----------------------------/
                                  | Yes
            +-------------------------------------------+
            |  Enable communication test mode*4         |
            |  (CmCTR. CTME [1:0] = 1)                  |
            +-------------------------------------------+
            +-------------------------------------------+
            |  Set to standard test mode*4              |
            |  (CmCTR. CTMS[1:0] = 00)                  |
            +-------------------------------------------+
                                  |
                                  v
                                [ A ]
```

【Note】 1. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.

2. Rewrite the CmICBCE bit and ICBCTME bit in the global test mode.

3. If you change the channel mode (the CSLPR bit of the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the mode selection bit until the mode is switched.

4. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.

Figure 2-2   Standard Test Mode Setting Procedure 1
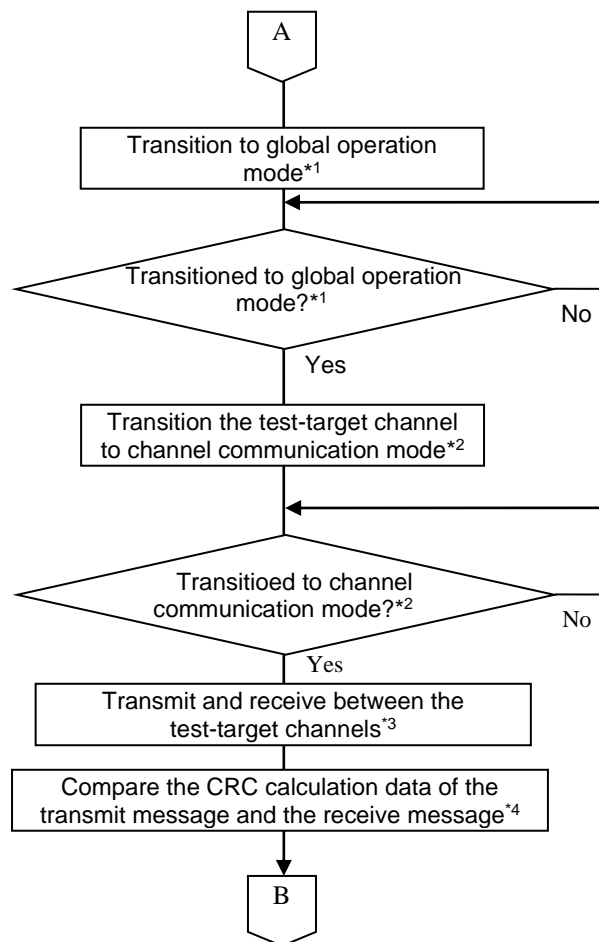
【Note】 1.   If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.
2. If you change the channel mode (the CSLPR bit of the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the mode selection bit until the mode is switched.
3. Set the transmit/receive settings for the channel to be tested.
4. When the communication test mode is enabled (CmCTR.CTME = 1), the CRC calculation data can be checked with the CRCREG[14:0] bit of the CmERFL register for a classical CAN frame, or with the CRCREG[20:0] bit of the FDCRC register for a CAN FD frame. When the communication test mode is disabled (CmCTR.CTME = 0), the CRCREG [14: 0] bit of the CmERFL register and the CRCREG [20: 0] bit of the FDCRC register are always "0".

Figure 2-3   Standard Test Mode Setting Procedure 2
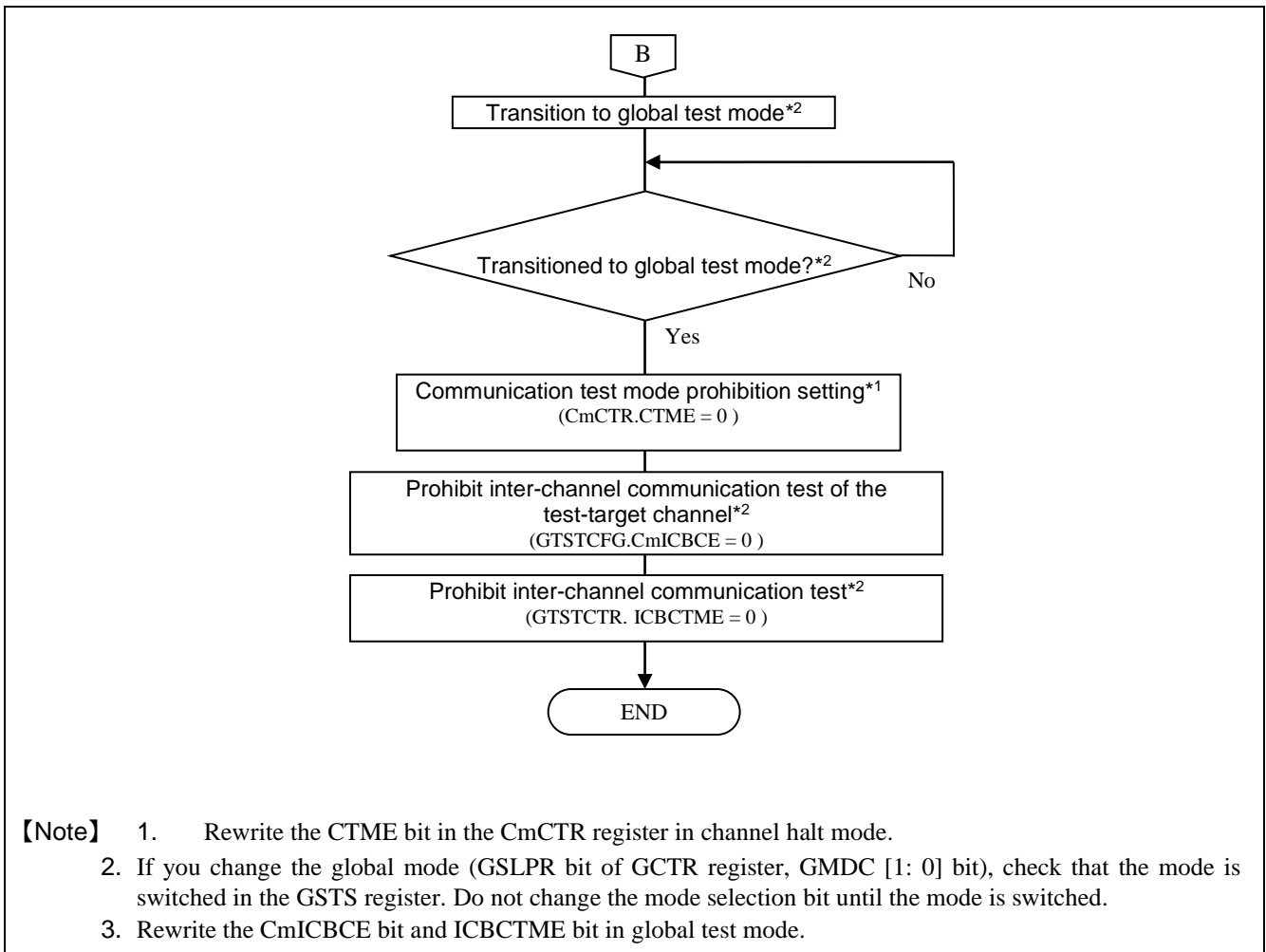
Figure 2-4   Standard Test Mode Setting Procedure 3

【Note】   1.   Rewrite the CTME bit in the CmCTR register in channel halt mode.

           2. If you change the global mode (GSLPR bit of GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.

           3. Rewrite the CmICBCE bit and ICBCTME bit in global test mode.

2.2 Listen-only Mode

In listen-only mode, only the receptive bit is transmitted on the CAN bus, not the ACK bit, the overload flag, or the active error flag. Both data frames and remote frames can be received. Therefore, listen-only mode can be used for bus monitoring and communication speed detection.

Do not transmit in listen-only mode (do not request transmission to the transmit/receive FIFO buffer, the transmit buffer, or the transmit queue).

Figure 2-5 shows the connection when listen-only mode is selected.
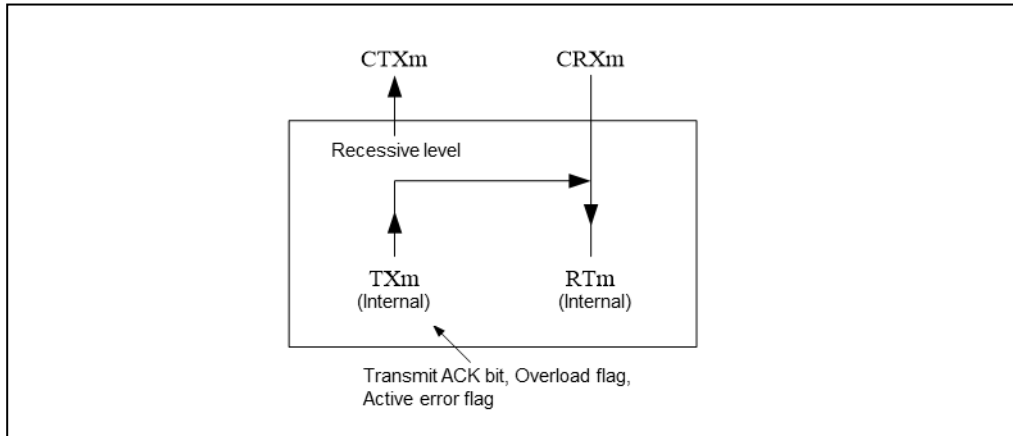
Figure 2-5   Connection When Listen-only Mode Is Selected

2.2.1   Listening-only Mode Setting Procedure

Figure 2-6 shows the procedure for setting the listen-only mode.

【Note】   1.   If you change the channel mode (the CSLPR bit in the CmCTR register, CHMDC [1: 0] bit),
                     check that the mode is switched in the CmSTS register. Do not change the mode selection bit until
                     the mode is switched.
          2. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.
          3. If necessary, set the reception settings for the channel used in listen-only mode.
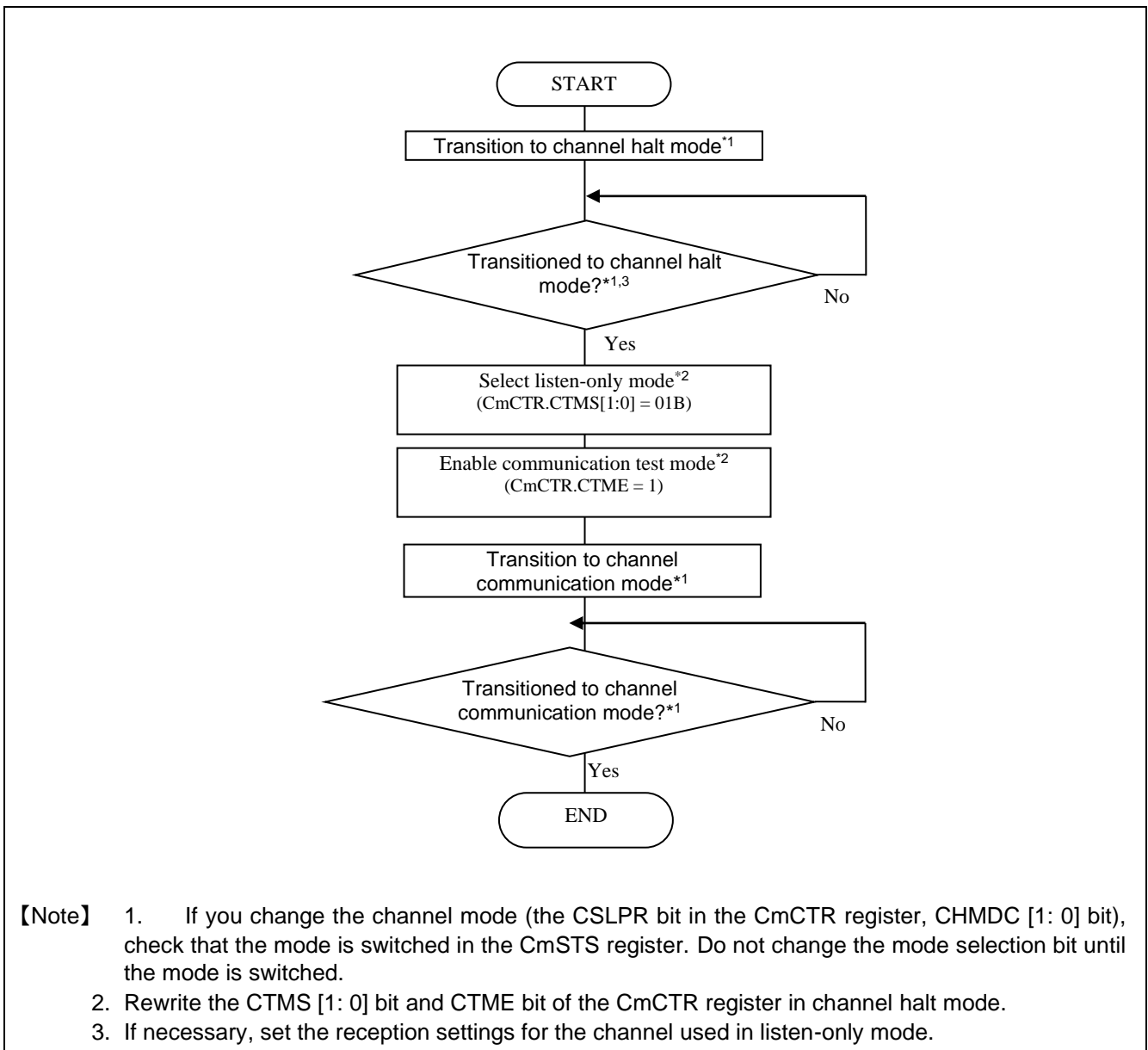
Figure 2-6   Listening-only Mode Setting Procedure

2.3   Self-test Mode (Loopback Mode)

In self-test mode, the message sent by the own node is compared with the receive rule, and the filtered message is stored in the buffer.

Messages sent by other CAN nodes will be compared only with the receive rule set to receive messages sent by other CAN nodes (GAFLIDj.GAFLLB = 0). When the mirror function and self-test mode are enabled at the same time, the self-test mode setting takes priority.

Table 2-1   Comparison of Receive Rules in Self-test Mode

Receive rule target message	Message transmit node	Comparison with receive rule
GAFLIDj.GAFLLB = 0	Other node	Yes
	Own node	Yes
GAFLIDj.GAFLLB = 1	Other node	No
	Own node	Yes

2.3.1   Self-test Mode 0 (External Loopback Mode)

Self-test mode 0 performs a loopback test of the channel, including the CAN transceiver.

In self-test mode 0, the message sent by the local node is received via the CAN transceiver. Received messages are stored in the buffer according to the receive rule. It also generates the ACK bit to receive the message sent by own node.

Figure 2-7 shows the connection when self-test mode 0 is selected.
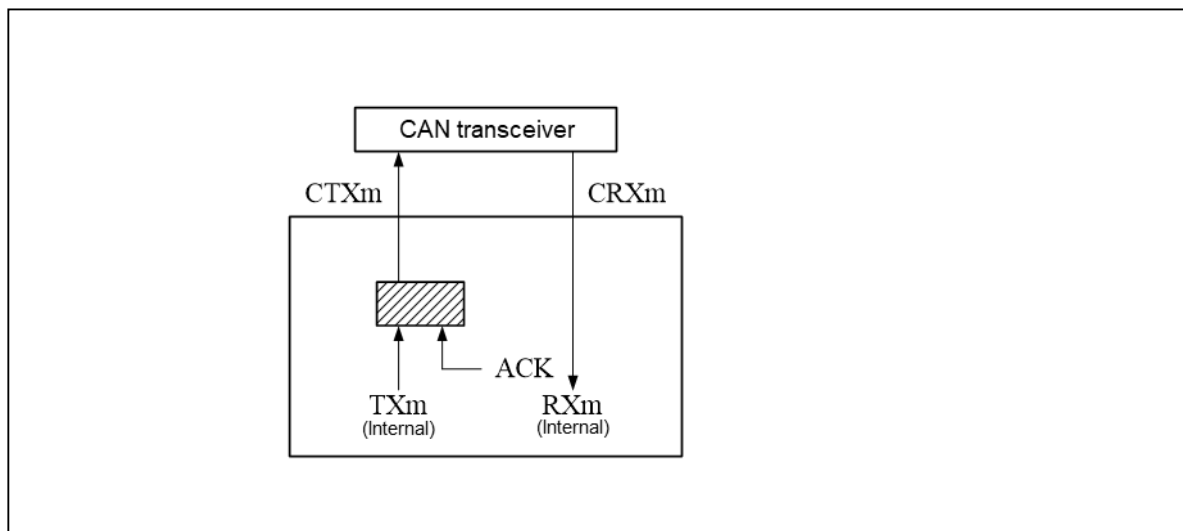
Figure 2-7   Connection When Self-test Mode 0 Is Selected

2.3.2   Self-test Mode 1 (Internal Loopback Mode)

Self-test mode 1 performs a loopback test of the channel inside the MCU.

In self-test mode 1, the message sent by the own node is received via the internal pin of the MCU. Received messages are stored in the buffer according to the receive rules. It also generates the ACK bit to receive the message sent by own node.

In this test, only the internal feedback from TXm to RXm inside the channel is performed. The external CTXm pin and external CRXm pin are disconnected from the internal pins, and the external CTXm pin outputs the recessive bit. (The CAN transceiver is not used.)

Figure 2-8 shows the connection when self-test mode 1 is selected.
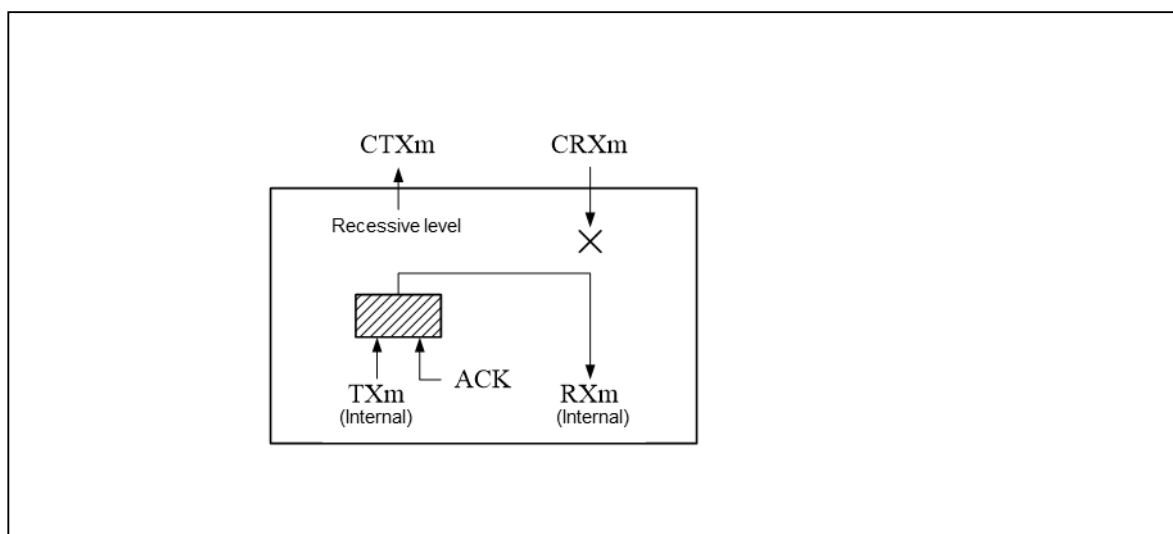
Figure 2-8   Connection When Self-test Mode 1 Is Selected

2.3.3   Self-test Mode Setting Procedure

Figure 2-9 shows the procedure for setting the self-test mode.

【Note】 1.   If you change the channel mode (the CSLPR bit in the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register.Do not change the mode selection bit until the mode is switched.

2. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.
3. Set the transmit/receive settings for the channel to be tested.
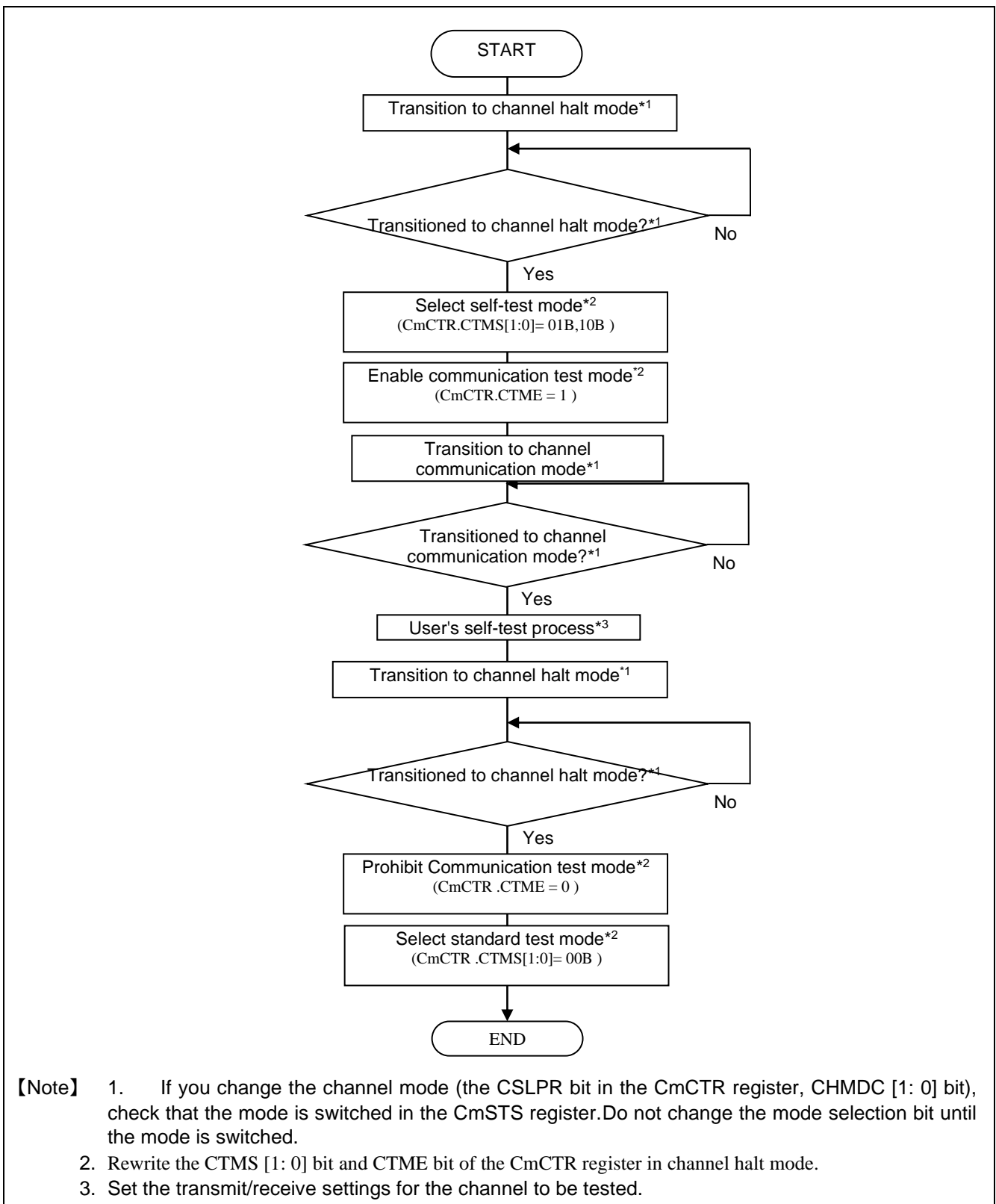
Figure 2-9   Self-test Mode Setting Procedure

2.4 Restricted Operation Mode (Only in CAN FD Mode)

In restricted operation mode, it generates an ACK bit when it receives valid data frames and remote frames, but it does not send these frames when it detects an error frame or overload frame transmit condition. When a condition is detected, it waits for the bus idle state to resynchronize to CAN communication. The receive error counter (REC) and transmit error counter (TEC) do not change when an error occurs.

Use the restricted operation mode only in the standard test mode (the CTMS [1: 0] bit of the CmCTR register is "00B").

Any transmission request is possible, and there are no restrictions.

2.4.1 Restricted Operation Mode Setting Procedure

Figure 2-10 shows the procedure for setting the restricted operation mode.
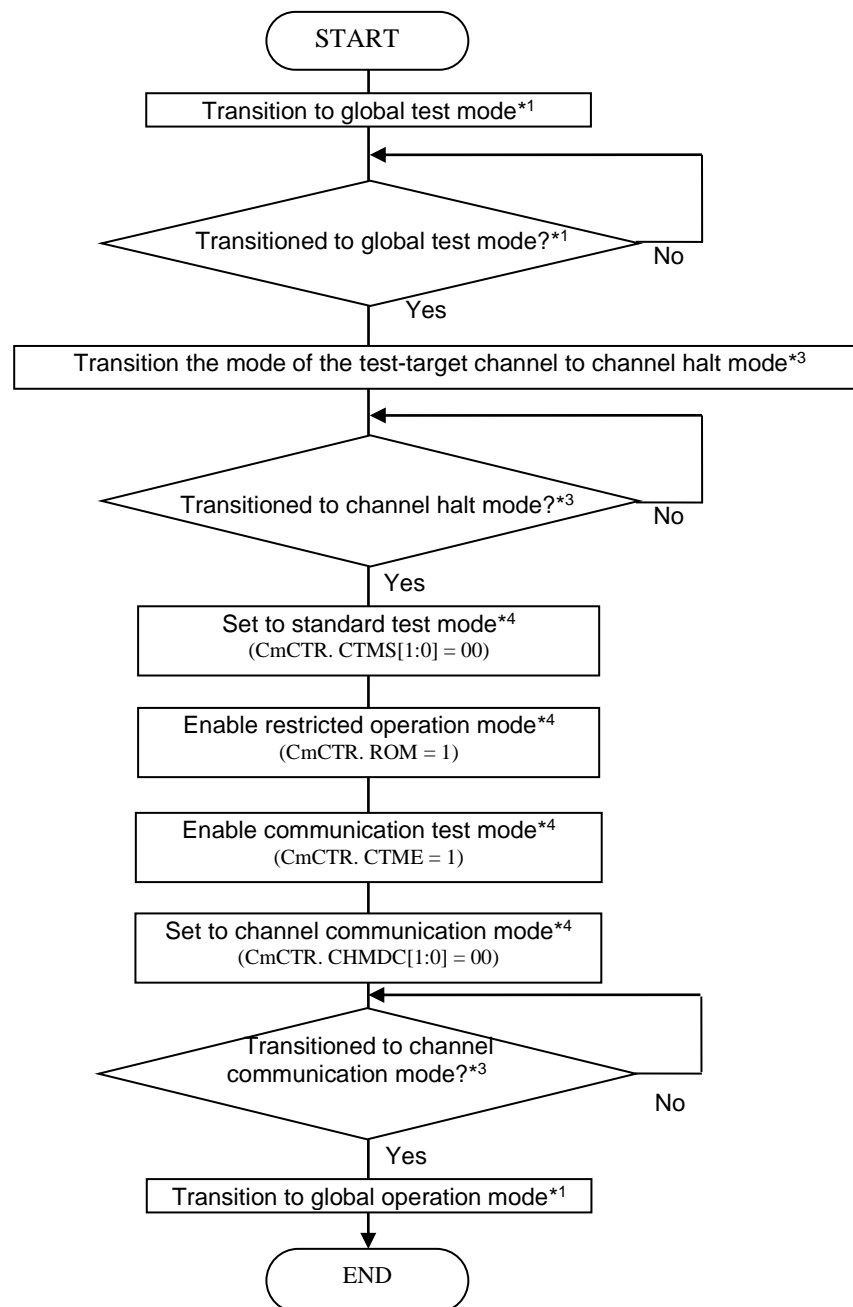
【Note】 1. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.
2. Rewrite the CmICBCE bit and ICBCTME bit in global test mode.
3. If you change the channel mode (the CSLPR bit of the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the mode selection bit until the mode is switched.
4. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.

Figure 2-10   Restricted Operation Mode Setting Procedure

2.5　Inter-channel Communication Test

The inter-channel communication test function allows CAN channels to be internally connected for the communication test.

In this test, only the internal feedback from the CTXm pin inside the channel to the CRXm pin is performed.

The external CRXm pin and external CTXm pin are disconnected from the internal pins, and the external CTXm pin outputs the recessive bit. (The CAN transceiver is not used.)

After setting transmission/reception for each channel, transmit/receive in channel communication mode. For the setting procedure, refer to "2.1.1 Standard Test Mode Setting Procedure".

By using the inter-channel communication function and the standard test mode, it is possible to test the CRC calculation circuit. For details on the CRC test, refer to "2.1 Standard Test Mode (CRC Test) Function".

Figure 2-11 shows the inter-channel communication test connection diagram.
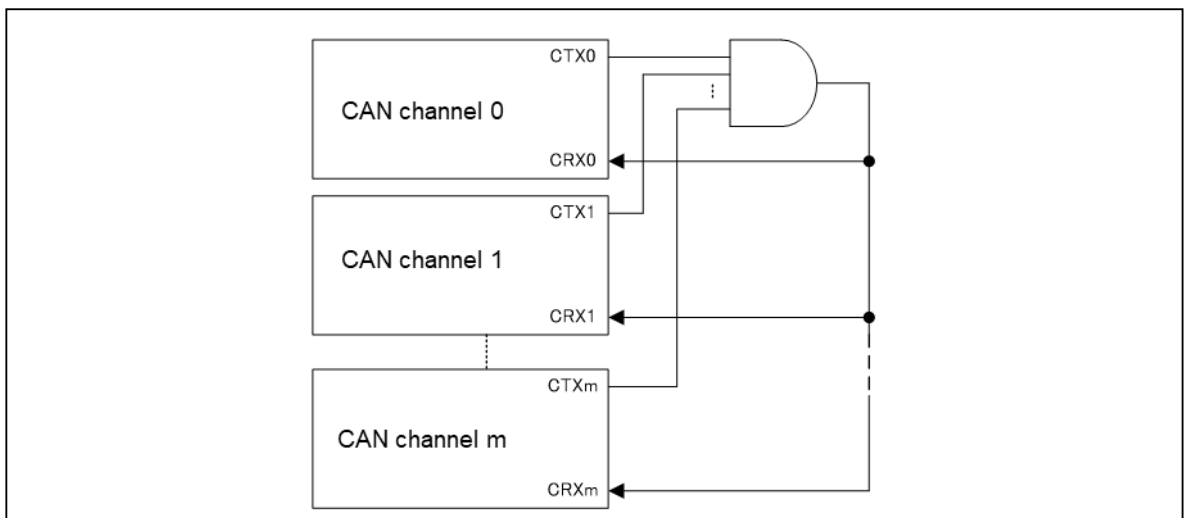
Figure 2-11　　Inter-channel Communication Test Connection Diagram

3.   RAM Test Function

3.1   RAM Read/write Test

When RAM test is enabled (GTSTCTR.RTME = 1), RAM read/write test can be performed for the entire RAM for CAN.

When the RAM test function is used, the RAM is divided into pages of 256 bytes each, and the page selection is set by the RTMPS [6:0] bit of the GTSTCFG register. The RAM in a page can be read or written by the RPGACCr register.

You can check that the RAM is normal by comparing the written value and the read value for the entire CAN RAM. After performing the RAM read / write test, write "H'00" to the CAN RAM to finish.

3.2   RAM Test Setting Procedure

Figure 3-1 shows the procedure for setting the RAM test (RAM read/write test).
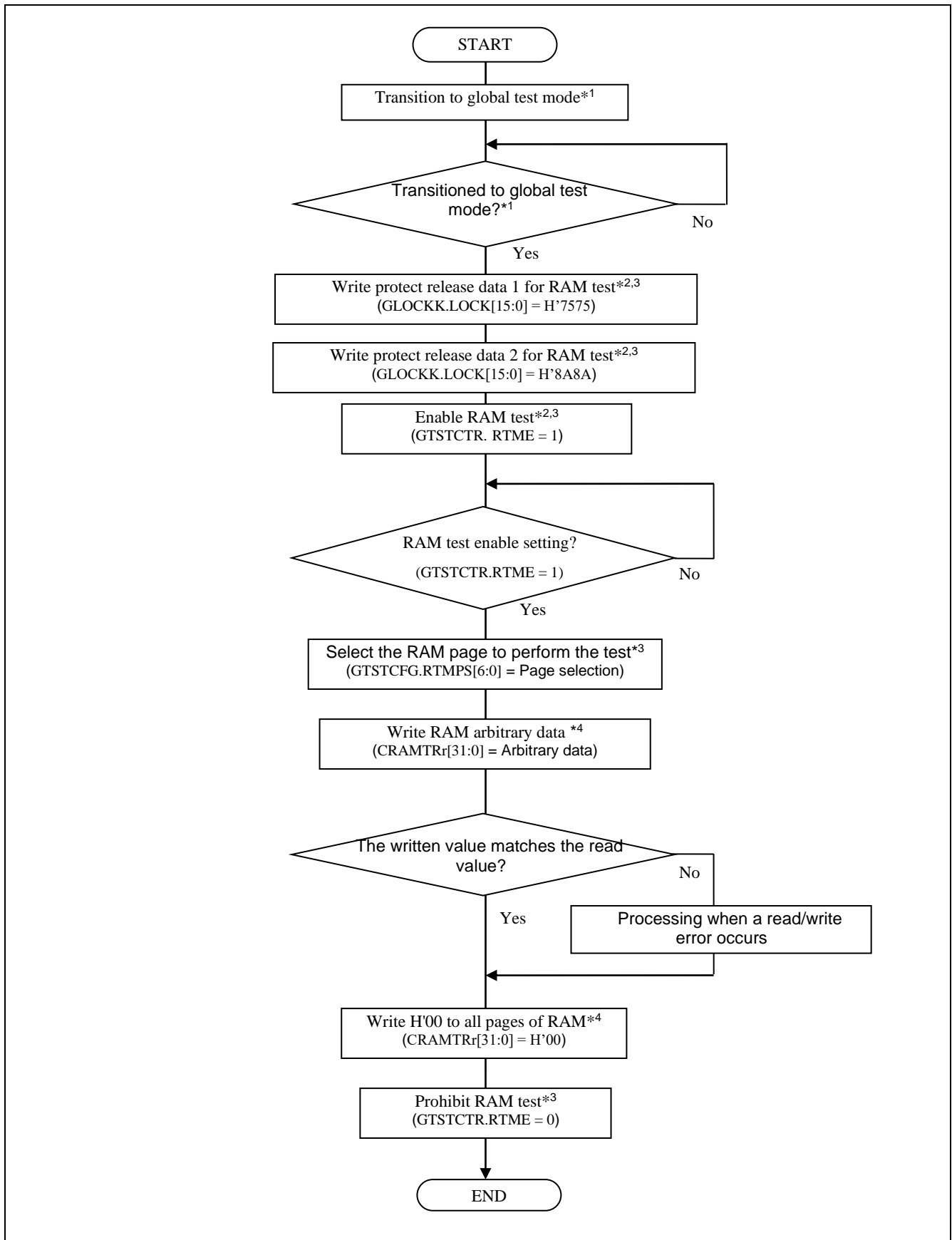
【Note】 1.   If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.

2. Be sure to execute the three instructions of writing the unprotect data 1 and 2 for the test function to the GLOCKK.LOCK [15: 0] bit and permitting the RAM test consecutively.

3. Rewrite the LOCK [15: 0] bit of the GLOCKK register, the RTME bit of the GTSTCTR register, and the RTMPS bit of the GTSTCFG register in global test mode.

4. Rewrite the CRAMTRr register in the global test mode with RAM test enabled.

Figure 3-1   RAM Test Setting Procedure

4.   Precautions for Processing Flow

4.1   About Functions

In this application note, there is a part that is functionalized even in the processing of single line, but this is only described as a function to clarify the processing for each function. When you actually create a program, you don't necessarily have to make it functional.

4.2   Settings for Each Channel, FIFO, and Buffer

In this application note, even if processing is required for each channel, FIFO, or buffer, only one processing is described. When actually creating a program, perform multiple processes as necessary.

4.3   Infinite Loop

To simplify the notation, there are some infinite loops in the processing flow. When actually creating a program, give each loop a time limit so that it can be exited during overtime. Figure 4-1 shows an example of processing when the loop time limit is set. Table 4-1 shows the transition time in global mode, and Table 4-2 shows the maximum transition time in channel mode.
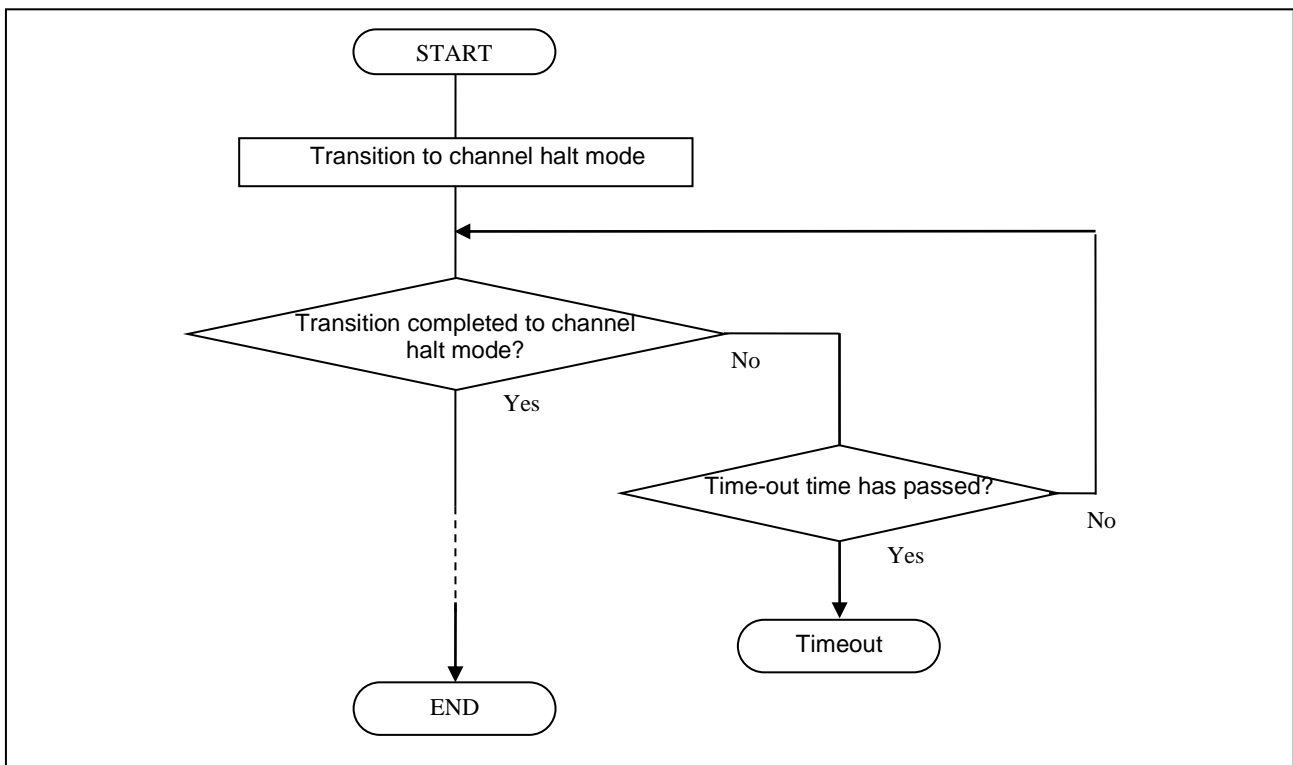
Figure 4-1   Example of Processing with Loop Time Limit

Table 4-1   Transition Time in Global Mode

Mode before transition	Mode after transition	Maximum transition time
Global stop	Global reset	3 clocks of pclk
Global reset	Global stop	3 clocks of pclk
Global reset	Global test	10 clocks of pclk
Global reset	Global operation	10 clocks of pclk
Global test	Global reset	2 CAN bit time[1], [2]
Global test	Global operation	3 clocks of pclk
Global operation	Global reset	2 CAN bit time[1], [2]
Global operation	Global test	2 CAN frames[1]

*1. It is the CAN bit time and CAN frame time of the slowest communication speed among the channels used.

*2. In CAN FD mode, the normal bit rate is CAN bit time.

Table 4-2   Transition Time in Channel Mode

Mode before transition	Mode after transition	Maximum transition time
Channel stop	Channel reset	3 clocks of pclk
Channel reset	Channel stop	3 clocks of pclk
Channel reset	Channel halt	3CANm bit time[1]
Channel reset	Channel communication	4CANm bit time[1]
Channel halt	Channel reset	2CANm bit time[1]
Channel halt	Channel communication	4CANm bit time[1]
Channel communication	Channel reset	2CANm bit time[1]
Channel communication	Channel halt	2 CANm frames

*1. In CAN FD mode, the normal bit rate is CANm bit time.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.0	2017.5.10	—	Initial edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused pins

   [Caution] Please dispose of unused pins according to "Handling of unused pins" in the text.
   The impedance of the input pins of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

   [Caution] The state of the product is undefined when the power is turned on.
   When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.
   For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.
   Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of Access to Reserved Addresses

   [Caution] Access to reserved addresses is prohibited.
   The address area has a reserved address allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

   [Caution] When resetting, release the reset after the clock has stabilized.
   When switching the clock during program execution, switch the clock after the switching destination clock is stable.
   In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

   [Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.
   Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

Notice

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No. 27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338