R32C/100 Series

Rewriting ROM Area Using EW1 Mode of CPU Rewrite Mode

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1. Abstract

This application note describes an example of rewriting the embedded flash memory using the EW1 mode in CPU rewrite mode.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):
MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the user's manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Setting Procedure

3.1 CPU Rewrite Mode

In CPU rewrite mode, the CPU executes software commands to rewrite the flash memory. The CPU accesses the flash memory via the dedicated flash memory rewrite buses instead of the CPU buses.
Figure 3.1 shows the Flash Memory Access Path in CPU Rewrite Mode.

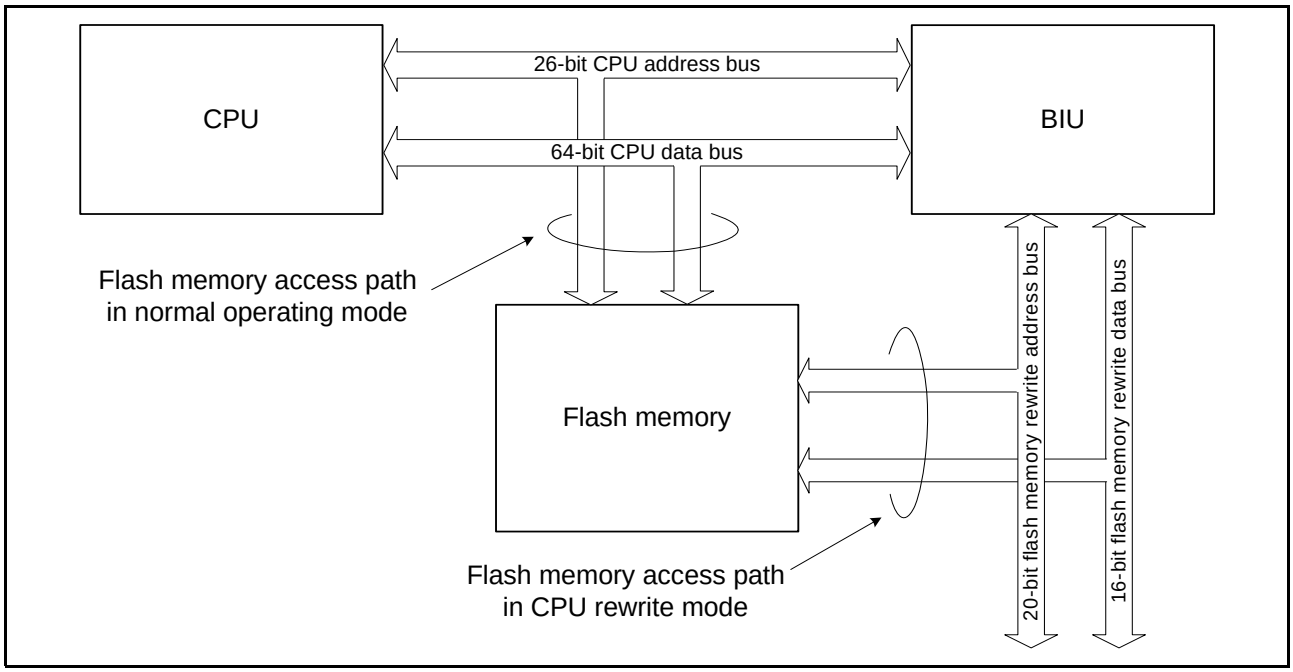

Figure 3.1 Flash Memory Access Path in CPU Rewrite Mode

3.2 EW1 Mode Features

EW1 mode allows the user to rewrite the user ROM and the data areas by issuing program and erase commands from the CPU rewrite program.
In EW1 mode, peripheral interrupts are not accepted during programming and erasing.
Table 3.1 shows the EW1 Mode Features.

Table 3.1 EW1 Mode Features

Item	Content
CPU operating modes	Single-chip mode
Rewrite program executable spaces	Internal spaces other than specified blocks to be rewritten, internal RAM
Restrictions on software commands	• Do not execute either the program or the block erase command for blocks where the rewrite control programs are written to • Do not execute the read status register command • Execute the enter read lock bit status mode command in RAM • Execute the enter read protect bit status mode command in RAM
Mode state after program/erase operation	Read array mode
CPU state during program/erase operation	In a hold state (I/O ports maintain the state before the command was executed)
Flash memory state detection	Reading the FMSR0 register by a program
Other restrictions	Disable interrupts (except NMI) and DMA transfer during program/erase operation

3.3 Flash Memory Rewrite Bus Timing

Bus setting for flash memory rewrite should be performed by the FEBC0 and/or FEBC3 registers. Refer to “Flash Memory Rewrite Bus Timing” and “Electrical Characteristics” for the appropriate bus setting.
Note that registers FEBC0 and FEBC3 in memory expansion mode share respective addresses with registers EBC0 and EBC3, That is, registers EBC0 and EBC3 should be set again after rewriting the FEBC0 and FEBC3 registers.

(1) Clock Conditions
MCU operates in single-chip mode and PLL mode before entering EW1 mode.
Table 3.2 lists the Clock Conditions after entering PLL mode. Table 3.3 lists the Clock-associated Registers Settings.

Table 3.2 Clock Conditions

Clock Name	Frequency
Main clock	16 MHz
PLL clock	100 MHz
Base clock	50 MHz
CPU clock	50 MHz
Peripheral bus clock	25 MHz
Peripheral clock source	25 MHz

Table 3.3 Clock-associated Registers Settings

Register Name	Setting Value	Comments
PLC0	04h	Refer to the user's manual for details.
PLC1	03h	Same as above
PM3	40h	Bits PM36 and PM35 are 10b (peripheral clock source: divided by 4)
CCR	1Fh	Bits BCD1 and BCD0 are 11b (base clock: divided by 2) Bits CCD1 and CCD0 are 11b (CPU clock: no division) Bits PCD1 and PCD0 are 01b (peripheral bus clock: divided by 2) BCS bit is 0 (base clock source: PLL clock selected)
PBC	0504h	Refer to the user's manual for details.
EBC0	0000h	Leave values as they are after reset due to operating in single-chip mode

(2) Flash Memory Conditions

Table 3.4 lists the flash memory standard values. These values are subject to change. Refer to "Electrical Characteristics" in the user's manual for details.

Table 3.4 Flash Memory CPU Rewrite Mode Timing

Symbol	Characteristics	Value		Unit
		Min.	Max.	
tcR	Read cycle time	200		ns
tsu(S-R)	Chip-select setup time for read	200		ns
th(R-S)	Chip-select hold time after read	0		ns
tsu(A-R)	Address setup time for read	200		ns
th(R-A)	Address hold time after read	0		ns
tw(R)	Read pulse width	100		ns
tcW	Write cycle time	200		ns
tsu(S-W)	Chip-select setup time for write	0		ns
th(W-S)	Chip-select hold time after write	30		ns
tsu(A-W)	Address setup time for write	0		ns
th(W-A)	Address hold time after write	30		ns
tw(W)	Write pulse width	50		ns

(3) Calculating the Necessary Number of Cycles

Calculate the number of cycles necessary to access the flash memory based on the clock and flash memory conditions for the setting value.

The reference clock is the base clock selected by setting bits BCD1 and BCD0 in the CCR register. The base clock is 50 MHz as listed in Table 3.2. Therefore, the value becomes 20 ns per cycle. The number of cycles in Table 3.5 are the values from Table 3.4 based on this cycle value.

Table 3.5 Required Number of Cycles

Symbol	Value		Unit	Cycles		Unit
	Min.	Max.		Min.	Max.	
tcR	200		ns	10		Cycles
tsu(S-R)	200		ns	10		Cycles
th(R-S)	0		ns	0		Cycles
tsu(A-R)	200		ns	10		Cycles
th(R-A)	0		ns	0		Cycles
tw(R)	100		ns	5		Cycles
tcW	200		ns	10		Cycles
tsu(S-W)	0		ns	0		Cycles
th(W-S)	30		ns	1.5		Cycles
tsu(A-W)	0		ns	0		Cycles
th(W-A)	30		ns	1.5		Cycles
tw(W)	50		ns	2.5		Cycles

(4) Bus Timing

The bus timing is determined based on the peripheral bus clock in Table 3.3 and Table 3.5.

The value of bits MPY1 and MPY0 that are determined by the peripheral bus clock, and the flash memory read and write cycles are required to determine the bus timing.

Table 3.6 shows the correlation between bits MPY1 and MPY0 and bits FWR4 to FWR0, and the number of read cycles when the peripheral bus clock is divided by 2.

Table 3.7 shows the correlation between bits MPY1 and MPY0, bits FSUW1 and FSUW0, and bits FWW1 and FWW0 and the number of write cycles when the peripheral bus clock is divided by 2. The shaded region indicates the setting value when both of the clock and cycle conditions are met.

Refer to the user's manual for details on the peripheral bus clock divided by 3 or divided by 4.

Table 3.6 Read Cycle and Bit Settings: MPY1 and MPY0, and FWR4 to FWR0 When Peripheral Bus Clock is Divided by 2 (unit: cycles)

FWR3 to FWR0 Bit Settings		FWR4 Bit Settings	MPY1 and MPY0 Bit Settings							
			10b				11b			
			mpy = 3				*mpy* = 4			
			tsu(S-R), tsu(A-R)	tw(R)	tcR	th(R-S), th(R-A)	tsu(S-R), tsu(A-R)	tw(R)	tcR	th(R-S), th(R-A)
0000b	*wr* = 1		4	3	4	0	6	5	6	0
		1	6	5	6	0	6	5	6	0
0001b	*wr* = 2	0	8	7	8	0	10	9	10	0
		1	8	7	8	0	10	9	10	0
0101b	*wr* = 3	0	10	9	10	0	14	13	14	0
		1	12	11	12	0	14	13	14	0
0110b	*wr* = 4	0	14	13	14	0	18	17	18	0
		1	14	13	14	0	18	17	18	0
1010b	*wr* = 5	0	16	15	16	0	22	21	22	0
		1	18	17	18	0	22	21	22	0
1011b	*wr* = 6	0	20	19	20	0	26	25	26	0
		1	20	19	20	0	26	25	26	0
1111b	*wr* = 7	0	22	21	22	0	30	29	30	0
		1	24	23	24	0	30	29	30	0

Table 3.7 Write Cycle and Bit Settings: MPY1 and MPY0, FSUW1 and FSUW0, and FWW1 and FWW0 When Peripheral Bus Clock is Divided by 2 (unit: cycles)

FSUW1 and FSUW0 Bit Settings		FWW1 and FWW0 Bit Settings		MPY1 and MPY0 Bit Settings							
				10b				11b			
				mpy = 3				*mpy* = 4			
				tsu(S-W), tsu(A-W)	tw(W)	tcW	th(W-S), th(W-A)	tsu(S-W), tsu(A-W)	tw(W)	tcW	th(W-S), th(W-A)
00b	*suw* = 0	00b	*ww* = 1	1	3	6	2	1	4	6	1
		01b	*ww* = 2	1	6	8	1	1	8	10	1
		10b	*ww* = 3	1	9	12	2	1	12	14	1
		11b	*ww* = 4	1	12	14	1	1	16	18	1
01b	*suw* = 1	00b	*ww* = 1	4	3	8	1	5	4	10	1
		01b	*ww* = 2	4	6	12	2	5	8	14	1
		10b	*ww* = 3	4	9	14	1	5	12	18	1
		11b	*ww* = 4	4	12	18	2	5	16	22	1
10b	*suw* = 2	00b	*ww* = 1	7	3	12	2	9	4	14	1
		01b	*ww* = 2	7	6	14	1	9	8	18	1
		10b	*ww* = 3	7	9	18	2	9	12	22	1
		11b	*ww* = 4	7	12	20	1	9	16	26	1
11b	*suw* = 3	00b	*ww* = 1	10	3	14	1	13	4	18	1
		01b	*ww* = 2	10	6	18	2	13	8	22	1
		10b	*ww* = 3	10	9	20	1	13	12	26	1
		11b	*ww* = 4	10	12	24	2	13	16	30	1

(5) Bus Timing Settings

Table 3.8 lists the optimal bus timing settings when the clock conditions and the flash memory conditions are met based on Table 3.6 and Table 3.7.

Table 3.8 Bus Timing Optimal Settings

Bit Symbol	Value	Function
FWR3 to FWR0	0101b	*wr* = 3
FWR4	0	No pulse width extension
FSUW1 and FSUW0	00b	*suw* = 0
FWW1 and FWW0	10b	*ww* = 3
MPY1 and MPY0	10b	*mpy* = 3 (peripheral bus clock divided by 2)

When the bus timing is set in each bit of the FEBC0 register, FEBC0 is 5885h.

Figure 3.2 shows the FEBC0 register setting.

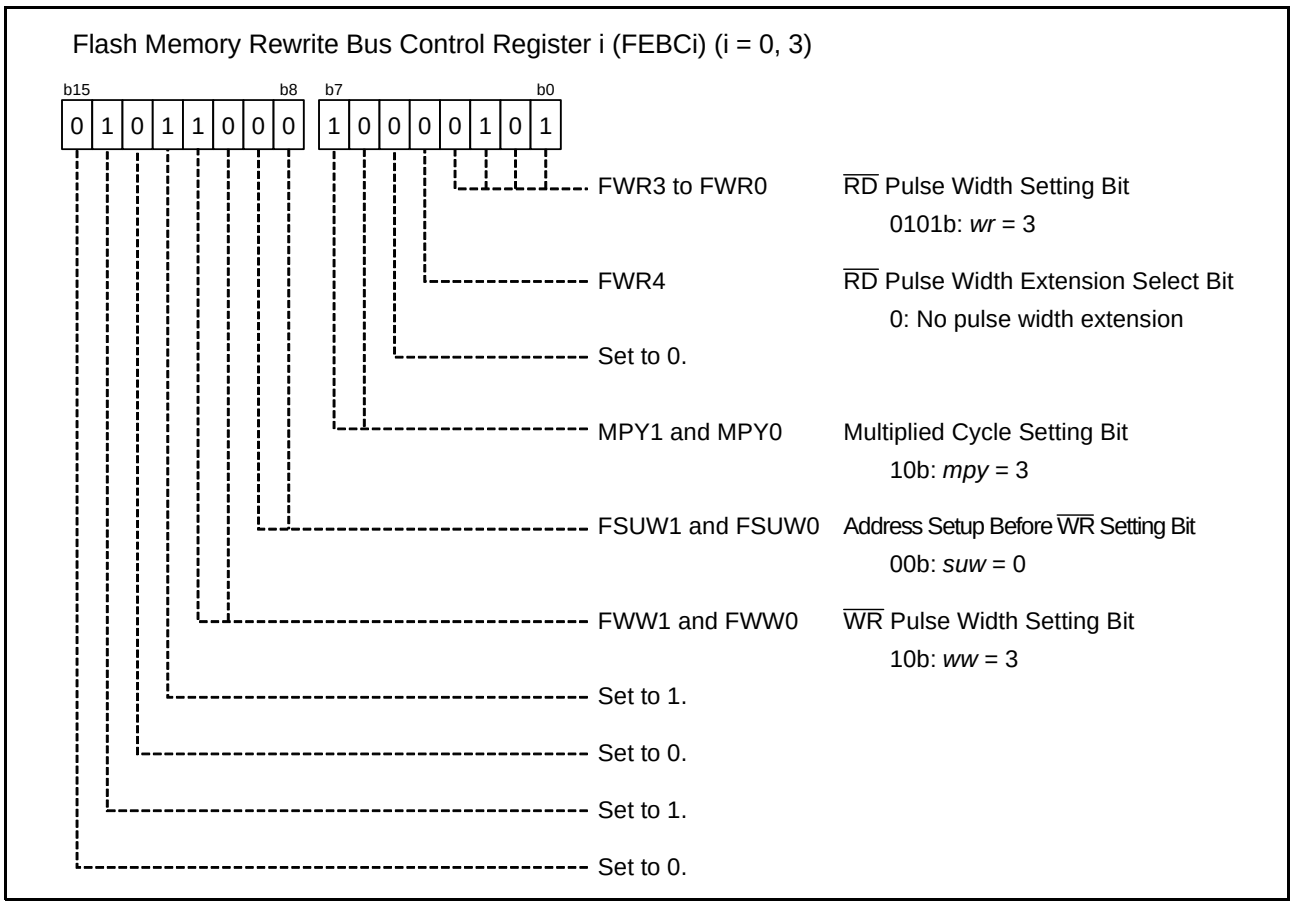

Figure 3.2 Flash Memory Rewrite Bus Control Register 0 (FEBC0)

(6) CPU Operating Mode and Flash Memory Rewrite

To rewrite the flash memory, the bus setting using by the FEBC0 and/or FEBC3 registers is required.

For exclusive use of single-chip mode, the FEBC3 register is not used. In this mode, do not change the reset value of registers CB01, CB12, and CB23. The bus setting for both the program area and data area can be performed using the FEBC0 register.

In cases other than the above, when the CPU operation is performed in memory expansion mode more than once, set registers CB01, CB12, and CB23 according to each setting range as shown in Table 3.9. The bus setting for program area and data area can be performed by the FEBC0 register and FEBC3 register, respectively.

Note that registers FEBC0 and FEBC3 in memory expansion mode share respective addresses with registers EBC0 and EBC3. That is, when the FEBCi register is set for the flash memory rewrite, the setting value for the EBCi register is accordingly changed (i = 0, 3). This may cause external devices allocated to the $\overline{CS0}$ space and/or $\overline{CS3}$ space in CPU rewrite mode to become inaccessible.

Table 3.9 lists the details of bus setting for the flash memory rewrite in each CPU operating mode.

Table 3.9 CPU Operating Mode and Flash Memory Rewrite

Item	CPU Operating Mode	
	Single-chip mode	Memory expansion mode
CB01 register	Hold the reset value 00h	Setting range: 04h to F8h Set value higher than that for the CB12 register
CB12 register	Hold the reset value 00h	Setting range: 03h to F7h Set value higher than that for the CB23 register and lower than that for the CB01 register
CB23 register	Hold the reset value 00h	Setting range: 02h to F6h Set value lower than that for the CB12 register
Bus setting for program area	FEBC0 register	FEBC0 register
Bus setting for data area	FEBC0 register	FEBC3 register
Status of $\overline{CS0}$ space and $\overline{CS3}$ space after the FEBCi register is set	N/A	• Separate bus format • 16-bit bus width • $\overline{RDY}$ ignored
Restrictions	None	• $\overline{HOLD}$ is ignored • In CPU rewrite mode, external devices become inaccessible to data with the bus format set for $\overline{CS0}$ space and/or $\overline{CS3}$ space as multiplexed bus • The change in bus timing may cause external devices in the $\overline{CS0}$ space and/or $\overline{CS3}$ space to become inaccessible

3.4 Setting Procedure

Figure 3.3 shows the CPU Rewrite Mode (EW1 Mode) Execution Flow.

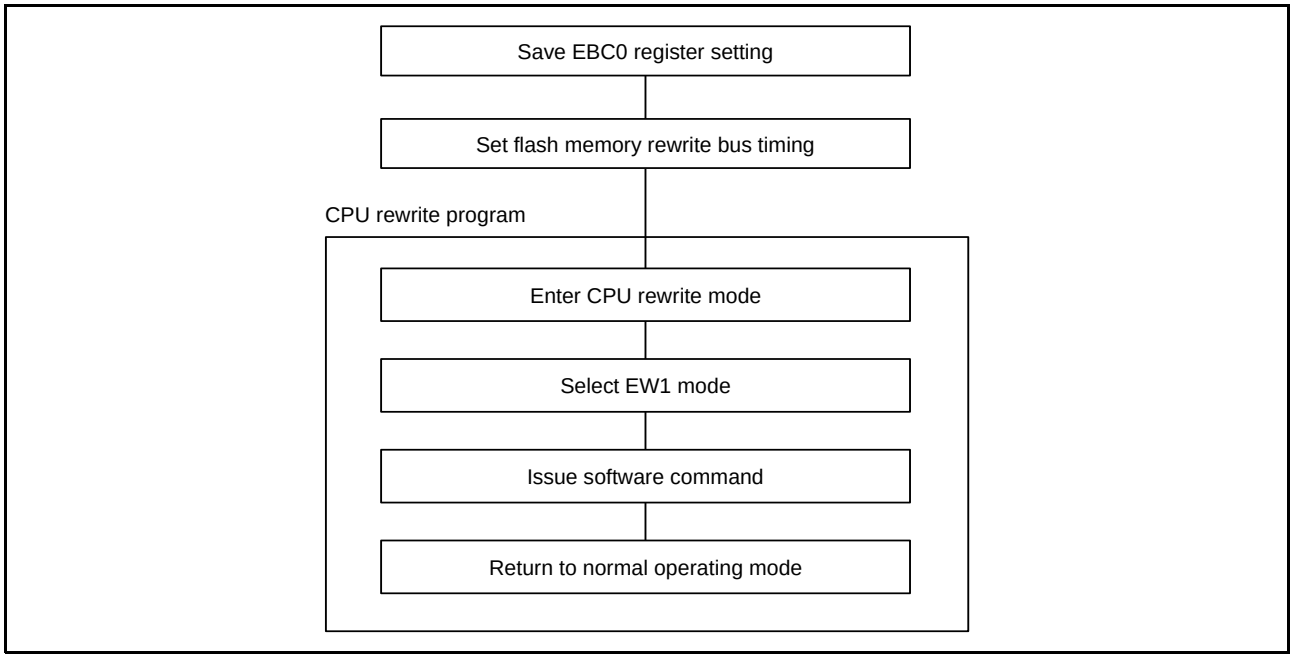

Figure 3.3 CPU Rewrite Mode (EW1 Mode) Execution Flow

3.5 Register Settings

Save EBC0 register setting
The EBC0 register and the FEBC0 register share a common address. Save the setting value in the EBC0 register to the internal RAM.

Set flash memory rewrite bus timing

b7 b0

AAh — Protect Release Register (PRR)

Control the protection for registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23.
AAh: Write enabled

b15 b8 b7 b0

0	1	0	1	1	0	0	0	1	0	0	0	0	1	0	1

Flash Memory Rewrite Bus Control Register i (FEBCi) (i = 0, 3)

Refer to 3.3 Flash Memory Rewrite Bus Timing for details.

- FWR3 to FWR0 — $\overline{RD}$ Pulse Width Setting Bits: 0101b: *wr* = 3
- FWR4 — $\overline{RD}$ Pulse Width Extension Select Bit: 0: No pulse width extension
- Set to 0.
- MPY1 and MPY0 — Multiplied Cycle Setting Bit: 10b: *mpy* = 3
- FSUW1 and FSUW0 — Address Setup Before $\overline{WR}$ Setting Bit: 00b: *suw* = 0
- FWW1 and FWW0 — $\overline{WR}$ Pulse Width Setting Bit: 10b: *ww* = 3
- Set to 1.
- Set to 0.
- Set to 1.
- Set to 0.

b7 b0

00h — Protect Disable Register (PRR)

Control the protection for registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12 and CB23.
Values other than AAh: Write disabled

The PRR register should be set to a value other than AAh (write disabled) after setting it to AAh (write enabled).

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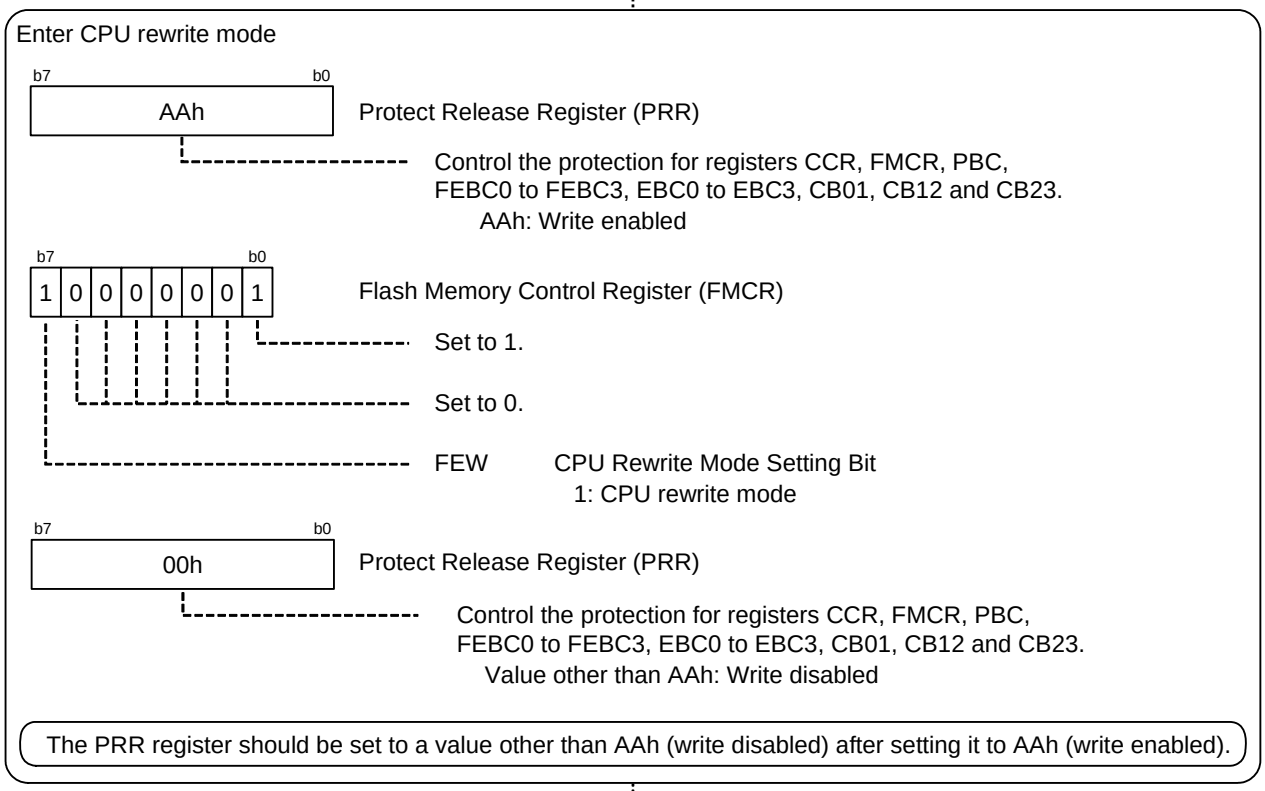

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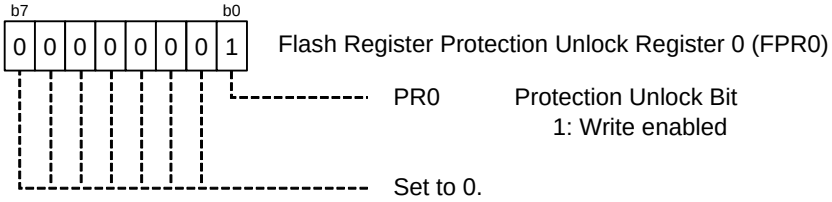
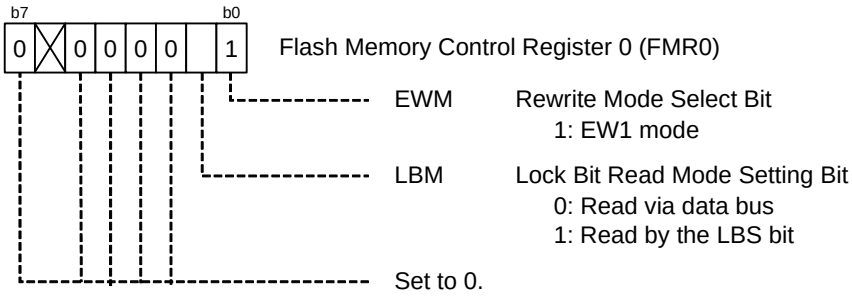
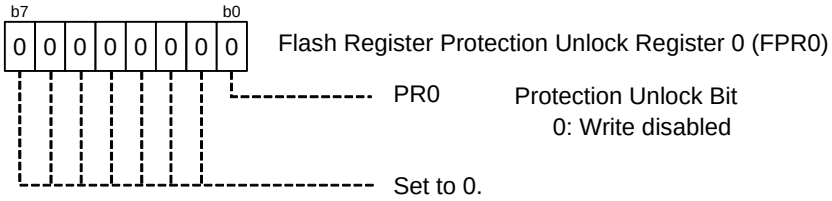
Select EW1 mode





When setting the FMR0 register, a bit rewrite access should be performed



The PR0 bit in the FPR0 register should be set to 0 (write disabled) after setting it to 1 (write enabled).

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Issue software command (first command)
Issue the embedded flash memory software command (first command).

Issue software command (second command or later)

The following register setting is required to execute multiple flash memory commands. Before issuing the last command, wait until the final command accept busy flag in flash memory control register 0 becomes 0.

Flash Memory Control Register 0 (FMR0)

EWM	Rewrite Mode Select Bit	1: EW1 mode
LBM	Lock Bit Read Mode Setting Bit	0: Read via data bus 1: Read by the LBS bit
LBS	Lock Bit Status Flag	0: Locked 1: Unlocked
RRDY	Read Ready Flag	0: Busy 1: Ready
FCA	Final Command Accept Busy Flag	0: Final command accept ready 1: Final command accept busy
Set to 0.		

Next, issue the embedded flash memory software command (last command).

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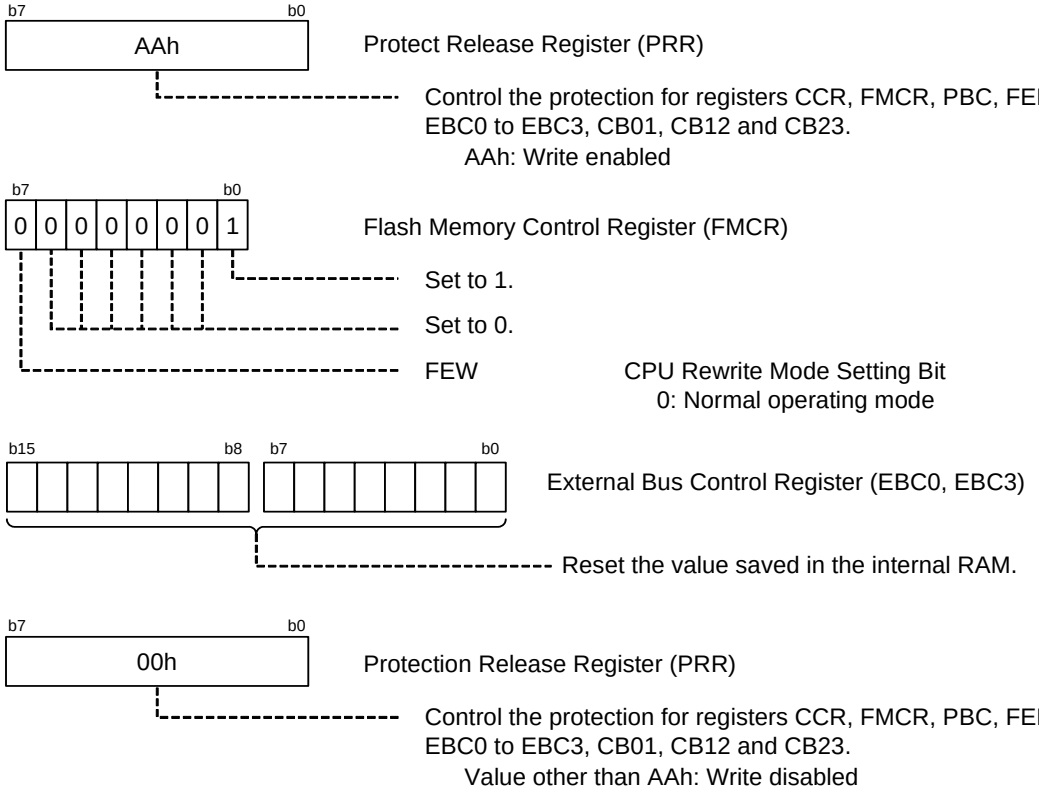
Return to normal operating mode and restore to EBC0 register setting



The PRR register should be set to any value other than AAh (write disabled) after setting it to AAh (write enabled).

3.6 Notes on Flash Memory Rewriting

(1) Note on Power Supply

- Keep the supply voltage constant within the range specified in the electrical characteristics while a rewrite operation on the flash memory is in progress. If the supply voltage goes beyond the guaranteed value, the device cannot be guaranteed.

(2) Note on Hardware Reset

- Do not perform a hardware reset while a rewrite operation on the flash memory is in progress.

(3) Note on Flash Memory Protection

- If an ID code written in an assigned address has an error, any read/write operation on the flash memory in standard serial I/O mode is disabled.

(4) Notes on Programming

- . Do not set the FEW bit in the FMCR register to 1 (CPU rewrite mode) in low speed mode or low power mode.
- The program, block erase, lock bit program, and protect bit program software commands are interrupted by an NMI, a watchdog timer interrupt, an oscillator stop detection interrupt, or a low voltage detection interrupt. If any of the software commands above are interrupted, erase the corresponding block and then execute the same command again. If the block erase command is interrupted, the lock bit and protect bit values become undefined. Therefore, disable the lock bit, and then execute the block erase command again.

(5) Notes on Interrupts

- Interrupts assigned to the relocatable vector table should not be accepted during program/erase operations.
- The watchdog timer interrupt should not be generated.
- If an NMI, a watchdog timer interrupt, an oscillator stop detection interrupt, or a low voltage detection interrupt is generated, the flash memory module automatically enters read array mode. Therefore this interrupt is enabled even during a rewrite operation. However, the rewrite operation in progress is aborted by an interrupt and registers FMR0 and FRSR0 are reset. When the interrupt handler has ended, set the EWM bit in the FMR0 register to 1 (EW1 mode) and the LBD bit in the FMR1 register to 1 (lock bit protection disabled) to re-execute the rewrite operation.

(6) Notes on Rewrite Control Program

- Do not rewrite blocks having the rewrite control program.

(7) Note on Number of Programming/Erase Operations and Software Command Execution Time

- The time to execute software commands (program, block erase, lock bit program, and protect bit program) increases as the number of program and erase operations increases. If the number of program and erase operations exceed the minimum endurance value specified in the electrical characteristics, it may take an unpredictable amount of time to execute the software commands. The wait time for executing software commands should be set much longer than the execution time specified in the electrical characteristics.

(8) Other Notes

- The required time to perform program/erase operations specified in the electrical characteristics found in the user's manual can be guaranteed within the minimum values of programming/erasure endurance specified in the same table. Even if the number of programming/erasure exceeds the minimum endurance value, the program/erase operation may be performed.
- Chips repeatedly programmed and erased for debugging should not be used for commercial products.

4. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

4.1 Description of the Sample Program

In the sample program, the MCU starts up in PLL mode, enters CPU rewrite mode (EW1 mode) triggered by an INT0 interrupt request, and stores data in block A (addresses 61000h to 61FFFh) and block 7 (addresses FFFA0000h to FFFAFFFFh). Block A and block 7 are block-erased and then programmed in the sample program. Figure 4.1 shows the Sample Program Memory Map.

The sample program execution status can be confirmed by the status of port P4. Table 4.1 shows the Port P4 Status.

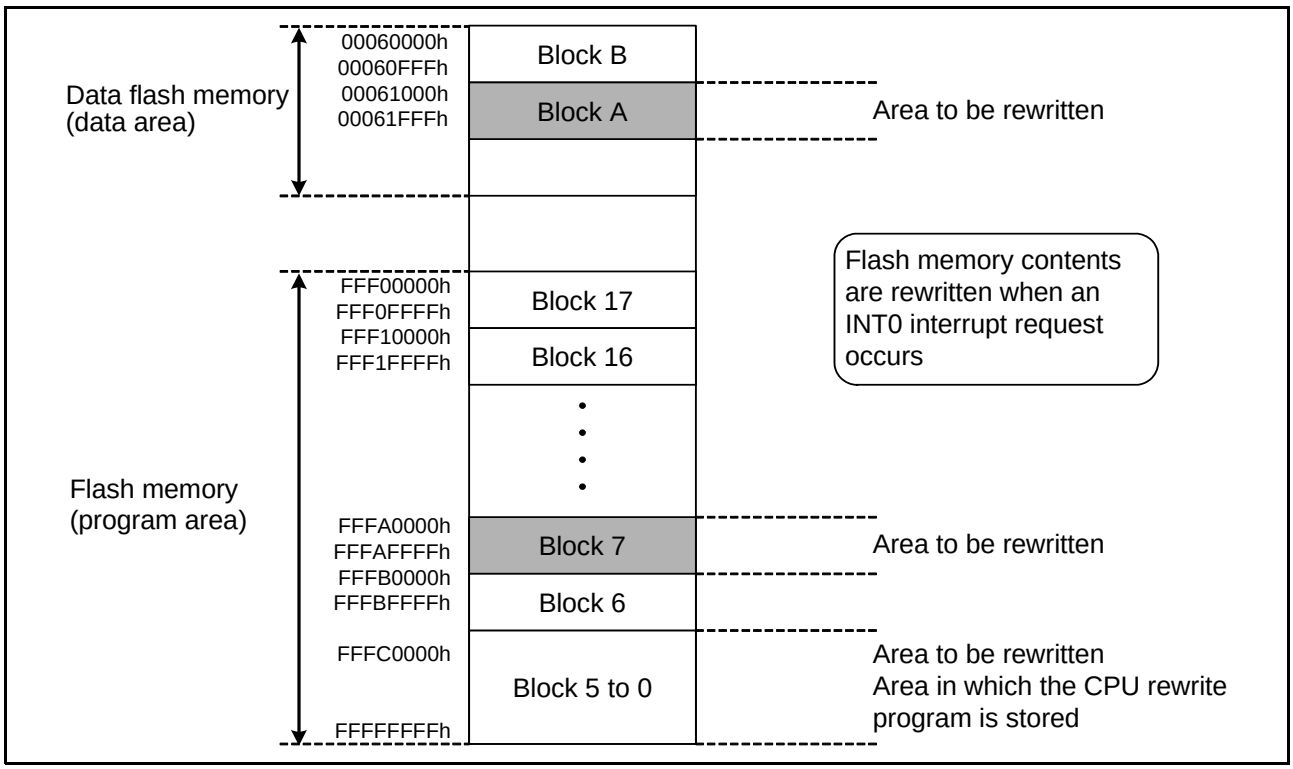


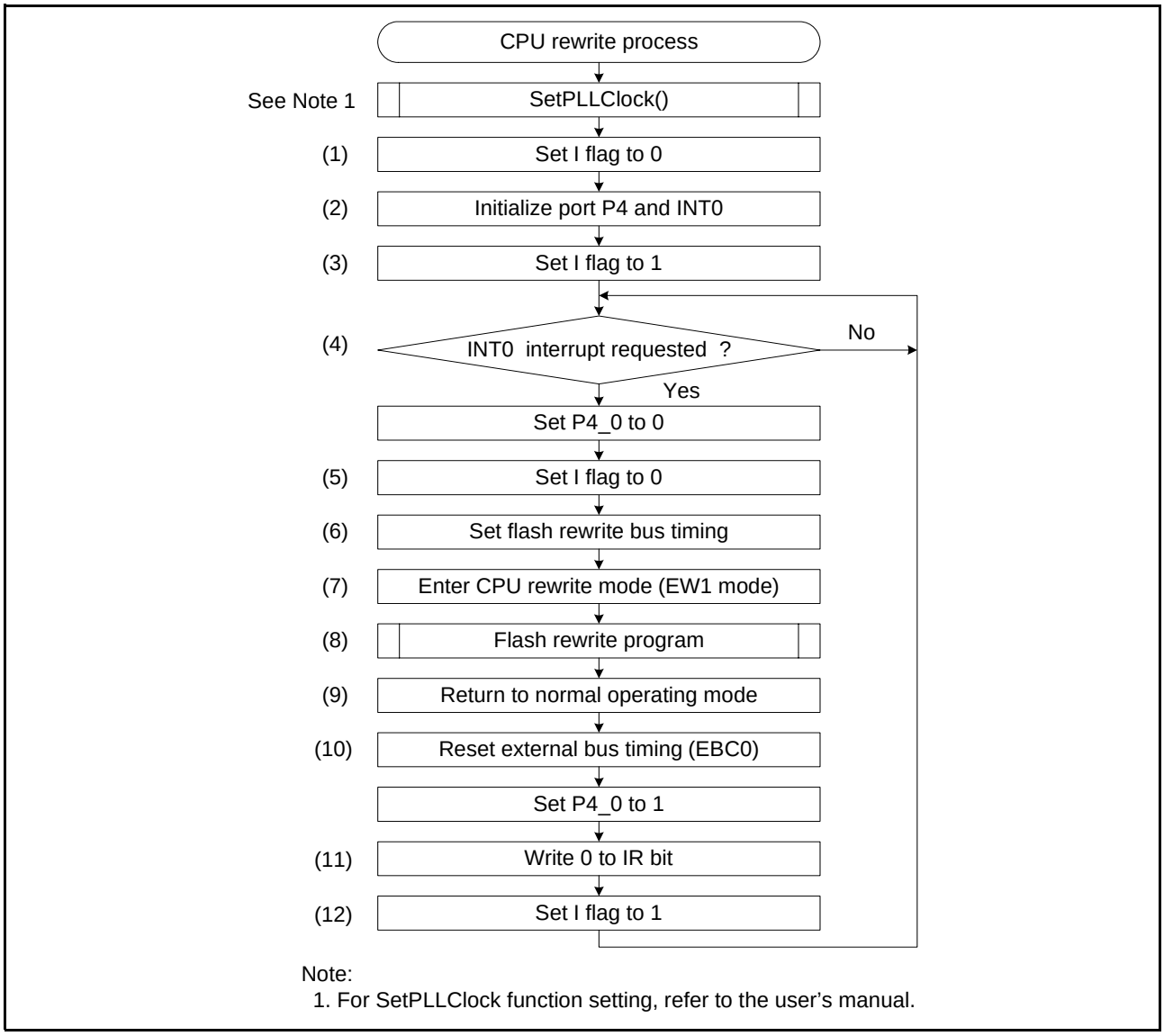
Figure 4.1 Sample Program Memory Map

Table 4.1 Port P4 Status

P4	Output Status 0	
	1	0
P4_0	Stopped	Rewriting CPU
P4_1	Program erase successfully completed	Erase error occurred
P4_2	Program successfully completed	Program error occurred

4.2 Program Flowchart

Figure 4.2 shows the entire process of the sample program.



Note:
1. For SetPLLClock function setting, refer to the user's manual.

Figure 4.2 CPU Rewrite Process

Figure 4.3 shows the process flowchart of the CPU rewrite program. Repeat program process for data to be written.

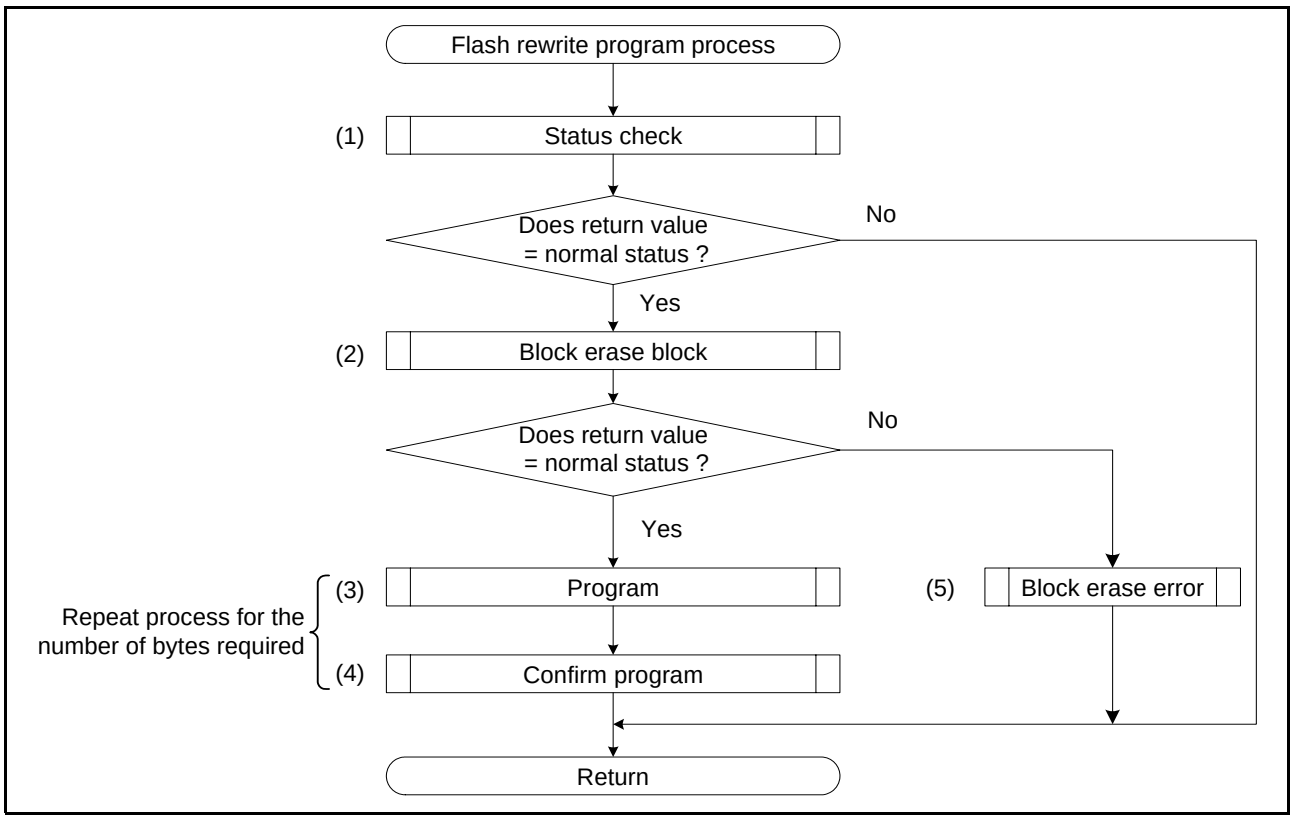


Figure 4.3 Flash Rewrite Program on RAM

(1) Block Erase

Figure 4.4 shows the flowchart of Block Erase Function. Write commands to the flash memory in 16-bit units.

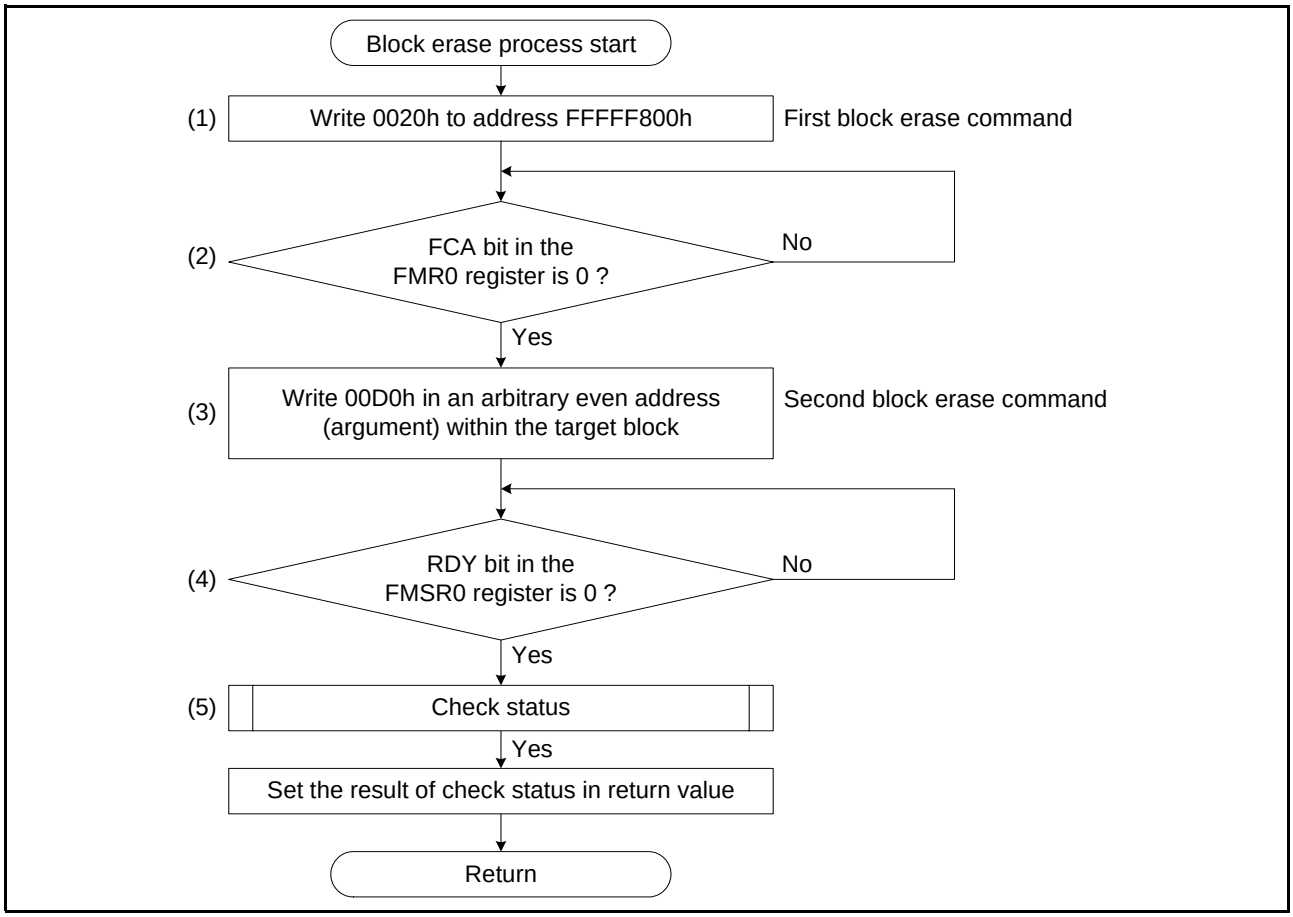


Figure 4.4 Block Erase Function

(2) Block Erase Error

Figure 4.5 shows the flowchart of Block Erase Error Function. Write commands to the flash memory in 16-bit units. When an erase error occurs in the block erase command, reexecute the block erase command after executing the clear status register command. Repeat the block erase at least three times after the erase error stops occurring.

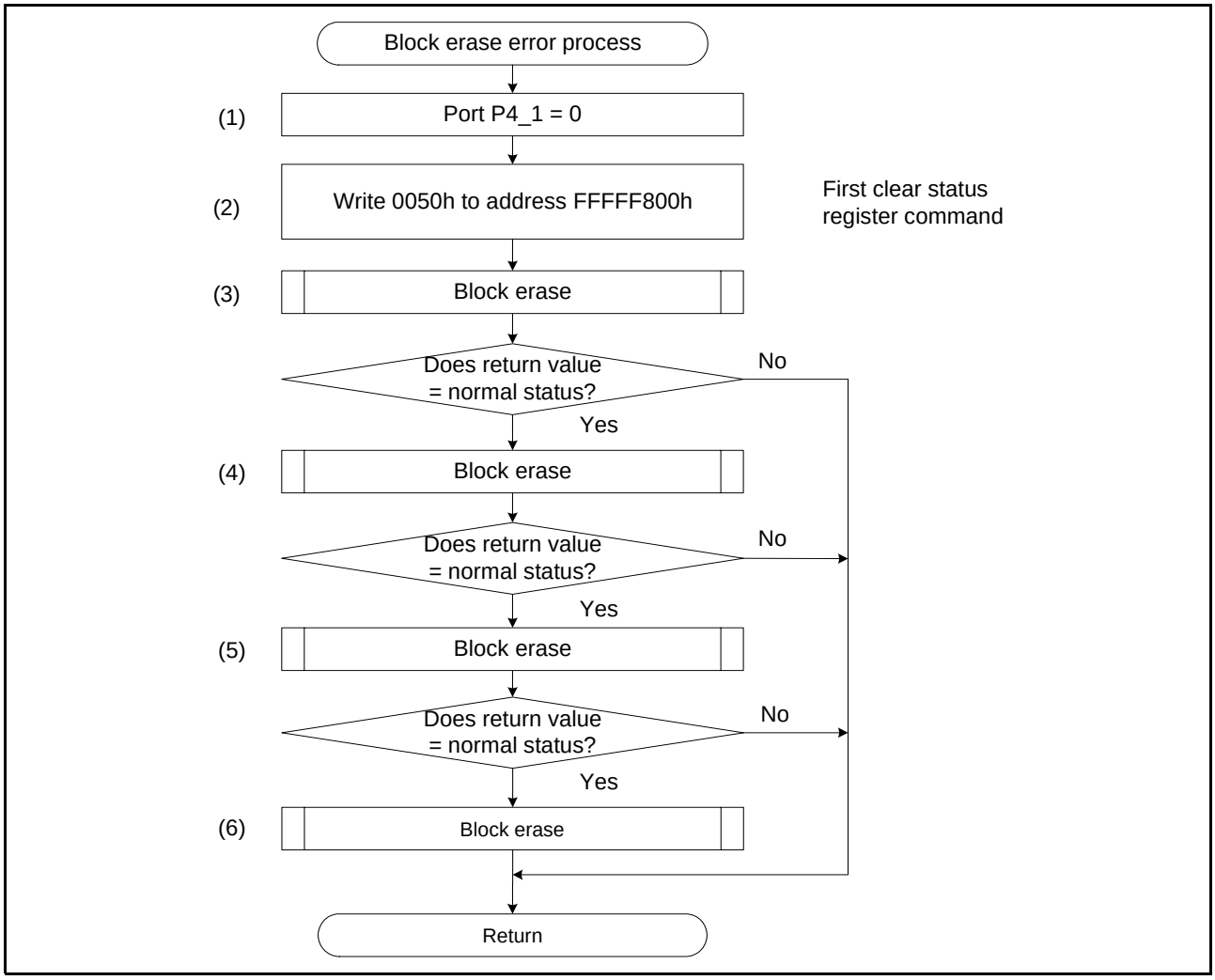


Figure 4.5 Block Erase Error Function

(3) Program

Figure 4.6 shows the flowchart of Program Function. Write commands to the flash memory in 16-bit units.

This program is executed in 64-bit units (4 words). The second through the fifth commands are a series of commands. Fix the 29 upper bits of the write address. In the 3 lower bits, set the following values in the order shown starting from the second command: 000b-010b-100b-110b (0h-2h-4h-6h or 8h-Ah-Ch-Eh).

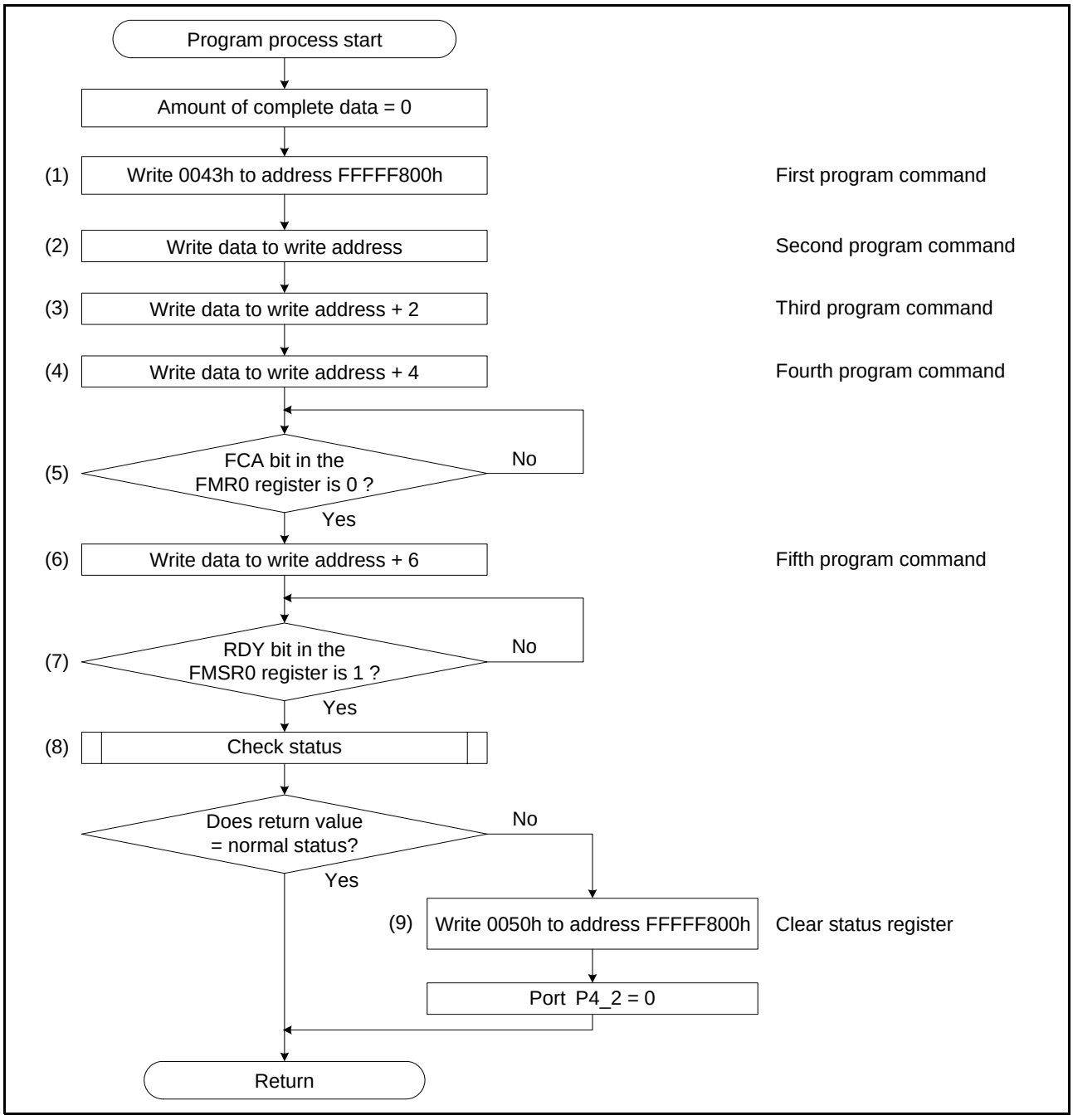


Figure 4.6 Program Function

(4) Program confirmation

Figure 4.7 shows the flowchart of Program Confirmation Function. Confirm whether the value written in the program function is the value expected.

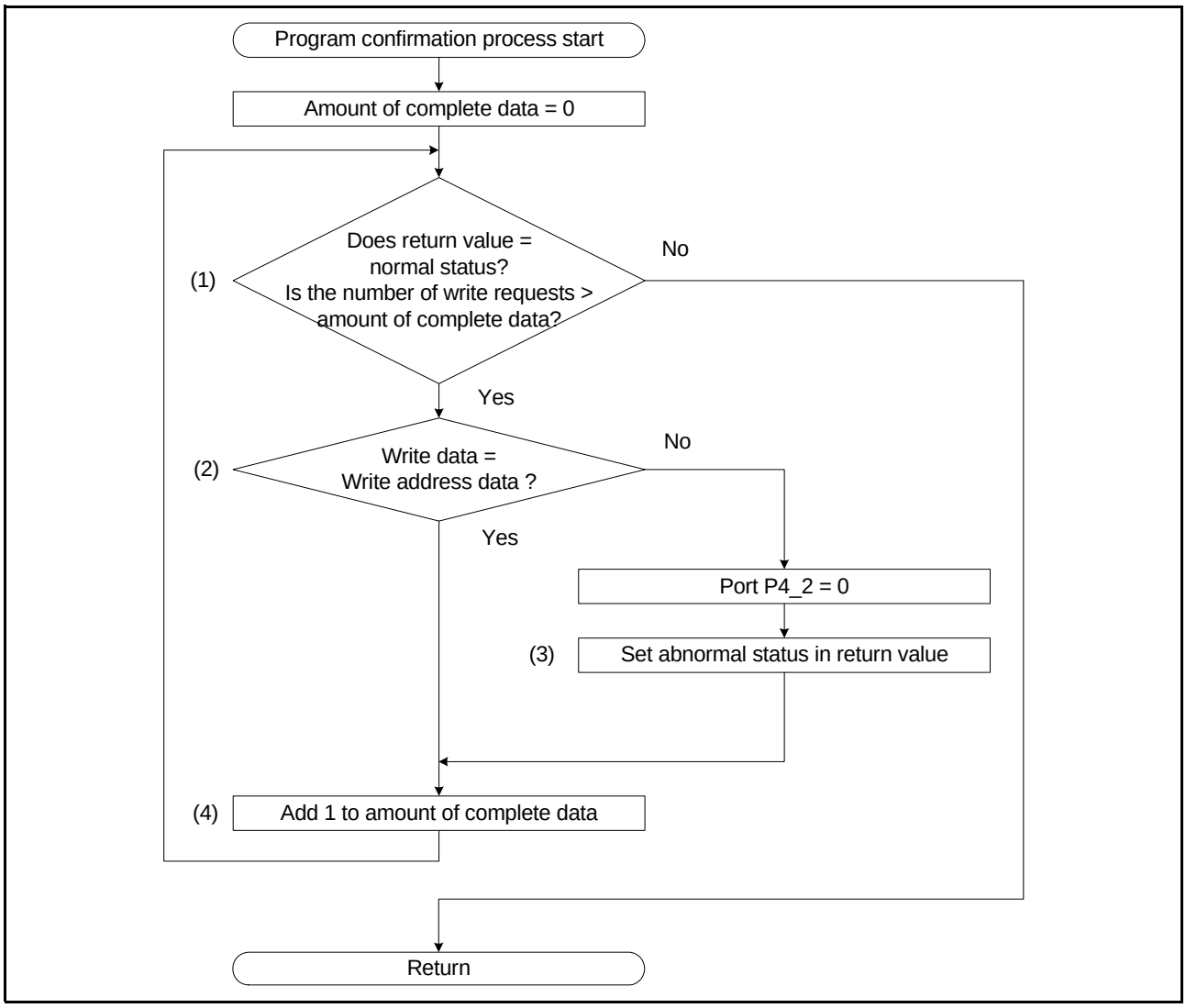


Figure 4.7 Program Confirmation Function

(5) Status Check

Figure 4.8 shows the flowchart of Status Check Function. When an error occurs, execute the clear status register command, then handle the error. If erase errors or program errors occur frequently even though the program is correct, the corresponding block may be disabled.

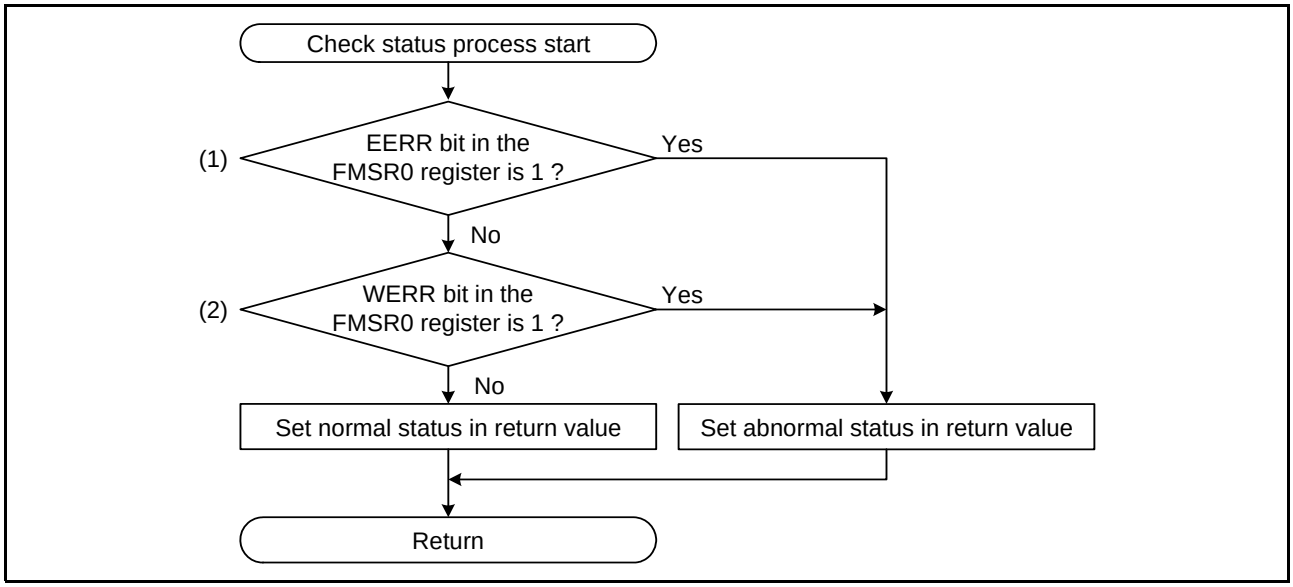


Figure 4.8 Status Check Function

5. Reference Documents

User's Manual
R32C/118 Group User's Manual Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C compiler manual
R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	R32C/100 Series Rewriting ROM Area Using EW1 Mode of CPU Rewrite Mode

Rev.	Date	Description	
		Page	Summary
1.00	May 28, 2010	-	First Edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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