Register setting configuration (PTX1xxR IOT Config Tool-based)

Panthronics AG

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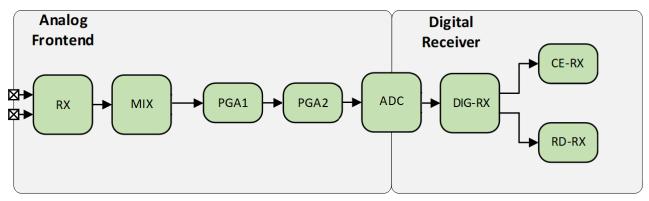
The purpose of this document is to provide a guide for the user to modify and optimize the RF performance of the PTX100R, PTX105R and PTX130R via various register settings. In addition to the antenna matching, the RF performance can also be fine-tuned by settings using the PTX1xxR IOT Config Tool (further called GUI).

Modules 8	Type A-106	Type A-212	Type A-424	Type A-848
 Configurations 	PGA1 gain	PGA1 gain	PGA1 gain	PGA1 gain
✓ Receiver				
Type A/B	18dB ~	18dB ~	18dB ~	18dB ~
Type F/V Y Transmitter	PGA2 gain	PGA2 gain	PGA2 gain	PGA2 gain
Power Settings	18dB ~	18dB ~	18dB 🗸	18dB ~
Waveshaping Type A	Rx Threshold	Rx Threshold	Rx Threshold	Rx Threshold
Waveshaping Type B	368	256	96	48 🔹
LPCD Settings	Rx Input Resistance	Rx Input Resistance	Rx Input Resistance	Rx Input Resistance
✓Card Mode				
Card Mode Application Configuration	10kOhm V	10kOhm V	10kOhm V	10kOhm V
Polling				
Debug Signals	Type B-106	Type B-212	Type B-424	Type B-848
Applications	PGA1 gain	PGA1 gain	PGA1 gain	PGA1 gain
Discovery	18dB V	18dB V	18dB V	18dB V
FeliCa DTE DDPC Measurements				
Signal Detector	PGA2 gain	PGA2 gain	PGA2 gain	PGA2 gain
Q-Measurement	21dB 🗸 🗸	18dB ~	18dB ~	18dB ~
Calibration	Rx Threshold	Rx Threshold	Rx Threshold	Rx Threshold
NDEF HCE T4T	160 🗢	256 \$	256 \$	256 \$
Test Signals and GPIOs	Rx Input Resistance	Rx Input Resistance	Rx Input Resistance	Rx Input Resistance
3	10kOhm V	10kOhm ~	10kOhm ~	10kOhm V



1 Configuration of receiver settings

In the PTX1xxR an IQ receiver architecture is used to cover all the various supported technologies, consisting of an analogue frontend and a digital baseband.



1.1 Analog frontend gain settings

Configuration of the gain in reader mode is very simple, because of applied modulation and coding schemes. This allows the input signal to be clipped and therefore the gain can be set to the highest possible value. However, this maximum value depends on the board and antenna setup and it must be taken care that the gain is not too high so that the noise on it's own is not already clipping the system.

1.1.1 Programmable Gain Amplifier 1 (PGA1)

PGA1 gain is set in a range from 0dB to 18dB with a step size of 3dB. For reader mode it can be set as high as possible (max. value is 18dB) taking into account the noise level. If the gain is too high the noise level alone can already clip the system and no data signal can be demodulated.

PGA1 gain	
18dB	~
0dB	
3dB	
6dB	
9dB	
12dB	
15dB	
18dB	
290	÷
Rx Input Resistance	
10kOhm	~



1.1.2 Programmable Gain Amplifier 2 (PGA2)

PGA2 gain is set in a range from 0dB to 30dB with a step size of 3dB. For reader mode it can be set as high as possible taking into account the noise level. If the gain is too high the noise level alone can already clip the system and no data signal can be demodulated.

PGA1 gain	
18dB	\sim
PGA2 gain	
18dB	\sim
3dB	~
6dB	
9dB	
12dB	
15dB	
18dB	
21dB	
24dB	
27dB	
30dB	× 1
	_

1.1.3 Signal detection threshold

Signal detection is the process of comparing the level of the filtered and processed input signal against a configurable threshold. This is needed in order to prevent the system from decoding pure noise as data when there is no actual signal present.

RX Threshold is in a range from 0 to 32767 with a step size of 1.

A debug function (section Applications / Signal Detector) is implemented in the GUI, which helps to fine tune the settings based on the HW configuration.

18dB	~
PGA2 gain	
18dB	~
Rx Threshold	
290	÷
Rx Input Resistance ,	
10kOhm	~

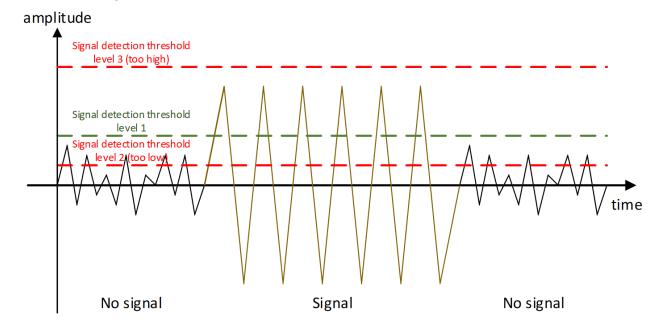


				_		
PGA1 range:	0dB	\sim	18dB ~	Full rar	nge	
GA2 range:	0dB	\sim	30dB ${\scriptstyle \lor}$	🗹 Full rar	nge	
GA1 Result:	PGA1	\sim	Warning:	This measu	rement might take up to se	everal minutes
GA2 Result:	PGA2	$^{\vee}$		Detect	:	
CD Rx Thres	hold					
Detect Type	A106			Apply	Detect Type A212	Apply
Detect Type	4424			Apply	Detect Type A848	Apply
Detect Type I	B106			Apply	Detect Type B212	Apply
Detect Type	8424			Apply	Detect Type B848	Apply
Detect Type	٧			Apply		
Detect Type	F212			Apply	Detect Type F424	Apply
HCE Rx Thres	hold					
Detect						
Threshold	d				Apply	
LPCD I/Q Lim	IT					
Detect						
I-Limit	:				Apply	
	5				Apply	

The signal detection threshold measurement has been developed in order to find the optimum value for this register based self diagnose test. Any change in the receiver settings requires a new value for this register.

The matching, antenna size and geometry and in general the overall system strongly influence the input level of the received signal at the RX pins of the PTX1xxR. Furthermore, processing and filtering of the signals in the digital receiver varies for different technologies. Therefore, the register values of the detection threshold must be changed individually for each technology.

1.1.4 Data signal and detection thresholds





In the figure shown above the signal detection threshold level 1 is the correct one, as it clearly separates the signal from the low level noise. One has to keep in mind that the input signal levels will also vary a lot depending on the position of the card in the field of the reader. If the detection threshold is set too low the system will start decoding noise and a lot of error notifications will be generated by the SW stack and forwarded to the application. In the opposite case, if the detection threshold is set too high, the system will never detect any signal.

1.2 RX Input resistance

The first component that is used to set the gain is the input resistor.

The selectable values are 5 and 10kOhm. Again, the proper setting depends on the board, antenna and the expected input voltages. Generally, in reader mode either the 5kOhm or 10kOhm should be used. The 5 and 10kOhm values are implemented as a polyphase network.

Rx Input Resistance

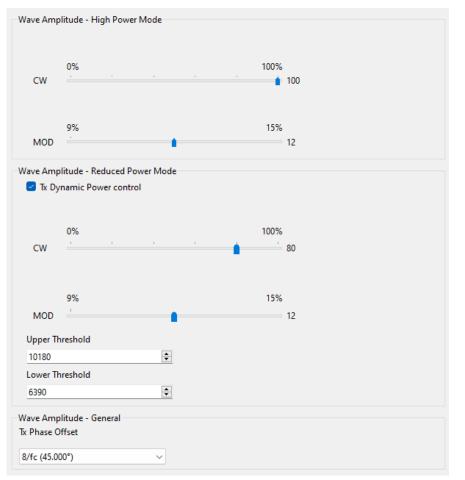
10kOhm



2 Configuration of transmitter settings

2.1 Power Settings

In the section Configurations / Transmitter / Power Settings is it possible to set the **CW** (continuous wave amplitude) and **MOD** (modulation index for Type B), for both **high power** mode and **reduced power** mode.



The **Dynamic Digital Power Control** (DDPC) is used to reduce the power level delivered from the output drivers of the PTX1xxR to the antenna based on the load condition.

The TX Dynamic Power Control box is used to enable (checked) or disable (unchecked) this feature.

The power switching mechanism is based on the measured receiver signal (RSSI) which reflect the coupling condition between the reader and the tag.

Upper Threshold is needed to switch to the High-Power wavebank, if the measured RSSI is above the defined value.

Lower Threshold is used to switch to the Reduced-Power wavebank, if the measured RSSI is below the defined value.

The two threshold values need to be determined by measuring the RSSI, with the reader and tag in the desired switching position, by setting the output drivers in high and low power condition.

A debug function is implemented in the GUI (section Applications / DDPC Measurements), which helps to fine tune this setting based on the HW configuration.

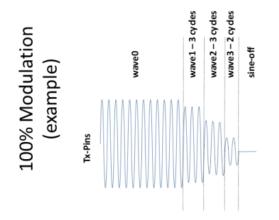


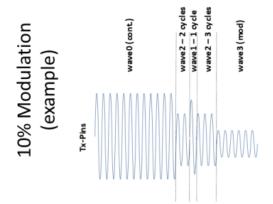
Start RSSI measure	ment		
High Power [%]	Hysteresis	High power low threshold	
100 🜩	100 🖨 🗌 Apply	10180 🜩	Apply
Reduced Power [%]	Hysteresis	Reduced power high threshold	
80 🜩	100 🖨 🗌 Apply	6390 ≑	Apply
Readouts:	32 🜩		
	n the selected power Read RSSI measureme		

The Read RSSI measurement will return the values to be used to set up the upper and lower threshold for switching between the high and low power levels. The hysteresis can be applied if the configured value is triggered unintentionally and uncontrolled switching between high and low power mode occurs.

2.2 Waveshaping

This feature shapes the pause pulses for type A and B separately. The falling and the rising edge of a pause pulse can be shaped within a range of 8 samples. It is used to get rid of over/undershoots as well as timing issues within the pulse (e.g. T3, T4 timings).





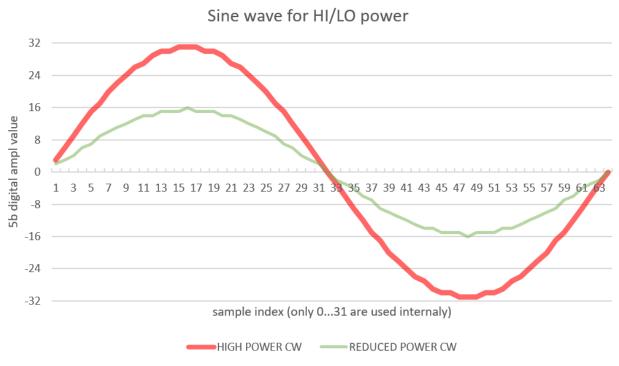
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PTX100R/105R IOT Config Tool																											-			>
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	8																													
Configurations		ation Edg	ge Co	ntigura	tor																									
∽ Receiver	High P	ower																												
Type A/B						Fall	ing Edg	je									Ri	ising	Edge											
Type F/V	Bitrate	(0	1		2	3		4		5	6		7		0		1		2	3	3	4		5		6		7	
✓ Transmitter	106 kBi	t/s 66%	~	51%	~ 309	6 V	off	~ 0	ff	off	\sim	off	$^{\vee}$ of	ff 🗸 🗸	of	~	off	~	off	\sim	off	\sim	off	\sim	off	\sim	off	\sim c	off	~
Power Settings	212 kB	it/s off		off	V off		off		66	off		off	V at	# V	of		- off		off		off		off		off		off	~ (.ff	
Waveshaping Type A Waveshaping Type B			_												_		-													
LPCD Settings	424 kBi	t/s_off		ott	~ off		off	~ 0	#	~ off		ott		+ ~	of	~	_ off		ott		off		ott		ott		ott	× (ott	~
✓ Card Mode	848 kBi	t/s_off	\sim	off	< ∼ off	\sim	off	\sim o	ff	< ∼ off	\sim	off	$^{\vee}$ of	f	of	~	off	\sim	off	\sim	off	\sim	off	\sim	off	\sim	off	\sim c	off	V
Card Mode																														
Application Configuration	Reduce	ed Powe	er i																											
Polling	neude																_													
Debug Signals						Fall	ing Edg	ge									R	sing	Edge											
Applications	Bitrate		D	1		2	3		4		5	6		7		0		1		2	3	3	4		5		6		7	
Discovery	106 kBi	it/s_off	~	off	✓ off	\sim	off	~ 0	ff	< ∼ off	\sim	off	$^{\prime}$ of	f	of	~	off	\sim	off	\sim	off	\sim	off	\sim	off	\sim	off	\sim (off	~
FeliCa DTE DDPC Measurements	212 kBi	it/s off	\sim	off	 ✓ off 	\sim	off	~ 0	ff	off	\sim	off	$^{\vee}$ of	f v	of		off	~	off	\sim	off	\sim	off	\sim	off	\sim	off	\sim c	off	~
Signal Detector	424 kB	it/s off		off	V off		off	× .	66	off		off	V at	# U	of		- off		off		off		off		off		off	~ (.ff	
Q-Measurement			_												_		-													
Calibration	848 kBi	t/s_66%	×	51%	× 309	6 ×	off	~ 0	ff	<_ off	× 1	off		f Y	of	~	off		off		off		off		off		off	\sim (off	
NDEF							_	_				_			_		- 1													
HCE T4T						_											- 1													
Test Signals and GPIOs																	- 1													
																	- 1													
								_									- 1													
																	- 1													
																	- 1													
																	- 1													
																	- 1													
					Waves	hapin	g Mod	ulatio	2 on Pat	3 ttern T	ype A	- Red	uced F	6 Power	7 Falling	Mod Edge														
					Symbo	lic TX	patte	n do	es no	t reflee	t real	wave	form s	hape o	n PICC/	lister	ier 📗													

In the GUI it is possible to combine different sine levels, in the eight wave cycles by specifying an amplitude value. Amplitudes for Type A and Type B can be set separately. By changing the wave amplitudes for the wave cycles, the output power can be fine-tuned, which makes it possible to model the wave shape to pass specific standard requirements.

In the example below, the sine wave is set to 100% for high power mode and 50% for reduced power.





Three wavebanks are available for TypeA and two for TypeB, where High- and Reduced power mode are independently configured. This means, 3 (TypeA) and 2 (TypeB) different wave amplitudes may be set for the wave cycles for each bitrate and power mode, but alltogether, the number of different amplitudes set is limited to a certain value.



3 Low Power Card Detection

In the section Configurations / Transmitter / LPCD Settings is it possible to set the parameters for tuning the low power card detection feature of the PTX1xxR.

D			
			100%
1 I	•	1	60
🗘 (μs)			
0x E (14) 0x B (11)			
	 ψ (μs) 0x E (14) 0x B (11) 	 τ τ	 τ φ φ φ τ τ

3.1 Overall Description / Principle

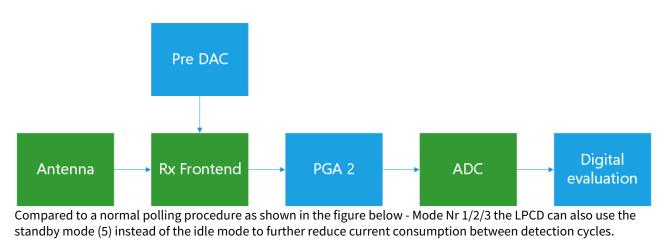
Low Power Card Detection (LPCD) is thought to reduce the amount of current consumed by the PTX during reader mode. With this mode enabled, the device can be active for a long time also in battery mode.

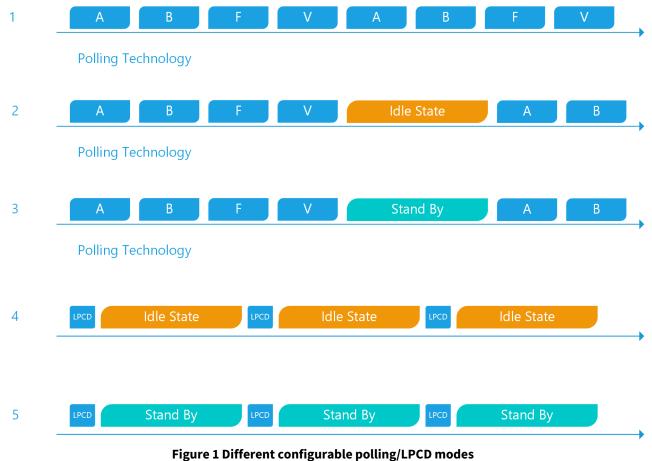
To achieve this the PTX uses only a reduced set of analogue and digital blocks during this mode and for a shorter time compared to default polling mode.

The following blocks are used during LPCD

- Transmitter on with **C**ontinuous **W**ave (CW)
- Rx Frontend → configured during Start-up
- PREDAC → configured during Start-up
- PGA2 → User specific configuration (Detection Range)
- ADC
- Digital Evaluation → User specific configuration (Sensitivity)







3.2 Normal LPCD Behavior

When the host starts the LPCD routine (Mode 4 & 5) an initial polling sequence is called to ensure no card is within the field and prevent false initial LPCD calibration.

If no card was detected the system starts the initial LPCD calibration (PRE-DAC). Directly after that the recalibration is called which sets the ADC to an already good start value (center). During the first few LPCD calls the recalibration is performed several times to compensate thermal and noise drifts. If a stable state is reached the device gets



powered up from the stand-by periods only for the short LPCD pulses (~75us) which dramatically reduces the current consumption.

3.3 Configuration

The configuration of the key parameters of the LPCD is done in the section Configurations / Transmitter / LPCD Settings of the GUI.

The four essential parameters are:

- Sampling Interval
- PGA2 Gain
- I-Limit
- Q-Limit

The transmitter sine amplitude can be adjusted for further current consumption reduction.

3.4 Parameter Details

3.4.1 Sampling Interval

To reduce influence of distortion over RF field/Supply the sampling interval between LPCD ADC samples can be increased from 0us (default) up to 255us.

The resulting LPCD pulse width increases by 32 * LPCD_Sampling_Interval + ~75us.

3.4.2 PGA2 Gain

This Parameter specifies the gain setting for I- and Q-branch which goes hand in hand with the detection range. Should be set between 15dB and 27dB.

3.4.3 I-Limit and Q-Limit

The I and Q Limits are used to adjust the sensitivity where the Q value should be lower than the I limit due to differently balanced detection path.

3.5 Configuration Procedure

3.5.1 1. Desired Sine Amplitude

For easier decision the following table shows the current consumption behavior for different amplitude and Standby/Idle time settings

	Current otion [%]		Si	ine Amplitude [%	6]	
		100	80	60	50	40
Discovery Idle time [s]	0,1	100	84	71	65	59



0,33	32	27	23	21	19
0,5	22	18	16	15	13
0,75	16	13	11	11	9
1	12	10	9	8	8

3.5.2 2. Sampling Interval Setting

Set Sampling Interval to 0us \rightarrow lowest current consumption.

3.5.3 3. PGA2 Gain Setting

Set initial LPCD_I/Q_Limits values to 0x0E for I-Limit and 0x0B for Q-Limit.

Now increase the PGA2 Gain setting step by step to increase the detection range and take a look on the false alarms. The value for PGA2 should start at 15dB and should be highest 27dB.

3.5.4 4. I-Limit and Q-Limit Setting

If the detection range from previous steps is already satisfying continue with the fine-tuning by adjusting the I-/Q-limits. Caused by the fact of wanted asymmetry in I and Q branches the I-branch should be held higher than Q-branch.

Start by setting both branches to a value where no false alarm occurs. Then start decreasing the Q branch limit. Last step will be the I branch adjustment.

3.6 Parameter Tuning

If the previous steps do not result in a good detection performance, depending on behavior following tweaks can be
done.

Behavior	Suggested configuration change	Impact
High false alarm rate / within wanted detection range	lower PGA 2 gain	lower noise, lower field change impact, decreases detection distance
	lower Q - limit	increases sensitivity on amplitude change
	lower I - Limit	
High false alarm rate / outside wanted detection range	increase Q - limit	higher ADC fluctuations are tolerated
	increase I - limit	



Behavior	Suggested configuration change	Impact
	increase SAMPLING_INTERVAL	more robust against distortions
	increase PGA 2 gain	higher field change impact; increases detection distance
	increase sine amplitude	higher field change impact
Good false alarm rate but short detection distance	increase PGA 2 gain	higher sensitivity
	decrease Q- and I - Limit	faster detection response, higher sensitivity
	increase sine amplitude	higher field change impact

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Ordering and Contact Information



Headquarters

Panthronics AG Sternaeckerweg 16 A-8041, GRAZ AUSTRIA

office@panthronics.com

Phone: +43 316 269 259 www.panthronics.com