Recommended External Circuitry for Renesas GaN FETs

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Part I: Introduction

Transphorm GaN FETs provide significant advantages over silicon (Si) superjunction MOSFETs by offering lower gate charge (Qg), faster switching speeds, and lower body-diode reverse recovery charge (Qrr). GaN FETs exhibit in-circuit switching speeds much higher than that of the current Si technologies. The inherent rapid switching of GaN devices reduces current/voltage cross-over power losses, enabling high frequency operation while simultaneously achieving high efficiency.

However, the accompanying high di/dt transient during switching, combined with parasitic inductances, generates noise voltages in the circuit. This noise can interfere with the gate and the driver of the device, and, in the worst case, creates sustained oscillation that must be prevented for safe operation of the circuit. This application note provides guidance on how to eliminate oscillation and how to achieve high switching current with a controlled di/dt.

Part II: Solutions to Suppress Oscillation

To avoid sustained oscillation, it is important to minimize noise generation, to minimize noise feedback, and to damp the ringing energy resulting from the high current/voltage transients. This can be achieved with the recommendations outlined below using a half-bridge switching circuit in Figure 1 as an example.

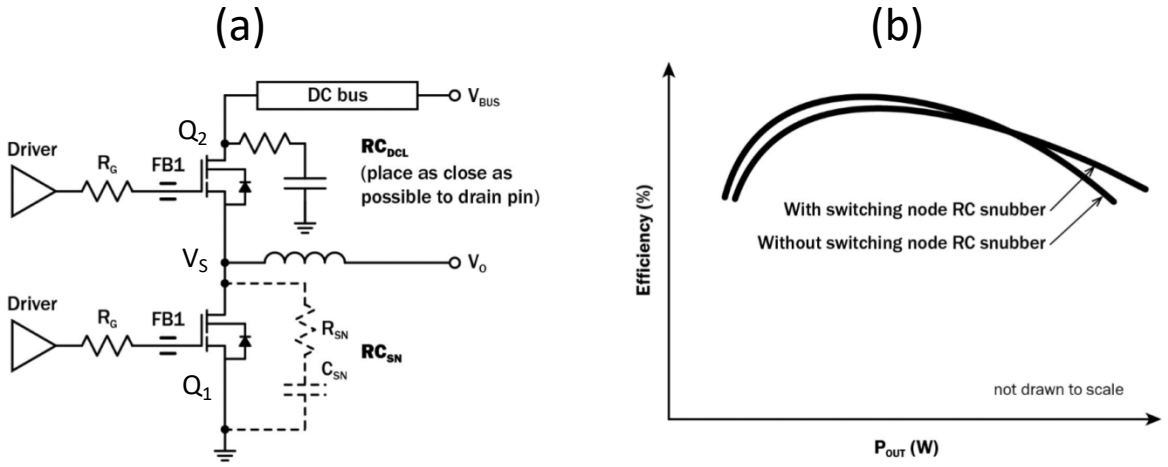


Figure 1. a) Half-bridge switching circuit and b) Efficiency vs. output power

1) Optimize the PCB layout to minimize external parasitic inductances and associated feedback. Use a large area ground plane for an overall low-noise base potential. Arrange the gate drive circuit on one side and the output circuit on the other side to minimize noise feedback from the output loop to the input loop. Place the driver circuit close to the gate of the device. Shorten the power loop by arranging the high-side and low-side devices close-by.

2) Use a gate ferrite bead [FB1 in Figure 1(a)] to prevent the high-frequency noise from entering the driver and logic circuits. This bead should be mounted close to the Gate lead of the device. NOTE: This is required even for single-ended non-half-bridge designs. The specification of the recommended gate ferrite beads are listed in Transphorm's GaN FET datasheets and also summarized in Table 2. The TO247 package includes a built-in gate ferrite bead for our Gen III devices but has been moved to the outside for our latest Gen IV (G4) devices. Please refer to page three of the datasheet to verify its position.

3) Use a DC-link RC snubber [RC_{DCL} in Figure 1(a)]. The DC rail or DC-link, when decoupled with a low-ESR fast capacitor, can be considered a high-Q C-L network at high frequencies (with "L" being the feed inductance of the DC bus). This can interact with the devices at voltage/current transients and lead to ringing. Adding an RC snubber across the DC-link close to the drain pin of the high-side device can effectively absorb the ringing energy, suppressing potential oscillation. This effect is shown in Figure 2 where the high-frequency ringing at 25 A turn-off is substantially damped with the RC_{DCL}. Since this snubber is not inserted at the switching node, it does not add switching loss to the circuit. NOTE: This is recommended even for single-ended non-half-bridge designs. *The practical values of the RC_{DCL} can be 2 sets of 6-10Ω/0.5W SMD resistors in series with a 10nF/600-1000V ceramic SMD cap, or 1 set of 3-4Ω/1W resistors in series with a 10-20nF/600-1000V cap if space is limited.*

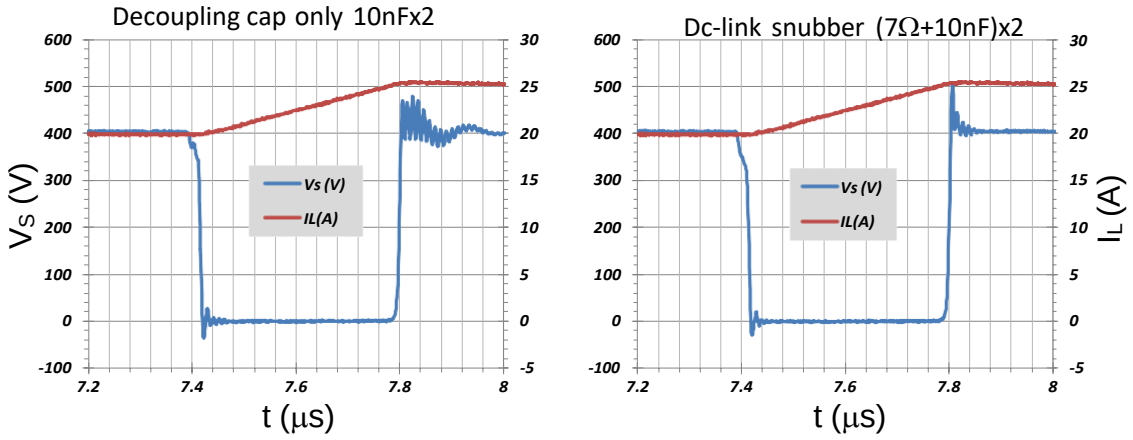


Figure 2. Half-bridge inductive switching waveforms with decoupling capacitor only and with DC-link snubber (RC_{DCL}) (Devices: TP65H050WS)

4) Adding a switching-node RC snubber [RC_{SN} in Figure 1(a)] can further reduce high-frequency ringing and help control di/dt transients at high operation currents. The effect of the RC_{SN} on switching waveform at a switching current >50 A is shown in Figure 3. Unlike the RC_{DCL}, the capacitance of the RC_{SN} does increase switching loss. The recommended snubber parameters with little degradation in efficiency are given in the datasheet and are summarized in Table 2 for both single R_G and dual $R_{G(ON)}$/$R_{G(OFF)}$ use.

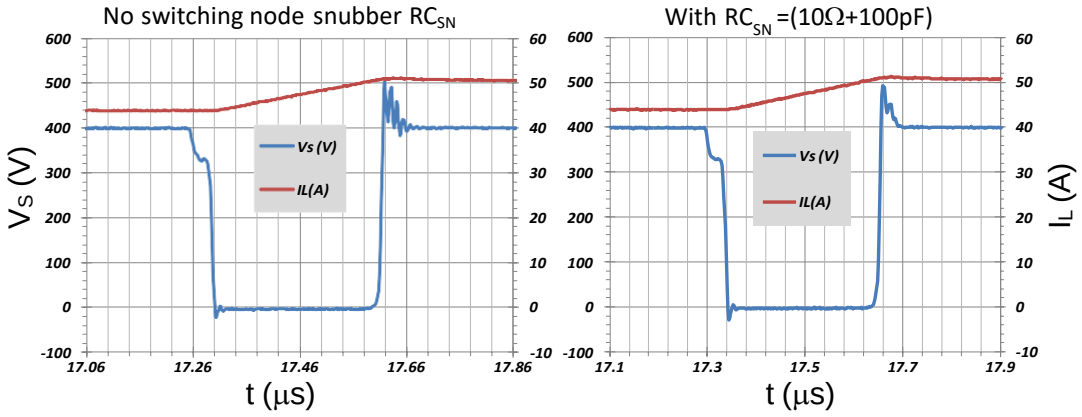


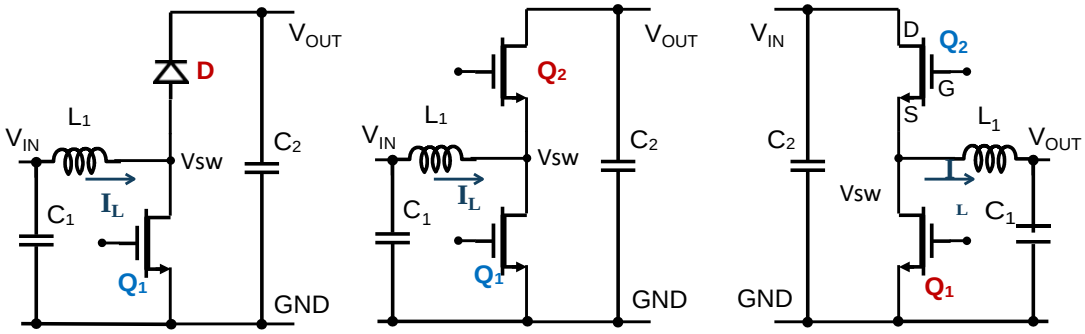
Figure 3. Effect of switching node snubber RC_{SN} on half-bridge inductive switching waveforms (Devices: TP65H035WS).

Part III: The di/dt Limits of GaN Switching Devices & Solutions for High-current Operation

Transphorm GaN FETs are designed for the highest robustness and reliability within the technology boundaries today. These devices can operate to their full voltage rating and at extremely high di/dt levels in normal operation mode (forward conduction when current enters the Drain). However, when used as a free-wheeling device in reverse conduction mode (current enters the Source when the Gate is off), there are di/dt limits beyond which the performance can be negatively affected. Although these reverse conduction di/dt limits in the range of 1900~3500 A/μs (depending on device & stress duration) are much greater than that of typical superjunction devices at ~60 A/us, care must be taken for best performance at high current levels since the di/dt value is a strong function of switching current.

It is important to note that this di/dt limit only applies to the device acting as a free-wheeling diode (FWD) and only applies to the duration when the FWD transitions from blocking voltage to reverse conducting current. Three cases are illustrated in Figure 4; the affected devices are the ones functioning as an FWD during dead-time when the inductor current commutates from the main switch to the reverse current of the FWD.

1) A boost converter that uses a SiC diode as the rectifier device – Not affected.
2) A synchronous boost that uses a GaN FET as the FWD – Q_2 affected.
3) A synchronous buck that uses a GaN FET as the FWD – Q_1 affected.



1) Boost converter
Q_1 di/dt limit: No

2) Boost converter
Q_1 di/dt limit: No
Q_2 di/dt limit: Yes

3) Buck converter
Q_1 di/dt limit: Yes
Q_2 di/dt limit: No

Figure 4. Identifying the device affected by the di/dt limit in three popular circuits: (1) boost converter, (2) synchronous boost converter, and (3) buck converter.

The maximum di/dt stress happens when the main switch [Q_1 in Figure 4 (2) or Q_2 in Figure 4 (3)] turns off and the inductor current redirects to the FWD instantly. The higher the turn-off current, the higher the reverse conduction di/dt. The reverse conduction di/dt limits ($di/dt_{(RM)}$) is listed in the datasheet (Table 1).

TP65H035G4WS

Electrical Parameters (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	29.5	A	V_{GS}=0V, T_C=100 °C ≤25% duty cycle
V_{SD}	Reverse voltage [j]	—	1.8	—	V	V_{GS}=0V, I_S=32A
		—	1.3	—		V_{GS}=0V, I_S=16A
t_{RR}	Reverse recovery time	—	59	—	ns	I_S=32A, V_{DD}=400V, di/dt=1000A/µs
Q_{RR}	Reverse recovery charge	—	150	—	nC	
$(di/dt)_{RM}$	Reverse diode di/dt [k]	—	—	3200	A/µs	Circuit implementation and parameters on page 3

Notes:
j. Includes dynamic $R_{DS(on)}$ effect
k. Reverse conduction di/dt will not exceed this max value with recommended R_G.

Table 1. TP65H035G4WS reverse diode conduction di/dt limits and associated max switching current when using the recommended R_G and RC_{SN}.

Note that the reverse diode switching current limits were obtained with the recommended circuit parameters [Figure 1(a) and Table 2]. The gate resistor(s) are important to control the di/dt and the addition of a switching node snubber RC_{SN} offers further improvements when operation current is high. The effect of RC_{SN} is shown in Figure 1(b): a slight reduction in low-load efficiency, but a significant enhancement at high load. In applications with Rg is equal to or higher than the recommended value, the RC_{SN} can be omitted. In all situations, care has to be taken to ensure junction temperature of the devices do not exceeding maximum rating.

Part IV: Additional Design Notes

1) Circuit and Layout Recommendations

- As GaN FETs switch extremely fast, we recommend using a driver(s) with sufficient Common Mode Transient Immunity (CMTI) so as not to cause disruption between the secondary and primary side of isolated drivers when in operation.
- When using the GaN FETs in a half bridge configuration, we recommend using an integrated half bridge gate driver(s) that offers overlap protection (interlock) to prevent outputs VOA and VOB from being high at the same time, such as the Skyworks Si823x series.

- Recommended deadtimes guidelines.

Device	C_{ISS}	Single R_G	Total Switching Time	Deadtime	Topology	Operating Frequency	Comment
TP65H070G4PS	638pF	50 Ω	112.8ns	220ns	Hard switched HB	100kHz	Estimated
TP65H050G4WS	1000pF	45 Ω	159.7ns	250ns	Hard switched HB	100kHz	Estimated
TP65H035G4WS	1500pF	30 Ω	174ns	330ns	Hard switched HB	70kHz	Dead time tested
TP65H015G5WS	5200pF	15 Ω	237.4ns	430ns	Hard switched HB	50kHz	Dead time tested

- Place the RC_{DCL} (required) as close as possible to the drain pin of the high-side GaN FET and ground it to the large ground plane.
- SMD mounting is recommended for all snubber components.
- A Gate resistor (R_G) is required for all devices.
- Gate ferrite beads (FB1) are required for all devices.
- If a smaller than recommended gate resistor is used, then a switching node RC snubber (RC_{SN}) is recommended.
- The gate ferrite bead and gate resistor prevent oscillation and reduce excessive di/dt when the GaN device is used in a half-bridge topology.
- The RC_{SN} slightly reduces light and medium load efficiency with the benefit of increased output power.
- The RC_{SN} implementation in a half-bridge has the advantage of allowing a higher peak turn-off switching current due to the reduction of the di/dt seen by the freewheeling device as the main conducting device turns off.

2) Recommended External Components for Gate Drive Circuit (may vary with PCBA layout)

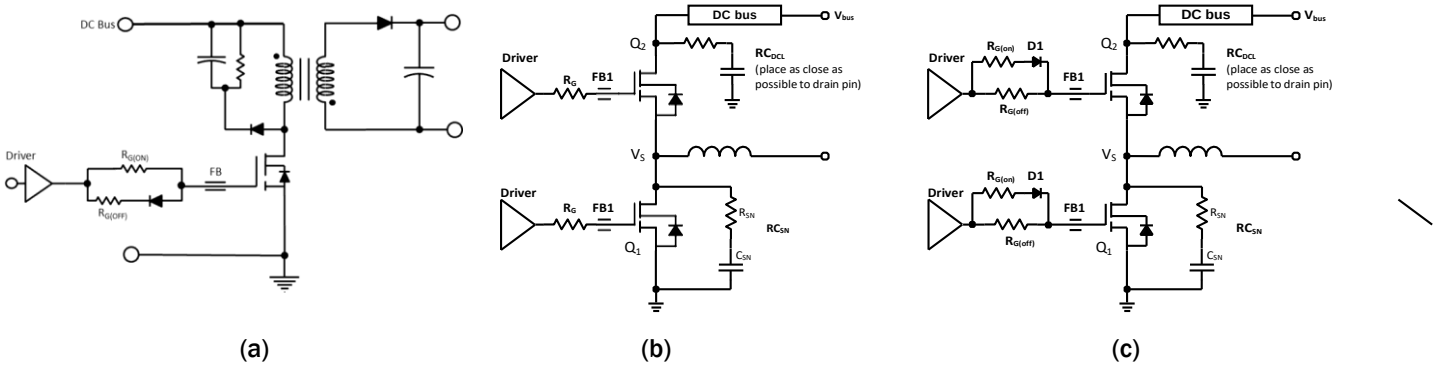


Figure 5. Driving circuits: (a) Singles ended with dual Rg – only used for dv/dt EMI control (b) Single output driver with a single Rg, (c) single output driver with different turn-on and turn-off Rg

Device Gate Drive Recommendations (may vary due to PCBA layout)										
Specifications	TP65H015G5WS	TP65H035G4x	TP65H050G4x	TP65H070G4x	TP65H150G4PS TP65H150G4LSG	TP65H150BG4JSG TP65H150G4LSGB	TP65H300G4LSG	TP65H300G4JSGB TP65H300G4LSGB	TP65H480G4JSG	TP65H480G4JSGB
	TO-247	TO-247/TOLL	TO-247/TO-263/TOLL	TO-220/TOLT/TOLL/PQFN	TO-220/PQFN	QFN	PQFN	QFN	PQFN	QFN
Gate Voltage Drive	**0V, 12 V**	**0V, 12 V**	**0V, 12V**	**0V, 12V**	**0V, 12V**	**0V, 6V -6V, 6V**	**0V, 12V**	**0V, 6V -6V, 6V**	**0V, 12V**	**0V, 6V -6V, 6V**
Recommended Single Gate Resistor (R_G) - Single ended topologies **(for EMI dv/dt control)**	15Ω	30Ω	45Ω/30Ω/18Ω	50Ω	50 to 70Ω	65Ω	30 to 60Ω	65Ω	30 to 60Ω	100 to 300Ω
Recommended Single Gate Resistor ($R_{G(ON)}$/$R_{G(OFF)}$) - Single ended topologies **(for EMI dv/dt control)**	5/15Ω	10/30Ω	TBD	TBD	TBD	65Ω to 150Ω , 0Ω to 10Ω 65Ω to 100Ω , 0Ω to 20Ω	100Ω to 300Ω , 0Ω to 15Ω	50Ω to 150Ω , 0Ω to 10Ω 50Ω to 100Ω , 0Ω to 20Ω	100Ω to 300Ω , 0Ω to 15Ω	65Ω to 150Ω , 0Ω to 10Ω 65Ω to 100Ω , 0Ω to 20Ω
Recommended Single Gate Resistor (R_G) - Half-bridge topologies	15Ω	30Ω	45Ω/30Ω/18Ω	50Ω	50 to 70Ω	65Ω	30 to 60Ω	65Ω	--	--
Recommended Single Gate Resistor ($R_{G(ON)}$/$R_{G(OFF)}$) - Half-bridge topologies	5/15Ω	10/30Ω	TBD	TBD	TBD	65Ω to 150Ω , 0Ω to 10Ω 65Ω to 100Ω , 0Ω to 20Ω	100Ω to 300Ω , 0Ω to 15Ω	50Ω to 150Ω , 0Ω to 10Ω 50Ω to 100Ω , 0Ω to 20Ω	--	--
DC Link Snubber (RC_{DCL})	[10pF, 3.3Ω] x 3	[4.7nF, 5Ω] x 2	[4.7nF, 8Ω] x 2	[10nF, 5Ω] x 2	[4.7nF, 2.5Ω]	[10nF, 3.3Ω]	[4.7 - 10nF, 5Ω]	[4.7 - 10nF, 5Ω]	[4.7 - 10nF, 5Ω]	[4.7 - 10nF, 5Ω]
Ferrite Bead Gate (FB1) @ 100 MHz	80-120Ω	200-270Ω	200-300Ω	200-300Ω	200 to 300Ω 240Ω	240Ω 330Ω	240Ω	240Ω	240Ω	240Ω
Switch node Snubber (RC_{SN}) - recommeded when using lower R_G values	[100pF, 10Ω] x 2-3	[100pF, 10Ω]	[200pF, 5Ω]	[68pF, 15Ω]	--	--	--	--	--	--
Datasheet Specification di/dt Maximums										
Specifications	TP65H015G5WS	TP65H035G4x	TP65H050G4x	TP65H070G4x	TP65H150G4PS TP65H150G4LSG	TP65H150BG4JSG TP65H150G4LSGB	TP65H300G4LSG	TP65H300G4JSGB TP65H300G4LSGB	TP65H480G4JSG	TP65H480G4JSGB
	TO-247	TO-247/TOLL	TO-247/TO-263/TOLL	TO-220/TOLT/TOLL/PQFN	TO-220/PQFN	QFN	PQFN	QFN	PQFN	QFN
Reverse diode max (di/dt), repetitive ($A/\mu s$) -di/dt_{RDMC}	3500	3200	2500	1900	--	--	--	--	--	--
When -3V ~ -5V turn-off is used, Rg can increase by 1.5x to 1.8x.										

Table 2. Recommended components for single ended and half-bridge circuits.

3) To Verify GaN FET Stable Operation

To verify adequate operational margin without oscillation, as a minimum observe the V_{DS} waveforms at the turn-on and turn-off switching edges at the application's maximum drain current. This may occur during start-up or at the application's maximum load step. A double-pulse or multi-pulse test is highly recommended utilizing the actual layout, with current levels at or greater than 120 percent of the application's anticipated peak current. Verify that the ringing on the V_{DS} waveform at the transition edges is adequately damped. See design guide DG004: Multi-pulse Testing for GaN Layout Verification.

The driver circuits with different configurations of driver and gate resistor are shown in Figure 5. A proper gate resistor is effective to limit the switching di/dt and keep the switching stable. As described in part III, the di/dt limit only applies to the device acting as a free-wheeling diode (FWD), i.e. the turn-off switching speed of the active device should be controlled, and only large turn-off Rg should be chosen but turn-on Rg can be small to reduce the turn-on power loss (except for single ended or flyback topologies where turn on is more important to reduce EMI and di/dt is not an issue due to no device operating as a FWD). The separate turn-on and turn-off Rg can be achieved using a Schottky diode in series with a $R_{G(ON)}$ resistor paralleling with a $R_{G(OFF)}$ resistor, as shown in Figure 5 (c). It should be noticed that the direction of diode is different from that in the gate driving circuit of Si MOSFET. The equivalent $R_{G(ON)}$ is $R_{G(ON)}*R_{G(OFF)}/(R_{G(ON)}+R_{G(OFF)})$, and turn-off R_G value is same with $R_{G(OFF)}$. The equivalent $R_{G(ON)}$ will be used if a dual output driver IC is used. Although there is no di/dt limit for turn-on, a proper $RG_{(ON)}$ should be carefully selected:

- to avoid cross-talk issues in high-speed switching half bridge circuit using 3 pin TO-220 and TO-247 packaged devices.
- EMI issues for single ended topologies such as flyback.