RAA271084: Designing a Power Supply Circuit for the RH850/U2A16

This document explains the connection example for the power management IC (PMIC) RAA271084 with the Renesas automotive 32-bit microcontroller (MCU) RH850/U2A16, and it provides important guidelines such as power-on/off requirements, low power mode supported by the RAA271084, and recommendations for both unused pins and one-time programmable (OTP) memory.

The RAA271084 contains a high-voltage primary buck/boost controller, a low-voltage synchronous buck controller, and five low-dropout (LDO) liner regulators; two of the LDO regulators can be used as trackers. The DCDC switching frequency, output voltage, power-up/down sequence, and other features can be configured using OTP memory.

Target Devices

- RAA271084
- RH850/U2A16

Contents

1. References

- RAA271084 Datasheet
- RH850/U2A-EVA Group User's Manual: Hardware
- U2A-EVA, U2A16, U2A8, U2A6 Switching Voltage Regulator (SVR) Guideline (LLWEB-10029051.pdf)

Note: References are the latest published version unless otherwise indicated.

2. Overview

In this document, two power solution examples are described for using the RH850/U2A16 with the RAA271084. The primary difference between the examples is whether the MCU SVR function is being used or not.

Example1 is a minimum BOM area solution. In this connection, the MCU VDD is directly supplied from the RAA271084 DCDC regulator output. The LDO1-4 outputs are used to supply other MCU power rails. The direct VDD supply can reduce the BOM area by eliminating the BOM for the MCU embedded voltage regulator (SVR). Use the References for the RH850/U2A16 SVR function details (see the Hardware manual and SVR guideline).

Example2 is flexible power supply solution. In this connection, the DCDC regulator supplies the MCU SVR and other power rails. Compared with Example1, the LDO outputs are not all used with MCU power rails; LDO3 and LDO4 are configured as trackers in this connection. In Example2, the LDO1 output voltage is set to 3.3V to supply the MCU power rail, which is supplied by LDO3 in Example1.

When DCDC2 output is set to 5V, the switching frequency must be 440kHz. When the DCDC2 output is 3.3V or less, the switching frequency can be 440kHz or 2.2MHz. DCDC1 switching frequency can be 440kHz or 2.2MHz.

Table 1. The RAA271084 Power Solution Examples for RH850/U2A16[1]

Power Solution Example		Example 1	Example 2
Target solution		Minimum BOM area solution	Flexible power supply solution
MCU SVR function		Unused	Used
PMIC regulator output voltage settings	DCDC1	5.7V	5.7V
	DCDC2	1.09V	5V
	LDO1	5V	3.3V
	LDO2	5V	5V
	LDO3	3.3V	5V (Tracker)
	LDO4	5V	5V (Tracker)
PMIC DCDC switching frequency	DCDC1	2.2MHz	440kHz
	DCDC2	2.2MHz	440kHz

1. Use the References for the RH850/U2A16 SVR function details (see the Hardware manual and SVR guideline).

2.1 Block Diagram of Power Configuration for the RH850/U2A16 without SVR [Example1]

The RAA271084 has two Bucks and five LDOs. These outputs are controlled by Wake1 and Wake2. Figure 1 shows an example of connection with the RH850/U2A16 and the RAA271084 without SVR.

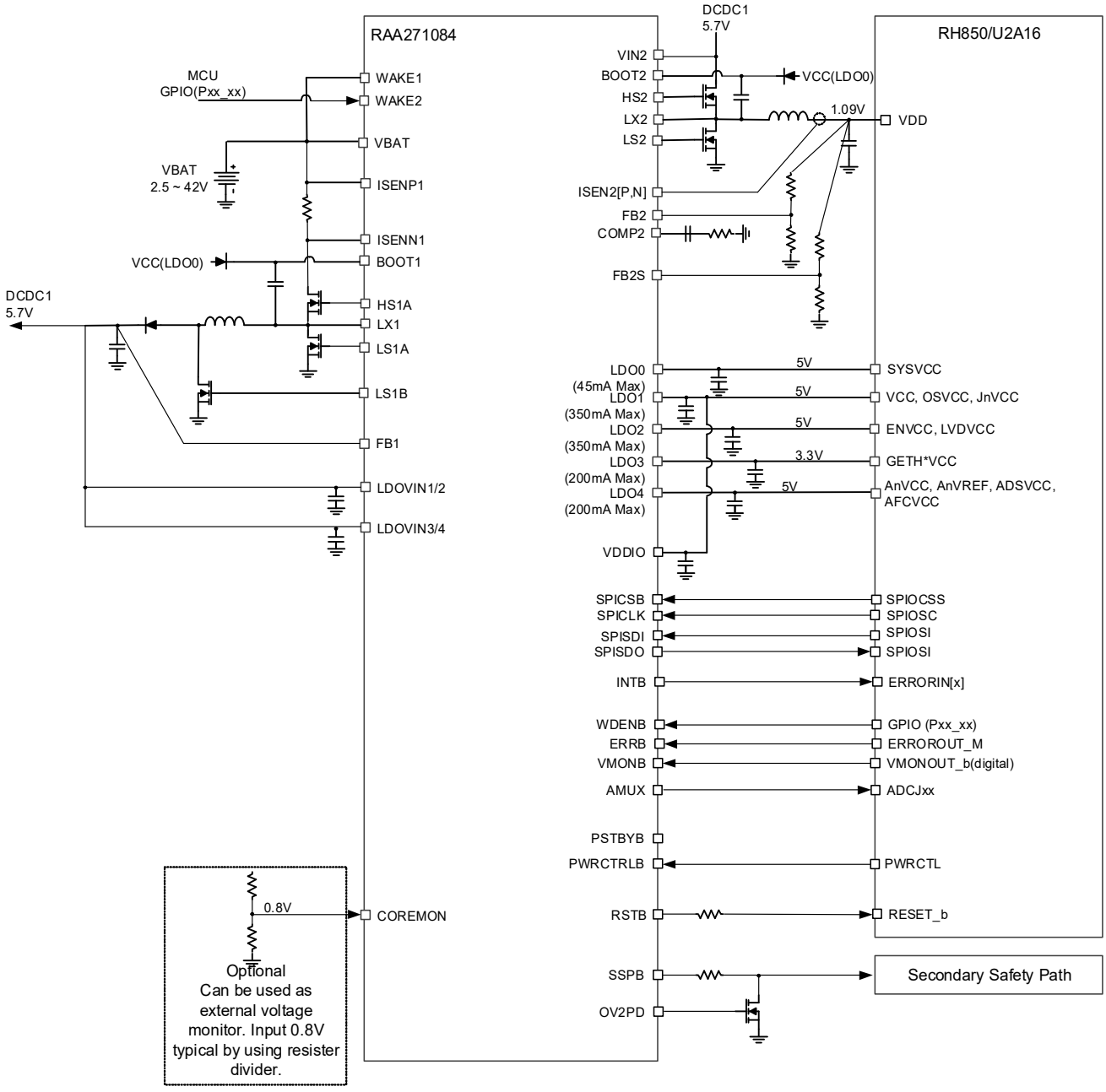

Figure 1. The RAA271084 Application Diagram with the RH850/U2A16 without SVR

Table 2. Regulator Connection at Example1

Regulators	Output voltage	PMIC Output current capability	Supply for
DCDC1	5.7V	-	The RAA271084 DCDC/LDO IN
DCDC2	1.09V	-	MCU VDD
LDO1	5V	350mA	MCU VCC
LDO2	5V	350mA	MCU EnVCC
LDO3	3.3V	200mA	MCU GETH*VCC
LDO4	5V	200mA	MCU AnVCC
VCC(LDO0)	5V	45mA	MCU SYSVCC

Table 3. I/O Connection

RAA271084		RH850/U2A16
Pin Number	Pin Name	Pin Name[1]
7	WAKE1	(VBAT)
8	WAKE2	GPIO(Pxx_xx)
10	OV2_PD	(External FET gate)
13	PSTBYB	(Open)
14	PWRCTLB	PWRCTL
23	COREMON	(Optional, external 0.8V)
24	AMUX	ADCJxx
25	SSPb	(Depends on System)
26	WDENb	GPIO(Pxx_xx)
27	VMONb	VMONOUT_b(digital)
28	ERRb	ERROROUT_M
29	RSTb	RESET_b
30	INTb	ERRORIN[x]
31	SPISDO	MSPI0SI
32	SPISDI	MSPI0SO
33	SPICLK	MSPI0SC
34	SPICSB	MSPI0CSS

1. Names in parenthesis () are not MCU pins.

2.2 Block Diagram of Power Configuration for the RH850/U2A16 with SVR [Example2]

Figure 2 shows an example of a connection with the RH850/U2A16 and RAA271084 with SVR. In this connection, LDO3 and LDO4 can be used as a tracker to supply external devices or circuits because of a DCDC2 5V supply to not only SVR but also other 5V power rails. The IO connection is the same as in Example1.

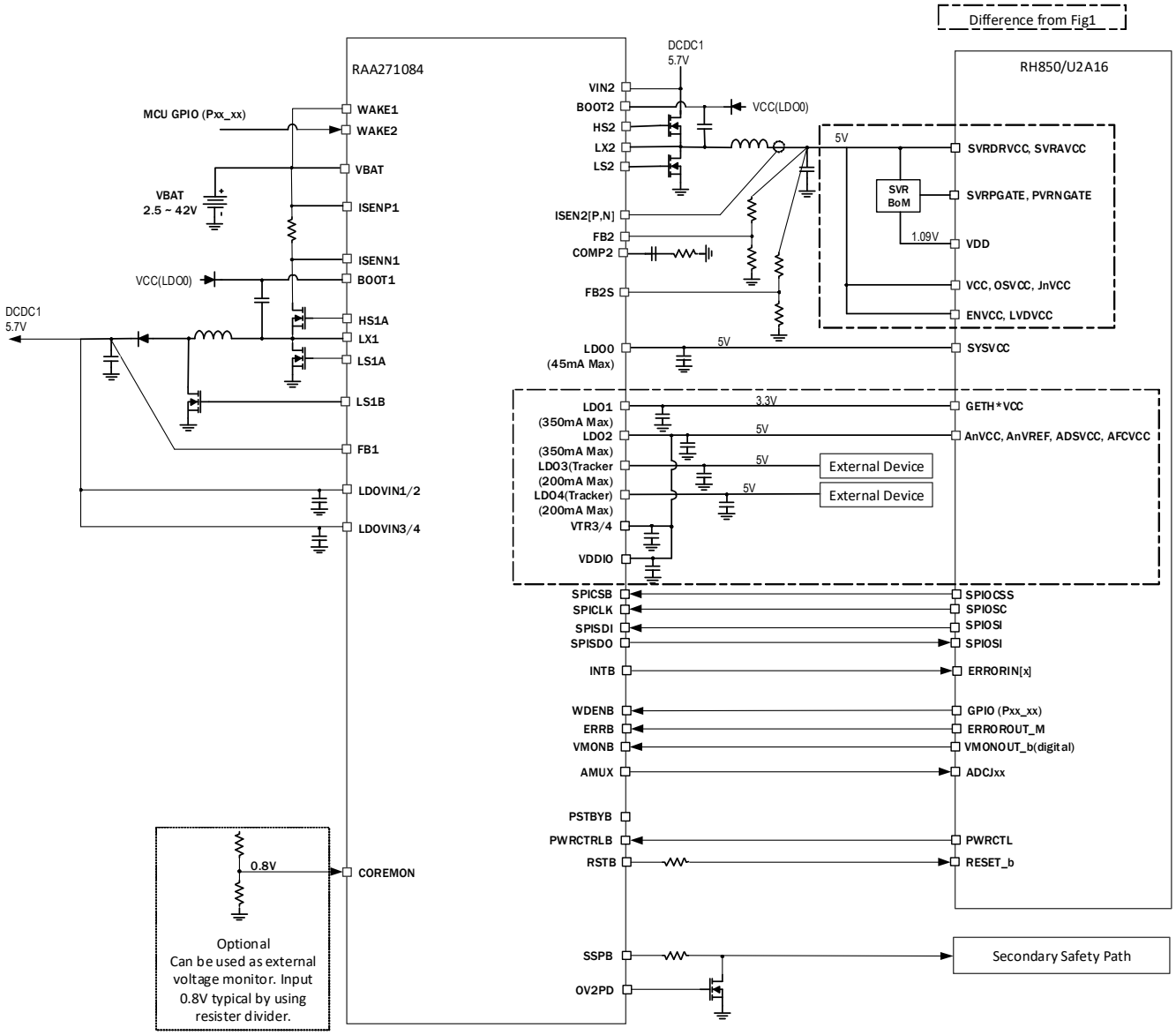

Figure 2. The RAA271084 Application Diagram with the RH850/U2A16 without SVR

Table 4. Regulator Connection at Example2

Regulators	Output Voltage	Output Current	Supply for
DCDC1	5.7V	-	The RAA271084 DCDC/LDO IN
DCDC2	5V	-	MCU SVR/VCC/EnVCC
LDO1	3.3V	350mA	MCU GETH*VCC
LDO2	5V	350mA	MCU AnVCC
LDO3/TRACKER	5V	200mA	External device
LDO4/TRACKER	5V	200mA	External device
VCC(LDO0)	5V	45mA	MCU SYSVCC

3. The RAA271084 Power-On/Off Requirements from the RH850/U2A16

The RH850/U2A16 is a sequence-free product, so only perform power-on-reset timing and power hold time when the regulators disable. Both requirements are satisfied by the RAA271084 if it is set for any of the OTP settings that involve power-on/off sequence timings (OPT_SEQ_CTRL, OPT_SLOT_TIME, OPT_SLOT_DCDC, OPT_SLOT_LDO, OPT_TOFF_TIME, OPT_RSTB_DLY).

In power-on timing, the RESET must keep L during t_{RESH1} after all the MCU power rails are supplied. The MCU power rails do not require the order of power supplies. The RAA271084 can be configured for the startup timing of each regulator and RSTB hold time. Any setting of OPT_SEQ_CTRL, OPT_SLOT_TIME, OPT_SLOT_DCDC, OPT_SLOT_LDO, or OPT_RSTB_DLY can satisfy the RH850/U2A16 requirement. Refer to the *RAA271084 Datasheet* (section, Timing Summary) for details about the configurable items and its timings.

In power-off timing, the power rails must keep High during t_{PWH} with RESET = Low to avoid damaging the device. The RAA271084 regulators can configure the off delay time (such as the Regulator output hold time when the regulator is disabled). Any settings of OPT_TOFF_TIME can satisfy the RH850/U2A16 requirement.

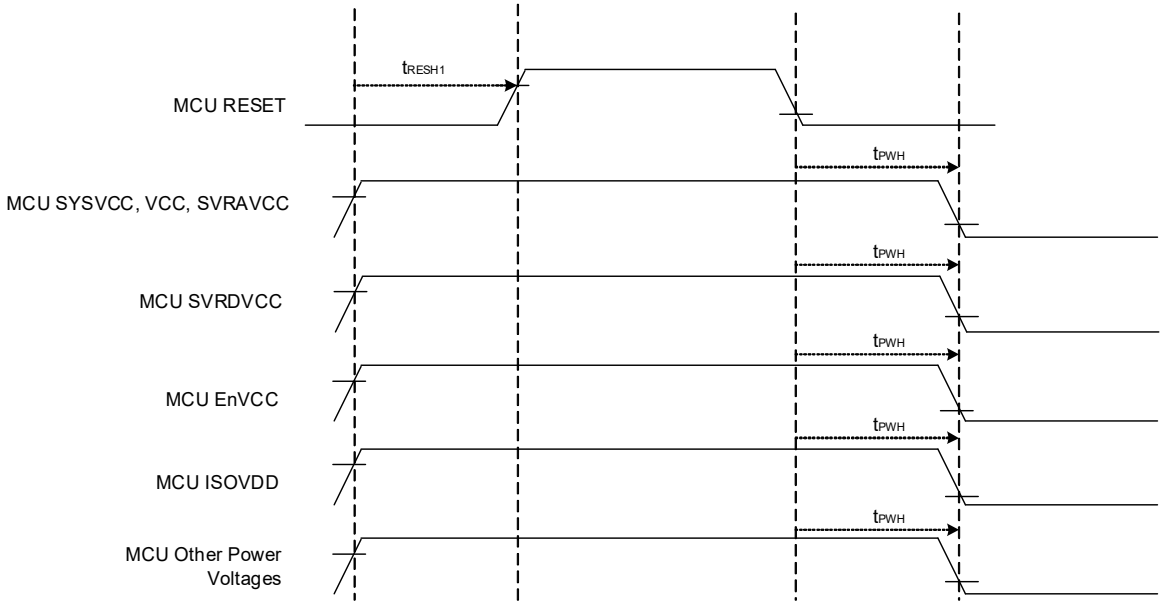

Figure 3. Power-On and Power-Off Timings – RH850/U2A16

Note: Refer to the RH850/U2A16 hardware manual (Section 55 Electrical Characteristics) for more details about the MCU power sequence.

4. The Settings to Support MCU Low Power Mode

The RH850/U2A16 uses the DeepSTOP mode as a low power mode. The RAA271084 has a dedicated DeepSTOP mode to support this setting. The RAA271084 stops the power supply for the MCU VDD during DeepStop mode. The regulator output state in DeepSTOP can be configured by OTP. The regulator output status is shown in Table 5. Refer to the *RAA271084 Datasheet* (in the section DeepSTOP Entry/Exit) for details about how to enter/exit the DeepSTOP mode.

In Example1, DCDC2 is disabled because it is a VDD supply. Other regulators are enabled to keep the MCU power supply.

In Example2, DCDC2 is enabled because it supplies the MCU SVR and other MCU power rails. The LDO3 and LDO4 is disabled because it does not supply to the MCU. The LDO3 and LDO4 output statuses depend on the connecting devices and system requirements.

Table 5. Regulator State at DeepSTOP Mode

Assumed Use Cases at DeepSTOP Mode							
Regulators	**LDO0**	**DCDC1**	**DCDC2**	**LDO1**	**LDO2**	**LDO3**	**LDO4**
Example1	On	On	Off	On	On	On	On
Example2	On	On	On	On	On	Off[1]	Off[1]

1. Depends on connecting devices and system requirements.

5. Recommendation for Unused Pins

This section describes recommendations for unused pins. Example1 and Example2 described in this document assume that all the functions of the RAA271084 are used. If there are any functions that are not used, the OTP configuration should be changed from the OTP recommendation value described in Table 7.

Table 6. Recommendation for the RAA271084 Unused Pins

Pin Number	Pin Name	I/O	Recommended Handling of Unused Pin	Note
3	NC	-	Open	-
7	WAKE1	Input	Connect to ground	Either WAKE1 or WAKE2 needs to be used.
8	WAKE2	Input	Connect to ground	Either WAKE1 or WAKE2 needs to be used.
10	OV2_PD	Output	Open	-
13	PSTBY	Input	Open	-
14	PWRCTRLB	Input	Open	-
15	LDOVO4	Output	Open	LDO4 is needed to be set as disable by OTP.
16	LDOVIN3/4	Input	Open	LDO3 and LDO4 are needed to be set as disable by OTP.
17	LDOVO3	Output	Open	LDO3 is needed to be set as disable by OTP.
18	VTR3/4	Input	Open	LDO3 and LDO4 are needed to be set as LDO output by OTP.
19	NC	-	Open	-

Table 6. Recommendation for the RAA271084 Unused Pins (Cont.)

Pin Number	Pin Name	I/O	Recommended Handling of Unused Pin	Note
20	LDOVO2	Output	Open	LDO2 is needed to be set as disable by OTP.
21	LDOVIN1/2	Input	Open	LDO1 and LDO2 are needed to be set as LDO output by OTP.
22	LDOVO1	Output	Open	LDO1 is needed to be set as disable by OTP.
23	COREMON	Input	Connect to ground	-
24	AMUX	Output	Open	-
25	SSPB	Output	Open	-
26	WDENB	Input	Connect to ground	-
27	VMONB	Input	Connect to ground	-
28	ERRB	Input	Connect to ground	-
30	INTB	Output	Open	-
31	SPISDO	Output	Open	-
32	SPISDI	Input	Open	-
33	SPICLK	Input	Open	-
34	SPICSB	Input	Open	-

6. OTP Recommendation

6.1 OTP Configuration in Example1 and Example2

The RAA271084 has a custom configuration saved in one-time programmable (OTP) memory. This section provides recommendation settings for Example1 and Example2 (see Overview). For more information about the device, see the *RAA271084 Datasheet*.

Table 7 shows the OTP settings for the use cases in Example1 and Example2.

Table 7. OTP Configuration in Example1/2

Address	Register Name	OTP Value Example1	OTP Value Example2
0x10	OPT_SEQ_CTRL	0x00	0x00
0x11	OPT_SLOT_TIME	0x00	0x00
0x12	OPT_SLOT_DCDC	0x00	0x00
0x13	OPT_SLOT_LDO	0x00	0x00
0x14	OPT_HP	0x00	0x00
0x15	OPT_DS	0x00	0x32
0x16	OPT_TOFF_TIME	0x00	0x00
0x30	OPT_ERRB_CTRL	0x00	0x00
0x31	OPT_VMONB_CTRL	0x00	0x00
0x82	OPT_WDT_CONFIG1	0x00	0x00

Table 7. OTP Configuration in Example1/2 (Cont.)

Address	Register Name	OTP Value Example1	OTP Value Example2
0x120	OPT_FLT_RESP1	0x00	0x00
0x121	OPT_FLT_RESP2	0x00	0x00
0x122	OPT_FLT_RESP3	0x00	0x00
0x123	OPT_FLT_RESP4	0x00	0x00
0x124	OPT_FLT_RESP5	0x00	0x00
0x125	OPT_FLT_RESP6	0x00	0x00
0x126	OPT_FLT_RESP7	0x00	0x00
0x127	OPT_FLT_RESP8	0x00	0x00
0x128	OPT_FLT_SHDN1	0x00	0x00
0x129	OPT_FLT_SHDN2	0x00	0x00
0x140	OPT_INTB_MASK1	0x00	0x00
0x141	OPT_INTB_MASK2	0x00	0x00
0x142	OPT_INTB_MASK3	0x00	0x00
0x143	OPT_INTB_MASK4	0x00	0x00
0x148	OPT_SSPB_MASK1	0x00	0x00
0x149	OPT_SSPB_MASK2	0x00	0x00
0x14A	OPT_SSPB_MASK3	0x00	0x00
0x14D	OPT_SSPB_MASK5	0x00	0x00
0x150	OPT_VOUT	0x2C	0x38
0x151	OPT_FB1_THRESH	0x00	0x00
0x152	OPT_FB2_THRESH	0x00	0x00
0x153	OPT_LDO1_THRESH	0x00	0x00
0x154	OPT_LDO2_THRESH	0x00	0x00
0x155	OPT_LDO3_THRESH	0x00	0x00
0x156	OPT_LDO4_THRESH	0x00	0x00
0x157	OPT_COREMON_THRESH	0x00	0x00
0x158	OPT_LDO0_THRESH	0x00	0x00
0x160	OPT_FAULT_DLY1	0x00	0x00
0x161	OPT_FAULT_DLY2	0x00	0x00
0x162	OPT_FAULT_DLY3	0x00	0x00
0x163	OPT_FAULT_DLY4	0x00	0x00
0x164	OPT_FAULT_DLY5	0x00	0x00
0x200	OPT_DEV_MODE1	0x30	0x00
0x201	OPT_DEV_MODE2	0x10	0x10
0x202	OPT_DEV_MODE3	0x00	0x00

Table 7. OTP Configuration in Example1/2 (Cont.)

Address	Register Name	OTP Value Example1	OTP Value Example2
0x203	SEL_DEV_MODE1	0x11	0x00
0x204	OPT_WAIT_DISCHG1	0x00	0x00
0x205	OPT_WAIT_DISCHG2	0x00	0x00
0x206	OPT_PD_CTRL	0x00	0x00
0x207	OPT_STATE_CTRL	0x00	0x00
0x208	OPT_SS	0x00	0x00
0x209	OPT_WDENB_CTRL	0x00	0x00
0x20B	OPT_PG_CTRL	0x00	0x00
0x20C	OPT_AMUX_BUF_OFFSET	0x00	0x00
0x20D	OPT_CALIB_OSC32K	0x00	0x00
0x20E	OPT_VDDIO	0x01	0x02
0x3C1	OTP ID1	0x21	0x22
0x3D0	OTP ID2	0x00	0x00

7. Revision History

Revision	Date	Description
1.00	Aug 26, 2024	Initial release.

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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