RA6M5 MCU Group

Security Manual

Introduction

The RA6M5 MCU Group incorporates many features that can be used to protect the content and operation of the MCU when it is integrated into an end product. This document describes these features and provides general recommendations for their use. Associated application notes and other applicable documents that provide more details are listed for reference.

Since the RA6M5 is a general-purpose MCU, this Security Manual cannot provide specific guidance for all possible use cases, nor can it offer system-level security recommendations. It is highly recommended that the application developer conduct a security analysis of the system into which the RA6M5 is integrated and create a threat model and security policy for the system and for the RA6M5, for example, using the ISO/SAE 21434 Threat Analysis and Risk Assessment (TARA) approach. It is the application developer's responsibility to decide what RA6M5 security features are necessary for the end product and to implement them appropriately.

Although this Security Manual describes the best secure practices for configuring the RA6M5 at the time of its release, the microcontroller threat landscape is constantly changing and evolving. Please refer to the notice at the end of this document.

Contents

1. Introduction

1.1 Overview

This application note describes the security-related features of the RA6M5 MCU Group and guides how to utilize these features to create a product with the appropriate level of cybersecurity, tailored to the threat model for the intended application.

NOTE: Ultimately, it is up to the discretion of the application developer to determine how to design the security architecture of the end product and what security features to employ. Critical items related to the proper functioning of the MCU and potential security threats are highlighted in red sections.

1.2 Security Features

The RA6M5 MCU provides the following security-related features:

- MCU product and chip-unique identification
- Hardware-enforced isolation using Arm® TrustZone® technology
- The SCE9 integrated security engine, providing cryptographic functions and secure key handling
- Immutable memory
- Various tamper detection features
- Device Lifecycle Management and authenticated debug

The RA Flexible Software Package (FSP) is the Renesas software platform available for use with the RA6M5 MCU Group. The FSP provides support for security solutions that are often required to secure an end-product, including:

- Creation of a cryptographic identity
- Secure boot
- Secure firmware updates
- Secure internet connectivity

1.3 References

The following documents are referenced in this application note. These documents are available from the Renesas website www.renesas.com.

Reference	Document Name	Document Number or URL
[RA6M5 User Manual]	RA6M5 Group User's Manual: Hardware	R01UH0891
[SCE_TADI TU]	Technical Update, Update of Secure Cryptographic Engine Event	TN-RA*-A0153A/E
[FSP User Manual]	RA Flexible Software Package Documentation	RA Flexible Software Package Documentation: Introduction (renesas.github.io)
[Boot Firmware]	Standard Boot Firmware for the RA Family MCUs Based on Arm® Cortex®-M33	R01AN5562
[SP800-22 Test Report]	NIST SP800-22r1a Random Number Statistical Test Report for RA6M5	R01AN6186EU0100
[SP800-90B Test Report]	NIST SP800-90B Entropy Assessment Report for RA6M5	R01AN6821EU0100

1.4 Additional Guidance Documentation

The following additional guidance documents are referenced in this application note. Please note that due to documentation update cycles, the RA6M5 MCU Group may not be explicitly referenced in the latest version of these documents. These documents are available from the Renesas website, www.renesas.com.

Reference	Document Name	Document Number
[Bootloader Basic]	RA6 Basic Secure Bootloader Using MCUboot and Internal Code Flash	R11AN0497
[Bootloader Dual Bank]	RA6 MCU Advanced Secure Bootloader Design using MCUboot and Code Flash Dualbank	R11AN0570
[Cloud Connectivity]	RA AWS MQTT/TLS Cloud Connectivity Solution - Ethernet	R11AN0605
[Cloud OTA]	RA AWS Cloud Connectivity and Firmware Update OTA on CK-RA6M5 v2 with Ethernet	R11AN0915
[Bootloader Encrypted]	RA6 Booting Encrypted Image using MCUboot and QSPI	R11AN0567
[Design with TrustZone]	Security Design with Arm TrustZone	R11AN0467
[Device Identity]	Device Identity with SCE9 and TrustZone	R11AN0475
[DLM]	Renesas RA Family Device Lifecycle Management for Cortex-M33	R11AN0469
[Plaintext Key Injection]	Injecting Plaintext User Keys	R11AN0473
[RA Tooling Primer]	RA Arm® TrustZone® Tooling Primer	R20AN0577
[SCE Modes]	Renesas Security Engine Operational Modes	R11AN0498
[Secure Key Injection]	Injection and Updating Secure User Keys for RA Family	R11AN0496

1.5 Development Tools

Renesas provides the following tools to support the development of security solutions.

Reference	Name	URL
[FSP]	Flexible Software Package (FSP) for Renesas RA MCU Family with e^2 studio IDE	www.renesas.com/fsp
[RASC]	RA Smart Configurator	www.renesas.com/fsp
[RFP]	Renesas Flash Programmer	https://www.renesas.com/software-tool/renesas-flash-programmer-programming-gui
[SKMT]	Security Key Management Tool	https://www.renesas.com/software-tool/security-key-management-tool

1.6 Abbreviations and Legend

The following abbreviations are used in this document.

Abbreviation	Meaning
BSP	Board Support Package
CAC	Clock Frequency Accuracy Measurement Circuit
DLM	Device Lifecycle Management
DPL	Deployed
ECC	Elliptic Curve Cryptography
ECDH/ECDHE	Elliptic Curve Diffie Hellman (Ephemeral)
FSP	Flexible Software Package

HRK	Hardware Root Key
HUK	Hardware Unique Key
IDAU	Implementation Defined Attribution Unit
IDE	Interactive Development Environment
ISR	Interrupt Service Routine
KAS	Key Agreement Scheme
KUK	Key-Update Key
LCK_BOOT	Lock Factory Bootloader
LCK_DBG	Lock Debugger
LVD	Low Voltage Detection
MAC	Message Authentication Code
MPU	Memory Protection Unit
NSECDBG_KEY	Non-secure Debug Key
NSECSD	Non-secure System Debug
RASC	RA Smart Configurator
RMA_KEY	Return Material Authorisation Key
RFP	Renesas Flash Programmer
SCE	Renesas Secure IP
RTC	Realtime Clock
SECDBG_KEY	Secure Debug Key
SSD	Secure System Debug
SKMT	Security Key Management Tool
TRNG	True Random Number Generator
TSN	Temperature Sensor
UFPK	User Factory Programming Key
W-UFPK	Wrapped User Factory Programming Key

The following figure illustrates the concepts presented in this document.

Symbol	Meaning
	A cryptographic key (plaintext)
	A cryptographic key encrypted by another key (inner key encrypted by the outer key)
	A cryptographic key wrapped (encrypted plus MAC) by another key (inner key wrapped by the outer key)

Figure 1. Graphical Representations of Cryptographic Keys

1.7 Software Platform

The RA Flexible Software Package (FSP) is a software package provided by Renesas for developing applications on RA Family MCUs. The FSP offers Board Support Packages, HAL drivers, and middleware for RA Family MCUs.

The FSP Platform Installer includes the e² studio IDE, toolchain, and FSP packs. Alternatively, the FSP Standalone Installer, along with the RA Smart Configurator, can be used with the IAR Embedded Workbench IDE or Arm Keil MDK.

These installers, plus additional information, can be found at www.renesas.com/fsp.

1.8 Vulnerability Reporting

Renesas is committed to proactively addressing any potential security vulnerabilities within our products. To report a security vulnerability, please visit www.renesas.com/psirt and follow the instructions on the webpage.

2. Identity

2.1 MCU Group Identity

The RA6M5 MCU Group chips contain a 16-byte read-only register that includes an immutable ASCII representation of the device part number. The PNRn Part Numbering Registers are documented in the [RA6M5 User Manual], including a part number listing.

This value can be obtained by using the FSP function `R_BSP_PartNumberGet()`.

For more details, refer to the following document:

- [RA6M5 User Manual]

2.2 Unique Identity

The RA6M5 MCU Group chips contain a 16-byte read-only register that includes an immutable 16-byte ID code (unique ID) for identifying the individual MCU. The UIDRn Unique ID Registers are documented in the [RA6M5 User Manual].

This value is guaranteed to be unique. It is serialised and therefore predictable, so it should not be used for identifying the end-product if a random or pseudorandom identifier is required.

This value can be obtained by using the FSP function `R_BSP_UniqueIdGet()`.

For more details, refer to the following document:

- [RA6M5 User Manual]

2.3 Cryptographic Identity

The RA6M5 MCU is not delivered with a provisioned cryptographic identity. The SCE9 security engine can be used to create an ECC (secp256r1 or secp384r1) or RSA (2048-bit) cryptographic identity by using the key (pair) generation capability of the security engine, which is statistically unique based on the SP800-90B conformance of the TRNG.

For more details, refer to the following documents and sections of this document:

- [RA6M5 User Manual]
- [FSP User Manual]
- [Device Identity]
- Section 5 SCE9 Cryptographic Functions
- Section 6 SCE9 Random Number Generation

3. Isolation

3.1 Arm® TrustZone®

The RA6M5 includes Arm TrustZone technology. TrustZone divides the system and the application into Secure and Non-secure domains. This separation applies to:

- On-chip flash memory (i.e., code flash)
- SRAM
- Peripherals
- Pins

For best security design practices, external memory should always be considered Non-secure.

The Secure, Non-secure Callable, and Non-secure regions of on-chip code flash and SRAM are enforced using an IDAU (Implementation-Defined Attribution Unit). The address range boundaries for flash and SRAM are programmed in non-volatile flash and applied before the reset vector is fetched. This ensures that malicious code cannot override the boundaries. These values are calculated automatically by the e^2 studio IDE when the application code is built, and by default, they are programmed at the start of a debug session. If necessary, these calculated values can be adjusted before being programmed and programmed independently of the debug session.

The security configuration of pins and peripherals is done using Peripheral Security Attribution Registers. The FSP's Board Support Package start-up code will initialize these attribution registers for the pins and peripherals according to the configuration set in the application project, using either the e^2 studio IDE or the RA Smart Configurator (RASC).

The system starts up in the Secure state. The application performs any secure initialization, such as firmware authentication, and then jumps to the Non-secure region for main application processing. Execution of Non-secure region code is then governed by TrustZone usage restrictions, which require all calls to Secure region code to utilize Non-secure Callable veneers. These veneers and accompanying guard functions can be configured with the e^2 studio IDE.

TrustZone access violations will generate a TrustZone access error. The application can optionally alert and/or record these events for logging unauthorized access attempts.

TrustZone usage is not mandatory. It is the responsibility of the application developer to assess the security risks of a monolithic architecture, determine whether to utilize TrustZone as an isolation mechanism, and identify which services and peripherals to place in the Secure region. The referenced documents below provide examples of how TrustZone can be utilized in an application.

For production programming, ensure that the TrustZone boundaries are accurately programmed. This must be done for all applications, even if TrustZone is not utilized by the application.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [RA Tooling Primer]
- [Design with TrustZone]

3.2 Memory Protection Unit (MPU)

The RA6M5 MCU Group features an Arm Cortex-M33 core, an Arm MPU, and a Bus Master MPU.

The Arm MPU can be used to protect memory regions by defining access permissions for different privilege states. See the Arm Developer documentation for more information about how to use the Arm MPU: Armv8-M Memory Model and Memory Protection User Guide.

The Arm Bus Master MPU provides memory protection for bus masters other than the CPU, namely DMAC/DTC. If access to a protected region is detected, the Bus Master MPU generates an internal reset or a non-maskable interrupt.

For more details, refer to the following documents:

- [RA6M5 User Manual]

3.3 SCE9

The SCE9 security engine is a cryptographic subsystem that is integrated into the MCU silicon, managed and protected by dedicated control logic. The cryptographic operations are physically isolated from the rest of the chip, with dedicated RAM for holding sensitive material (i.e., plaintext keys) during cryptographic operations. SCE9 is further protected with TrustZone isolation technology.

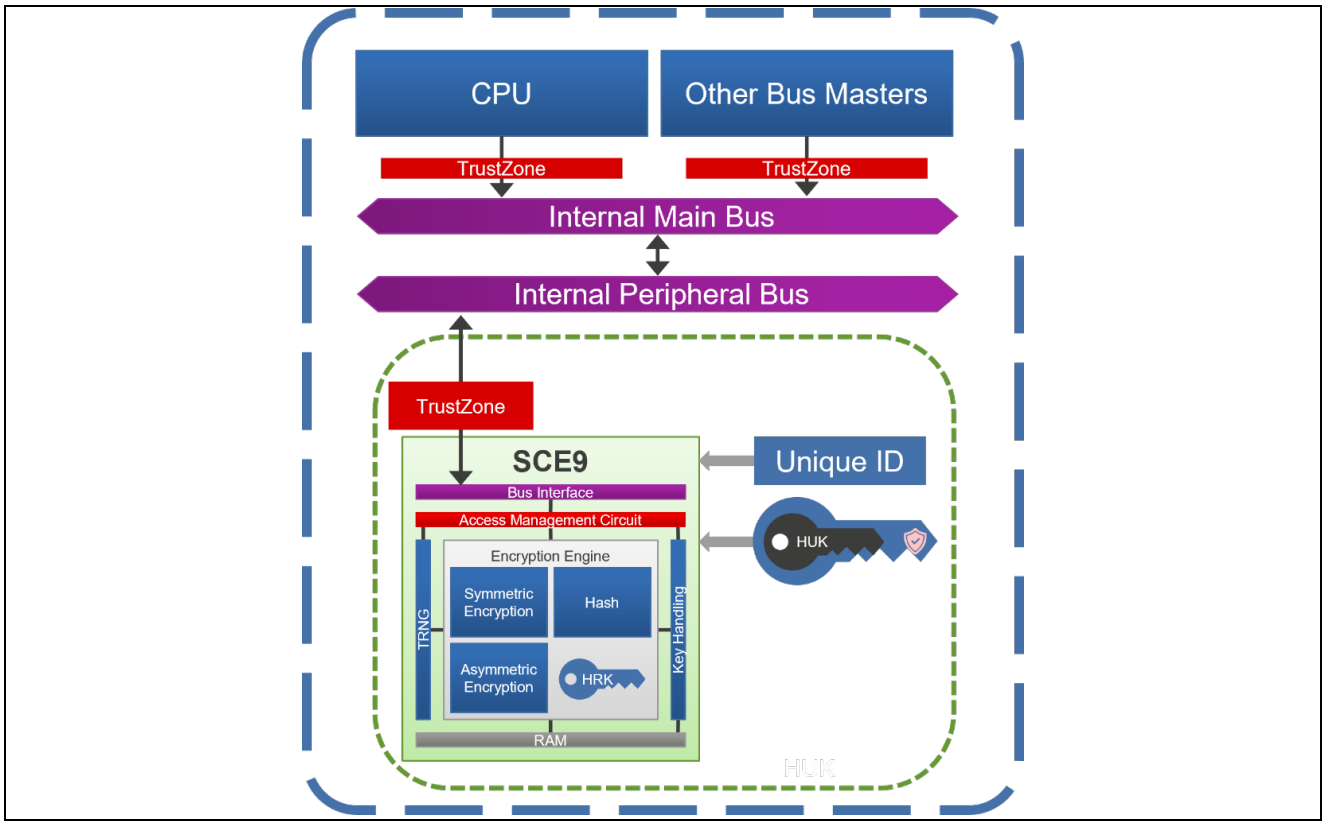

Figure 2. SCE9 On-chip Isolation

For more details, refer to the following documents and sections of this document:

- [RA6M5 User Manual]
- [SCE Modes]
- Section 4 SCE9 Secure Key Injection, Storage, and Usage
- Section 5 SCE9 Cryptographic Functions
- Section 8.2 SCE9 Protection Features

4. SCE9 Secure Key Injection, Storage, and Usage

4.1 SCE9 Operational Modes

The SCE9 can function in two operational modes: Protected mode and Compatibility Mode. These modes are supported by various APIs, offering different levels of physical key protection.

The secure key storage mechanism differs between the two modes, resulting in incompatible, securely stored keys. Therefore, the Flexible Software Package supports using **only one operational mode within a single project**. Note that applications that utilize a bootloader are implemented with a separate project for the bootloader, enabling Protected Mode use by the bootloader and Compatibility Mode use by the rest of the application.

For more details, refer to the following documents and sections of this document:

- [SCE Modes]
- [FSP User Manual]
- Section 8.2 SCE9 Protection Features

4.1.1 SCE9 Protected Mode Operation

Protected Mode is designed to enforce best practice security design and implementation by supporting only the use of securely stored (i.e., wrapped) private keys. As such, the application can guarantee that there is no exposure of plaintext private keys on any CPU or externally accessible bus.

Both private and public keys must be securely injected. During the injection process, a MAC is appended to the key data. For most cryptography operations, this MAC is required; the only exception is for public keys used in Key Agreement Schemes (KAS) supporting ECDH/ECDHE.

Protected Mode is utilized via the FSP Crypto APIs, which are designed to be compatible across Renesas' RA, RX, and RZ families, facilitating simplified code reuse.

Refer to section 8.2 SCE9 Protection Features for more information about the protection features included in Protected Mode operation.

4.1.2 SCE9 Compatibility Mode Operation

Compatibility Mode is designed to facilitate integration with legacy systems and software while still supporting secure key injection, storage, and usage. In Compatibility Mode, plaintext private keys can be used for cryptographic functions, simplifying integration with third-party stacks and libraries.

Compatibility Mode is utilized through the PSA Certified Crypto APIs, ensuring alignment with the Arm ecosystem.

Refer to section 8.2 SCE9 Protection Features for more information about the protection features included in Compatibility Mode operation.

Since plaintext key material can be present and used in the application, it is essential that the developer evaluates and accepts any associated risks.

For security best practices, private keys that are stored in non-volatile memory should be stored securely, as explained in section 4.3 Secure and Plaintext Key Injection and Update. Depending on the threat model, it may be acceptable to store session keys in plaintext in RAM.

Plaintext private keys should be protected via other key protection mechanisms, such as isolation in the Secure region.

4.2 Secure Key Storage

The secure key storage mechanism utilizes the chip's Hardware Unique Key, a 256-bit key that is unique to each chip and accessible only by the SCE9 security engine. Application keys that have been wrapped with this key via a key injection or key update process can be stored securely at any location in any memory. This mechanism provides unlimited secure key storage and cloning protection.

For additional protection, it is recommended to store wrapped keys in the Secure region if the application utilizes TrustZone.

Keys that have been generated, injected, or updated in Protected Mode cannot be used in Compatibility Mode, and vice versa.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]
- [Secure Key Injection]
- [Plaintext Key Injection]

4.3 Secure and Plaintext Key Injection and Update

The secure key injection process leverages the MCU's hardware root key, a key that is contained within the SCE9 security engine and is common across all chips. This key is used only for the secure key injection process. It is not used for secure storage of application keys, and it is not accessible outside the security engine.

There are some differences between Protected Mode and Compatibility Mode, but the basic concept for secure key injection is the same for both modes.

Keys that have been generated, injected, or updated in Protected Mode cannot be used in Compatibility Mode, and vice versa.

To protect both the Renesas MCU Hardware Root Key and the developer's application keys, no sensitive key material is transferred between Renesas and the application developer. Instead, as shown in Figure 3. Secure Key Injection, the developer creates an intermediary key called a User Factory Programming Key (UFPK). This key is PGP-encrypted and sent to the Renesas Key Wrap Service, an automated secure server that wraps the UFPK (creating a W-UFPK), PGP-encrypts it, and returns it to the developer.

A non-trivial key that is not duplicated from Renesas examples or other publicly available cryptography references must be used for the UFPK.

Application keys are injected by providing both the W-UFPK and the UFPK-encrypted application key(s) to the SCE9. The security engine unwraps the W-UFPK to obtain the UFPK, then decrypts the encrypted application key. It then wraps the application key with the MCU's HUK. Figure 3. Secure Key Injection shows an overview of this process.

Key preparation steps where keys are exposed in plaintext must be performed in a secure environment.

It is recommended to use different UFPKs for prototype development with test keys and for production programming of mass production keys.

The RA6M5 cannot be personalized to accept only specific W-UPFKs for application key injection; therefore, the production programming flow must protect against malicious key injection. To guard against supply chain attacks, it is recommended to issue the “Initialize” boot firmware command to erase the chip before key injection.

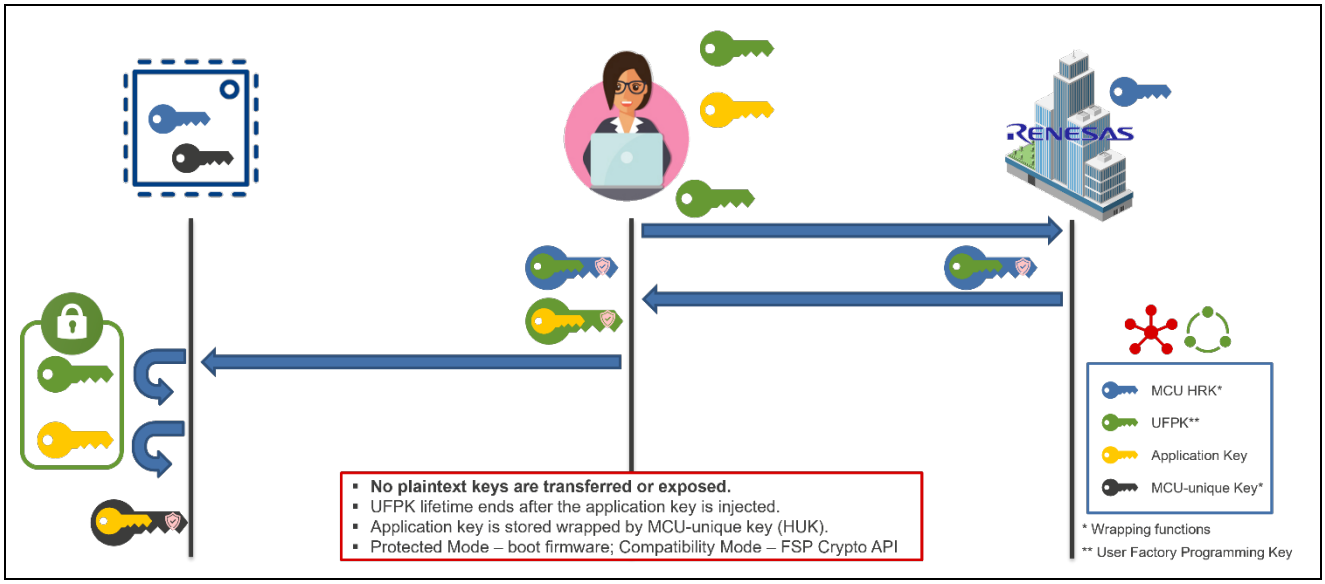

Figure 3. Secure Key Injection

On the RA6M5, Protected Mode secure key injection is performed using the factory boot firmware, and Compatibility Mode secure key injection is performed using APIs contained in the FSP.

Renesas provides the following tools to support this process:

- Security Key Management Tool (SKMT), available here: https://www.renesas.com/software-tool/security-key-management-tool. This tool can create sample keys and prepare keys for secure key injection and secure key update.
- Renesas Flash Programmer (RFP), available here: https://www.renesas.com/software-tool/renesas-flash-programmer-programming-gui. This tool can securely inject Protected Mode keys using the MCU’s factory boot firmware.

Select third-party programming tools also support secure key injection.

Plaintext key injection is supported only by Compatibility Mode and is performed using APIs contained in the FSP.

The following sections provide more details about the secure and plaintext key injection and update processes.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]
- [Boot Firmware]
- [SCE Modes]
- [Secure Key Injection]
- [Plaintext Key Injection]
- [SKMT]
- [RFP]

4.3.1 SCE9 Protected Mode Key Injection

Keys used with Protected Mode must be securely injected or securely updated. The wrapped keys can then be used with the FSP Crypto APIs.

Secure key injection is performed using the programming interface and the MCU's factory boot firmware. As shown in Figure 4. Protected Mode Secure Key Injection, the W-UFPK and encrypted application key are both provided to the MCU using the appropriate factory boot firmware command. The factory boot firmware uses the security engine to decrypt the application key and wrap it with the MCU's HUK. The boot firmware then stores the key at the designated location in memory.

Keys injected via this mechanism cannot be used with the PSA Certified Crypto APIs, which use SCE9 in Compatibility Mode.

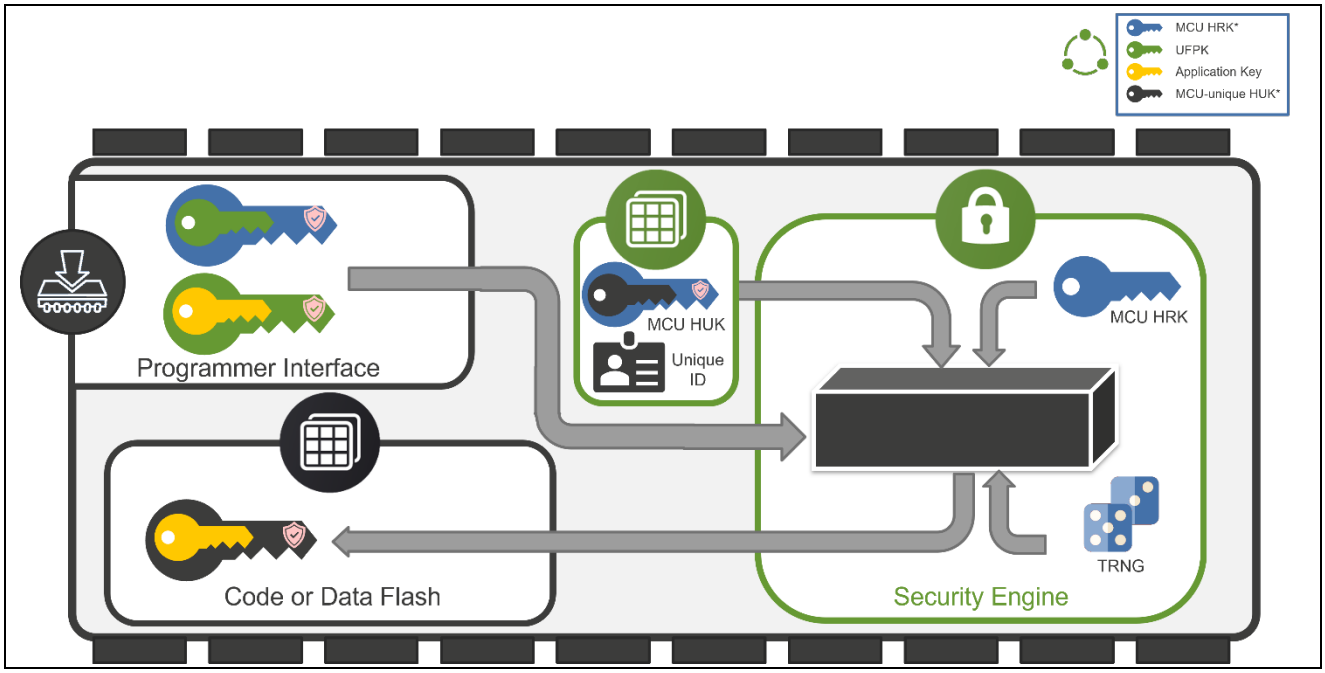

Figure 4. Protected Mode Secure Key Injection

The production programming flow should be designed such that the programming interface is locked after secure key injection to prevent malicious key injection.

After the programming interface is locked (see section 12.1 Device Lifecycle Management and Debug Authentication), application keys can no longer be injected. Instead, the application must be updated with new keys via Key-Update Keys (KUKs).

During initial provisioning, an application should be provisioned with one or more KUKs. As shown in Figure 5. Key-Update Key Injection, Key-Update Key injection functions identically to application key injection.

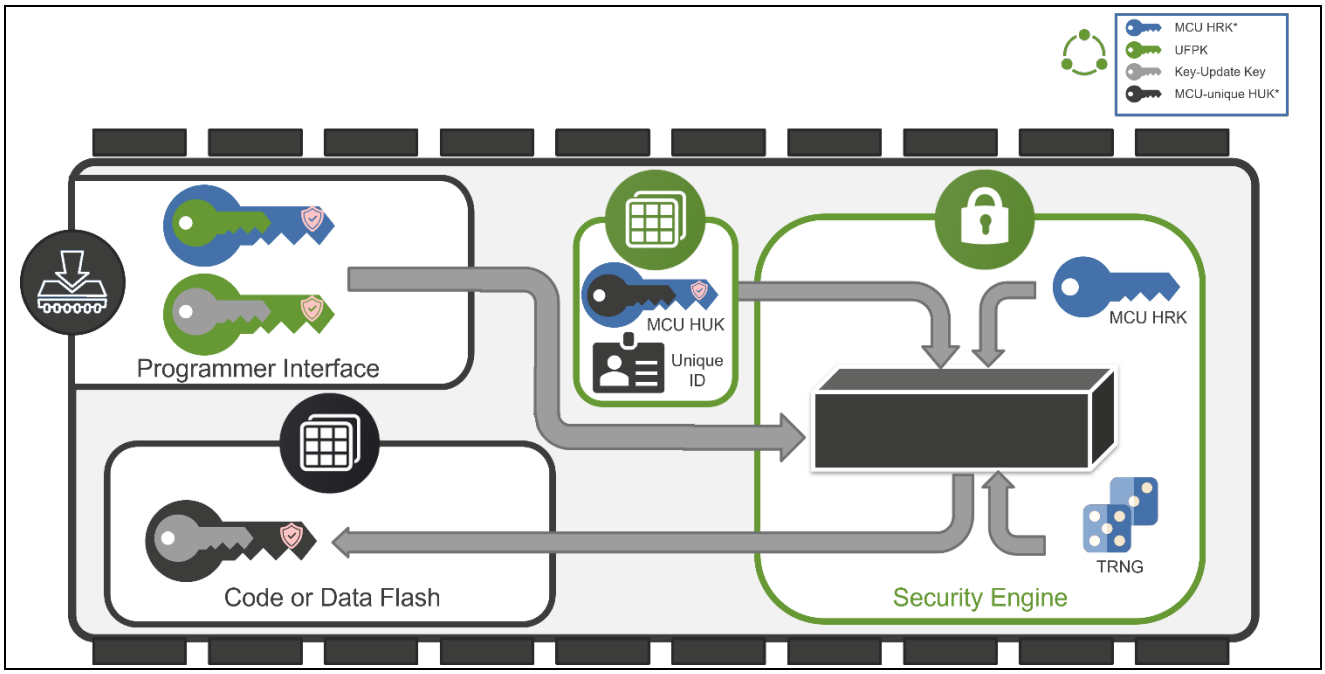

Figure 5. Key-Update Key Injection

To update an application key, the new application key must be wrapped with the Key-Update Key. The application code then uses the appropriate FSP Crypto API to update the specific key type of the new application key. As shown in Figure 6. Protected Mode Key Update, this enables secure key update, with no plaintext key exposure outside the security engine.

Keys updated via this mechanism cannot be used with the PSA Certified Crypto APIs, which use SCE9 in Compatibility Mode.

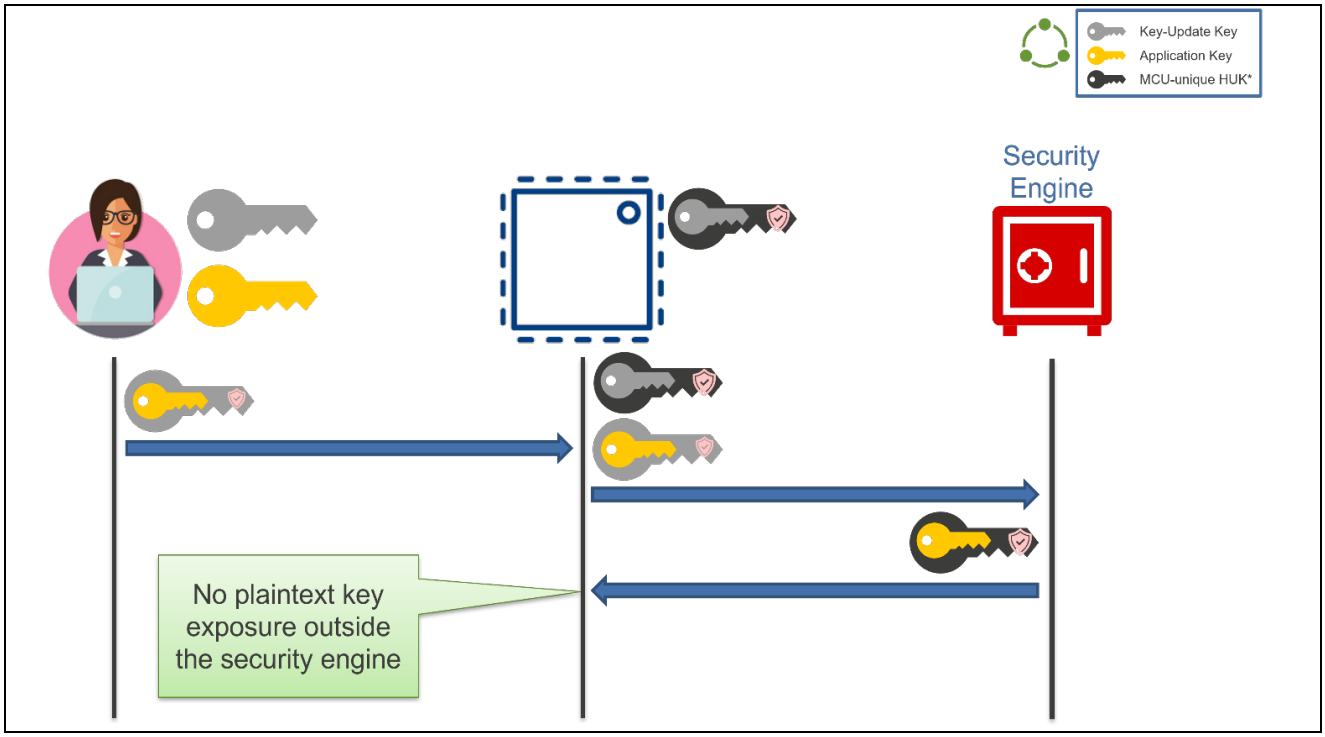

Figure 6. Protected Mode Key Update

4.3.2 SCE9 Compatibility Mode Key Injection

Keys used with Compatibility Mode must use the FSP Key Injection module and be either securely injected or injected as plaintext. The wrapped keys can then be used with the PSA Certified Crypto APIs.

Keys injected via this mechanism cannot be used with the FSP Crypto APIs, which use SCE9 in Protected Mode.

Secure key injection is performed using the FSP Key Injection module. As shown in Figure 7. Compatibility Mode Secure Key Injection, the W-UFPK and encrypted application key are both provided to the API. The SCE driver uses the security engine to decrypt the application key and wrap it with the MCU's HUK. The application code must then store the key at a designated location in memory.

It is recommended not to include either secure key injection API code or any W-UFPKs in end-product firmware. This can be done by utilizing a programming tool that executes the secure key injection code from the MCU RAM or by erasing the flash memory that contains the secure key injection code.

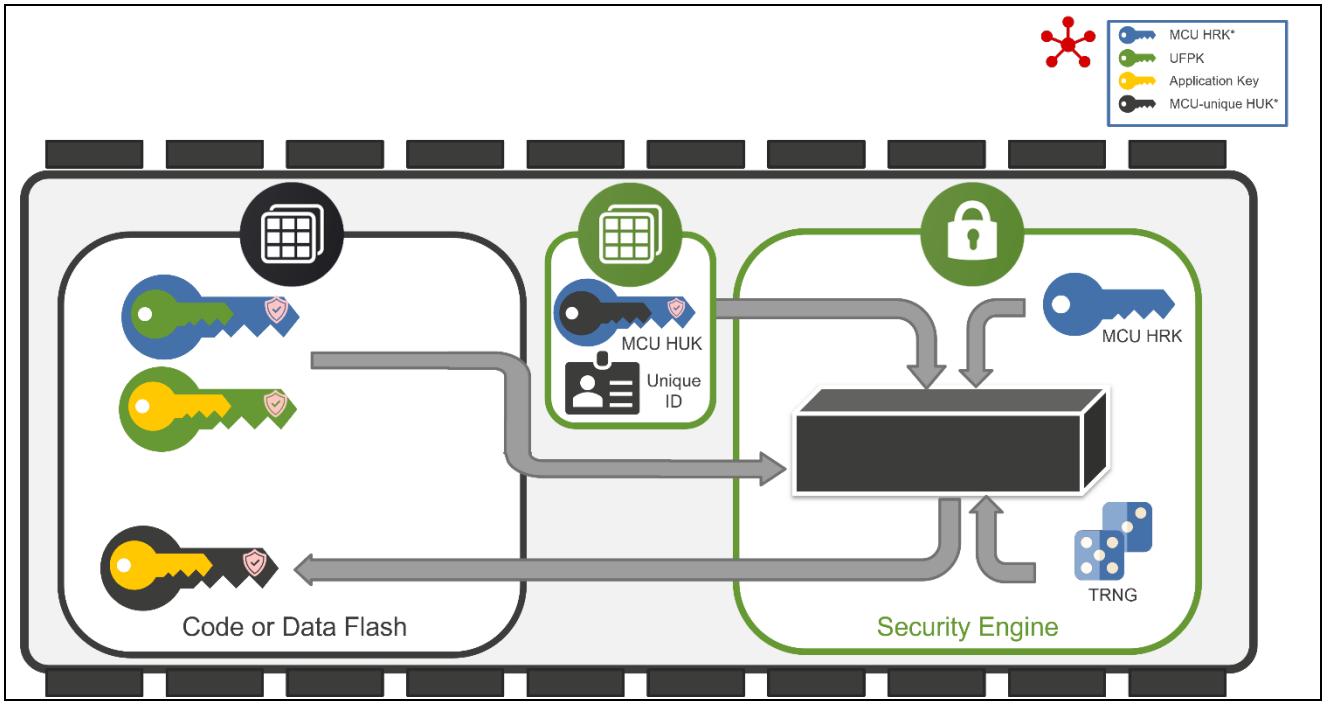

Figure 7. Compatibility Mode Secure Key Injection

Plaintext key injection is also performed using the FSP Key Injection module. As shown in Figure 8. Compatibility Mode Plaintext Key Injection, the plaintext application key is provided to the API. The SCE driver utilizes the security engine to encrypt the plaintext key using the MCU's HUK. The application code must then store the wrapped key at a designated location in memory.

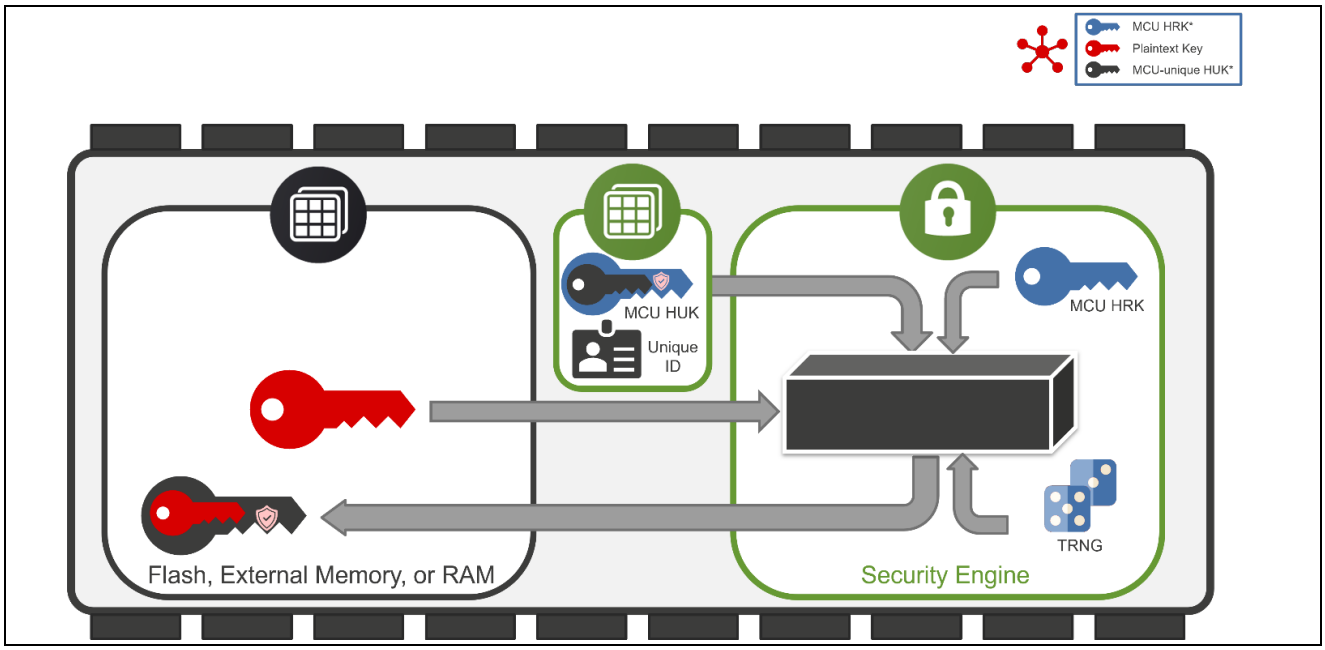

Figure 8. Compatibility Mode Plaintext Key Injection

There is no explicit support in Compatibility Mode for Key Update. It is recommended to securely inject one or more keys that will serve as Key-Update Keys and manually perform the decryption and plaintext key injection of the new key. See Figure 9. Compatibility Mode Key Update for an overview of this process.

Since plaintext key exposure occurs outside the security engine, it is recommended to perform the entire key update operation in the Secure region.

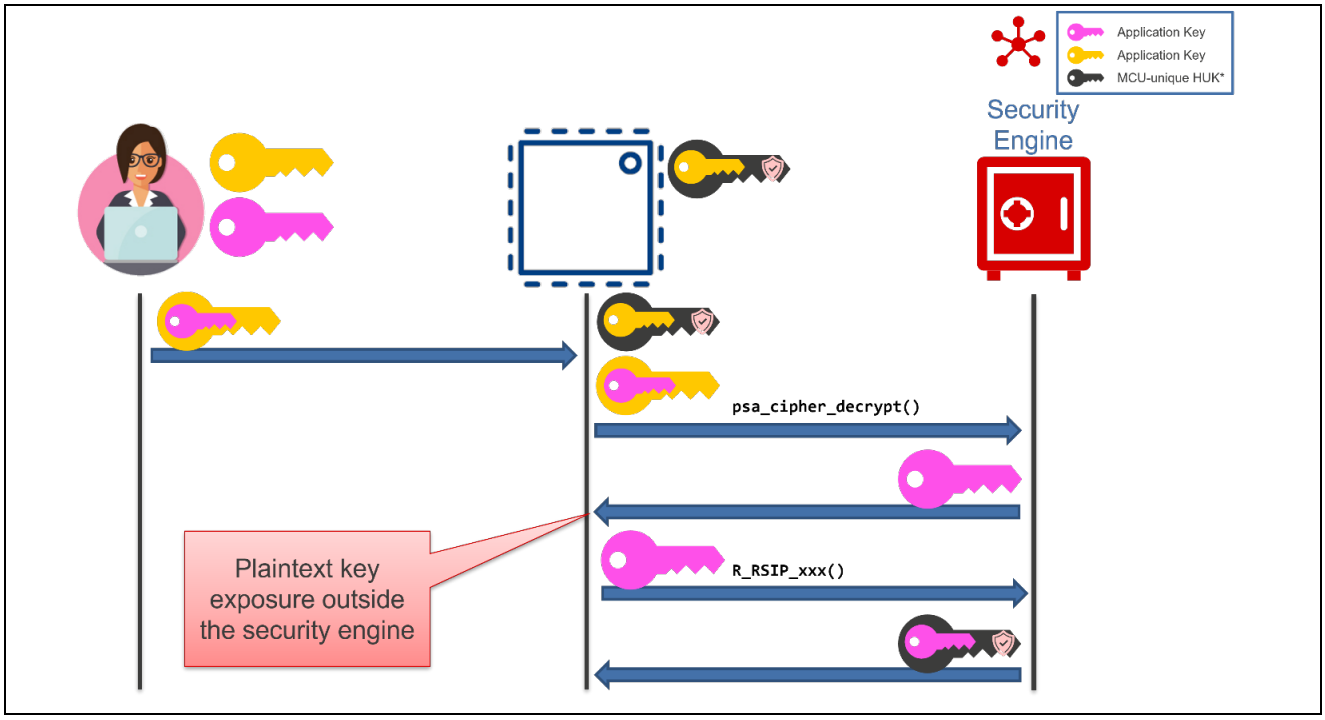

Figure 9. Compatibility Mode Key Update

5. SCE9 Cryptographic Functions and Key Generation

The SCE9 security engine provides hardware acceleration for basic cryptographic functions. The FSP Crypto APIs (Protected Mode) and PSA Certified Crypto APIs (Compatibility Mode) provide any needed software support.

Table 1 SCE9 Cryptographic Operations lists the cryptographic algorithms supported by the security engine.
Table 2 SCE9 Key Generation lists the cryptographic key generation supported by the security engine.

The application code should utilize cryptographic algorithms with sufficient strength, as appropriate to the application's threat model.

Table 1 SCE9 Cryptographic Operations

Algorithm	Operations	Specification	Key lengths	Modes
AES	Encryption, decryption, and MAC	NIST FIPS PUB 197 NIST SP800-38A (ECB, CBC, CTR) NIST SP800-38B (CMAC) NIST SP800-38C (CCM) NIST SP800-38D (GCM, GMAC)	128 and 256 bits	ECB, CBC, CTR, CCM, GCM, CMAC, GMAC
ECC	Signature generation, signature verification	NIST FIPS PUB 186-5	Curves: NIST P-256, NIST P-384; Brainpool P256r1, P384r1	N/A
RSA	Signature generation, signature verification, encryption, decryption	IETF RFC 8017 FIPS PUB 186-5	2048 bits	N/A
RSA	Signature verification, encryption	IETF RFC 8017 FIPS PUB 186-5	3072 and 4096 bits	N/A
HMAC	Keyed Hash	NIST FIPS PUB 198-1	256 bits	SHA-256
KDF	Key Agreement	NIST SP 800-56A	128 and 256 bits	SHA-256
Key Wrapping	Wrap/Unwrap	RFC3394	128 and 256 bits	N/A
SHA	Hash	NIST FIPS PUB 180-4	N/A	SHA-224, SHA-256

Table 2 SCE9 Key Generation

Algorithm	Specification	Key lengths
AES	NIST FIPS PUB 197	128 and 256 bits
ECC – SEC prime curves	FIPS PUB 186-5	256 and 384 bits
ECC – Brainpool prime curves	RFC5639	256 and 384 bits
RSA	IETF RFC 8017	2048 bits

For more details, refer to the following document:

- [RA6M5 User Manual]

6. SCE9 Random Number Generation

The RA6M5 MCU Group implements random number generation by utilizing the True Random Number generation capability of the SCE9 security engine. The TRNG implementation consists of an SP800-90A compliant DRBG that is fed by an SP800-90B compliant seed, which is generated from an entropy source. Each TRNG request generates a 128-bit random number.

This feature has passed internal testing for both SP800-22 and SP800-90B compliance (see [SP800-22 Test Report] and [SP800-90B Test Report]).

The TRNG is initially seeded by calling the APIs to initialize the security engine:

- Protected Mode: `R_SCE_Open()`
- Compatibility Mode: `mbedtls_platform_setup()`

Periodic reseeding of the TRNG is typically recommended for most applications that utilize a TRNG. Reseeding the TRNG can be performed as follows:

The reseeding interval for Protected Mode must be manually implemented by the application code. The application code must call `R_SCE_Close()` followed by `R_SCE_Open()` to reseed the TRNG.

The reseeding interval for Compatibility Mode is configured by defining the macro `MBEDTLS_CTR_DRBG_RESEED_INTERVAL` and setting it to the number of calls to psa_generate_random() that can be made before reseeding is required. The macro can be defined and set using either the e^2 studio IDE or the RA Smart Configurator (*MbedTLS (Crypto Only) module* > *RNG*). Reseeding will occur automatically if needed when `psa_generate_random()` is called.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [SP800-22 Test Report]
- [SP800-90B Test Report]

7. Immutable Memory

The code flash blocks of the MCU can be configured to be immutable. This property is commonly used to protect critical assets that define the device's identity and control access to the device through a secure firmware update mechanism. Refer to the [RA6M5 User Manual] for the sizes and addresses of the MCU's code flash blocks.

An application that intends to be configured with immutable flash blocks can be prototyped by using the Block Protect Setting Register (BPS) and the Bank Select Register Secure (BPS_SEC) to temporarily configure the blocks as read-only. These settings can be modified using either self-programming or issuing the "Initialize" boot firmware command.

Production programming of the end-product should also use the equivalent bits in the Permanent Block Protect Setting Register (PBPS) and the Permanent Block Protect Setting Register Secure (PBPS_SEC) to make these blocks permanently immutable. Any programming of the PBPS or PBPS_SEC bits from 1 to 0 is permanent, and the chip can no longer be erased using the "Initialize" boot firmware command.

The BPS, BPS_SEC, PBPS, and PBPS_SEC registers can be set using the FSP Configurator in the e^2 studio IDE or the RA Smart Configurator.

The code flash blocks that contain the Root of Trust should be made immutable. The immutable Root of Trust contains items such as a secure boot solution, root keys, and certificates.

If a chip is returned to Renesas for failure analysis, the DLM state transition to RMA_REQ (Return Material Authorization Request) will not erase any blocks that have their associated PBPS or PBPS_SEC bit set. Information in these blocks will be visible to Renesas during the RMA process.

The Protection Programming Flag (FSPR) bit is used to prevent modification of the startup area selection and to disallow the “Chip Erase” command. Any programming of the FSPR bit from 1 to 0 is permanent, and the chip can no longer be erased using the “Initialize” boot firmware command.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]

8. Tamper Protection

8.1 Passive Tamper Detection

Passive tamper detection is provided by the Realtime Clock (RTC) peripheral of the MCU. The RTC can be configured such that a change on one of the input capture pins, RTCICn, triggers a capture of the current RTC value (i.e., the current time) and an optional interrupt. The captured value is retained after reset.

Refer to the detailed description of this peripheral and its associated electrical characteristics as stated in the [RA6M5 User Manual] for the requirements and limitations of this hardware feature.

Figure 10. Passive Tamper Detect shows the passive tamper components included in the RTC.

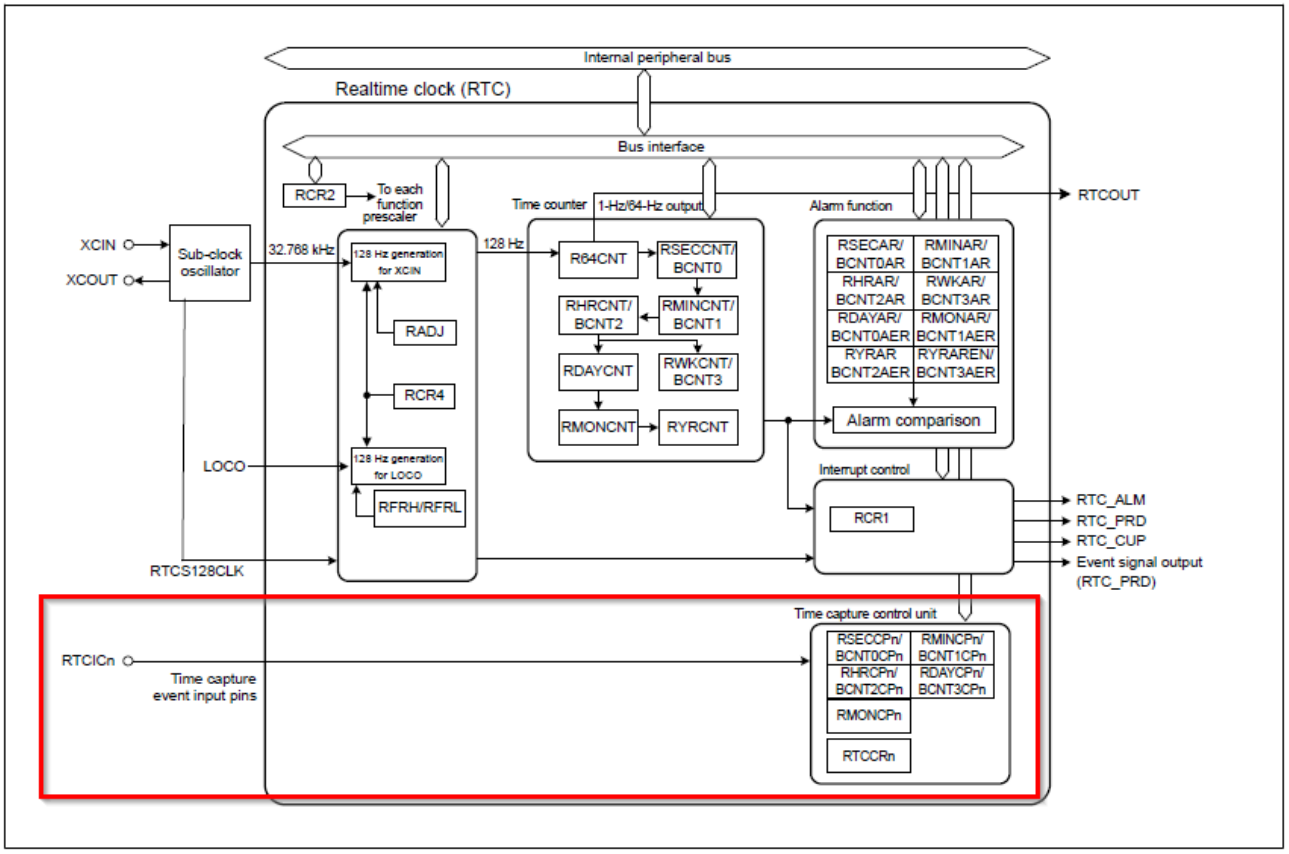

Figure 10. Passive Tamper Detect

Use of the passive tamper detection feature is application-specific and dependent on the end product’s threat model. A typical use of passive tamper detection is to detect breaches in the enclosure that would grant an attacker physical access to a sensitive area of the end product.

It is recommended to place the code that interacts with this peripheral in the Secure region if the application utilizes TrustZone.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]

8.2 SCE9 Protection Features

SCE9 includes protection features designed to safeguard key material against physical and logical attacks.

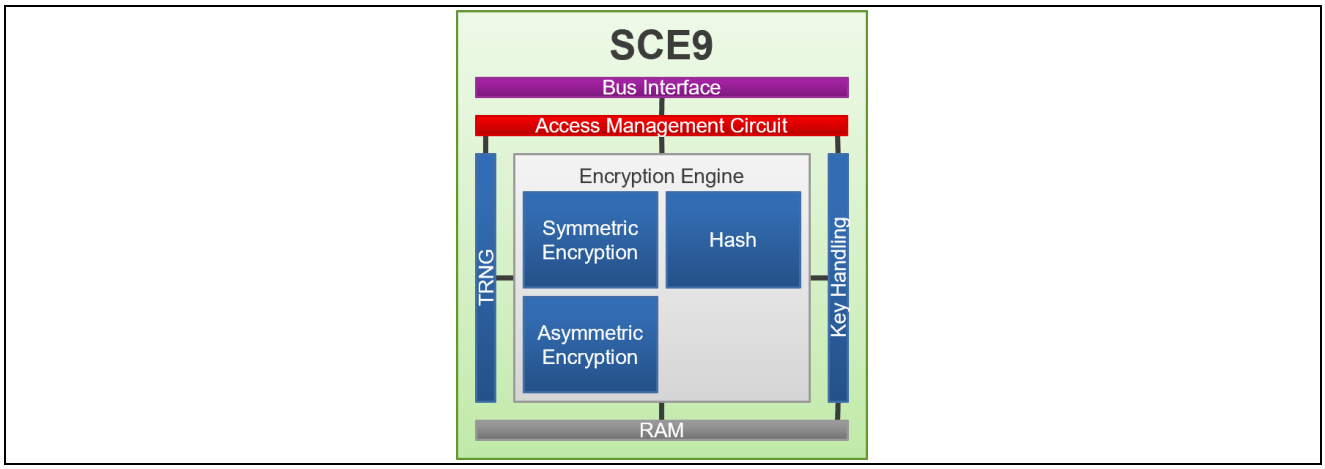

Figure 11. SCE9 Block Diagram

As shown in Figure 11. SCE9 Block Diagram, access to the internal components of the security engine is protected by the Access Management Circuit. The software driver provided in the FSP must be used to perform the various cryptographic functions supported by SCE9. This driver performs the proper authenticated access sequence to interface with the SCE9's Access Management Circuit. Improper access attempts via the CPU or the debugger will result in the Access Management Circuit generating an interrupt (SCE_TADI) and locking the security engine, preventing it from performing cryptographic functions. A device reset is required to clear the error.

The application should use the e^2 studio IDE or the RA Smart Configurator to enable the SCE_TADI interrupt event and call an application-defined ISR. The SCE signal will be armed during the SCE initialization process. The interrupt should be enabled immediately after SCE initialization and disabled before SCE shutdown. It is essential to note that repeating the initialization process will trigger the interrupt, even if the shutdown process has been performed. To prevent any issues, clear the interrupt status before enabling the interrupt; otherwise, the interrupt will trigger when SCE is initialized for a second time.

It is recommended to place the code that interacts with this peripheral in the Secure region if the application utilizes TrustZone.

The following sections provide more details about the additional hardware protection features that are available for each operational mode of the security engine. For more details, refer to the following documents:

- [RA6M5 User Manual]
- [SCE_TADI TU]
- [FSP User Manual]
- [SCE Modes]
- Section 3.3 SCE9
- Section 4 SCE9 Secure Key Injection, Storage, and Usage
- Section 5 SCE9 Cryptographic Functions

8.2.1 SCE9 Protected Mode Protection Features

Protected Mode provides timing attack protection for both symmetric and asymmetric cryptographic algorithms, implementing constant-time algorithms when handling key material.

Protected Mode also provides SPA/DPA protections on AES operations.

In Protected Mode, all keys, both public and private, must be securely injected such that they have an associated MAC that binds them to the specific MCU chip. When performing cryptographic operations with either a public or private key, the MAC associated with the key is verified before any cryptographic operation is performed with that key. If the MAC verification fails, an error is returned.

8.2.2 SCE9 Compatibility Mode Protection Features

Compatibility Mode offers protection against timing attacks for both symmetric and asymmetric cryptographic algorithms, implementing constant-time algorithms when handling key material.

SPA/DPA protections are not provided for AES operations. This security risk must be analyzed and accepted when considering the use of Compatibility Mode.

When performing cryptographic operations with a wrapped private key, the MAC associated with the key is verified before any cryptographic operation is performed with that key. If the MAC verification fails, an error is returned.

Public keys in Compatibility Mode do not have a MAC. The security risk of using non-authenticated public keys must be analyzed and accepted when considering Compatibility Mode.

8.3 Operational Temperature Monitoring

Some attacks involve operating the MCU outside its specified temperature range to induce erroneous behavior. The on-chip Temperature Sensor (TSN) peripheral can be used to monitor the die temperature.

Refer to the detailed description of this peripheral and its associated electrical characteristics as stated in the [RA6M5 User Manual] for the requirements and limitations of this hardware feature.

The application code must periodically check the die temperature, compare it to the device’s operating range, and trigger a fault if the temperature is outside the range.

If temperature attacks are in scope for the application’s threat model, this check should be performed at a rate consistent with the application's threat model.

It is recommended to place the code that interacts with this peripheral in the Secure region if the application utilizes TrustZone.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]

8.4 Operational Voltage Monitoring

Some attacks involve operating the MCU outside its specified voltage range to induce erroneous behavior. The Low Voltage Detection (LVD) peripheral can be used to monitor the voltage level input to the VCC and EXLVD pins and alert if a selectable voltage threshold is crossed.

Refer to the detailed description of this peripheral and its associated electrical characteristics as stated in the [RA6M5 User Manual] for the requirements and limitations of this hardware feature.

The MCU features three programmable voltage monitors.

Voltage Monitor 0 can be configured to be active immediately upon reset, using the voltage level selected in the Option-Setting Memory, which resets the MCU if the voltage drops below the selected value. Option Function Select Register 1 can be set to be in the Secure region to effectively place Voltage Monitor 0 in the Secure region.

It is recommended to configure Voltage Monitor 0 to be active immediately upon reset at a level appropriate for the application, and to configure Option Function Select Register 1 to be in the Secure region to mitigate voltage fault injection attacks.

Voltage Monitor 1 and Voltage Monitor 2 can be configured for more advanced voltage detection scenarios.

It is recommended to place the code that interacts with the LVDs in the Secure region if the application utilizes TrustZone.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]

8.5 Clock Protection

Some attacks involve varying the frequency of the MCU clock to try to induce erroneous behavior. The Clock Frequency Accuracy Measurement Circuit (CAC) peripheral counts pulses of the measurement target clock using a measurement reference clock. If the number of pulses falls outside an allowable range, an interrupt is generated.

Refer to the detailed description of this peripheral and its associated electrical characteristics as stated in the [RA6M5 User Manual] for the requirements and limitations of this hardware feature.

If the application uses an external clock and clock attacks are within the scope of the application’s threat model, the application should utilize the CAC.

It is recommended to place the code that interacts with this peripheral in the Secure region if the application utilizes TrustZone.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]

9. Internet Connectivity

The RA6M5 MCU Group includes a one-channel Ethernet Controller (ETHERC) compliant with the Ethernet or IEEE802.3 Media Access Control (MAC) layer protocol, plus one channel for the Ethernet DMA Controller (EDMAC) for the Ethernet Controller (ETHERC). These peripherals can be used to provide wired internet connectivity.

The majority of cybersecurity threats faced by a device that incorporates an internet-connected microcontroller will involve the internet connection. It is vital to understand both the threat model and the regulatory compliance requirements of the end-product.

The EU Cyber Resilience Act (CRA) requires that any product placed on the EU market that incorporates an RA6M5 microcontroller and may have a direct or indirect logical or physical data connection to a device or network must employ adequate security measures.

Secure connectivity requirements apply to both public and private infrastructure. A connected device should not be considered exempt from security requirements simply because it is connected to private infrastructure.

TCP connections should include the TLS protocol; UDP connections should include the DTLS protocol.

Ethernet stacks are highly complex software that are a prime target for cyberattacks. Ethernet stack providers, including the RA Family FSP, regularly provide updates containing fixes for security vulnerabilities. The Ethernet stack in the end-product should be updatable such that these fixes can be deployed to the end product. Anti-rollback protection on these updates should also be provided to prevent an attacker from regressing the end-product firmware to an older version with exploitable vulnerabilities.

For more details, refer to the following documents:

- [RA6M5 User Manual]
- [FSP User Manual]
- [Cloud Connectivity]
- [Cloud OTA]
- [FSP]

10. Secure Boot

To ensure the secure initialization of the application, it is recommended to utilize and potentially customize the secure bootloader solution provided in the FSP.

10.1 Second Stage Bootloader

The RA6M5 does not have a built-in (i.e., First Stage) secure bootloader; however, it is possible to implement an immutable bootloader using the secure bootloader solution provided in the FSP.

The FSP includes a port of the TrustedFirmware MCUboot project, an open-source secure boot and firmware update solution for 32-bit microcontrollers. Secure boot is usually very application-specific; therefore, Renesas provides multiple examples of how the secure boot solution can be used. Note that secure boot and secure firmware updates are provided as a unified solution.

Review the threat model and start-up time requirements of the application when implementing secure boot. Since all code flash on the RA6M5 is stored inside the chip, and the programmer and debugger interface should be locked upon deployment, it may be sufficient to implement only the secure firmware update portion of the secure bootloader solution.

It is recommended to make the code flash blocks that contain MCUboot immutable to form the application's immutable Root of Trust.

For more details, refer to the following documents:

- [Bootloader Basic]
- [Bootloader Dual Bank]
- [Bootloader Encrypted]
- Section 7 Immutable Memory

11. Secure Firmware Update

The ability to update firmware in an end product is becoming a standard requirement, especially if the product is connected to public infrastructure such as the internet. Any firmware update, whether through public infrastructure or a private connection, should be performed securely.

The FSP includes a port of the TrustedFirmware MCUboot project, an open-source secure boot and firmware update solution for 32-bit microcontrollers. Secure firmware updates are usually very application-specific; therefore, Renesas provides multiple examples of how the secure firmware update solution can be utilized. Note that secure boot and secure firmware updates are provided as a unified solution.

There are many items to consider when devising a secure firmware update strategy, including:

How will the new image be received? Is it received over a secure channel, or does the image need to be encrypted for transfer to the product? A TLS connection can usually be considered a secure channel.

The authenticity of the image needs to be verified before it is programmed for execution. Therefore, the entire image must be received and stored locally. Will the new image be stored on-chip or in an external memory?

If the new image is stored externally before installation, does it need to be encrypted so that an attacker cannot physically extract the plaintext binary?

Be sure to consider the threat model for the end product when architecting a firmware update strategy.

It is recommended to make the code flash blocks that contain MCUboot immutable to form the application's immutable Root of Trust.

For more details, refer to the following documents:

- [Bootloader Basic]
- [Bootloader Dual Bank]
- [Bootloader Encrypted]
- Section 7 Immutable Memory

12. Provisioning

12.1 Device Lifecycle Management and Debug Authentication

The RA6M5 supports authenticated Device Lifecycle Management (DLM) and debug authentication to provide IP protection and support product failure analysis. Figure 12. Device Lifecycle Management Overview shows an overview.

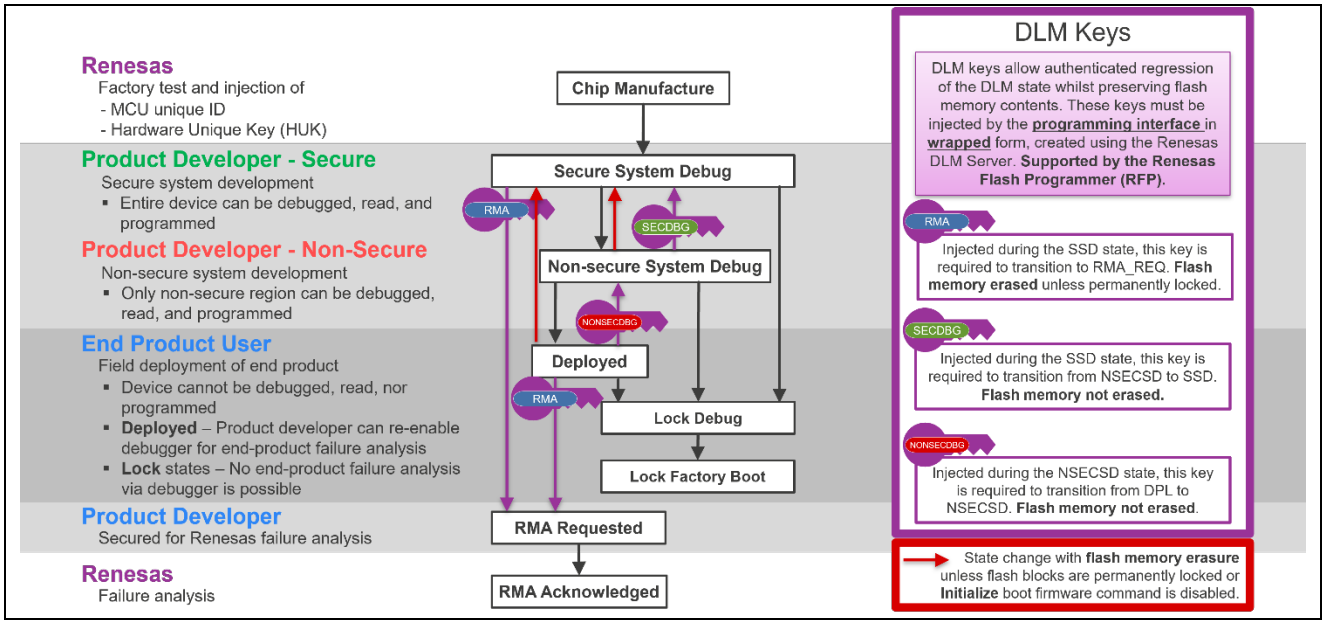

Figure 12. Device Lifecycle Management Overview

MCUs are delivered in the Secure System Debug (SSD) state. In this state, the product developer has complete access to all user-accessible memory and peripherals. If the application does not utilize TrustZone as an isolation mechanism, the entire application is developed in this DLM state. If the application does utilize TrustZone, the Secure region application code is programmed and debugged in this state.

If the application utilizes TrustZone, the MCU should be transitioned to the Non-secure System Debug (NSECSD) state to program and debug the Non-secure region application code.

When the MCU is programmed for incorporation in an end-product, there are several available options:

- If there is no desire to either re-enable the debugging capability of the MCU or maintain the ability to send the MCU to Renesas for failure analysis in the event of possible MCU failure, then the MCU should be transitioned to either Lock Debug (LCK_DBG) or Lock Factory Boot (LCK_BOOT). These transitions are permanent.
- To maintain the ability to send the MCU to Renesas for failure analysis in the event of possible MCU failure, an RMA_KEY must be injected when the device is in the SSD state. The MCU must be transitioned to the Deployed (DPL) state.
- To maintain the ability to re-enable debugging of the Non-secure region, an NSECDBG_KEY must be injected when the device is in the NSECSD state.

- To maintain the ability to re-enable debugging of the Secure region, including re-enabling debugging of an application that does not utilize TrustZone as an isolation mechanism, then a NSECDBG_KEY must be injected when the device is in the NSECSD state, and a SECDBG_KEY must be injected when the device is in the SSD state.

If a chip is returned to Renesas for failure analysis, the DLM state transition to RMA Requested (RMA_REQ) will not erase any blocks that have their associated PBPS or PBPS_SEC bit set. Information in these blocks will be visible to Renesas during the RMA process.

Key preparation steps where mass production keys are exposed in plaintext must be performed in a secure environment. Test keys used for prototype development can be created and prepared on a development PC.

The process of preparing and injecting DLM keys is similar to the secure key injection process for Protected Mode, described in section 4.3 Secure and Plaintext Key Injection and Update.

The most secure configuration is LCK_BOOT; however, the application use case may require the ability to re-enable programming and/or debugging of the end-product. In this case, non-trivial keys that are not duplicated from Renesas examples or other publicly available cryptography references must be used.

Renesas provides the following tools to support this process:

- Security Key Management Tool (SKMT) - This tool can create sample keys and prepare the DLM keys for secure injection. [SKMT]
- Renesas Flash Programmer (RFP) - This tool can perform DLM state transition using the MCU's factory boot firmware. [RFP]

Select third-party programming tools also support secure key injection.

For more details, refer to the following documents and sections of this document:

- [RA6M5 User Manual]
- [DLM]
- [SKMT]
- [RFP]
- Section 4.3 Secure and Plaintext Key Injection and Update

13. Website and Support

Visit the following URLs to learn about key elements of the RA family, download components and related documentation, and get support:

RA Product Information	renesas.com/ra
RA6M5 Product Information	renesas.com/RA6M5
RA Product Support Forum	renesas.com/ra/forum
RA Flexible Software Package	renesas.com/FSP
Renesas Support	renesas.com/support
Renesas PSIRT	renesas.com/psirt

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.25.25	—	Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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