Renesas RA0 Series

Low Power Consumption Guide

Introduction

This application note explains general methods for achieving low power consumption and how to configure the power-saving features available in the RA0 series. It describes techniques for reducing power consumption by configuring CPU/peripheral hardware clocks and utilizing Sleep Mode, Software Standby Mode, and Snooze Mode.

Target Device

RA0 series

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

Methods for Reducing Power Consumption in Microcontrollers

There are several ways to reduce the power consumption of a microcontroller

(1) Use of low-power modes
(2) Selecting a low-power mode suitable for the processing task
(3) Using an appropriate oscillator and oscillation frequency
(4) Proper handling of unused pins

(1) Use of low-power modes

The operation of a microcontroller can be broadly classified into two modes: the normal operation mode, in which programs are executed, and the low-power mode, which can be entered when program execution is not required.

In many applications, the CPU does not need to be executing programs continuously. There are often periods when the CPU is idle, such as when waiting for an external input signal or a timer event. By switching from the normal operation mode to a low-power mode during these idle periods, power consumption can be significantly reduced.

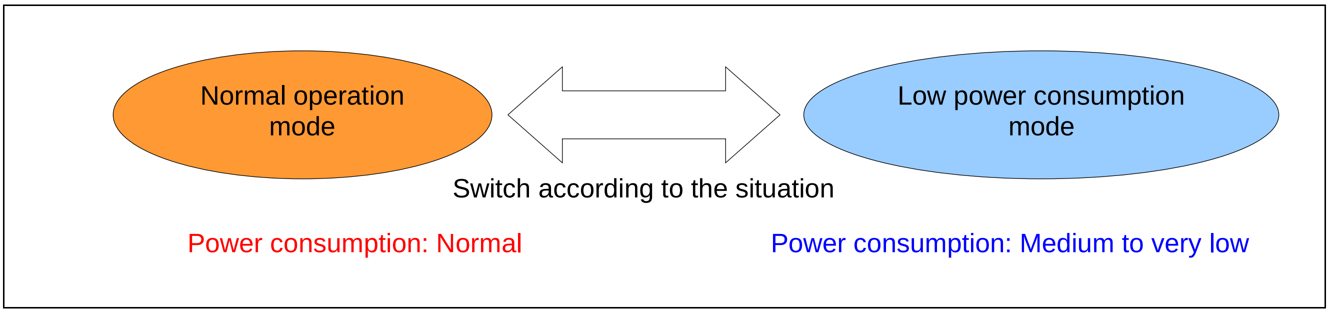

Figure 0-1 Basic microcontroller operating modes

(2) Selecting a low-power mode suitable for the processing task

The RA0 series offers several low-power modes, including Sleep Mode, Software Standby Mode, and Snooze Mode. It is important to select the most suitable low-power mode based on the system requirements.

- **Sleep mode:**

The CPU operation is halted, while peripheral functions remain active. Although power consumption is higher than in Software Standby Mode, this mode allows for faster wake-up.

- **Software Standby mode:**

Both the CPU and the system clock are stopped to minimize power consumption.
However, it takes longer to resume operation compared to Sleep Mode.

- **Snooze mode:**

During Software Standby Mode, the clock operation of certain peripheral functions (such as ADC, SAU, and DTC) can be resumed, allowing them to operate with low power consumption.
This mode is suitable for intermittent data collection or monitoring without activating the CPU.

① For quicker recovery from low power mode

If fast recovery from a low-power mode is a priority, Sleep mode should be selected. However, depending on the clock source used, Software Standby mode may also offer sufficiently fast wake-up times. Choose the optimal mode based on your system requirements. (Wake-up time from Software Standby mode: 0.9 µs when using the High-Speed On-Chip Oscillator with fast startup enabled.)

② When operating peripheral functions during low power mode

If specific peripheral functions need to operate during Software Standby mode, it is necessary to select the most suitable mode—Sleep mode, Software Standby mode, or Snooze mode—based on power consumption and functional requirements.

- Sleep mode
  - When using interval or capture operations with TAU
- Software Standby mode
  - When using peripheral functions that can operate with only the sub-system clock, such as RTC or TML32
  - When using IICA in slave mode with the wake-up function
- Snooze mode
  - When using SAU for slave reception or receiving data via UART
  - When monitoring analog signals with the A/D converter

③ Switching between low-power mode and normal operation mode

It is necessary to consider the system's average power consumption. The operating mode should be selected based on the duration and power consumption of both the standby and normal operation states. In general, if the standby period is long, Software Standby Mode—which offers the lowest power consumption—is effective. If the system frequently exits standby, Sleep Mode—with its shorter wake-up time—is more suitable.

A summary of the above is shown in Table 0-1.

Table 0-1 Low-Power Mode Suitable for the Application

Application	Suitable Low-Power Mode
Applications that periodically alternate between normal operation and standby (with long standby periods)	Software Standby mode
Applications that frequently alternate between normal operation and standby (requiring fast standby recovery)	Sleep mode
Applications that operate some peripheral functions (ADC, SAU, DTC) during standby periods	Snooze mode

(3) Using an appropriate oscillator and oscillation frequency

Crystal oscillators offer excellent frequency accuracy but have the characteristic of relatively long oscillation stabilization times. Since power is consumed during the stabilization period, longer stabilization times tend to increase power consumption. Therefore, in applications where frequency accuracy is not especially critical, using a ceramic oscillator or a High-Speed On-Chip Oscillator (HOCO) can shorten the stabilization time and reduce power consumption.

Ceramic oscillators have lower frequency accuracy compared to crystal oscillators but have the advantage of shorter stabilization times, which contributes to power reduction.

The High-Speed On-Chip Oscillator (HOCO) has even lower frequency accuracy than ceramic oscillators; however, compared to using a ceramic oscillator, it can further reduce power consumption. Additionally, because no external oscillator is required, it helps reduce component costs. The characteristics of each clock source are shown in Table 0-2.

Generally, operating frequency and power consumption have a proportional relationship. Therefore, if system processing speed is not a priority, lowering the operating frequency can reduce power consumption.

Table 0-2 Features of each clock

	Oscillation frequency accuracy	Oscillation stabilization time
Crystal oscillator	Very high accuracy (around 0.001 %)	Long (several ms to several tens of ms)
Ceramic resonator	Inferior to quartz crystal oscillators (about 0.5 %)	Short (tens of μs to hundreds of μs)
High-speed on-chip oscillator	Inferior to ceramic resonators (about 1 %)	Short (4.4μs (max.))

(4) Proper handling of unused pins

If unused microcontroller pins are left floating, their voltage levels can become unstable due to external noise or electromagnetic interference, potentially causing unintended internal circuit state transitions. This can lead to unwanted current flow and increased power consumption. Therefore, proper handling of unused pins plays an important role not only in preventing malfunctions and improving noise immunity but also in reducing power consumption.

For unused pins configured as input ports, connect them to the power supply voltage (VCC) or ground (VSS) through pull-up or pull-down resistors. This stabilizes the input voltage and suppresses the influence of power supply noise. It is important to place the resistors as close to the pins as possible. If the wiring between the resistor and the pin is long, that wiring may act as an antenna, drawing external noise into the microcontroller.

Unused pins configured as output ports should generally be left open. However, if the output level of an open port changes frequently, the port itself can become a source of noise. Therefore, it is recommended to fix the output level through software control.

1. Low power consumption function

1.1 RA0 series low-power modes

Here is the explanation of the three low-power modes supported by the RA0 series:

① Sleep mode

In Sleep Mode, the CPU operation is stopped, but the values of the CPU internal registers are retained. Peripherals other than the CPU continue to operate.

If the Independent Watchdog Timer (IWDT) is set to auto-start and the OFS0.IWDTSTPCTL bit is set to 1, the IWDT count operation stops during Sleep Mode. If OFS0.IWDTSTPCTL is 0, the counting continues.

② Software Standby Mode

In Software Standby Mode, the CPU, most built-in peripherals, and oscillators stop operating. However, the CPU internal register values, SRAM data, and the states of built-in peripherals and I/O ports are retained.

Since most oscillators stop in this mode, power consumption is significantly reduced.

If the IWDT is set to auto-start and the OFS0.IWDTSTPCTL bit is 1, the IWDT count operation stops simultaneously with the transition to Software Standby Mode. If the bit is 0, counting continues.

③ Snooze mode

When a snooze request is received during Software Standby Mode, the MCU transitions to Snooze Mode. In Snooze Mode, the CPU operation remains stopped, but some peripherals (ADC, SAU, DTC) can operate.

Figure 1-1 shows the states of Normal Operation Mode and each low-power mode.

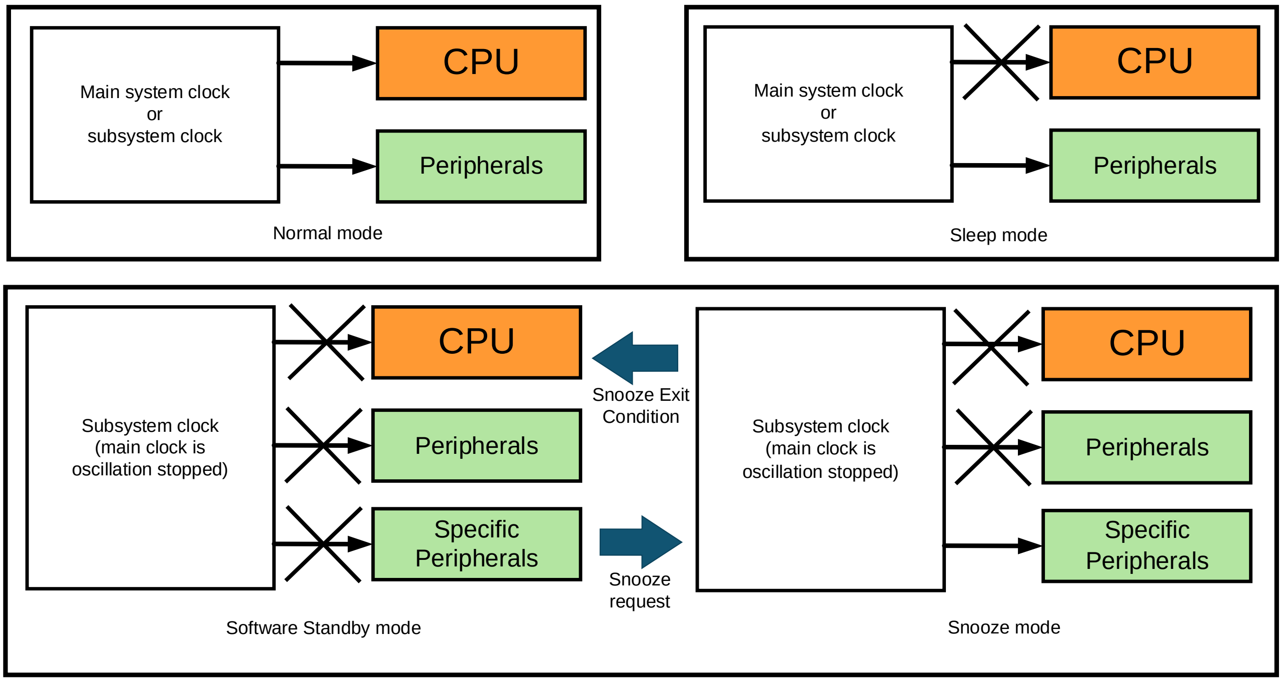

Figure 1-1 Status of each operation mode

1.2 How to shift to/from low power mode

The transition to and release from the low power modes are outlined in Figure 1-2 below. For more details and precautions for use, please refer to the “Low Power Modes” section in the User’s Manual: Hardware.

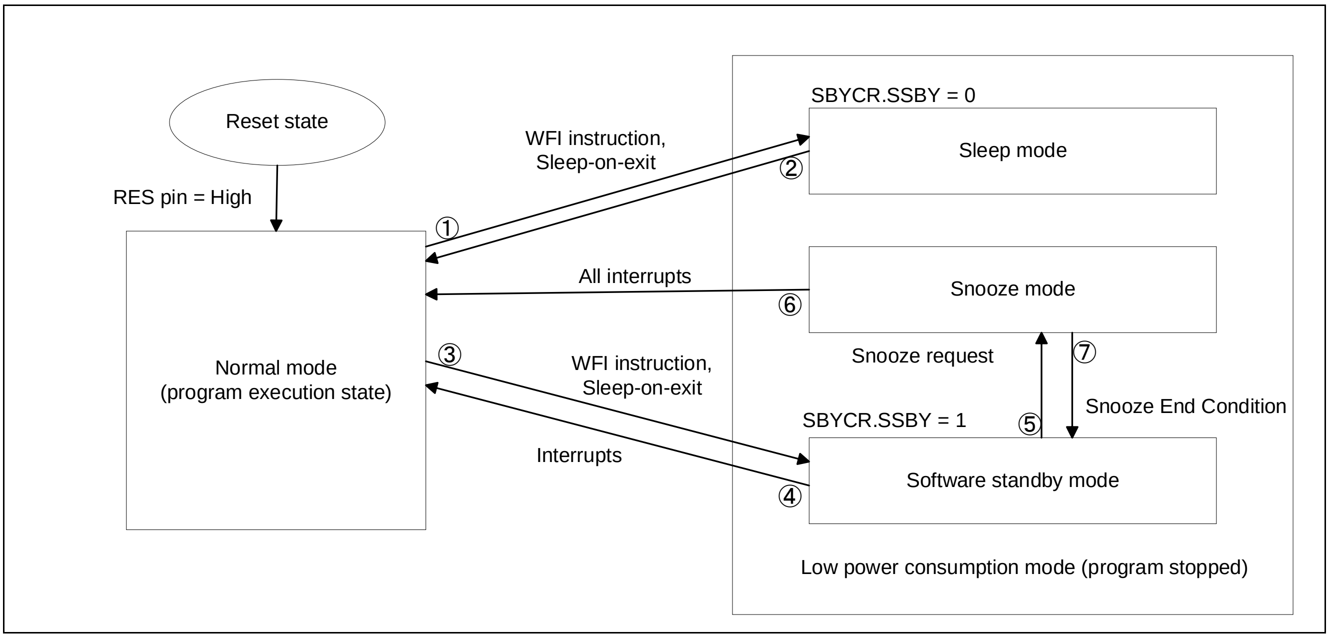

Figure 1-2 Transition of each operation mode

① Entering Sleep Mode
When the SSBY bit in the SBYCR register is set to 0 and the WFI instruction is executed, the clock supply to the CPU is stopped, and the system transitions to Sleep mode.

② Sleep mode release
Sleep mode is mainly exited by an interrupt signal, such as an external interrupt or timer interrupt. In addition, a reset from the RES pin, an internal reset caused by an IWDT underflow, or a reset triggered by voltage monitoring or an SRAM parity error can also cause the system to exit Sleep mode.

③ Shift to software standby mode
When the SSBY bit in the SBYCR register is set to 1 and the WFI instruction is executed, the system transitions to Software Standby mode.
Note that the system cannot enter Software Standby mode during flash memory program/erase operations. Please execute the WFI instruction only after these operations have been completed.

④ Exit software standby mode
Software Standby mode can be exited by enabled interrupts, a reset from the RES pin, a power-on reset, and similar events. After exiting the mode, the oscillator that was operating prior to the transition restarts, and once the source clock for ICLK stabilizes, the MCU returns to normal operation mode.

⑤ Shift to snooze mode

Receipt of a snooze request during software standby mode causes the MCU to enter snooze mode. Available snooze requests for switching to snooze mode are shown in Table 1-1.

Table 1-1 Snooze request available to switch to snooze mode

Snooze request output source	Control register	
	Register	Bit
SAU0	SSC0	SWC
ADC12	ADM2	AWC
ICU（for DTC）	DTCENSTn	STm

Except when using the DTC during Snooze mode, set the DTCST.DTCST bit to 0 before executing the WFI instruction. If the DTC is required during Snooze mode, set the DTCST.DTCST bit to 1 before executing the WFI instruction.

⑥ Cancel snooze mode

Snooze mode is released by an interrupt (GPIO edge detection, RTC interrupt) or a reset (RES pin reset, IWDT reset) available in software standby mode.

⑦ Return from snooze mode to software standby mode

When the processing of peripheral functions operating in snooze mode is completed and the snooze request is cleared, the MCU exits snooze mode and automatically returns to software standby mode.

1.2.1 Sleep mode settings using FSP

Figure 1-3 shows how to set the sleep mode in FSP.

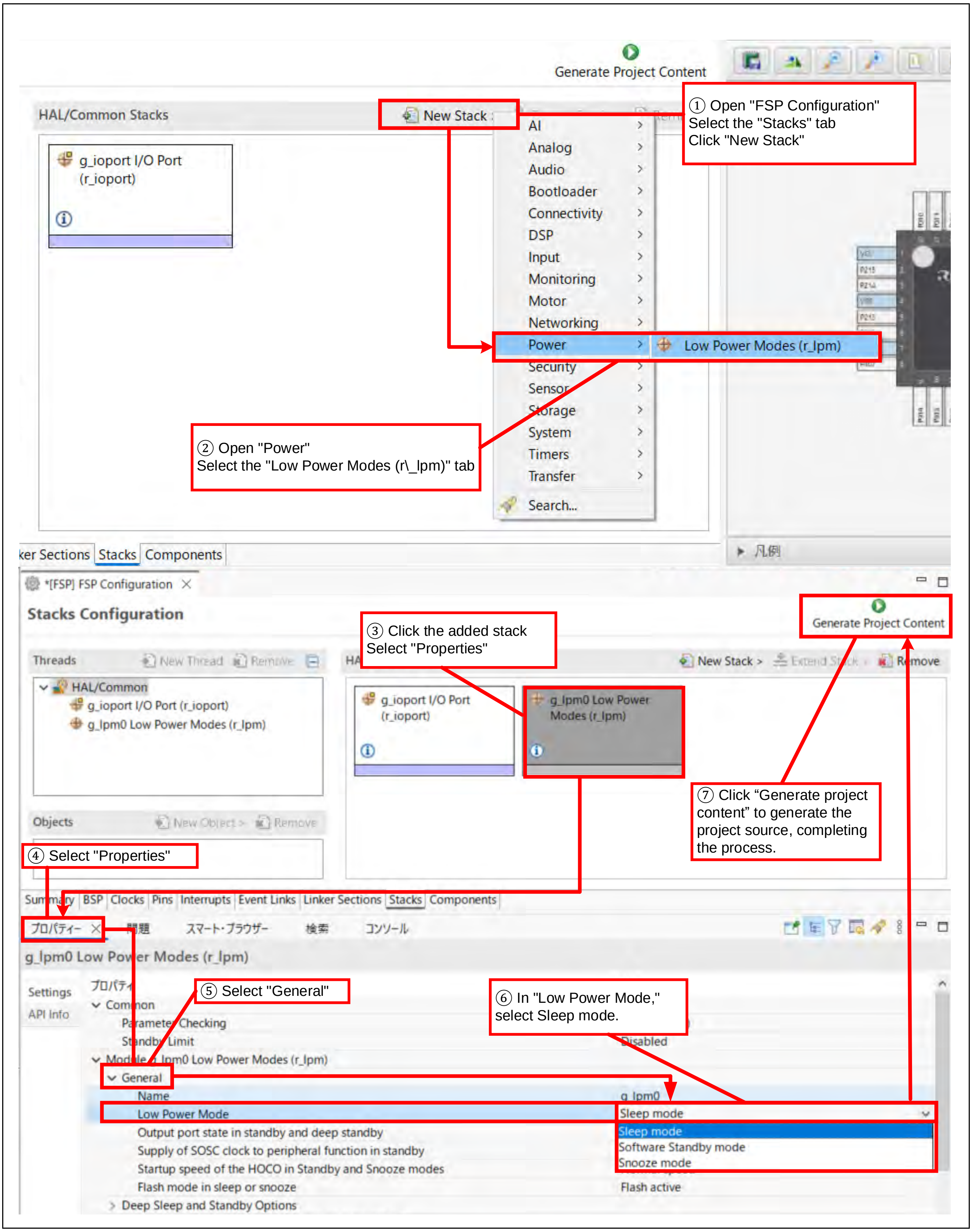

Figure 1-3 Sleep Mode Settings

The usage of API functions after FSP configuration is shown in Figure 1-4. For more details about the APIs, please refer to the Module Resource Page of the FSP.

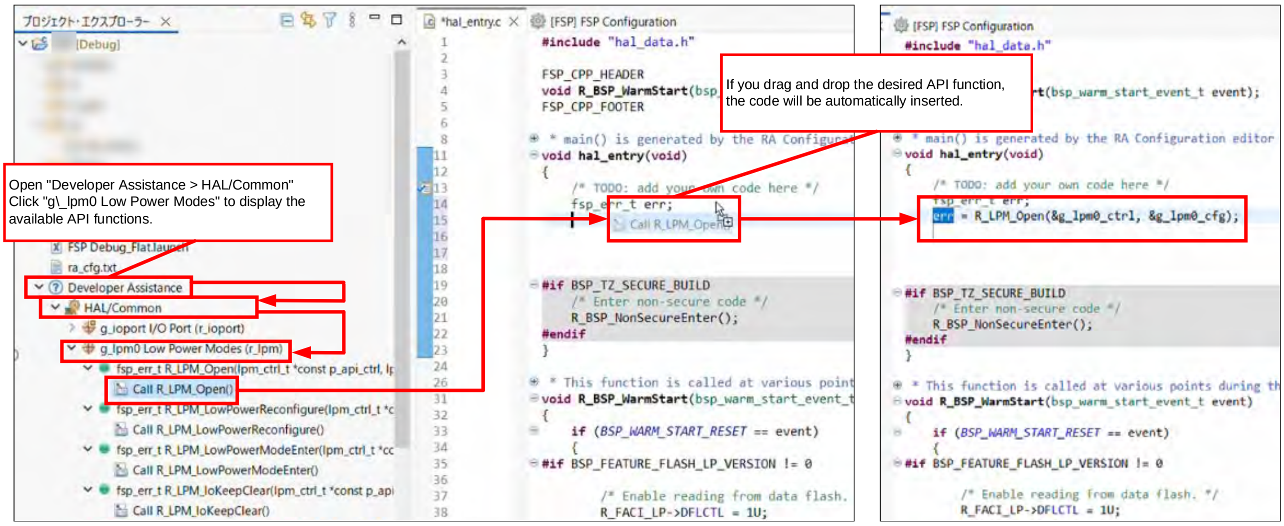

Figure 1-4 How to Use the API

When the r_lpm module configured in the FSP is named "g_lpm0" and the Low Power Mode is set to "sleep mode," an example flowchart showing the transition to Sleep mode and its release is illustrated in Figure 1-5.

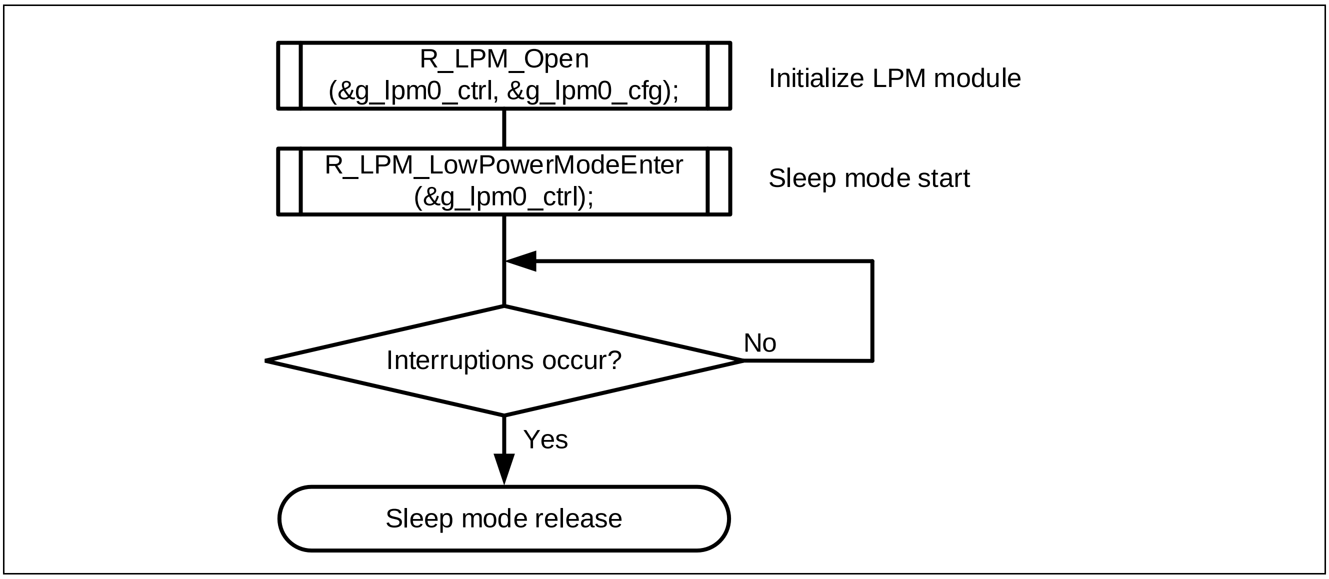

Figure 1-5 Sleep mode transition/release flow

1.2.2 Setting up software standby mode using FSP

The method for configuring Software Standby mode in the FSP is shown in Figure 1-6.

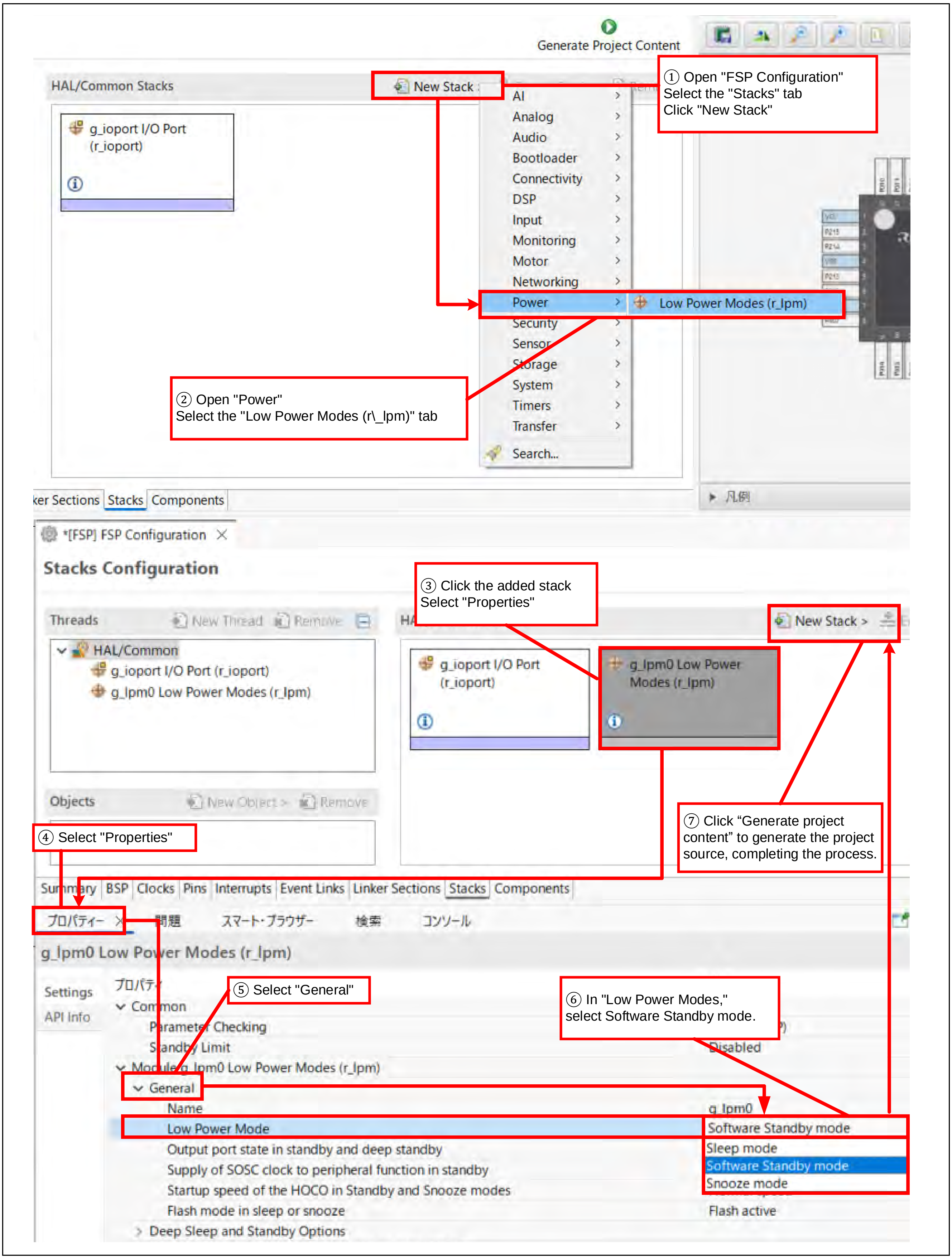

Figure 1-6 Software standby mode setting

An example of interrupt settings for releasing Software Standby mode is shown in Figure 1-7. The figure illustrates the configuration for releasing the mode via an interrupt from IRQ0.

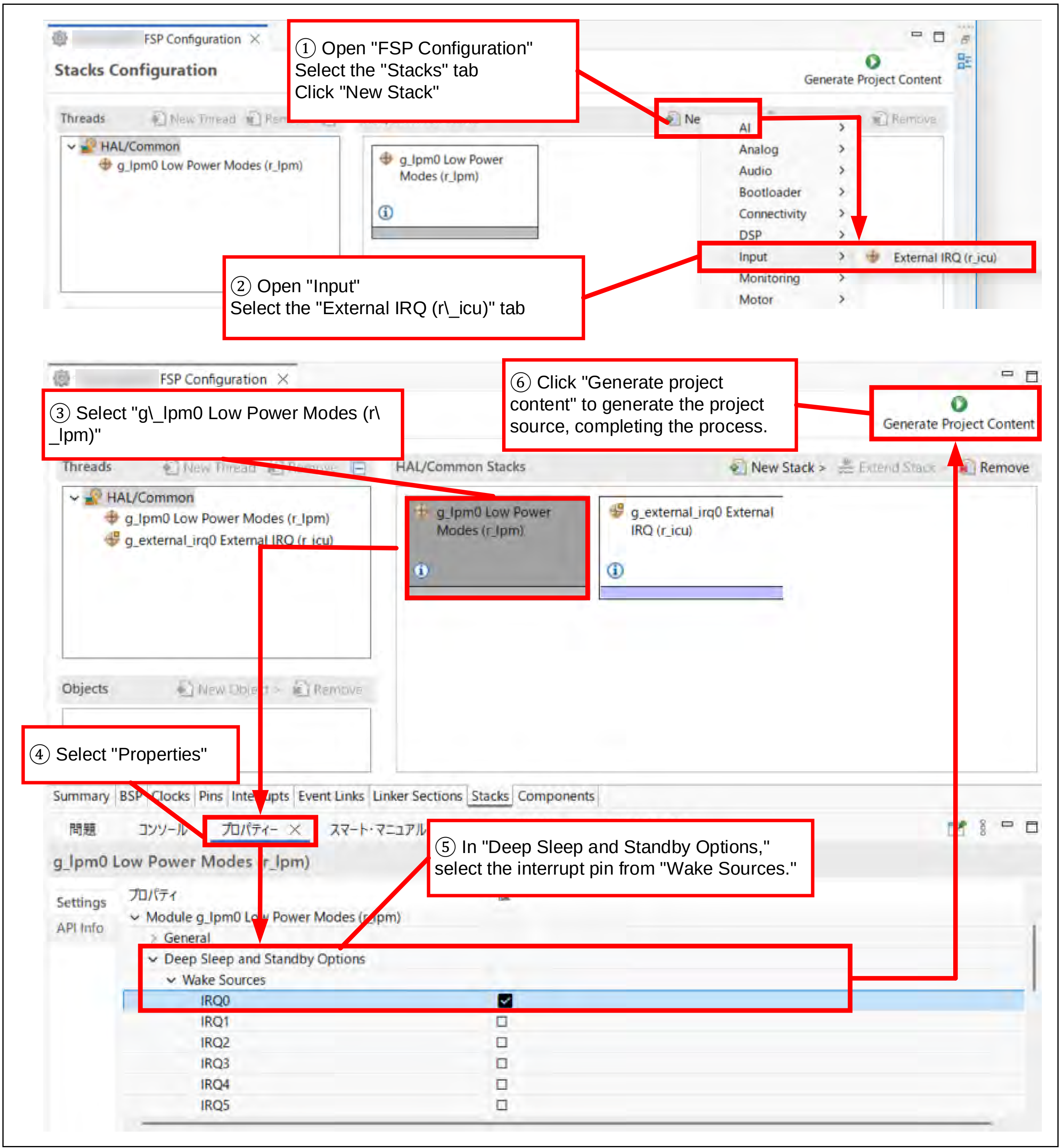

Figure 1-7 Setting of interrupts for releasing software standby mode

The usage of API functions after FSP configuration is shown in Figure 1-8. For details about the APIs, please refer to the Module Resource Page of the FSP.

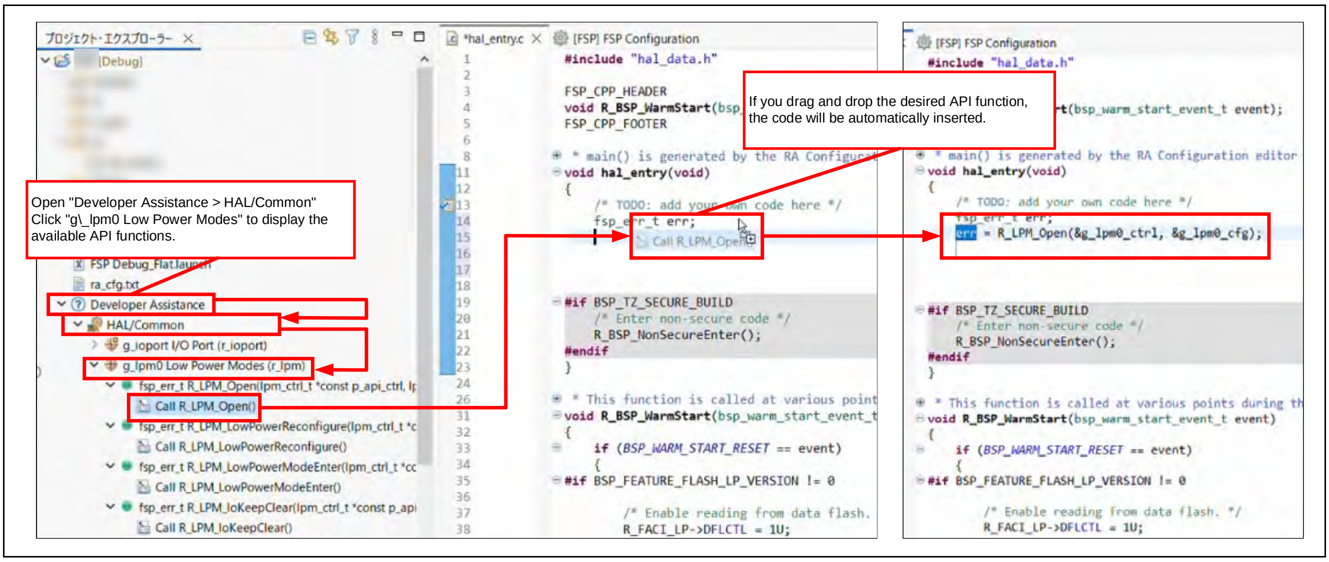

Figure 1-8 How to use the API

When the r_lpm module configured in the FSP is named "g_lpm0," the Low Power Mode is set to "Software Standby mode," and the Wake Source is set to "IRQ0," an example flowchart illustrating the transition to and release from Software Standby mode is shown in Figure 1-9.

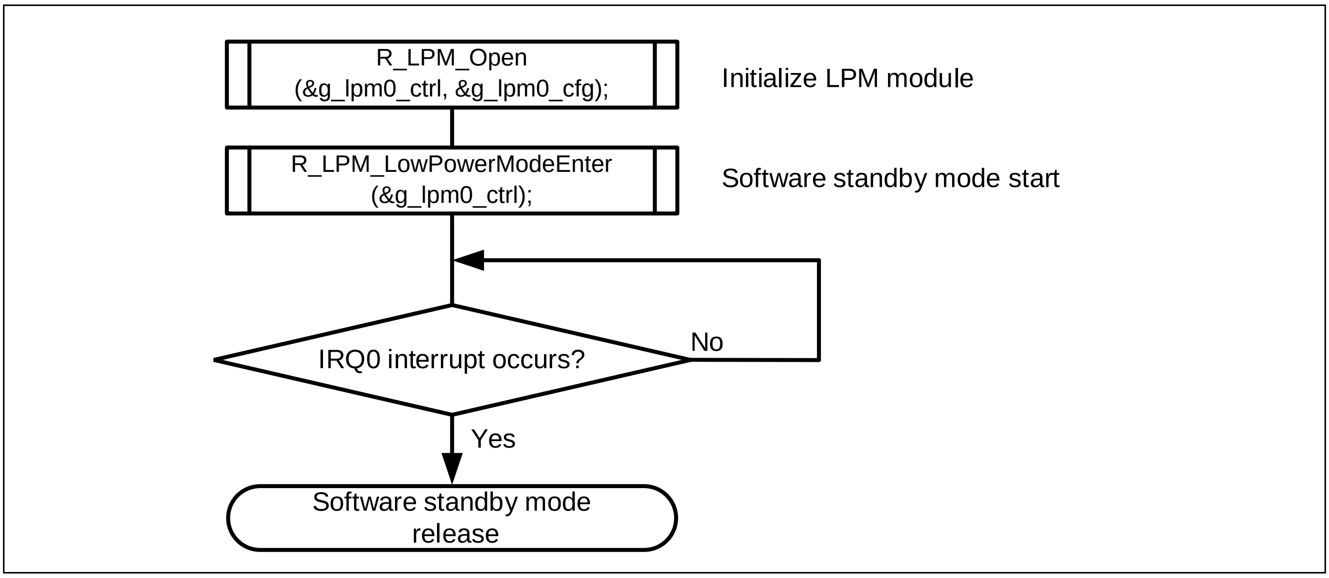

Figure 1-9 Software standby mode transition/release flow

1.2.3 Setting Snooze Mode using FSP

The method for configuring Snooze mode in the FSP is shown in Figure 1-10.

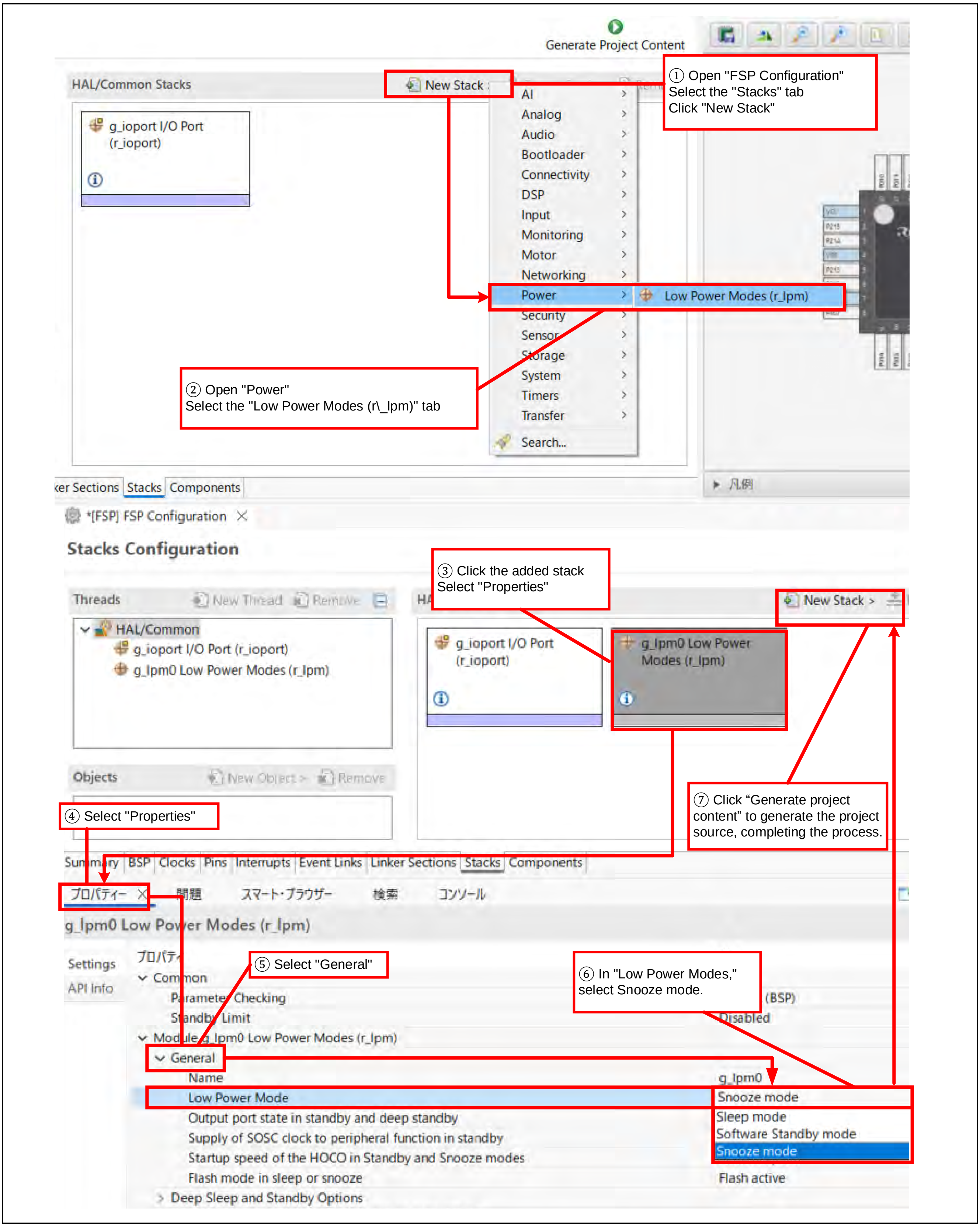

Figure 1-10 Snooze mode setting

【Note】When using the DTC during Snooze mode, set DTCENSETx to 1. Writing a 1 to this bit selects the corresponding event as a trigger for starting the DTC.

An example of interrupt settings for releasing Snooze mode is shown in Figure 2-11. Figure 1-11 illustrates the configuration for releasing the mode via an interrupt from IRQ0.

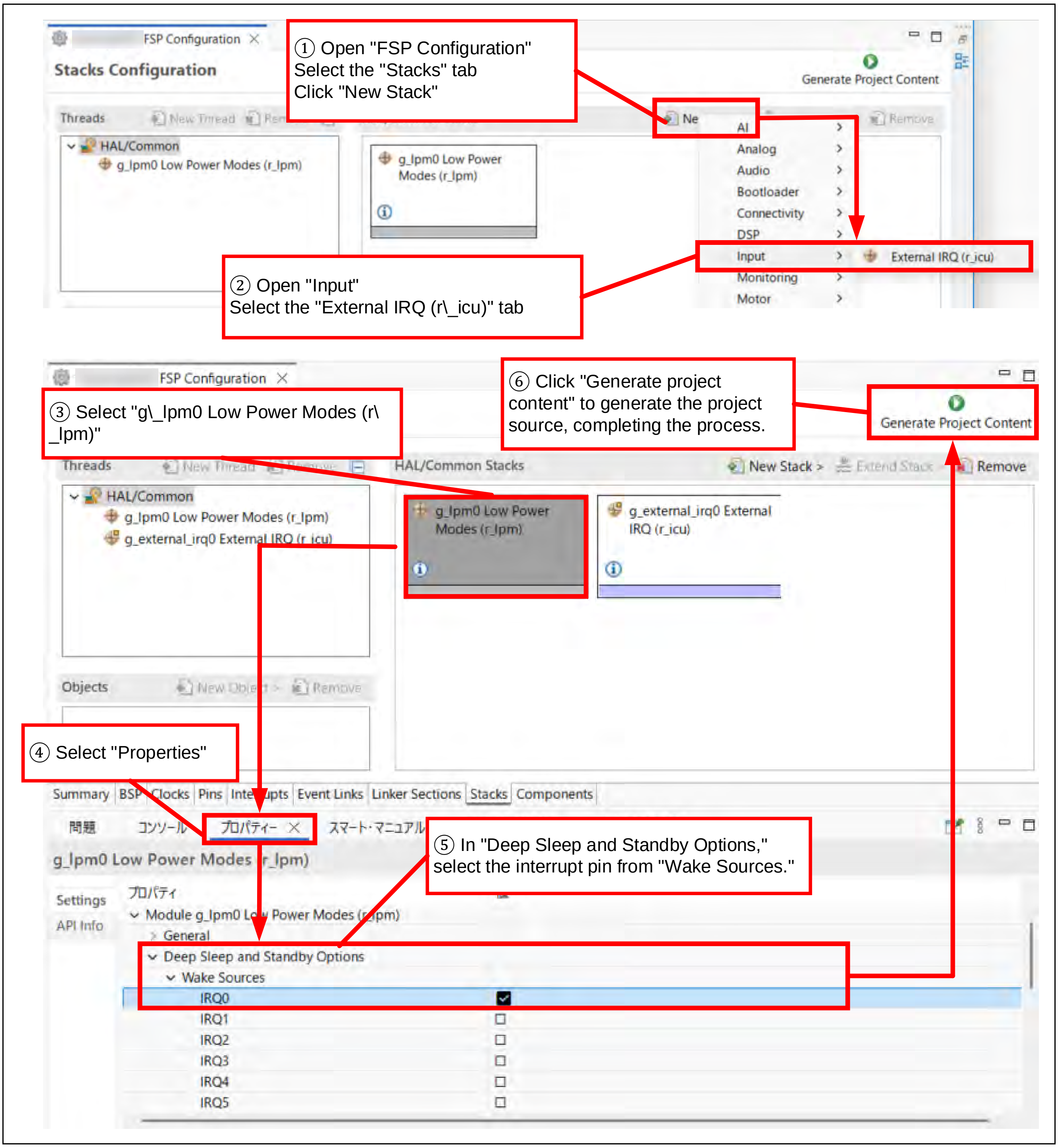

Figure 1-11 Interrupt setting for snooze mode release

Figure 1-12 shows how to use the API functions after configuring the FSP. For more details about the API, please refer to the Module Resource Page of the FSP.

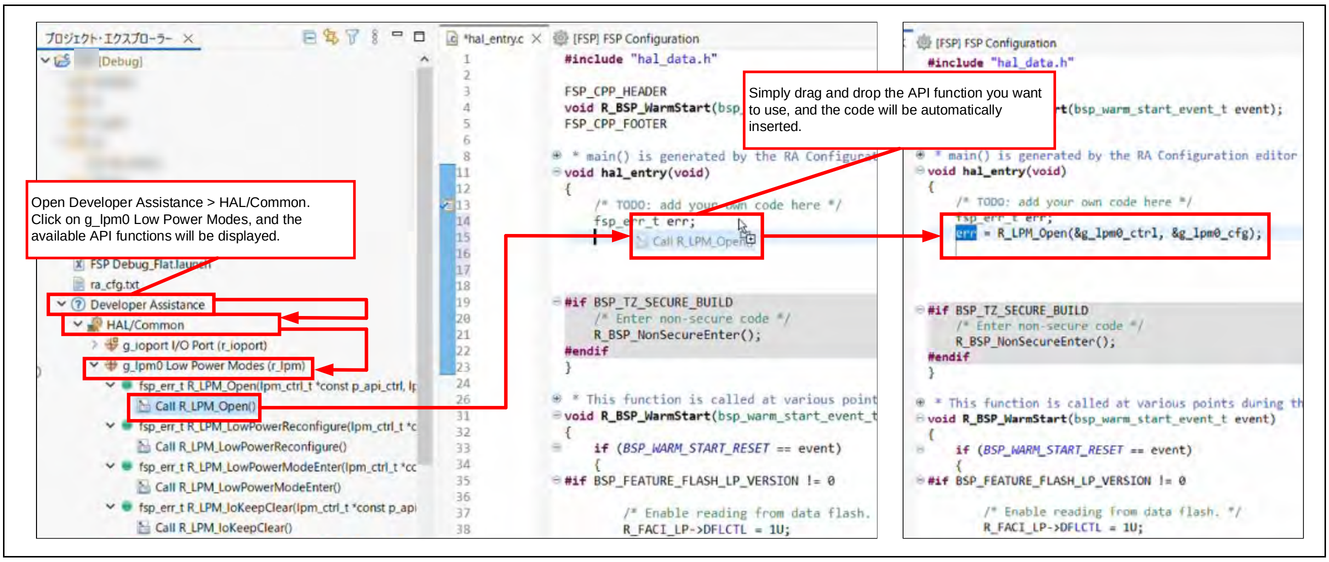

Figure 1-12 How to use the API

Figure 1-13 shows a flowchart illustrating an example of entering and exiting Snooze mode.
In this example, the r_lpm module configured in the FSP is named g_lpm0, the Low Power Mode is set to Snooze mode, and the Wake Sources are set to IRQ0.

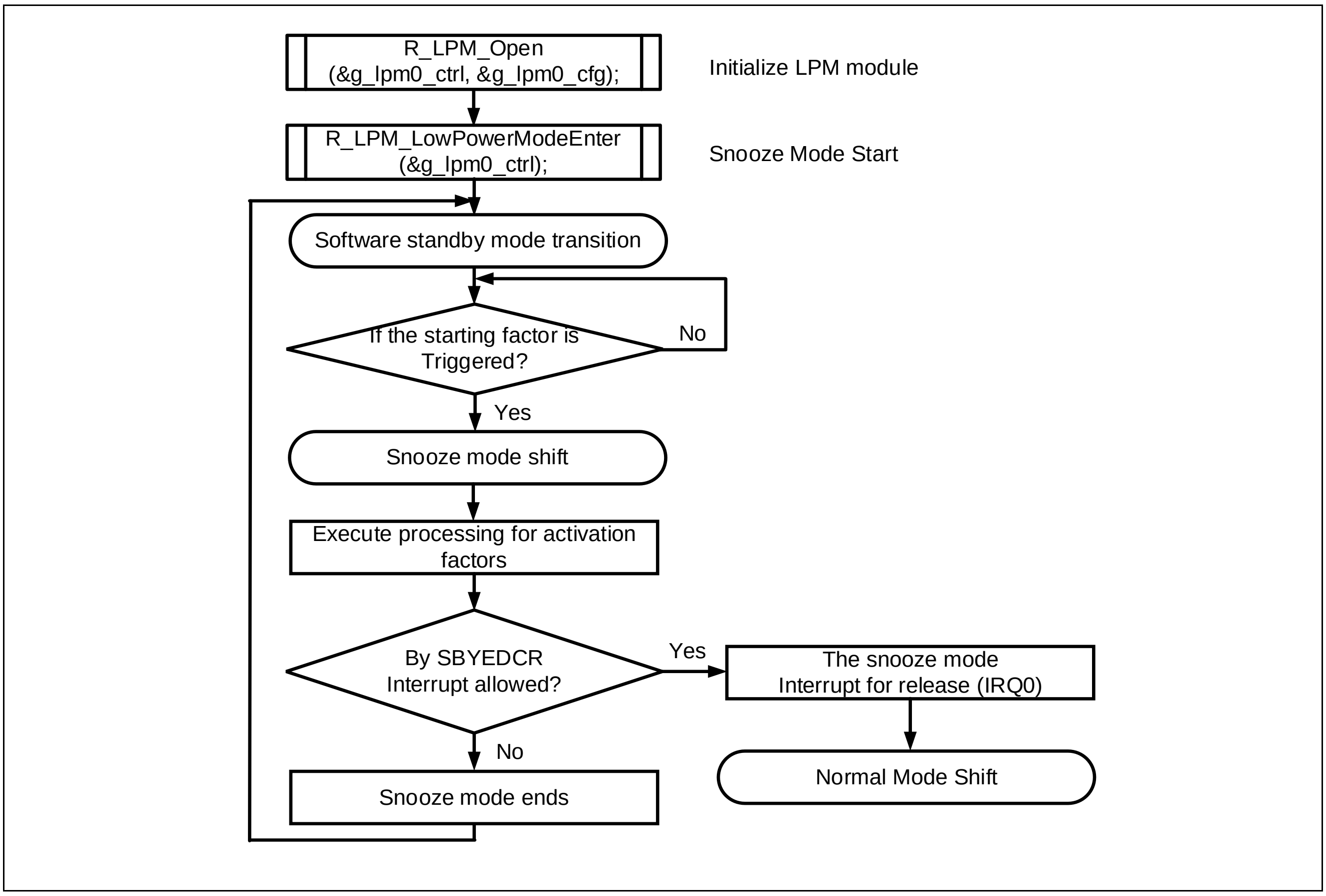

Figure 1-13 Snooze Mode Entry/Exit Flow

1.3 Module stop function

By using the module stop function, you can reduce power consumption by stopping the clock supply to each on-chip peripheral module, thereby transitioning the specified module to the module stop state.
When you set the corresponding MSTPmi bit in the MSTPCRn register (n = A to D) to “1,” the target module stops operating, while the CPU continues to operate independently.
To resume operation, clear the MSTPmi bit to “0,” and the module will restart operation at the end of the current bus cycle.
Note that after releasing the reset, all modules except for the DTC are in the module stop state. Also, when the MSTPmi bit is set to “1,” access to the corresponding module is not possible, so make sure to set it to “0” before accessing the module.

1.3.1 Module Stop Configuration Method

By using the Module Stop Control Register, you can stop the clock supply to each peripheral function and place the specified module into a stopped state.
Here, we illustrate how to set and release the module stop state for [this module]. For information about other modules, please refer to the user manual.

Figure 1-14 shows the relationship between the bits in the MSTPCRA register and the corresponding peripheral modules. Setting each bit to “1” stops the clock supply to the corresponding module, placing it into the module stop state.

Bit positon	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSTPCRA	1	1	1	1	1	1	1	1	1	MSTPA22	1	1	1	1	1	1

DTC Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

Figure 1-14 MSTPCRA register

Figure 1-15 shows the relationship between the bits in the MSTPCRB register and the corresponding peripheral modules. Setting each bit to “1” stops the clock supply to the corresponding module, placing it into the module stop state.

Bit positon	31	30	29	28	27	26	25	24	23	22	21	20	19	18
MSTPCRB	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit positon	15	14	13	12	11	10	9	8	7	6	5	4	3	2
MSTPCRB	MSTPB 15	1	1	1	1	MSTPB 10	1	1	MSTPB 7	MSTPB 6	1	1	1	1

SAU0 Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

SAU1 Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

UART0 Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

IICA0 Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

Figure 1-15 MSTPCRB register

Figure 1-16 shows the relationship between the bits of the MSTPCRC register and the corresponding peripheral modules. Setting each bit to “1” stops the clock supply to the corresponding module, putting it into the module stop state.

TRAG Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

Bit positon	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSTPCRC	1	1	1	MSTPC28	1	1	1	1	1	1	1	1	1	1	1	1

Bit positon	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSTPCRC	1	MSTPC14	1	1	1	1	1	1	1	1	1	1	1	1	MSTPC1	1

ELC Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

CRC Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

Figure 1-16 MSTPCRC register

Figure 1-17 shows the relationship between the bits of the MSTPCRD register and the corresponding peripheral modules. Setting each bit to “1” stops the clock supply to the corresponding module, putting it into the module stop state.

RTC Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

ADC12 Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

Bit positon	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSTPCRD	1	1	1	1	1	1	1	1	1	1	MSTPD 23	1	1	1	1	MSTPD 16

Bit positon	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSTPCRD	1	1	1	1	1	1	1	1	1	1	1	MSTPD 4	1	1	1	MSTPD 0

TML32 Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

TAU0 Module stop setting
0: Cancel the module-stop state
1: Enter the module-stop state

Figure 1-17 MSTPCRD register

1.3.2 Configuring the module stop function using FSP

Since the module stop function cannot be configured using FSP, it is necessary to add code manually. Table 1-2 shows examples of setting each module stop control register to “1.”

Table 1-2 Module Stop Control Register Code List

Module	Code
DTC	R_SYSTEM->MSTPCRA_b.MSTPA22 = 1; 注
SAU0	R_MSTP->MSTPCRB_b.MSTPB6 = 1;
SAU1	R_MSTP->MSTPCRB_b.MSTPB7 = 1;
IICA0	R_MSTP->MSTPCRB_b.MSTPB10 = 1;
UARTA	R_MSTP->MSTPCRB_b.MSTPB15 = 1;
CRC	R_MSTP->MSTPCRC_b.MSTPC1 = 1;
ELC	R_MSTP->MSTPCRC_b.MSTPC14 = 1;
TRING	R_MSTP->MSTPCRC_b.MSTPC28 = 1;
TAU0	R_MSTP->MSTPCRD_b.MSTPD0 = 1;
TML32	R_MSTP->MSTPCRD_b.MSTPD4 = 1;
ADC12	R_MSTP->MSTPCRD_b.MSTPD16 = 1;
RTC	R_MSTP->MSTPCRD_b.MSTPD23 = 1;

【Note】Please check that DTCST.DTCST is set to 0.

1.4 Flash Operation Mode

By selecting an appropriate power control mode according to the operating frequency and operating voltage, you can reduce power consumption during Normal mode, Sleep mode, and Snooze mode.

Since the flash memory consumes a large amount of internal current during high-speed access, “High mode” offers faster operation at the cost of higher power consumption. On the other hand, by using “Middle mode” or “Low mode,” it is possible to reduce the internal clock speed and relax timing, thereby lowering the current required for read and write operations and reducing power consumption. The following is an overview of each mode.

① High-speed mode

The maximum operating frequency of ICLK during flash read operations is 32 MHz. The operating voltage range during flash read operations is 1.8 V to 5.5 V. However, when the operating voltage is between 1.6 V and 1.8 V, the maximum ICLK operating frequency during flash read operations is limited to 4 MHz.

② Middle-speed mode

In this mode, power consumption can be reduced compared to High-speed mode under the same conditions.
The maximum operating frequency of ICLK during flash read operations is 24 MHz. The operating voltage range during flash read operations is 1.6 V to 5.5 V. However, when the operating voltage is between 1.6 V and 1.8 V, the maximum ICLK operating frequency during flash read operations is limited to 4 MHz.
During flash program/erase (P/E) operations, the operating frequency range is 1 MHz to 24 MHz, and the operating voltage range is 1.6 V to 5.5 V.
However, when the operating voltage is between 1.6 V and 1.8 V, the maximum operating frequency during flash program/erase (P/E) operations is limited to 4 MHz.

③ Low-speed mode

The maximum operating frequency of ICLK during flash read operations is 2 MHz. The operating voltage range during flash read operations is 1.6 V to 5.5 V.

④ Subosc-speed mode

The maximum operating frequency of ICLK during flash read operations is 37.6832 kHz. The operating voltage range during flash read operations is 1.6 V to 5.5 V. Flash memory program/erase (P/E) operations are prohibited. Oscillators other than the sub-clock oscillator and the low-speed on-chip oscillator must not be used.

1.4.1 Setting Flash Operation Mode

By setting the MODE[1:0] bits of the FLMODE register, you can switch the flash operation mode. Figure 1-18 shows the relationship between the bits of the FLMODE register and the operation modes.

Bit positon	7	6	5	4	3	2	1	0
FLMODE	MODE[1.0]		0	0	0	0	0	0

Selection of Operating Mode
00: Setting Prohibited
01: Low-speed mode
10: Middle-speed mode
11: High-speed mode

Figure 1-18 FLMODE resistor

1.4.2 Setting flash operation mode using FSP

This section describes how to set the flash operation mode using FSP. Selecting the flash operation mode requires that operating conditions, such as the ICLK frequency, fall within the specified range. By setting the clock frequency using the API functions of the r_cgc module, the flash operation mode is automatically configured to the appropriate setting.

Figure 1-19 shows how to configure the r_cgc module using FSP.

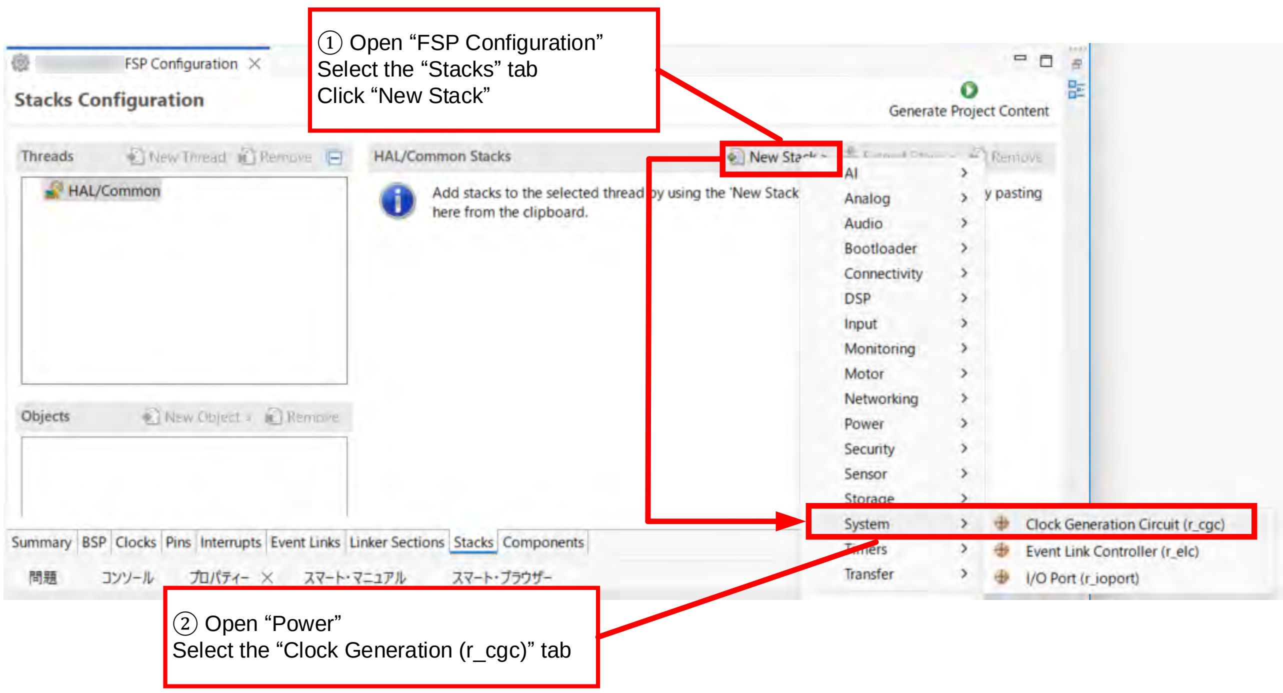

Figure 1-19 r_cgc module configuration

After configuring FSP, switch the clock frequency in the code using API functions. Figure 1-20 shows a flowchart example of setting the HOCO to divide by 16. When setting the ICLK, the flash operation mode is also configured accordingly.

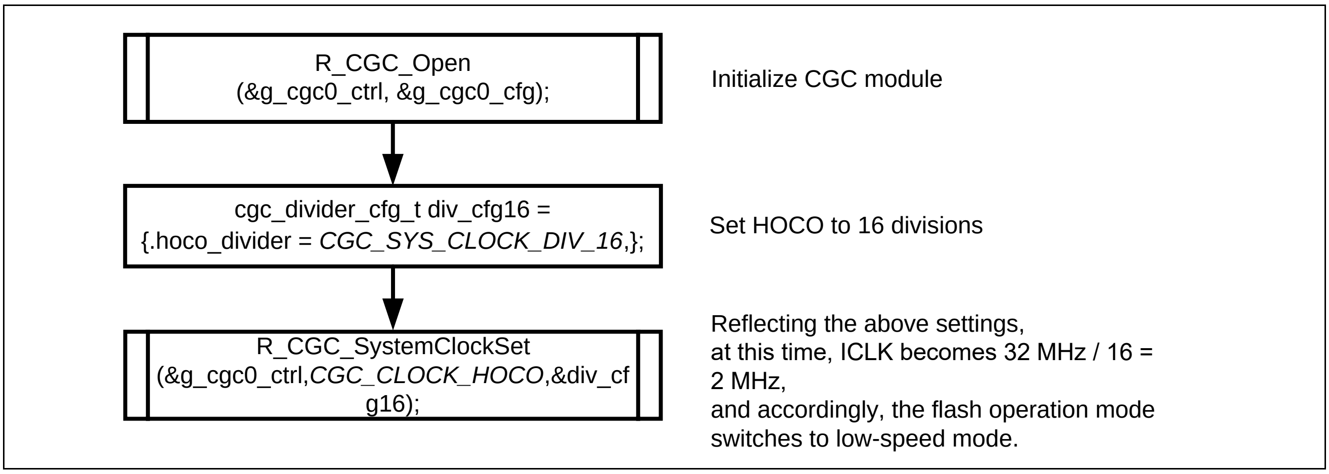

Figure 1-20 Clock frequency switching

1.5 Sub-clock oscillator drive mode

The drive strength of the sub-clock oscillator can be reduced in the order of “Normal Mode → Low Power Mode 1 → Low Power Mode 2 → Low Power Mode 3” by setting the SODRV[1:0] bits in the Clock Operation Mode Control Register (CMC). Lowering the drive strength gradually reduces the current consumed by the oscillator, allowing further reduction of overall power consumption during Sleep Mode or Software Standby Mode. Table 1-3 shows the current consumption for each sub-clock oscillator drive mode.

Table 1-3 Current consumption by sub-clock oscillator drive mode

Drive mode	SBYCR.RTCLPC = 0 (typ)[注1]	SBYCR.RTCLPC = 1 (typ)[注2]
Normal mode	0.8(μA)	0.62(μA)
Low-power mode 1	0.65(μA)	0.49(μA)
Low-power mode 2	0.51(μA)	0.34(μA)
Low-power mode 3	0.3(μA)	0.13(μA)

【Note】 1. SBYCR.RTCLPC = 0: Supplies the SOSC clock to peripherals during Software Standby or Snooze mode.
2. SBYCR.RTCLPC = 1: Does not supply the SOSC clock to peripherals other than the real-time clock during Software Standby or Snooze mode.

1.5.1 Setting Sub-clock Oscillation Drive Capability

By setting the SODRV[1:0] bits in the CMC register, the drive capability of the sub-clock oscillator can be switched between the following four levels. Figure 1-21 shows the relationship between the bits in the CMC register and the corresponding operation modes.

Bit positon	7	6	5	4	3	2	1	0
CMC	MOSEL[1:0]		-	SOSEL	XTSEL	SODRV[1:0]		MODRV

MODRV: Main clock oscillator drive capability switching
0: 1MHz ~ 10MHz
1: 10MHz ~ 20MHz

SODRV[1:0]: Sub clock oscillator drive capability switching
00: Low power mode 1
01: Normal mode
10: Low power mode 2
11: Low power mode 3

XTSEL: Clock oscillator selection
0: Port mode
1: Oscillator mode

SOSEL: Sub-clock oscillator switching
0: Port mode
1: Oscillator mode

MOSEL[1:0]: Main-clock oscillator switching
01: Oscillator mode
11: External clock mode
Other: Port mode

Figure 1-21 CMC register

1.5.2 Setting the sub-clock oscillator drive mode using FSP

Figure 1-22 shows an example of setting the sub-clock oscillator drive capability using FSP.

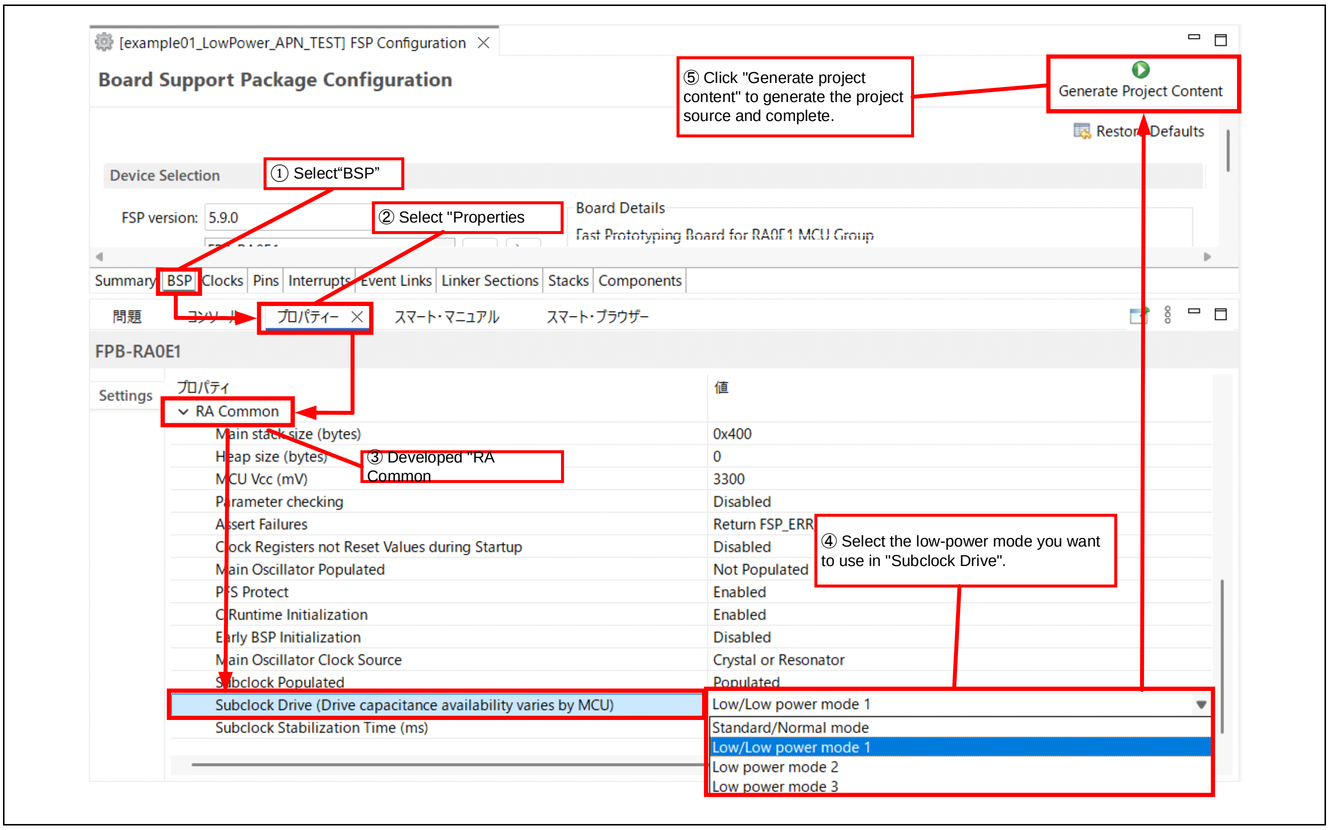

Figure 1-22 Sub-clock oscillator drive capability setting

1.6 RAM operating modes

By setting the RAM to operate in low-power mode or shutdown mode, it is possible to achieve operation with lower power consumption.

1.6.1 Setting the RAM operating mode

By setting the RAMSD[1:0] bits of the PSMCR register, you can switch the RAM operation mode. Figure 1-23 shows the relationship between the bits in the PSMCR register and the corresponding operation modes.

Bit positon	7	6	5	4	3	2	1	0
PSMCR	-	-	-	-	-	-	RAMSD[1:0]	

RAM operating mode
00: Normal mode (Continue operation)
01: Setting prohibited
10: Standby mode
11: Shutdown mode

Figure 1-23 PSMCR register

【Note】 Shutdown mode applies to all RAM except the range 0x2000_4000 to 0x2000_4FFF. RAM in the range 0x2000_4000 to 0x2000_4FFF continues operating and retains data.
【Note】 Do not access RAM while in standby mode or shutdown mode.
【Note】 When RAM returns from shutdown mode to normal mode, the contents of RAM outside the range 0x2000_4000 to 0x2000_4FFF become undefined.
【Note】 When SYOCDCR.DBGEN is set to 1, RAM does not enter shutdown mode.
【Note】 Set the RAMSD[1:0] bits. This register is protected by the PRCR.PRC1 bit.

1.6.2 Setting RAM operating mode using FSP

Since the RAM operation mode cannot be configured in FSP, it is necessary to add individual code.

Figure 1-24 shows the flow for switching from normal mode to shutdown mode, and Figure 1-25 shows the flow for switching from shutdown mode to normal mode.

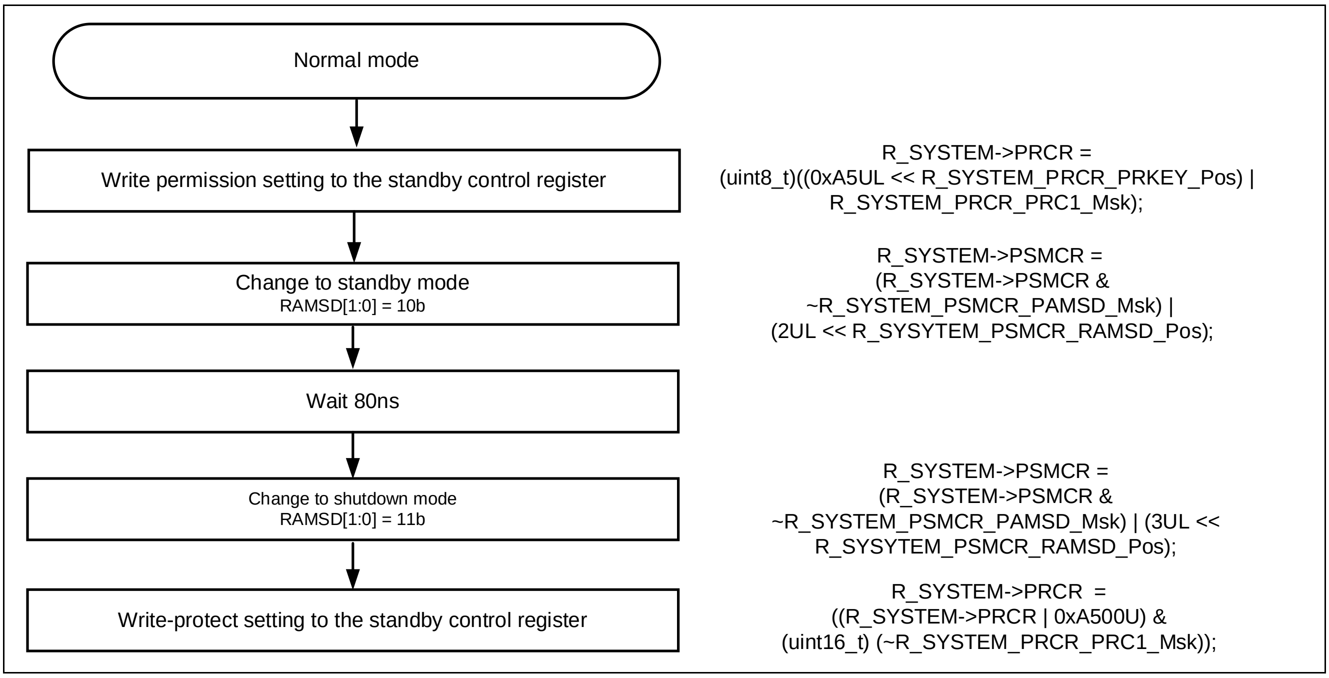

Figure 1-24 Change from normal mode to shutdown mode

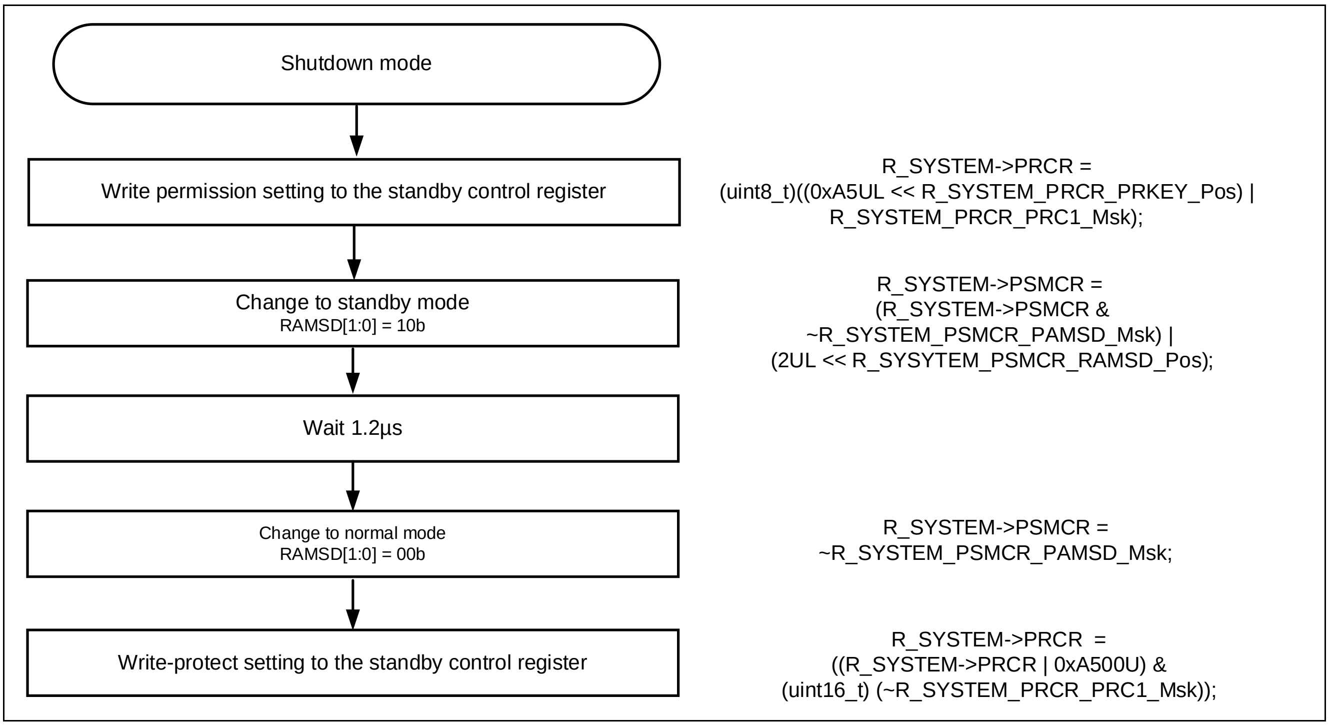

Figure 1-25 Change from shutdown mode to normal mode

【Note】 When transitioning from Shutdown mode back to Normal mode, the contents of RAM outside the range 0x2000_4000 to 0x2000_4FFF become undefined. Please initialize any RAM areas you intend to use.

1.7 A/D operating voltage mode

The ADC12 provides the following four operating voltage modes. You can adjust the balance between speed and power consumption according to your application.

- Normal Mode 1 (LV=00): Fastest conversion speed with the highest power consumption.
- Normal Mode 2 (LV=01): Slightly slower conversion speed than Normal Mode 1, but with reduced power consumption.
- Low-Voltage Mode 1 (LV=10): Achieves faster conversion than Normal Mode 2 while further reducing power consumption.
- Low-Voltage Mode 2 (LV=11): Slowest conversion speed, but with the lowest power consumption.

1.7.1 Setting the A/D operating voltage mode

By using the LV[1:0] bits in the ADM0 register, you can select the “operating voltage mode.” Depending on the LV[1:0] setting, the power supplied to the ADC12’s internal drive circuit and the number of sampling/conversion clock cycles required will change, enabling lower power consumption. Figure 1-26 shows the relationship between the ADM0 register bits and the corresponding operating modes.

Bit positon	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR[2:0]			LV[1:0]		ADCE

Select Conversion Clock (fAD)
000: PCLKB/32
001: PCLKB/16
010: PCLKB/8
011: PCLKB/4
100: PCLKB/2
101: PCLKB
Others: Setting prohibited.

A/D voltage comparator operation control
0: Stops A/D voltage comparator operation
1: Enables A/D voltage comparator operation

Select Operation voltage mode
00: Normal mode 1
01: Normal mode 2
10: Low voltage mode 1
11: Low voltage mode 2

Specification of the A/D conversion channel selection mode
0: Select mode
1: Scan mode

A/D conversion operation control
0: Stops conversion operation
1: Enables conversion operation

Figure 1-26 ADM0 register

1.7.2 Setting the A/D operating mode using FSP

Figure 1-27 shows how to configure the A/D operating voltage mode in FSP.

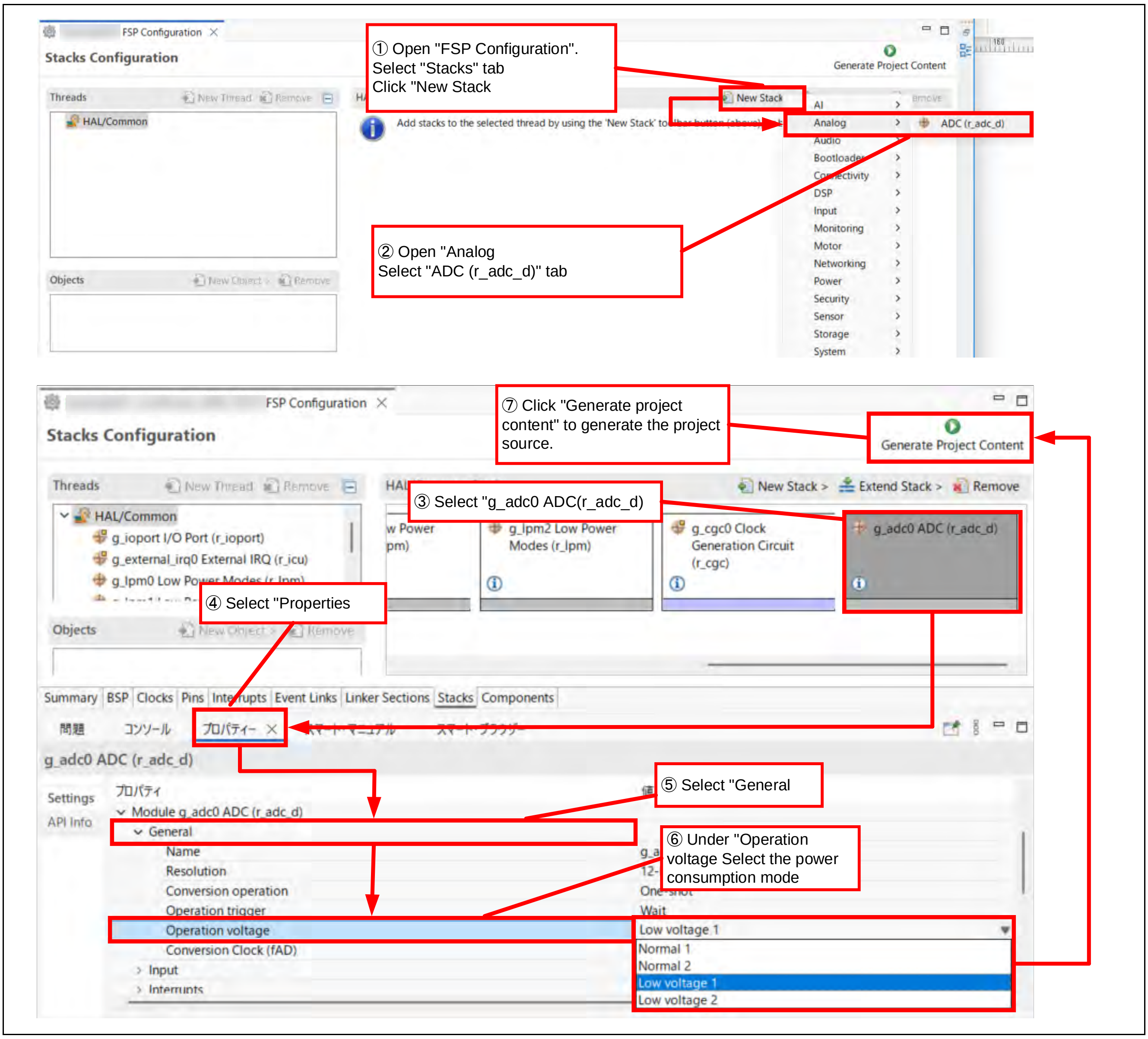

Figure 1-27 A/D operating voltage mode setting

When using Low-Voltage Mode 1 or Low-Voltage Mode 2, the A/D conversion clock frequency must be 24 MHz or lower. If the ICLK is set to 32 MHz, configure the PCLK division ratio in the Conversion Clock (fAD) settings to 2 or higher (PCLK/2, PCLK/4, PCLK/8, etc.), as shown in Figure 1-28.

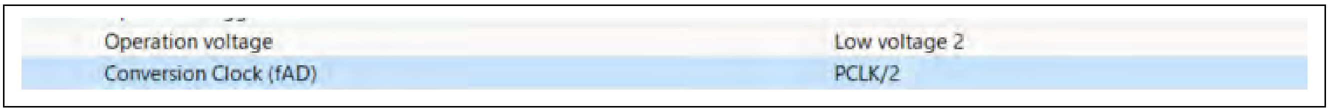

Figure 1-28 A/D conversion clock frequency setting

After configuring FSP, the operating voltage mode is set at the point when R_ADC_D_Open(adc_ctrl_t *p_ctrl, adc_cfg_t const *const p_cfg) is called in the code.

2. Precautions for achieving low power consumption

2.1 Handling of unused terminals

If unused pins are left floating, leakage current may increase, leading to higher power consumption. Therefore, for unused ports, configure pull-up or pull-down resistors when set to input mode, or release them when set to output mode, to stabilize pin levels and prevent unnecessary power usage.
This section mainly provides examples of how to configure pull-up and pull-down settings. For other configurations and details, please refer to the “Handling of Unused Pins” section in the User’s Manual: Hardware.

2.1.1 Setting up the processing of unused terminals using FSP

For RA0E1, unused pins configured as inputs among the pins belonging to ports P0x to P4x need to be properly handled to prevent the effects of noise and unnecessary current leakage.

These settings can be configured by opening the “Pins” tab in the FSP Configuration.
As a confirmation procedure, if the Mode of the target pin is set to “Input mode,” check that “Pull-up/down” is not set to “None.

As an example, in Figure 2-1, P201 is set to “Input mode” with “Input pull-up” configured, which correctly handles it as an unused pin. In this way, for RA0E1, unused pins configured as inputs on P0x to P4x should be stabilized by configuring either pull-up or pull-down resistors.

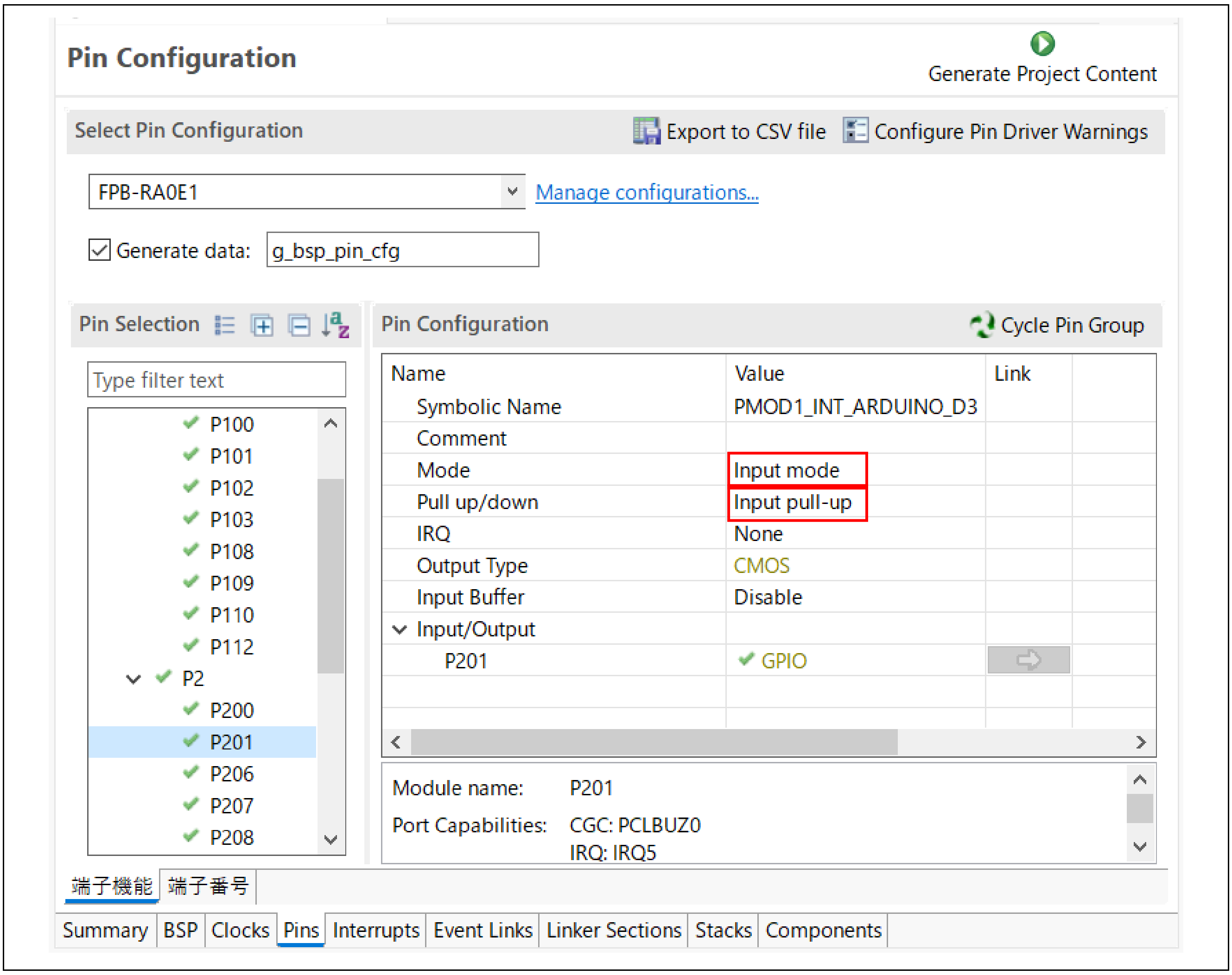

Figure 2-1 Unused terminal processing settings

2.2 Setting the Standby Control Register (SBYCR)

In addition to the SSBY bit, which sets the transition destination after executing the WFI instruction when moving from Normal mode to a low power mode, the SBYCR register also contains other settings related to low power modes. Figure 2-2 shows the relationship between the SBYCR register bits and the corresponding modes.

Bit positon	15	14	13	12	11	10	9	8
SBYCR	SSBY	-	-	-	-	-	RTCLPC	FWKUP

Software Standby Mode Select
0: Sleep mode
1: Software Standby mode.

Setting for Starting the High-speed On-chip Oscillator at the times of release from Software Standby Mode and of Transitions to Snooze Mode
0: Flash active
1: Flash stop

SOSC Setting in Software Standby Mode or in Snooze Mode
0: Enables supply of SOSC clock to peripheral functions
1: Stops supply SOSC clock to peripheral functions other than the Realtime clock

Bit positon	7	6	5	4	3	2	1	0
SBYCR	FLSTP	-	-	-	-	-	-	-

Flash Mode in Sleep Mode or in Snooze Mode
0: Flash active
1: Flash stop

Figure 2-2 SBYCR register

2.2.1 Flash operation/stop setting

By using the FLSTP bit in the Standby Control Register (SBYCR), you can select whether the flash operates or stops during Sleep mode or Snooze mode. Stopping the flash during Sleep mode or Snooze mode reduces power consumption. However, this also increases the time required to exit Sleep mode or Snooze mode, and flash programming or erasing cannot be performed.

2.2.2 Peripheral Functions Operated by Sub-clock Oscillator

By using the RTCLPC bit in the Standby Control Register (SBYCR), you can select whether to supply the SOSC clock to peripherals other than the RTC. Stopping the SOSC clock supply to peripherals other than the RTC during Software Standby mode or Snooze mode can reduce power consumption.

2.2.3 Setting the Standby Control Register using FSP

① Figure 2-3 shows how to configure the settings in FSP to stop flash operation during Sleep mode or Snooze mode. In the RA0 series, the default setting is for the flash to operate during Sleep mode or Snooze mode. Therefore, to stop flash operation, you need to follow the procedure shown in Figure 2-3.

② Figure 2-4 shows how to configure the settings in FSP to stop supplying the SOSC clock to peripherals other than the RTC during Software Standby mode or Snooze mode.

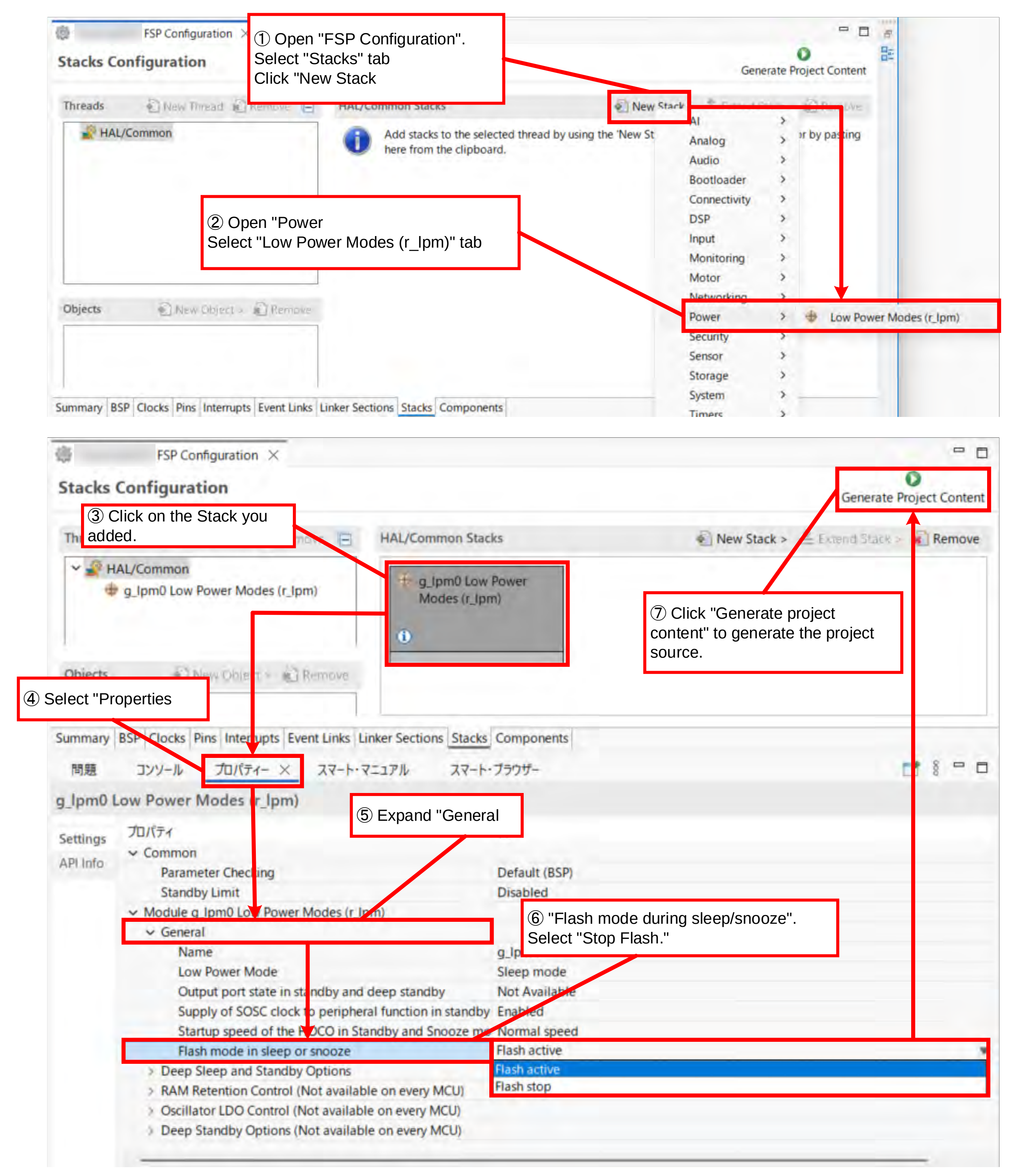

Figure 2-3 Flash operation stop setting

Please refer to Figure 1-3 and Figure 1-10 for how to configure Sleep Mode and Snooze Mode. After configuring in FSP, the flash operation stop setting will be applied when the function R_LPM_Open (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg) is called in the code.

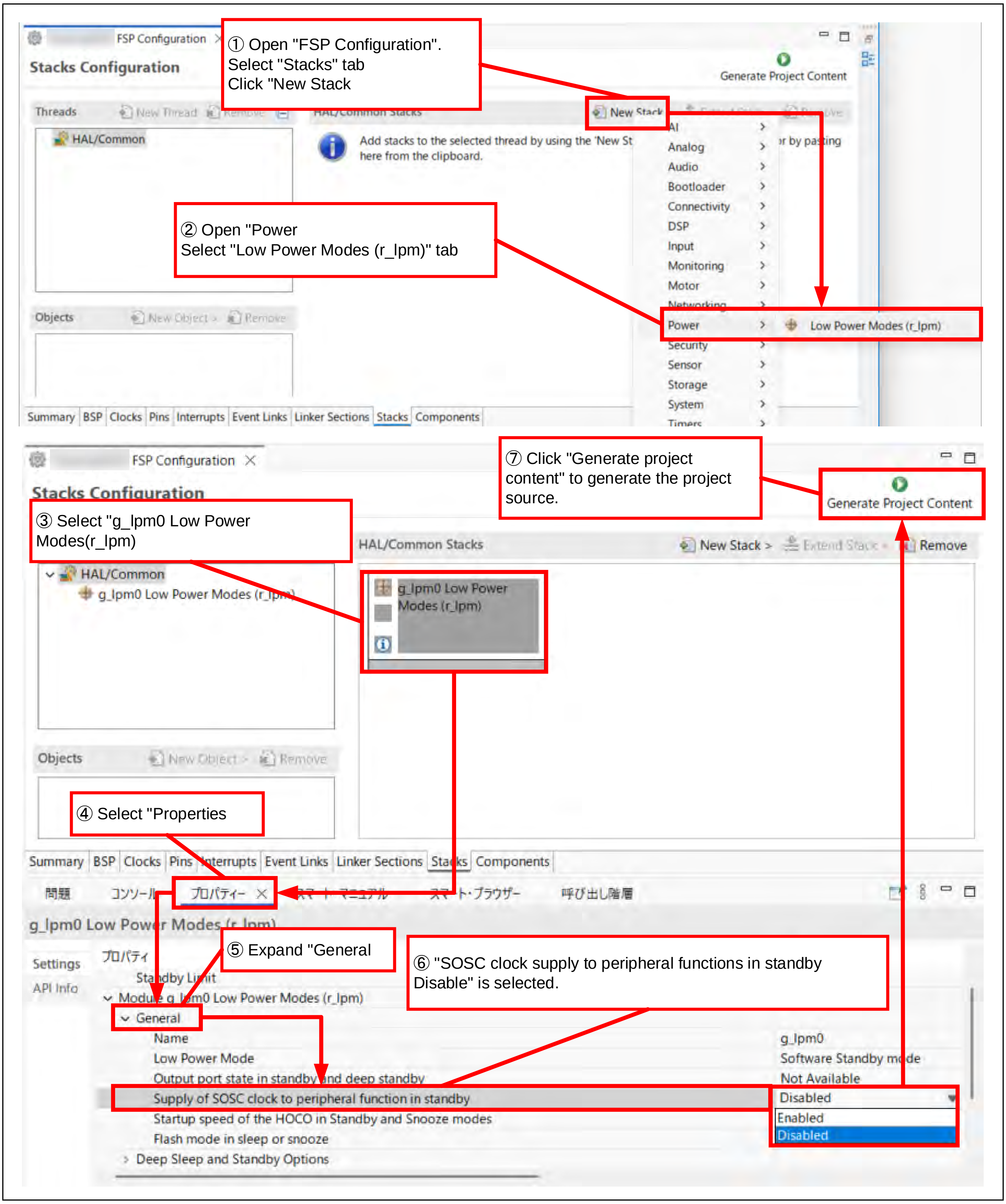

Figure 2-4 SOSC clock supply stop setting

Please refer to Figure 1-3 and Figure 1-10 for how to configure Software Standby mode and Snooze mode. After configuring FSP, the setting to stop supplying the SOSC clock to peripherals other than the RTC will be applied when R_LPM_Open (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg) is called in the code.

3. Reference documents

RA0E1 User's Manual: Hardware（R01UH1040EJ0120）

RA0E2 User's Manual: Hardware（R01UH1090EJ0110）

RA0E3 User's Manual: Hardware（R01UH1165EJ0100）

RA0L1 User's Manual: Hardware（R01UH1143EJ0110）

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025.9.3	-	Initial version
1.10	2026.3.11	-	Minor update

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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