R9A06G062GNP

RTK0EE0013D10003BJ Design data

Introduction

This document describes the design data of “Sub-GHz Wireless Communication Evaluation Kit for Japan” (RTK0EE0013D10003BJ).

The design data includes Circuit diagram, Parts list, Gerber data and Board layout diagram.

Target Device

R9A06G062GNP

Contents

1. Overview 2
1.1 Related documents 2
1.2 Appearance of the RTK0EE0013D10003BJ 2
1.3 Appearance of the RTK0EE0013D11001BJ (Daughter board) 3
1.4 Appearance of the RTK0EE0013D12001BJ (Mother board) 3
2. Configuration of Application Note 4
3. Board layer structure of the RTK0EE0013D11001BJ (Daughter board) 6
Revision History 7

1. Overview

This document aim to deliver the design data of the RTK0EE0013D10003BJ. The design data includes Circuit diagram, Parts list, Gerber data and Board layout diagram. The RTK0EE0013D10003BJ consists of a daughter board and a mother board.

1.1 Related documents

The following document is related to the application note. Also refer to this document when using this application note.

- Design Guidelines for Circuit Boards with the Sub-GHz Transceiver (R35AN0013)

1.2 Appearance of the RTK0EE0013D10003BJ

The appearance of the RTK0EE0013D10003BJ is shown in **Figure 1-1**.

Figure 1-1 : Appearance of the RTK0EE0013D10003BJ

1.3 Appearance of the RTK0EE0013D11001BJ (Daughter board)

The appearance of the RTK0EE0013D11001BJ is shown in **Figure 1-2**.

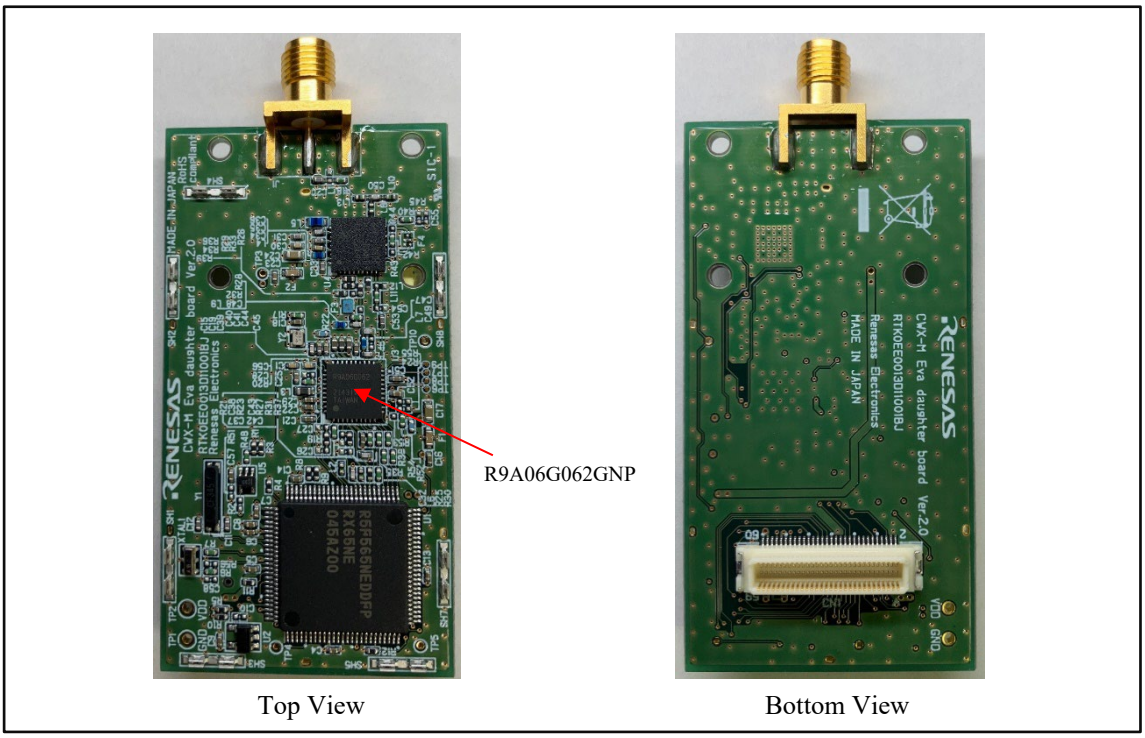

Figure 1-2 : Appearance of the RTK0EE0013D11001BJ (Daughter board)

1.4 Appearance of the RTK0EE0013D12001BJ (Mother board)

The appearance of the RTK0EE0013D12001BJ is shown in **Figure 1-3**.

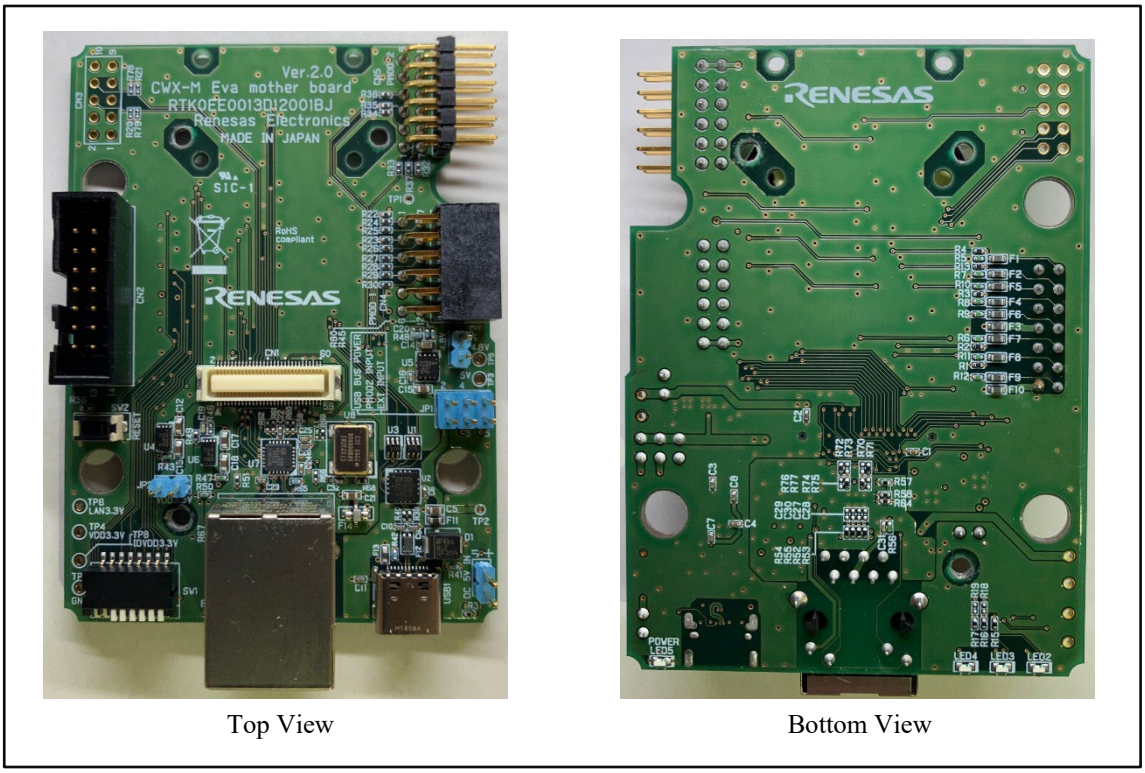

Figure 1-3 : Appearance of the RTK0EE0013D12001BJ (Mother board)

2. Configuration of Application Note

This Application Note contains the following contents listed in **Table 2-1** and **Table 2-2**.

Table 2-1 : Configuration of Application Note-1

File organization	Description
r02an0047ej0100-sub-ghz.pdf	This application note
RTK0EE0013D10003BJ_Design_Data	
01_Daughter board	
01_Circuit_Diagram	
RTK0EE0013D11001BJ_Circuit_Diagram.pdf	Circuit diagram
02_Parts_List	
RTK0EE0013D11001BJ_Parts_List.pdf	Parts list
03_Gerber_Data	
RTK0EE0013D11001BJ_LA.G01	L1: Analog signal, Parts layer
RTK0EE0013D11001BJ_L2.G02	L2: GND layer
RTK0EE0013D11001BJ_L3.G03	L3: Power supply, GND layer
RTK0EE0013D11001BJ_LB.G04	L4: Digital signal, GND layer
RTK0EE0013D11001BJ_RA.G05	L1: Resist
RTK0EE0013D11001BJ_RB.G06	L4: Resist
RTK0EE0013D11001BJ_SA.G07	L1: Silk
RTK0EE0013D11001BJ_SB.G08	L4: Silk
RTK0EE0013D11001BJ_GA.G09	Dimensions
RTK0EE0013D11001BJ_MA.G11	L1: Solder Mask
RTK0EE0013D11001BJ_MB.G12	L4: Solder Mask
RTK0EE0013D11001BJ_HO.dr1	Drill data
04_Board_Layout_Diagram	
RTK0EE0013D11001BJ_Board_Layout_Diagram.pdf	Board layout diagram

Table 2-2 : Configuration of Application Note-2

File organization	Description
r02an0047ej0100-sub-ghz.pdf	This application note
RTK0EE0013D10003BJ_Design_Data	
02_Mother board	
01_Circuit_Diagram	
RTK0EE0013D12001BJ_Circuit_Diagram.pdf	Circuit diagram
02_Parts_List	
RTK0EE0013D12001BJ_Parts_List.pdf	Parts list
03_Gerber_Data	
RTK0EE0013D12001BJ_LA.G01	L1: Signal, Parts layer
RTK0EE0013D12001BJ_L2.G02	L2: GND layer
RTK0EE0013D12001BJ_L3.G03	L3: Power supply layer
RTK0EE0013D12001BJ_LB.G04	L4: Signal, Parts layer
RTK0EE0013D12001BJ_RA.G05	L1: Resist
RTK0EE0013D12001BJ_RB.G06	L4: Resist
RTK0EE0013D12001BJ_SA.G07	L1: Silk
RTK0EE0013D12001BJ_SB.G08	L4: Silk
RTK0EE0013D12001BJ_GA.G09	Dimensions
RTK0EE0013D12001BJ_MA.G11	L1: Solder Mask
RTK0EE0013D12001BJ_MB.G12	L4: Solder Mask
RTK0EE0013D12001BJ_HO.dr1	Drill data
04_Board_Layout_Diagram	
RTK0EE0013D12001BJ_Board_Layout_Diagram.pdf	Board layout diagram

3. Board layer structure of the RTK0EE0013D11001BJ (Daughter board)

The board layer structure is shown in **Figure 3-1** and **Figure 3-2**. This daughter board is designed with a 4-layer board.

Board material : ELC-4765 (SUMITOMO BAKELITE CO.,LTD.)

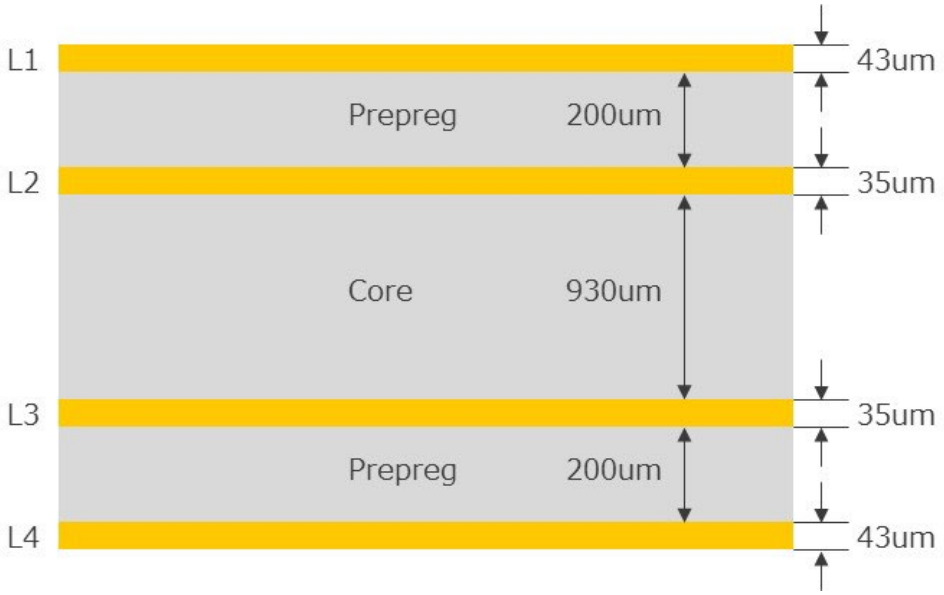

Figure 3-1 : Board layer structure

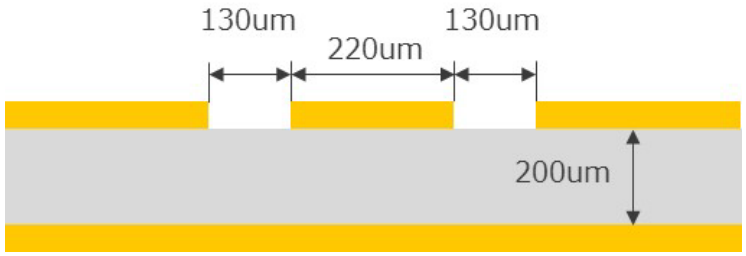

Figure 3-2 : RF unit 50 Ohm impedance line

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan 31, 2023		First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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