R8C/M13B Group

IrDA Infrared Communication

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Introduction

This application note describes a method for performing IrDA communication using the R8C/M13B Group serial interface (UART0) and Infrared Data Association (IrDA) interface.

Target Device

R8C/M13B Group

Contents

1. Specifications

- Transmit and receive 4 bytes of data using the IrDA communication function.
- Use channel 0 for the serial interface.
- Set 8-bit data length and 1-bit stop bit length for the communication data format.
- Set LSB first for the transfer format.
- Set 9600 bps for the bit rate.

2. Applicable Conditions

Table 2.1 Applicable Conditions

Item	Description
Operating frequencies	• XIN clock: 19.6608 MHz • System base clock (fBASE): 19.6608 MHz • System clock (f): 19.6608 MHz • CPU clock (fs): 19.6608 MHz
Operating mode	High-speed clock mode
Development tool	Manufactured by Renesas Electronics High-performance Embedded Workshop Version 4.07
C/C++ compiler	Manufactured by Renesas Electronics M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options	-D__UART0__–c –finfo –dir “$(CONFIGDIR)” –R8C (Use the default setting of High-performance Embedded Workshop.)

3. Operations

3.1 Transmission

Figure 4 shows the transmit operation. Transmission in IrDA communication is performed through the software processing shown in Figure 3.1. In this application note, 4 bytes of data (00h, 33h, 55h, and AAh) are transmitted.

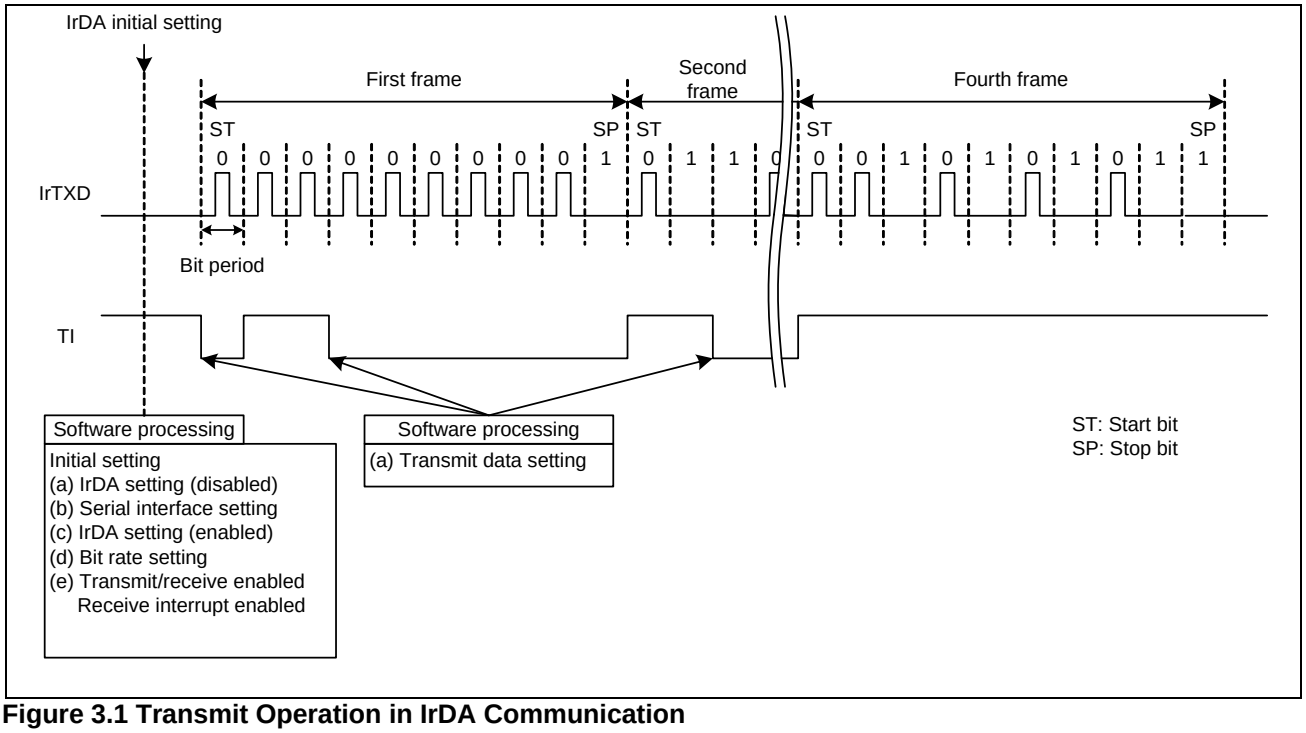


Figure 3.1 Transmit Operation in IrDA Communication

3.2 Reception

Figure 3.2 shows the receive operation. Reception in IrDA communication is performed through the software processing shown in Figure 3.2.

In this application note, reception is performed using receive interrupts. After 4 bytes of data is received, the receive interrupts are disabled and reception is completed.

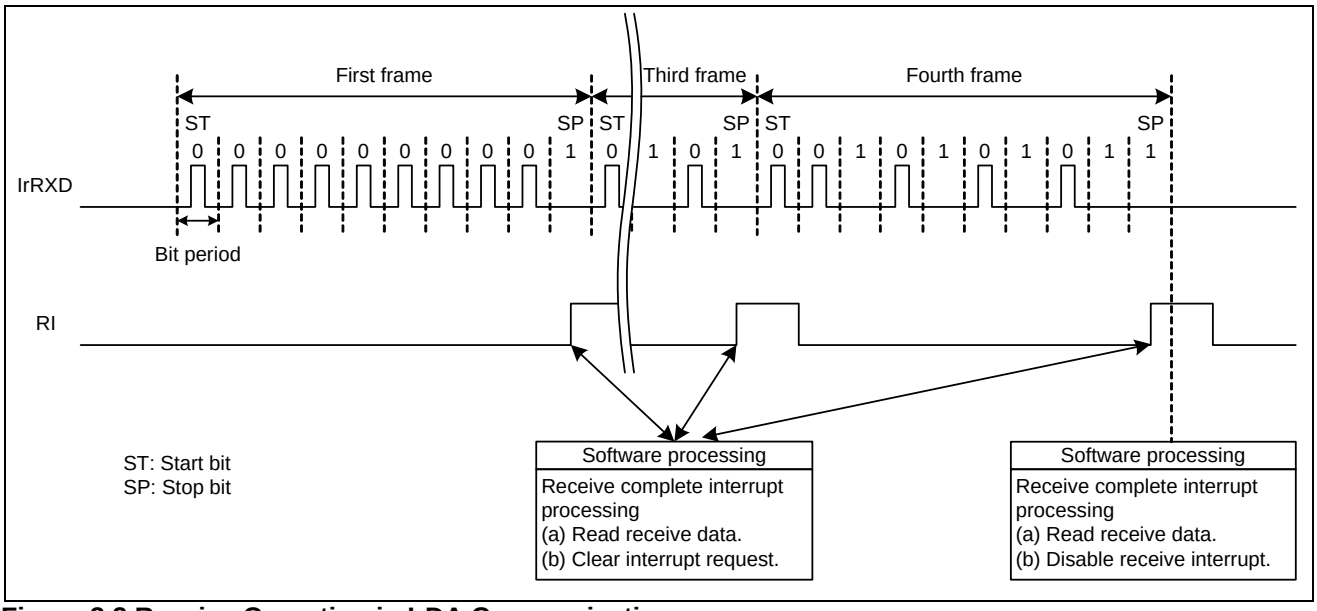


Figure 3.2 Receive Operation in IrDA Communication

4. Software

4.1 Functions

Table 4.1 Functions

Function Name	Function
main	Main routine Initialize the receive buffer and transmit the transmit data.
mcu_init	System clock setting Perform the clock setting.
irda_init	IrDA interface initial setting Perform the initial setting to use the IrDA interface.
_uart0_receive	UART0 receive interrupt handling When a receive error is detected during reception, disable transmission and reception, and the serial interface.

4.2 Internal Registers

Module Standby Control Register (MSTCR) **Address: 00012h**

Bit	Symbol	Bit Name	Setting	Function	R/W
6	MSTUART0	UART0 standby bit	0	0: Active	R/W

Protect Register (PRCR) **Address: 00013h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0	PRC0	Protect bit 0	0/1	Writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2 0: Disabled 1: Enabled	R/W

Module Standby Control Register 1 (MSTCR1) **Address: 00017h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0	MSTIRDA	IrDA standby bit	0	0: Active	R/W

External Clock Control Register (EXCKCR) **Address: 00020h**

Bit	Symbol	Bit Name	Setting	Function		R/W
0	CKPT0	P3_1 and P4_5 pin function select bits	1	P3_1 pin 1 1: XIN	P4_5 pin 1 1: XOUT	R/W
1	CKPT1		1			

On-Chip Oscillator Control Register (OCOCR) **Address: 00021h**

Bit	Symbol	Bit Name	Setting	Function	R/W
1	LOCODIS	Low-speed on-chip oscillator oscillation stop bit	0	0: Low-speed on-chip oscillator on	R/W

System Clock f Control Register (SCKCR) **Address: 00022h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0	PHISSEL0	CPU clock division ratio select bits	0	These bits are used to select the division ratio of the system clock (f) to generate the CPU clock (fs). b2 b1 b0 0 0 0: fs = System clock with no division	R/W
1	PHISSEL1		0		R/W
2	PHISSEL2		0		R/W
6	HSCKSEL	High-speed on-chip oscillator/XIN clock select bit	0	0: XIN clock	R/W

System Clock f Select Register (PHISEL) **Address: 00023h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0 to 7	PHISEL0 to PHISEL7	System clock division select bits	00h	These bits are used to set the division ratio of the system base clock (fBASE) to generate the system clock (f) and the A/D converter clock (fAD). • System clock (f) f = fBASE/(n + 1)	R/W

Clock Stop Control Register (CKSTPR) **Address: 00024h**

Bit	Symbol	Bit Name	Setting	Function	R/W
7	SCKSEL	System base clock select bit	1	1: fHSCK	R/W

Interrupt Priority Level Register 9 (ILVL9) **Address: 00049h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0	ILVL90	UART0 reception interrupt priority level setting bits	0/1	b5 b4 0 0: Level 0 (interrupt disabled) 0 1: Level 1	R/W
1	ILVL91		1		R/W

UART0 Transmit/Receive Mode Register (U0MR) **Address: 00080h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0	SMD0	Serial I/O mode select bits	0/1	b2 b1 b0 0 0 0: Serial interface disabled 1 0 1: UART mode, transfer data 8 bits long	R/W
1	SMD1		0		R/W
2	SMD2		0/1		R/W
3	CKDIR	Internal/external clock select bit	0	0: Internal clock	R/W
4	STPS	Stop bit length select bit	0	0: 1 stop bit	R/W
5	PRY	Odd/even parity select bit	0	0: Odd parity	R/W
6	PRYE	Parity enable bit	0	0: Parity disabled	R/W

UART0 Bit Rate Register (U0BRG) **Address: 00081h**

Bit	Function	Setting Range	R/W
0 to 7	If the set value is n, U0BRG divides the count source by n + 1.	7Fh	W

UART0 Transmit Buffer Register (U0TB) **Address: 00082h**

Bit	Symbol	Function	R/W
0 to 8	–	Transmit data	W

UART0 Transmit/Receive Control Register 0 (U0C0) **Address: 00084h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0	CLK0	U0BRG count source select bits	0	b1 b0 0 0: f1	R/W
1	CLK1		0		R/W
4	DFE	RXD0 digital filter enable bit	0	0: Digital filter disabled	R/W
5	NCH	Data output select bit	0	0: TXD0 pin is set to CMOS output	R/W
7	UFORM	Transfer format select bit	0	0: LSB first	R/W

UART0 Transmit/Receive Control Register 1 (U0C1) Address: 00085h

Bit	Symbol	Bit Name	Setting	Function	R/W
0	TE	Transmit enable bit	0/1	0: Transmission disabled 1: Transmission enabled	R/W
1	TI	Transmit buffer empty flag	–	0: Data present in the U0TB register 1: The U0TB register empty	R
2	RE	Receive enable bit	0/1	0: Reception disabled 1: Reception enabled	R/W
3	RI	Receive complete flag	–	0: The U0RB register empty 1: Data present in the U0RB register	R
4	U0IRS	UART0 transmit interrupt source select bit	0	0: Transmit buffer is empty (TI = 1)	R/W
5	U0RRM	UART0 continuous receive mode enable bit	0	0: Continuous receive mode disabled	R/W

UART0 Receive Buffer Register (U0RB) Address: 00086h

Bit	Symbol	Bit Name	Function	R/W
0 to 8	–	Receive data		R
12	OER	Overrun error flag	0: No overrun error has occurred 1: An overrun error has occurred	R
13	FER	Framing error flag	0: No framing error has occurred 1: A framing error has occurred	R
14	PER	Parity error flag	0: No parity error has occurred 1: A parity error has occurred	R
15	SUM	Error sum flag	0: No error has occurred 1: An error has occurred	R

UART0 Interrupt Flag and Enable Register (U0IR) Address: 00088h

Bit	Symbol	Bit Name	Setting	Function	R/W
2	U0RIE	UART0 receive interrupt enable bit t	0/1	0: Receive interrupt disabled 1: Receive interrupt enabled	R/W
3	U0TIE	UART0 transmit interrupt enable bit	0	0: Transmit interrupt disabled	R/W
6	U0RIF	UART0 receive interrupt flag	0/1	0: No receive interrupt requested 1: Receive interrupt requested	R/W

Port 1 Function Mapping Register 1 (PMH1) **Address: 000C9h**

Bit	Symbol	Bit Name	Setting	Function	R/W
0	P14SEL0	Port P1_4 function select bits	0/1	bx b1 b0 0 0 0: I/O port or AN4 input 0 0 1: TXD0/IrTXD (bx: P14SEL2 bit in the PMH1E register)	R/W
1	P14SEL1		0		R/W
2	P15SEL0	Port P1_5 function select bits	1	bx b3 b2 0 0 1: RXD0/IrRXD (bx: P15SEL2 bit in the PMH1E register)	R/W
3	P15SEL1		0		R/W

Port 1 Function Mapping Expansion Register (PMH1E) **Address: 000D1h**

Bit	Symbol	Setting	Function	R/W
0	P14SEL2	0	The P1_4 pin function is selected in conjunction with bits P14SEL0 to P14SEL1 in the PMH1 register.	R/W
2	P15SEL2	0	The P1_5 pin function is selected in conjunction with bits P15SEL0 to P15SEL1 in the PMH1 register.	R/W

IrDA Control Register (IRCR) **Address: 0019Ch**

Bit	Symbol	Bit Name	Setting	Function	R/W
1	UART_SEL	UART0 or UART1 select bit	0	0: UART0	R/W
2	IRRXINV	IrRXD data inversion bit	0	0: IrRXD input is used as receive data without modification	R/W
3	IRTXINV	IrTXD data inversion bit	0	0: Transmit data is output from IrTXD without modification	R/W
4	IRCKS0	IrDA clock select bits	0	b6 b5 b4 0 0 0: Pulse width = B × 3/16 (3/16 of the bit rate)	R/W
5	IRCKS1		0		R/W
6	IRCKS2		0		R/W
7	IRE	IrDA enable bit	1	1: IrDA enabled (TXD/IrTXD pin functions as IrTXD pin, and RXD/IrRXD pin functions as IrRXD pin)	R/W

4.3 Constant

Table 4.2 Constant

Label Name	Constant	Description	Function Name
DATA_NUM	4	Number of transmit/receive data bytes	main

4.4 Data Table

Table 4.3 Data Table

Label Name	Description	Memory size	Function Name
t_buf []	Array of transmit data {00h, 33h, 55h, AAh}	4 bytes	main

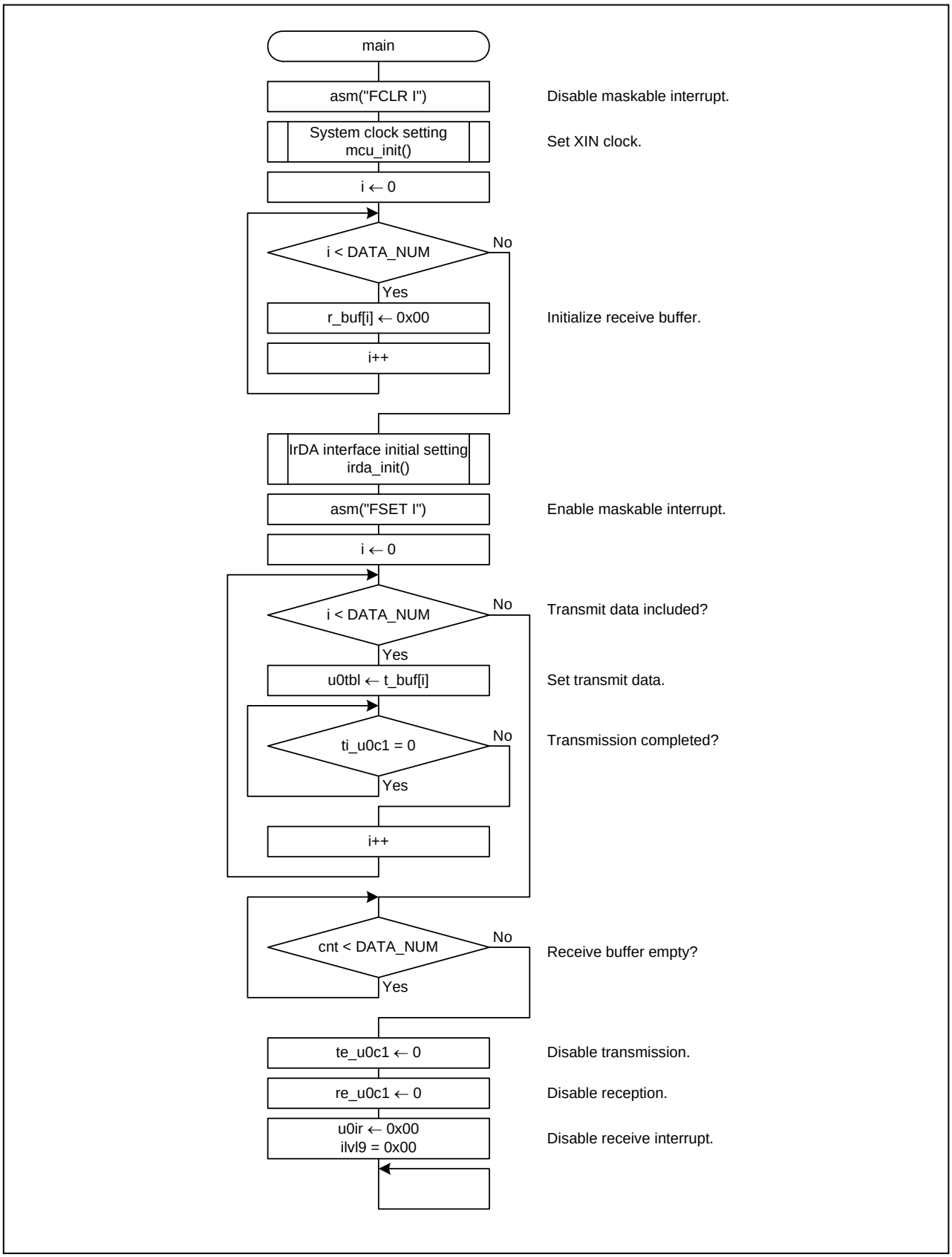
4.5 RAM Usage

Table 4.4 RAM Usage

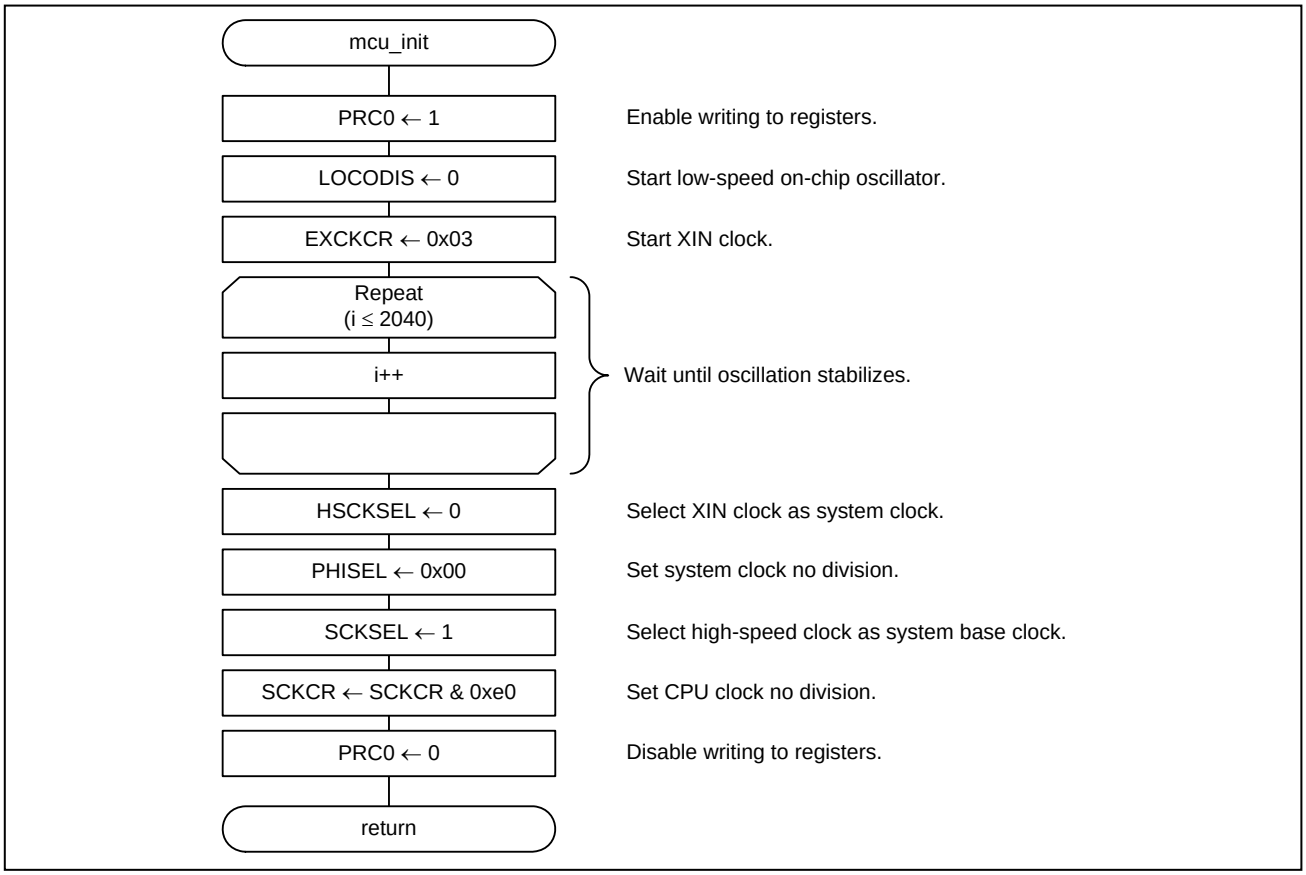
Label Name	Description	Memory size	Function Name
cnt	Counter for the number of received data	1 byte	main, _uart0_receive
r_buf []	Buffer for storing received data	4 bytes	main, _uart0_receive
er_buf []	Buffer for storing receive error flag	4 bytes	_uart0_receive

5. Flowcharts

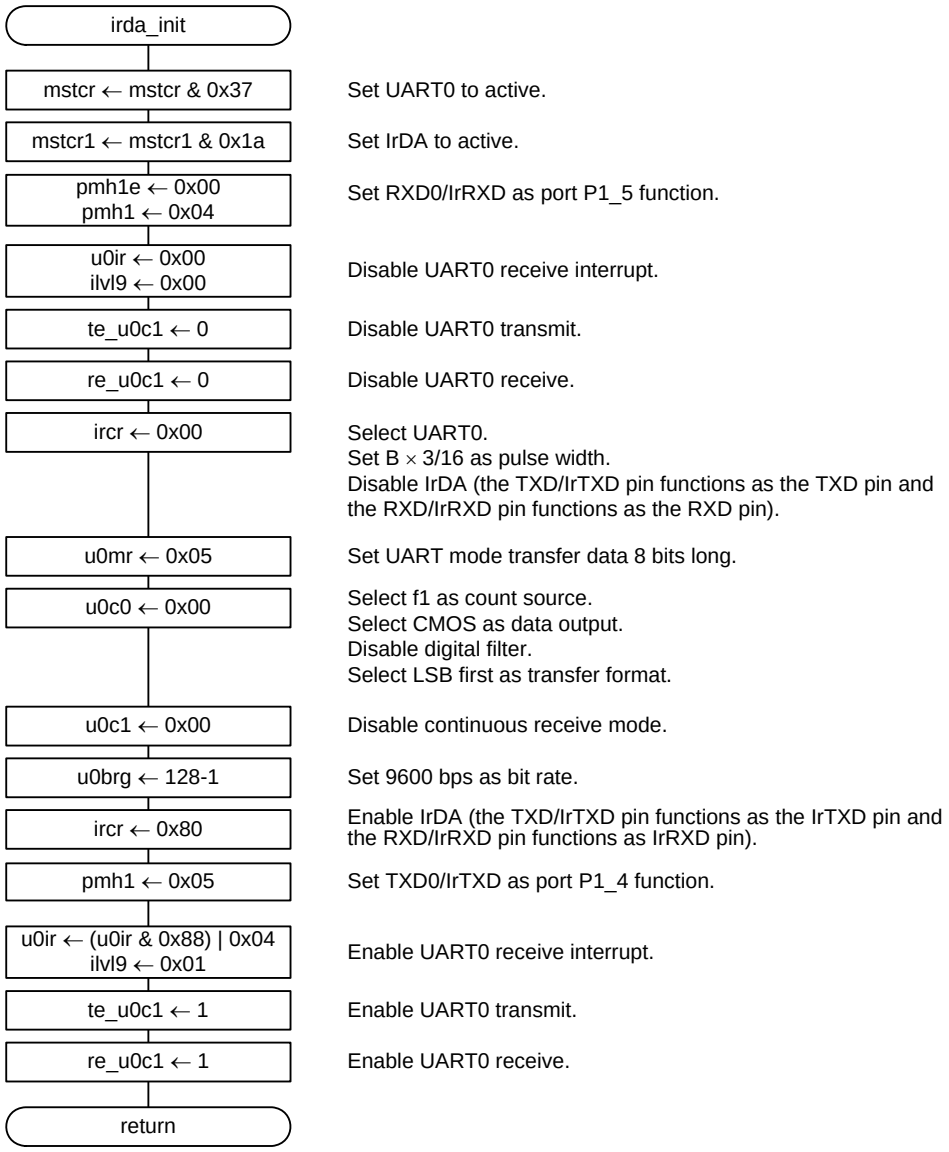
5.1 main Function



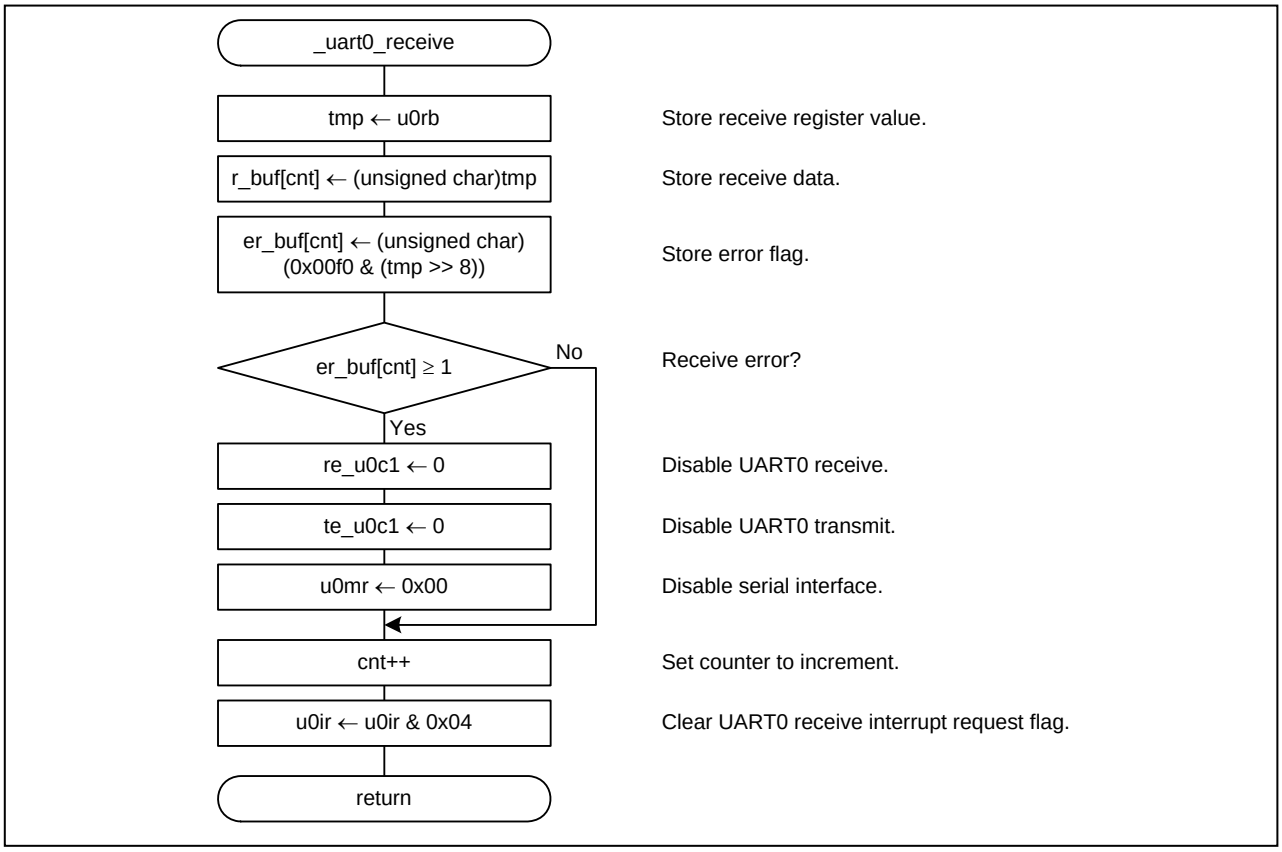
5.2 mcu_init Function



5.3 irda_init Function



5.4 _uart0_receive Function



6. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

7. Reference Documents

R8C/M13B Group User’s Manual: Hardware Rev.1.00

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar. 10, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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