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R8C/35C Group

A/D Key Read

1. Abstract

This document describes the setting method and an application example to perform multiple key inputs via a single analog input using the A/D convertor (one-shot mode).

2. Introduction

The application example described in this document applies to the following MCU and parameters.

- MCU : R8C/35C Group
- VCC/AVCC, VREF : 5 V

The sample program in this application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

3.1 Program Outline

As Figure 3.1 shows, connect an analog input pin (one pin) with more than one key and resistor so the voltage applied to the analog input pin varies according to the key pressed.

The analog voltage input to the P0_7/AN0 pin is A/D converted every 5 ms. After A/D conversion is performed 10 times, add the conversion results together, then subtract the largest and smallest values. Dividing this value by 8 (averaging) results in the A/D determination value. This means the A/D determination value is fixed every 50 ms.

Use the A/D conversion determination value to identify which key is pressed. Each key has a corresponding key code. Compare this key code with the key code calculated previous time. If they are same, set this key code as the determined key code.

Main settings

- Select the P0_7/AN0 pin for analog input
- Select one-shot mode as the A/D operating mode
- Select f1 as the fAD clock source
- Select fAD divided-by-2 as the ϕAD operation clock
- Select 10-bit resolution
- Select a software trigger as the A/D conversion start condition
- Disable the A/D open-circuit detection assist function
- Generate the measure period in timer RA

Figure 3.1 shows a connection example of keys, Table 3.1 lists the values and key codes used for key determination, Figure 3.2 shows the block diagram of A/D converter, and Table 3.2 lists the pin used and its function.

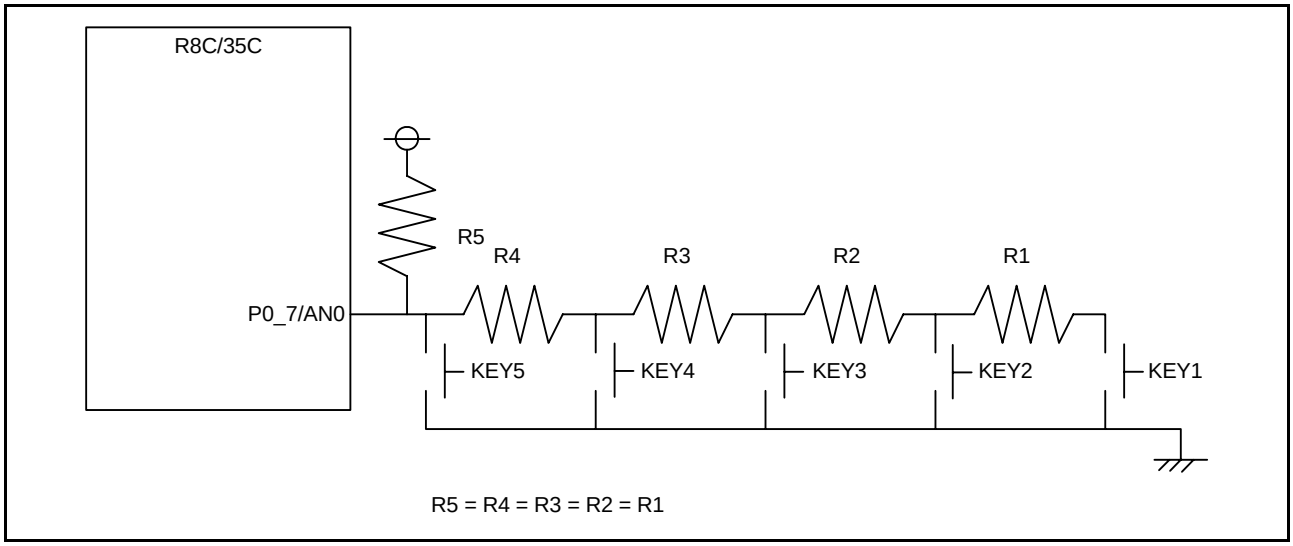


Figure 3.1 Connection Example of Keys

Table 3.1 Values and Key Codes Used for Key Determination

Pressed Key	No Key	KEY 1	KEY 2	KEY 3	KEY 4	KEY 5
Desired AN0 voltage value	5 V	4 V	3.75 V	3.333 V	2.5 V	0 V
Desired A/D conversion value	1023	820	769	684	514	0
Value for determination	1023 to 921	920 to 794	793 to 726	725 to 599	598 to 257	256 to 0
Key code	0	1	2	3	4	5

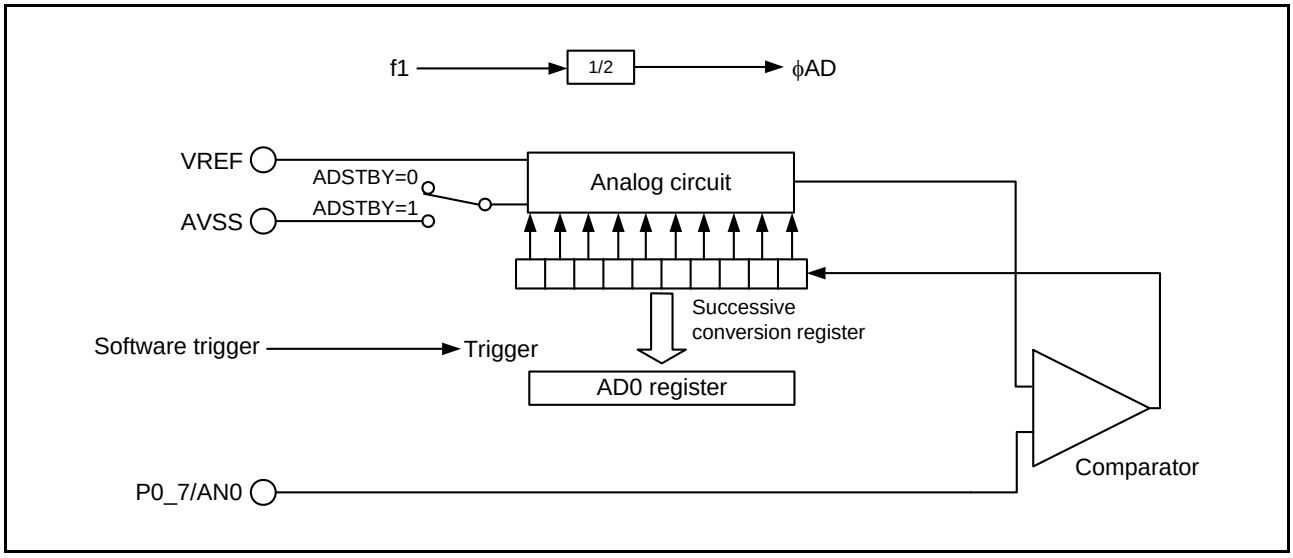


Figure 3.2 A/D Converter Block Diagram

Table 3.2 Pin and Function

Pin Name	I/O	Function
P0_7/AN0	Input	A/D key input

3.1.1 Memory

Table 3.3 Memory

Memory	Size	Remarks
ROM	402 bytes	In the rej05b1331_src.c module
RAM	14 bytes	In the rej05b1331_src.c module
Maximum user stack	9 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options. The above applies to the following conditions:

C compiler: M16C/60, 30, 20, 10, and Tiny and R8C/Tiny Series Compiler V.5.45 Release 00
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35C Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (high-speed on-chip oscillator).		

Declaration	void timer_ra_init(void)		
Outline	Timer RA associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the SFR registers to use timer RA in timer mode.		

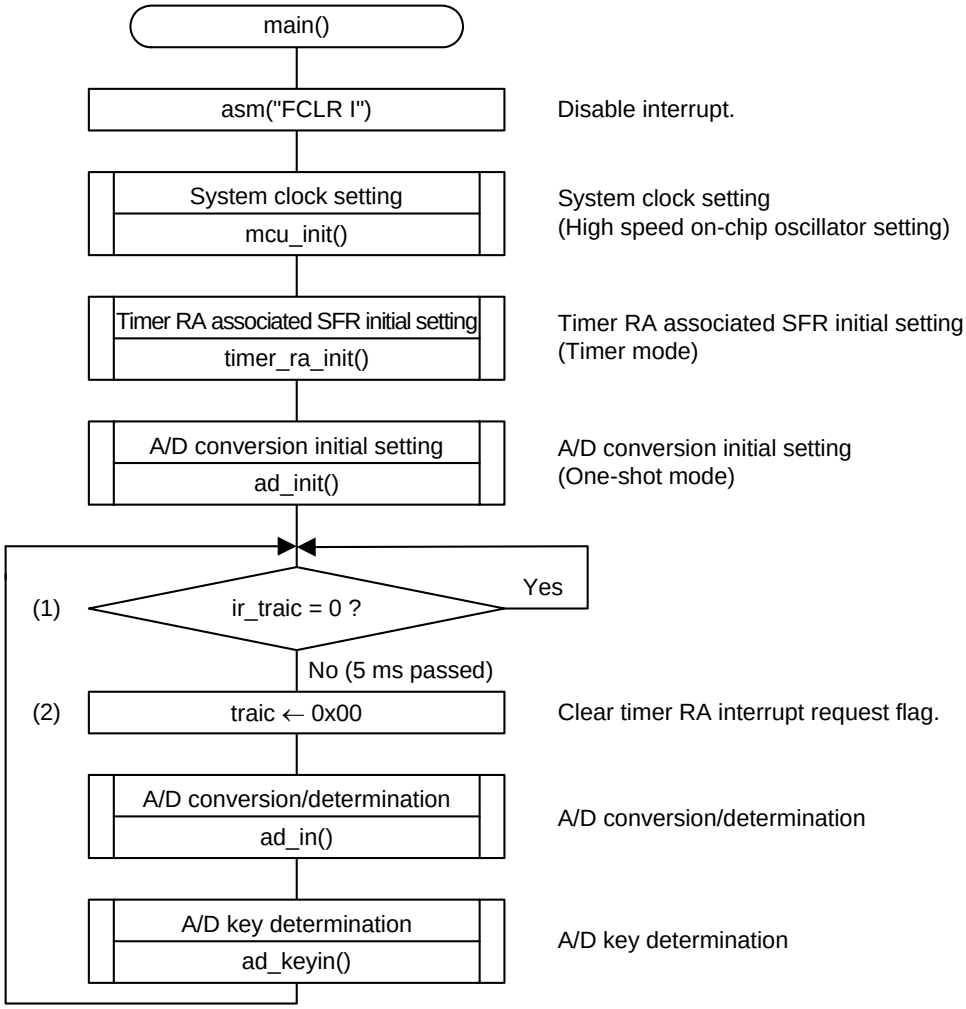
Declaration	void _ad_init(void)		
Outline	A/D conversion initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the SFR registers to use A/D conversion in one-shot mode.		

Declaration	void ad_in(void)		
Outline	A/D conversion/determination		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char f_ad_fix		A/D value determination flag
	unsigned short ad_fix		A/D determination value
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform A/D conversion and calculate A/D determination value. A/D determination value is calculated by averaging the A/D conversion results after subtracting the largest and smallest value from the sum of 10-time A/D conversion results.		

Declaration	void ad_keyin(void)		
Outline	A/D key determination		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char f_ad_fix		A/D value determination flag
	unsigned short ad_fix		A/D determination value
	unsigned char ad_key_code		Determined key code
	unsigned char last_ad_fix		Previous fixed key code
Returned value	Type	Value	Meaning
	None	—	—
Function	Compare current key code to the previous key code. If they are same, set the current key code as the determined key code.		

4.2 Main Function

• Flowchart



• Register Setting

(1) Wait until an timer RA interrupt request is generated.

(2) Clear an timer RA interrupt request flag.

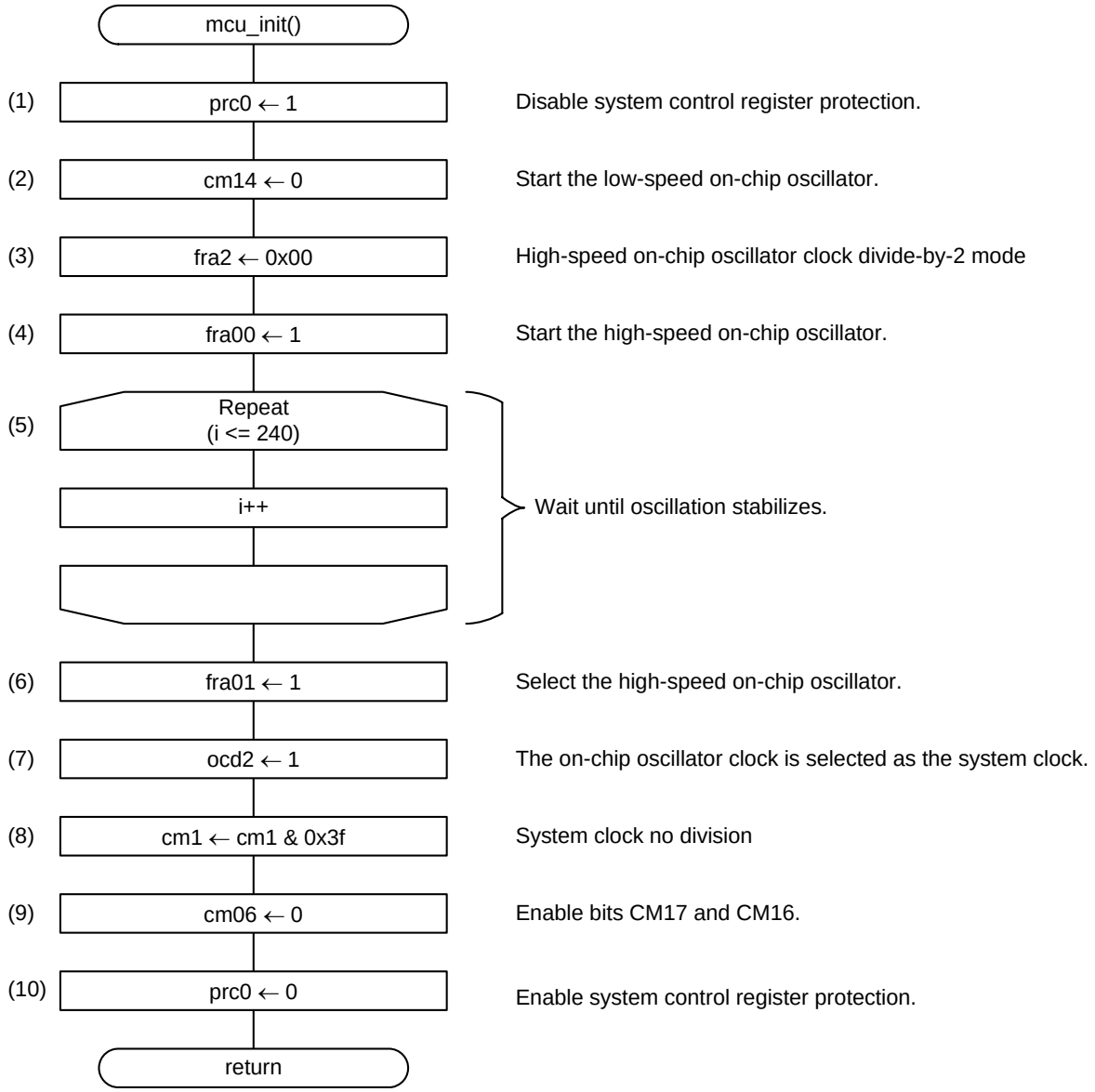
Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

4.3 System Clock Setting

- Flowchart



• Register Setting

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

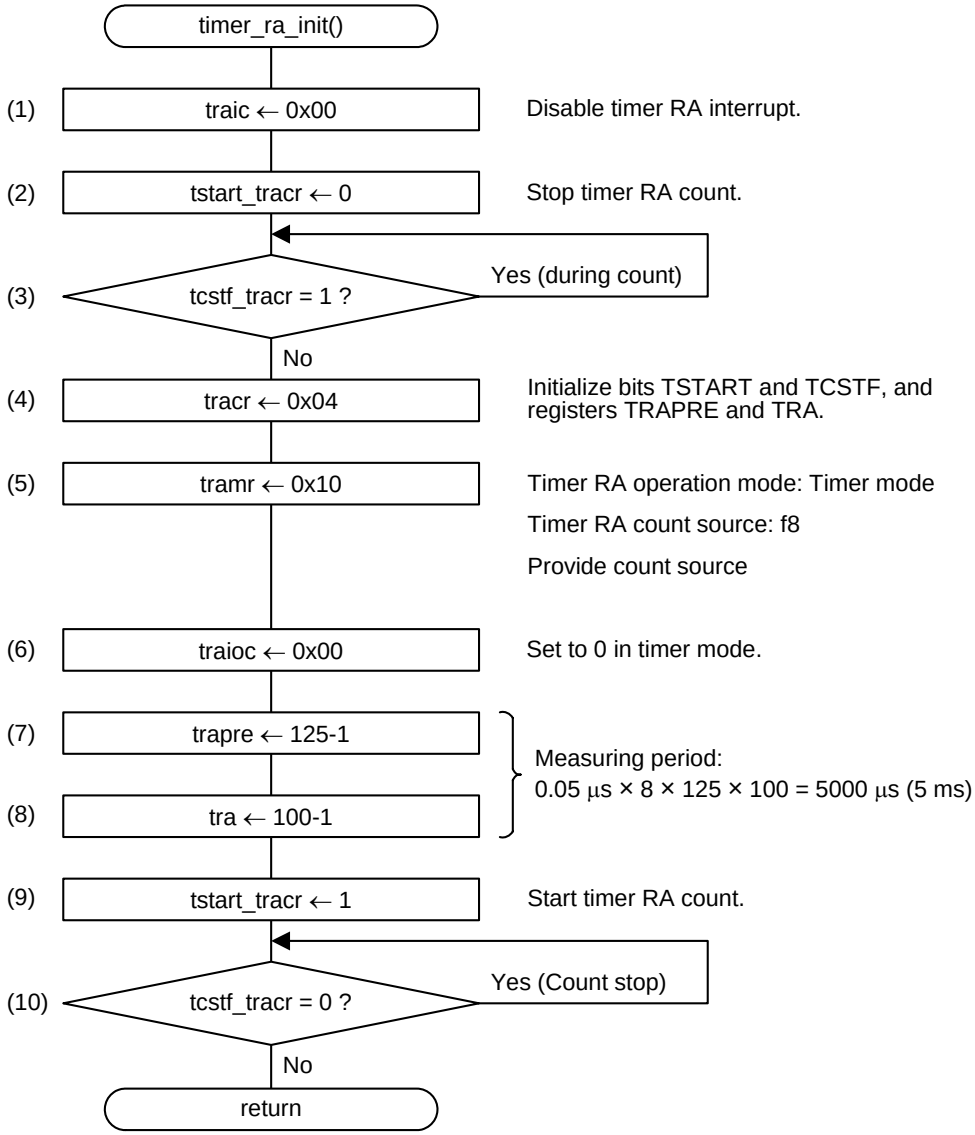
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Timer RA associated SFR initial setting

- Flowchart



• Register Setting

(1) Disable an timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(2) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(3) Wait until timer RA count stops.

(4) Initialize bits TSTART and TCSTF, and registers TRAPRE and TRA register.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	0	—	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops	R
b2	TSTOP	Timer RA count forcible stop bit	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W
b4	TEDGF	Active edge judgment flag	0: Active edge not received	R/W
b5	TUNDF	Timer RA underflow flag	0: No underflow	R/W

(5) Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 1: f8	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source	R/W

(6) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAIOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. When using hardware LIN function, set to 1.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

(7) Set “125-1” (7Ch) to the timer RA prescalor register.

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	1	1	1	1	0	0

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W

(8) Set “100-1” (63h) to the timer RA register.

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	1	0	0	0	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts on underflow of TRAPRE register	00h to FFh	R/W

(9) Start timer RA counter.

Timer RA Control Register (TRACR)

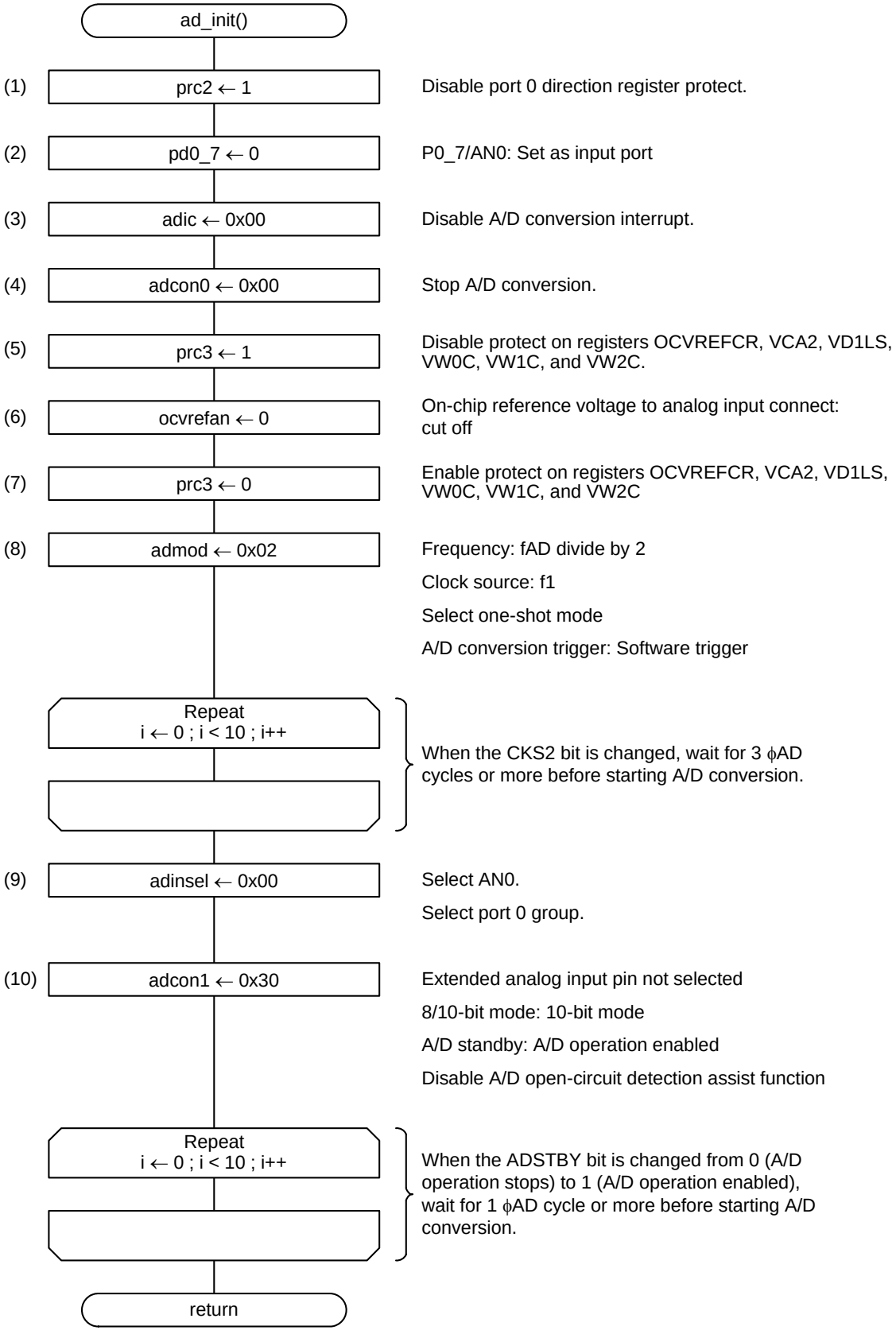
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

(10) Wait until timer RA counter starts.

4.5 A/D Conversion Initial Setting

- Flowchart



• Register Setting

(1) Enable writing to the port 0 direction register.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 1: Write enabled	R/W

(2) Set P0_7 direction bit to input port.

Port P0 Direction Register (PD0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	x	x	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	PD0_7	Port P0_7 direction bit	0: Input mode (functions as an input port)	R/W

(3) Disable A/D conversion interrupt.

Interrupt Control Register (ADIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(4) Stop A/D conversion.

A/D Control Register 0 (ADCON0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: Stop A/D conversion	R/W

(5) Enable writing to the registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1		x	x

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(6) Cut off on-chip reference voltage from the analog input.

On-Chip Reference Voltage Control Register (OCVREFCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCVREFAN	On-chip reference voltage to analog input connect bit	0: On-chip reference voltage and analog input are cut off	R/W

(7) Disable writing to the registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0		x	x

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

(8) Set the A/D mode register.

A/D Mode Register (ADMOD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 1 0: fAD divided by 2	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit	0: Select f1	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3 0 0 0: One-shot mode	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion start by software trigger (ADST bit in the ADCON0 register)	R/W
b7	ADCAP1			R/W

(9) Set the analog input pin to AN0 and A/D input group to port P0.

A/D Input Select Register (ADINSEL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	x	x	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Analog input pin select bit	b7 b6 0 0 0: AN0	R/W
b1	CH1			R/W
b2	CH2			R/W
b6	ADGSEL0	A/D input group select bit	b7 b6 0 0: Port P0 group selected	R/W
b7	ADGSEL1			R/W

(10) Set A/D control register 1.

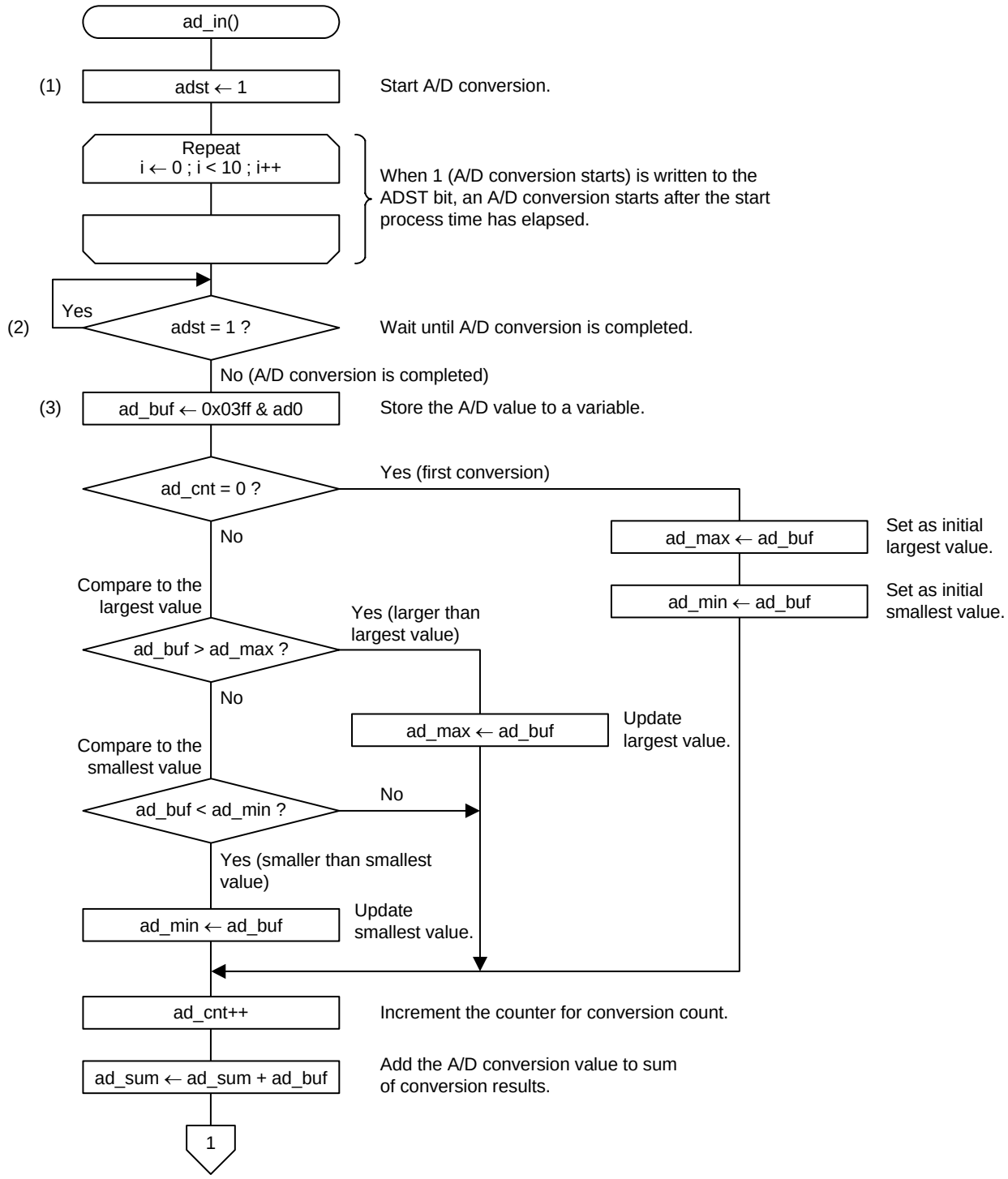
A/D Control Register 1 (ADCON1)

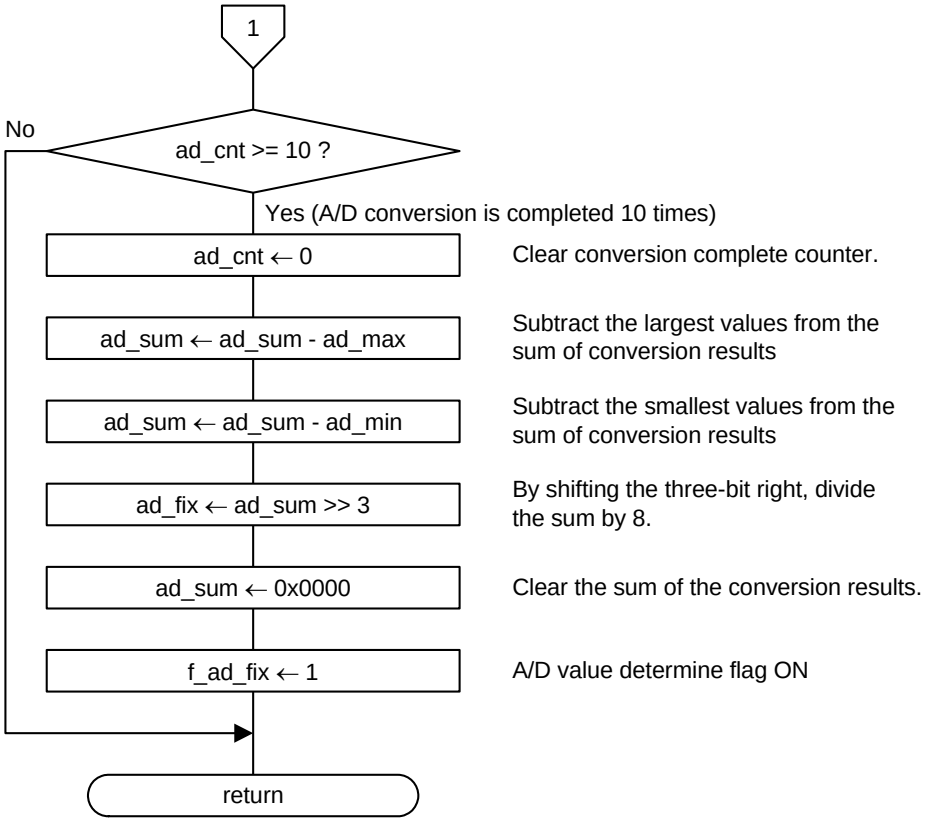
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	1	1	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input pin select bit	0: Extended analog input pin not selected	R/W
b4	BITS	8/10-bit mode select bit	1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit	1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit	0: Disabled	R/W

4.6 A/D Conversion/Determination

- Flowchart





• Register Setting

(1) Start A/D conversion.

A/D Control Register 0 (ADCON0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	—	1

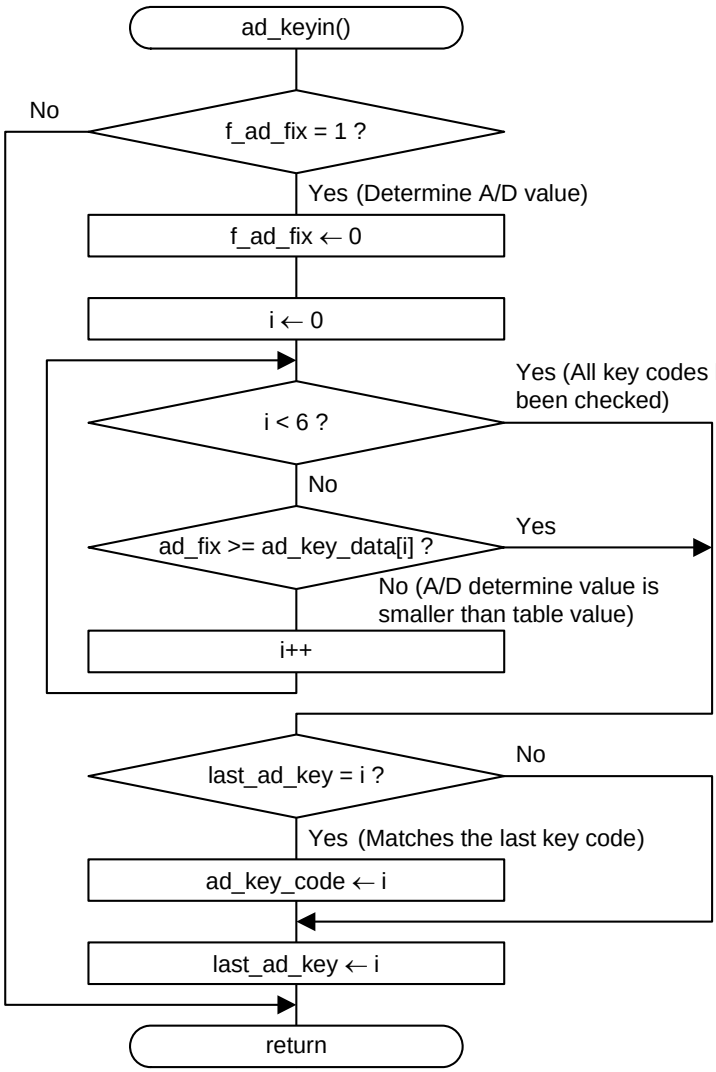
Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	1: Start A/D conversion	R/W

(2) Wait until A/D conversion is completed.

(3) Read A/D conversion result in AN0.

4.7 A/D Key Determination

- Flowchart



Judge A/D value determination flag.

Clear A/D value determination flag.

Clear loop counter.

Judge whether all key codes have been checked.

Judge whether the A/D determination value is larger than table value.

Increment loop counter.

Judges whether the current key code matches the last key code.

Determine key code.

Update last key code.

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

Hardware Manual
R8C/35C Group Hardware Manual Rev.0.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	R8C/35C Group A/D Key Read

Rev.	Date	Description	
		Page	Summary
1.00	Oct 22, 2009	–	First Edition issued

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