R8C/33T Group

Note of the touch detection with the voltage monitor processing

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Introduction

Touch panel microcomputer R8C/33T group builds hardware (SCU: sensor control unit) that perceives the contact of the human body by measuring the stray capacity generated between the touch electrode and the human body into.

In this application note, because the touch detection may be stopped when the voltage monitor interrupt is generated, it explains how to prevent the voltage monitor interrupt makes touch detection stop.

Target Device

R8C/33T group

Contents

1. Non-maskable interrupt and Touch detecting

1.1 Outline

R8C/33T series have the touch detection circuit SCU (sensor control unit) and the DTC (data transfer controller) for transmitting the measurement data on RAM, and these are used for the measurement of touch.

Because DTC stops the data transfer by the interrupts of voltage monitor, overflow and the other non-maskable interrupts, the touch measurement may be stopped when the non-maskable interrupts is generated while measuring touch.

In this application note, it explains the method of continuing the touch detection even the non-maskable interrupts is generated while touch measurement.

1.2 Flow of SCU hang-up by non-maskable interrupt (Image)

Figure 1-1 shows flow of SCU hang-up by non-maskable interrupt.

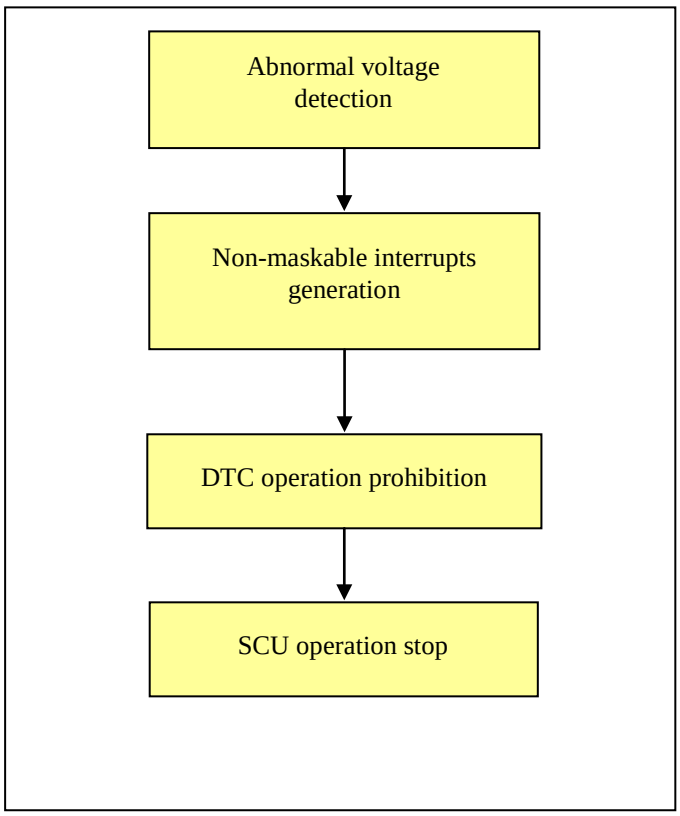


Figure 1-1 flow of SCU hang-up by non-maskable interrupt

1.3 Countermeasure

If the touch detects by SCU with non-maskable interrupts, it is necessary to do as follows;

- Just after the non-maskable interrupt is generated, the Non-maskable Interrupt generation Bit (NMIF) in DTC Activation Control Register (DTCTL) sets to ‘0’.
- The voltage monitor 1 &2 interrupts can be selected to ‘maskable interrupt’, it should be selected.

2. Rerated register and it's operation

2.1 Specification of the voltage monitor process

Table 2-1 shows the specification of voltage detecting circuit. When the circuit detects the target voltage, the process of the voltage monitor1 &2 will be the interrupt process and be able to select 'Non-maskable' or 'Maskable' . In this case, reset does not work.

Table 2-1 Specification of voltage detecting circuit（Quotation from R8C/33T hardware manual）

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Detection voltage	Selectable among 4 levels using the OFS register.	Selectable among 16 levels using the VD1LS register.	Fixed level
	Monitor	None	The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC is higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0	None	None
	Interrupts	None	Voltage monitor 1 interrupt Non-maskable or maskable selectable Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1	Voltage monitor 2 interrupt Non-maskable or maskable selectable Interrupt request at: Vdet2 > VCC and/or VCC > Vdet2
Digital filter	Switching enable/ disable	No digital filter function	Supported	Supported
	Sampling time	—	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

2.2 The specification of DTC

Table 2-2 shows the DTC Activation Control Register. When the non-maskable interrupt is generated, NMIF bit sets to '1' and DTC is stopped. It is possible that NMIF bit set '0' by the user firmware.

Table 2-2 DTC Activation Control Register（Quotation from R8C/33T hardware manual）

15.2.8 DTC Activation Control Register (DTCTL)

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. This bit is set to 0 when the read result is 1 and 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

NMIF Bit (Non-Maskable Interrupt Generation Bit)

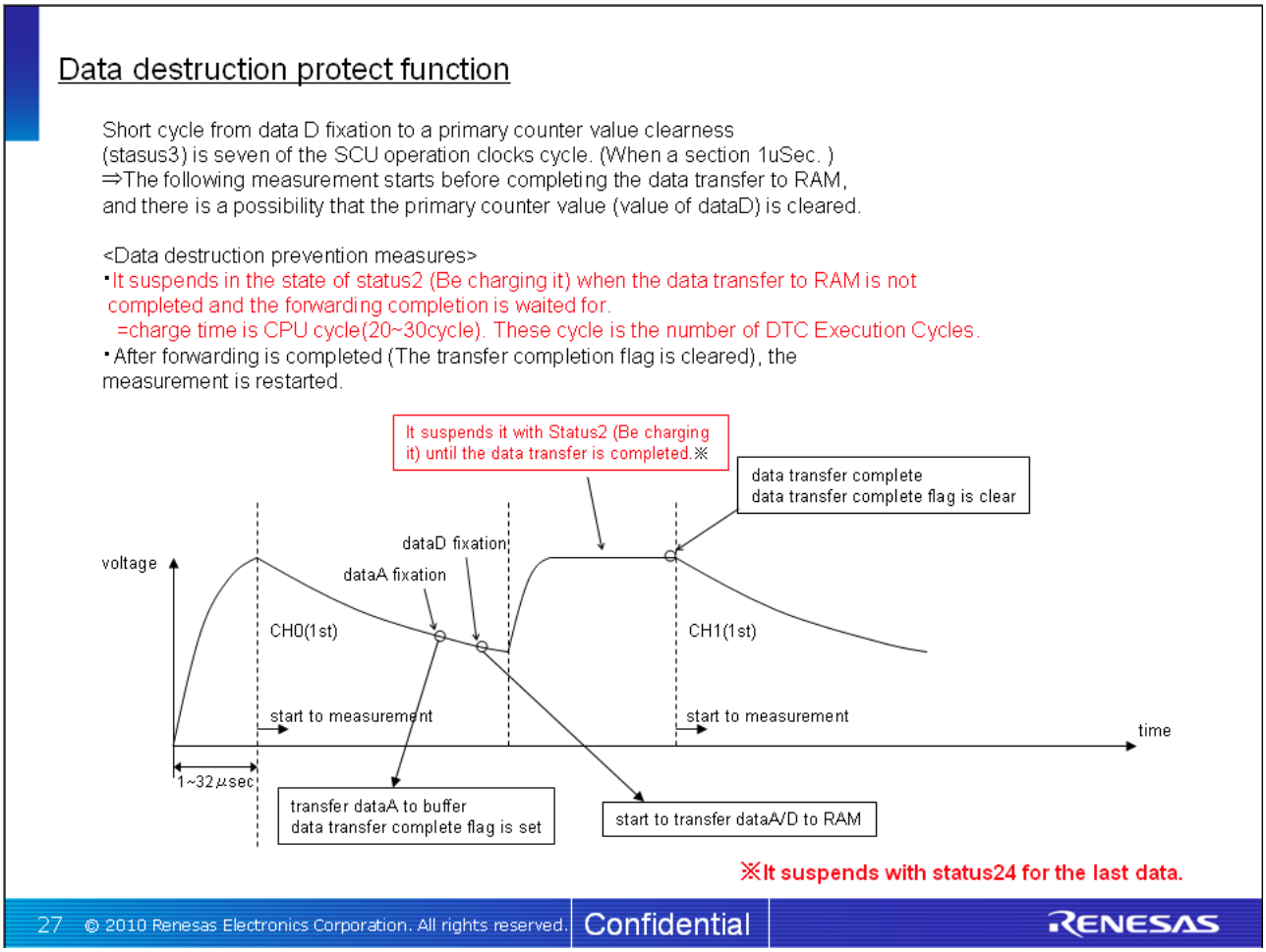
The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during DTC transfer, the transfer is continued until it is completed.

When an interrupt source is the watchdog timer, wait for the following cycles before writing 0 to the NMIF bit:
If the WDTC7 bit in the WDTC register is set to 0 (divide-by-16 using the prescaler), wait for 16 cycles of the CPU clock after the interrupt source is generated.
If the WDTC7 bit is set to 1 (divide-by-128 using the prescaler), wait for 128 cycles of the CPU clock after the interrupt source is generated.
When an interrupt source is oscillation stop detection, set to the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before writing 0 to the NMIF bit.

2.3 Relation of measurement by SCU and DTC data transfer

Table 2-3 shows Data destruction protect function. SCU scans automatically all CH, but it can not scan next CH without finishing recent data transfer by DTC. Because if SCU starts measurement before the register data transfers to RAM by DTC, the register data will be clear and the fail data will transfer to RAM.

Table 2-3 Data destruction protect function（Quotation from R8C/33T professional manual）



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Revision Record

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		Page	Summary
1.00	May 23 2013	—	Numbering change(Content is as same as R01AN0342EJ0100)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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