R8C/25 Group

Timer RD in PWM3 Mode

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1. Abstract

This document describes how to set up and use timer RD in PWM3 mode in the R8C/25 Group.

2. Introduction

The application example described in this document is applied to the following MCU and parameter(s):

• MCU: R8C/25 Group

This program can be used with other R8C/Tiny Series which have the same special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

Note on oscillation stabilization wait time
In chapter 4.2.1 , select the high-speed on-chip oscillator after starting the high-speed on-chip oscillator and waiting until oscillation stabilizes.

3. Applications

3.1 Timer RD

Timer RD has two 16-bit timers (channels 0 and 1). Each channel has four I/O pins.
The operation clock of timer RD is f1 or fOCO40M. Table 3.1 lists the Timer RD Operation Clocks.

Table 3.1 Timer RD Operation Clocks

Conditions	Operation Clock of Timer RD
The count source is f1, f2, f4, f8, f32, or TRDCLK input (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to a value from 000b to 101b).	f1
The count source is fOCO40M (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 110b).	fOCO40M

Figure 3.1 shows a Block Diagram of Timer RD. Timer RD has five modes:

- Timer mode
  - Input capture function — Transfer the counter value to a register with an external signal as the trigger
  - Output compare function — Detect register value matches with a counter (Pin output can be changed at detection)

The following four modes use the output compare function:

- PWM mode — Output pulse of any width continuously
- Reset synchronous PWM mode — Output three-phase waveforms (six) without sawtooth wave modulation and dead time
- Complementary PWM mode — Output three-phase waveforms (six) with triangular wave modulation and dead time
- PWM3 mode — Output PWM waveforms (two) with a fixed period

In the input capture function, output compare function, and PWM mode, channels 0 and 1 have the equivalent functions, and functions or modes can be selected individually for each pin. Also, a combination of these functions and modes can be used in one channel.
In reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, a waveform is output with a combination of counters and registers in channels 0 and 1.

Tables 3.2 to 3.10 list the Pin Functions of timer RD.

Table 3.2 Pin Functions TRDIOA0/TRDCLK(P2_0)

Register	TRDOER1	TRDFCR			TRDIORA0		Function
Bit	EA0	PWM3	STCLK	CMD1, CMD0	IOA3	IOA2_IOA0	
Setting value	0	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	0	00b	1	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	0	00b	X	1XXb	Timer mode trigger input (input capture function)(1)
		1	1	XXb	X	000b	External clock input (TRDCLK)(1)
	Other than above						I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_0 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function) and external clock input (TRDCLK).

Table 3.3 Pin Functions TRDIOB0(P2_1)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA0	Function
Bit	EB0	PWM3	CMD1, CMD0	PWMB0	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_1 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.4 Pin Functions TRDIOC0(P2_2)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	EC0	PWM3	CMD1, CMD0	PWMC0	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_2 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.5 Pin Functions TRDIOD0(P2_3)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	ED0	PWM3	CMD1, CMD0	PWMD0	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_3 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.6 Pin Functions TRDIOA1(P2_4)

Register	TRDOER1	TRDFCR		TRDIORA1	Function
Bit	EA1	PWM3	CMD1, CMD0	IOA2_IOA0	
Setting value	0	X	1Xb	XXXb	Complementary PWM mode waveform output
	0	X	01b	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above				I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_4 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.7 Pin Functions TRDIOB1(P2_5)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA1	Function
Bit	EB1	PWM3	CMD1, CMD0	PWMB1	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_5 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.8 Pin Functions TRDIOC1(P2_6)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	EC1	PWM3	CMD1, CMD0	PWMC1	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_6 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.9 Pin Functions TRDIOD1(P2_7)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	ED1	PWM3	CMD1, CMD0	PWMD1	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_7 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.10 Pin Functions $\overline{\text{INT0}}$(P4_5)

Register	TRDOER2	INTEN		PD4	Function
Bit	PTO	INT0PL	INT0EN	PD4_5	
Setting value	1	0	1	0	Pulse output forced cutoff signal input
	Other than above				I/O port or $\overline{\text{INT0}}$ interrupt input

X: can be 0 or 1, no change in outcome

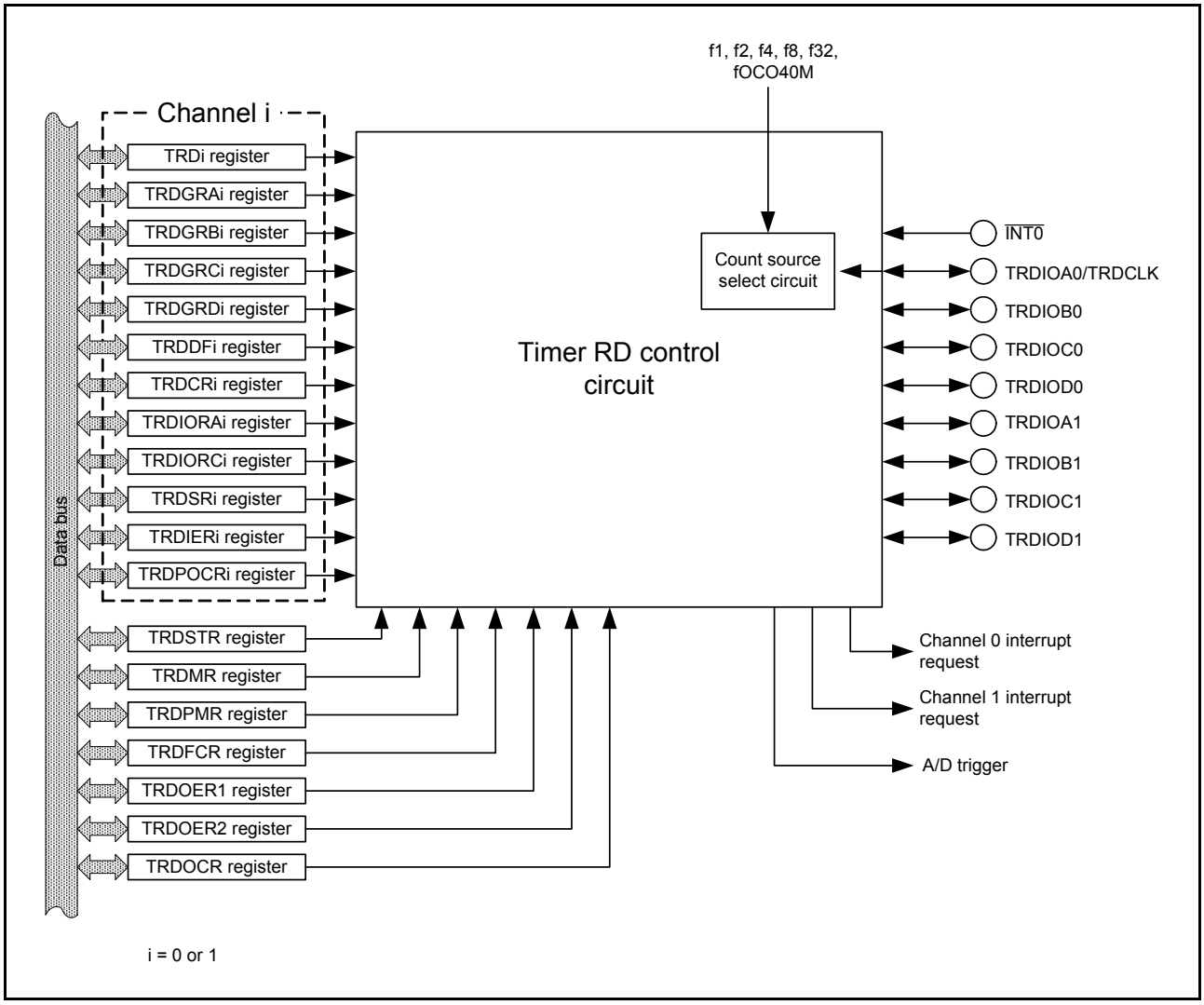


Figure 3.1 Block Diagram of Timer RD

3.2 Count Sources

The count source selection method is the same in all modes. However, in PWM3 mode, the external clock cannot be selected.

Table 3.11 Count Source Selection

Count Source	Selection
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in the TRDCRi register.
fOCO40M(1)	The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator frequency). Bits TCK2 to TCK0 in the TRDCRi register is set to 110b (fOCO40M).
External signal input to TRDCLK pin	The STCLK bit in the TRDFCR register is set to 1 (external clock input enabled). Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (count source: external clock). The valid edge is selected by bits CKEG1 to CKEG0 in the TRDCRi register. The PD2_0 bit in the PD2 register is set to 0 (input mode).

i = 0 or 1

NOTE:

1. The count source fOCO40M can be used with VCC = 3.0 to 5.5 V.

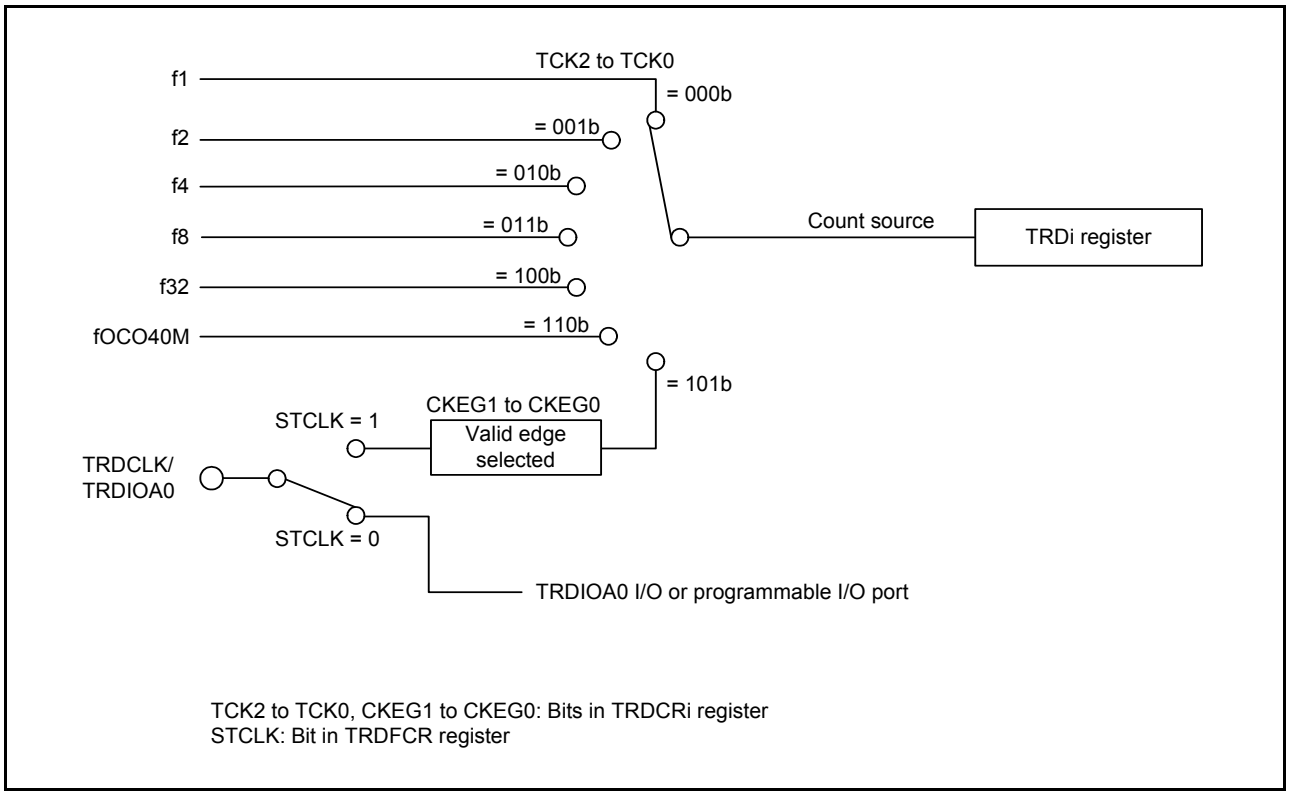


Figure 3.2 Block Diagram of Count Source

Set the pulse width of the external clock which inputs to the TRDCLK pin to three cycles or above of the operation clock of timer RD (refer to **Table 3.1 Timer RD Operation Clocks**).

When selecting fOCO40M for the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) before setting bits TCK2 to TCK0 in the TRDCRi register (i = 0 or 1) to 110b (fOCO40M).

3.3 Buffer Operation

The TRDGRCi (i = 0 or 1) register can be used as the buffer register of the TRDGRAi register, and the TRDGRDi register can be used as the buffer register of the TRDGRBi register by means of bits BFCi and BFDi in the TRDMR register.

- TRDGRAi buffer register: TRDGRCi register
- TRDGRBi buffer register: TRDGRDi register

Buffer operation depends on the mode. Table 3.12 lists the Buffer Operation in Each Mode.

Table 3.12 Buffer Operation in Each Mode

Function and Mode	Transfer Timing	Transfer Register
Input capture function	Input capture signal input	Transfer content in TRDGRAi (TRDGRBi) register to buffer register
Output compare function PWM mode	Compare match with TRDi register and TRDGRAi (TRDGRBi) register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Reset synchronous PWM mode	Compare match withTRD0 register and TRDGRA0 register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Complementary PWM mode	• Compare match with TRD0 register and TRDGRA0 register • TRD1 register underflow	Transfer content in buffer register to registers TRDGRB0, TRDGRA1, and TRDGRB1
PWM3 mode	Compare match with TRD0 register and TRDGRA0 register	Transfer content in buffer register to registers TRDGRA0, TRDGRB0, TRDGRA1, and TRDGRB1

i = 0 or 1

When using the TRDGRCi or TRDGRDi register as a buffer register for the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, bits IMFC and IMFD in the TRDSRi register are set to 1 by a compare match with the TRDi register.

3.4 Pulse Output Forced Cutoff

In the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, the TRDIOji (i = 0 or 1, j = either A, B, C, or D) output pin can be forcibly set to a programmable I/O port by the $\overline{\text{INT0}}$ pin input, and pulse output can be cut off.
The pins used for output in these functions or modes can function as the output pin of timer RD when the applicable bit in the TRDOER1 register is set to 0 (enable timer RD output). When the PTO bit in the TRDOER2 register is set to 1 ($\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled), all bits in the TRDOER1 register are set to 1 (disable timer RD output, the TRDIOji output pin is used as the programmable I/O port) after "L" is applied to the $\overline{\text{INT0}}$ pin. The TRDIOji output pin is set to the programmable I/O port after "L" is applied to the $\overline{\text{INT0}}$ pin and waiting for one to two cycles of the timer RD operation clock (refer to **Table 3.1 Timer RD Operation Clocks**).

Set as below when using this function:

- Set the pin status (high impedance, "L" or "H" output) to pulse output forced cutoff by registers P2 and PD2.
- Set the INT0EN bit in the INTEN register to 1 (enable $\overline{\text{INT0}}$ input) and the INT0PL bit to 0 (one edge).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Set the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRDOER2 register to 1 (enable pulse output forced cutoff signal input $\overline{\text{INT0}}$).

According to the selection of the POL bit in the INT0IC register and change of the $\overline{\text{INT0}}$ pin input, the IR bit in the INT0IC register is set to 1 (interrupt request). Refer to the **R8C/25 Group Hardware Manual** for details of interrupts.

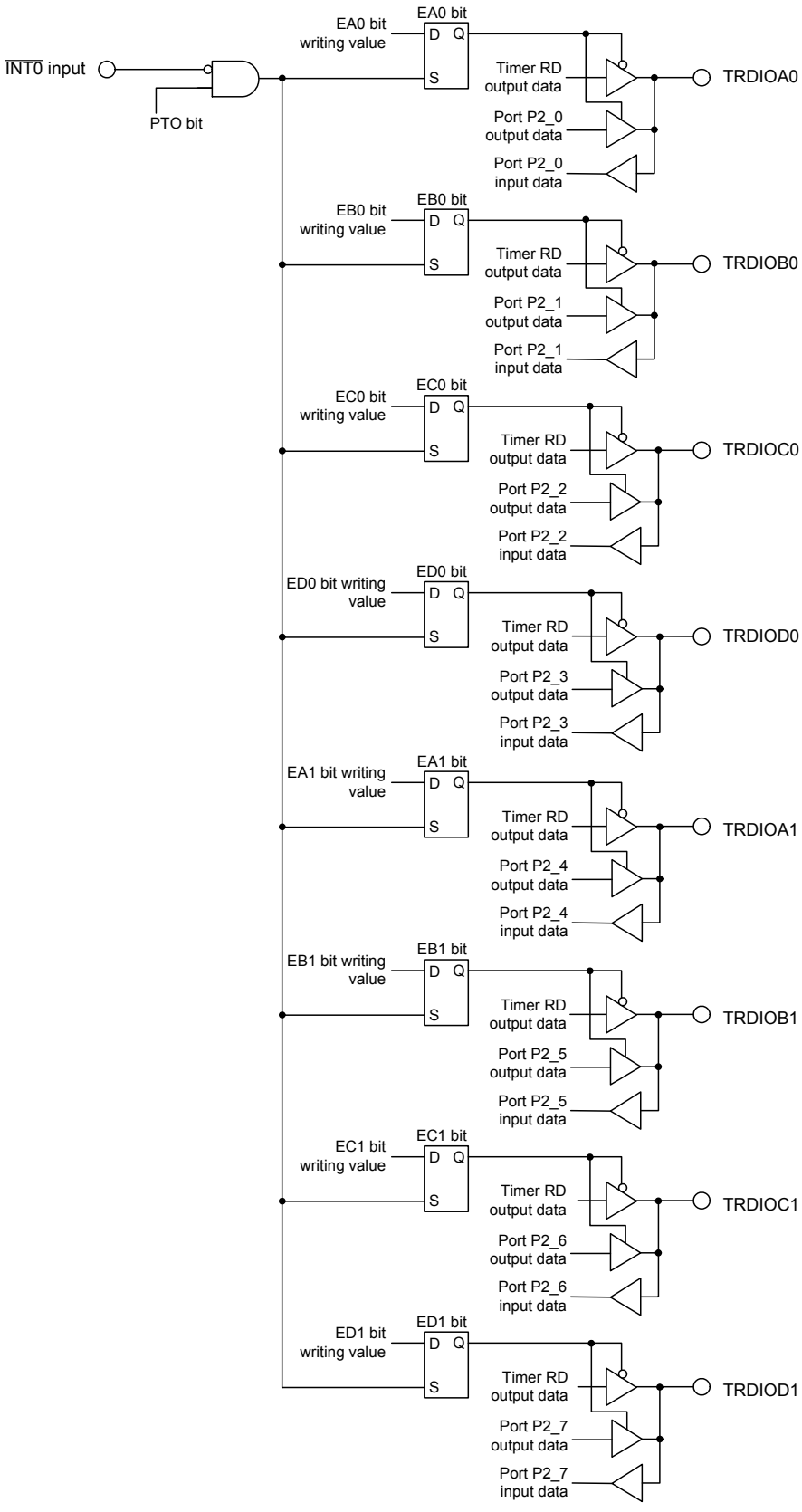


Figure 3.3 Pulse Output Forced Cutoff

3.5 PWM3 Mode

In this mode, three normal-phases and three counter-phases of the PWM waveform (three-phase, triangular wave modulation, and with dead time) are output with the same period.
Figure 3.4 shows a Block Diagram of PWM3 Mode, and Table 3.13 lists the PWM3 Mode Specifications. Figures 3.5 to 3.12 show the Registers Associated with Complementary PWM Mode, and Figure 3.13 shows an Operating Example of PWM3 Mode.

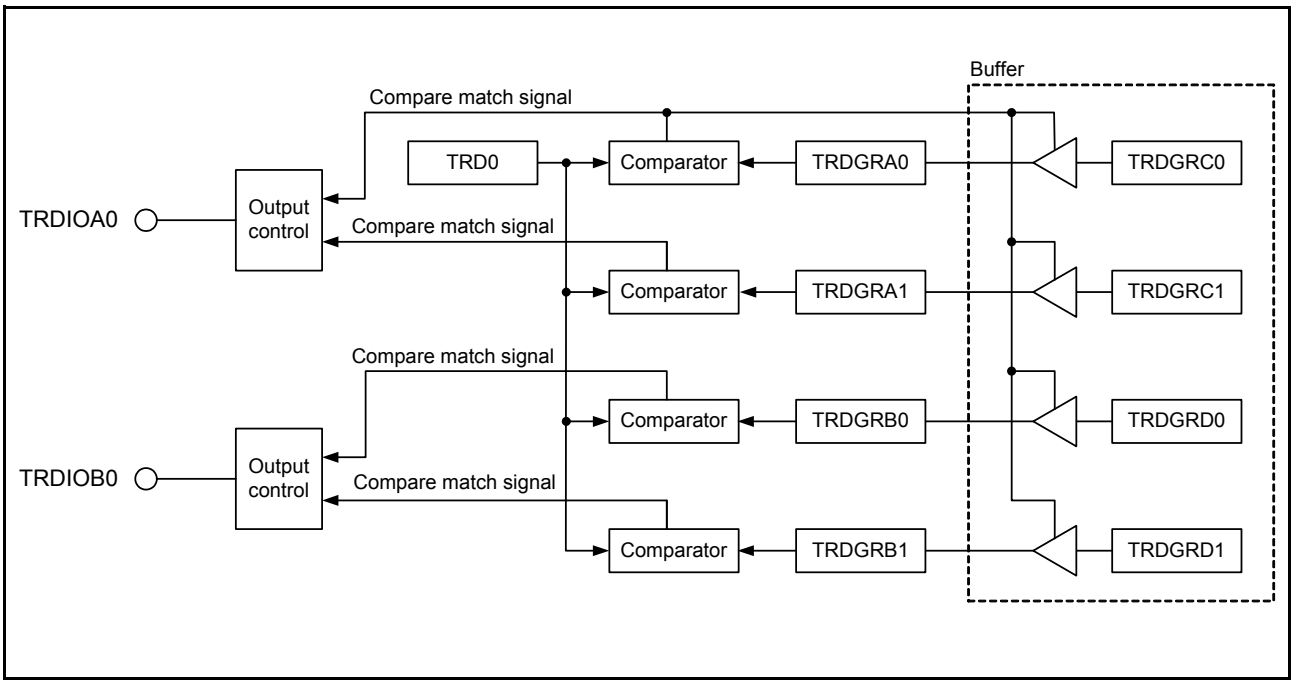
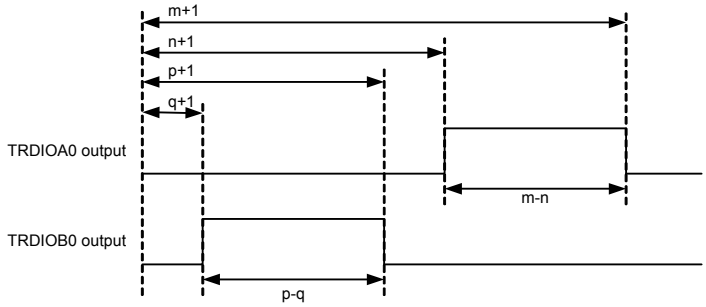


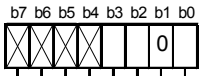
Figure 3.4 Block Diagram of PWM3 Mode

Table 3.13 PWM3 Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M
Count operations	The TRD0 register is incremented (the TRD1 is not used).
PWM waveform	PWM period: 1/fk × (m+1) Active level width of TRDIOA0 output: 1/fk × (m-n) Active level width of TRDIOB0 output: 1/fk × (p-q) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRA1 register p: Value set in the TRDGRB0 register q: Value set in the TRDGRB1 register  (When “H” is selected as the active level)
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. • The PWM output pin holds output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the same time as the TRD0 register is set to 0000h at compare match with the TRDGRA0 register. • The PWM output pin holds level after output change by compare match.
Interrupt request generation timing	• Compare match (The content of the TRDi register matches the content of the TRDGRji register.) • The TRD0 register overflows
TRDIOA0, TRDIOB0 pin functions	PWM output
TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or INT0 interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Select functions	• Pulse output forced cutoff signal input (refer to **3.4 Pulse Output Forced Cutoff**) • Active level selectable by pin

i = 0 or1; j = either A, B, C, or D

Timer RD Start Register(1)



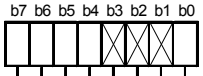
Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0: Count stops(2) 1: Count starts	RW
TSTART1	TRD1 count start flag(5)	0: Count stops(3) 1: Count starts	RW
CSEL0	TRD0 count operation select bit	0: Count stops at compare match with the TRDGRA0 register after the count is cleared 1: Count continues at compare match with the TRDGRA0 register after the count is cleared	RW
CSEL1	TRD1 count operation select bit(1) [this bit is not used in PWM3 mode]	0: Count stops at compare match with the TRDGRA1 register after the count is cleared 1: Count continues at compare match with the TRDGRA1 register after the count is cleared	RW
— (b7 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:

1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **3.7.1 TRDSTR Register** of **Notes on Timer RD**.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Timer RD Mode Register



Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	Set this bit to 0 (TRD0 and TRD1 operate independently) in PWM3 mode.	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	RW

Figure 3.5 Registers TRDSTR and TRDMR in PWM3 Mode

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0					0	0

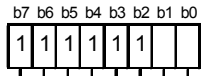
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM3 mode.	RW
CMD1			RW
OLS0	Normal-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
OLS1	Counter-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
ADTRG	A/D trigger enable bit (enabled in complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
ADEG	A/D trigger edge select bit (enabled in complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
STCLK	External clock input select bit	Set this bit to 0 (external clock input disabled) in PWM3 mode.	RW
PWM3	PWM3 mode select bit(2)	Set this bit to 0 (PWM3 mode) in PWM3 mode.	RW

NOTES:
1. Set bits CMD1 to CMD0 w hen both the TSTART0 and TSTART1 bits are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the PWM3 bit setting is enabled.

Figure 3.6 TRDFCR Register in PWM3 Mode

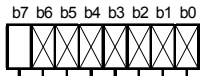
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	0: Enable output 1: Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	RW
EB0	TRDIOB0 output disable bit	0: Enable output 1: Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	Set these bits to 1 (programmable I/O port) in PWM3 mode.	RW
ED0	TRDIOD0 output disable bit		RW
EA1	TRDIOA1 output disable bit		RW
EB1	TRDIOB1 output disable bit		RW
EC1	TRDIOC1 output disable bit		RW
ED1	TRDIOD1 output disable bit		RW

Timer RD Output Master Enable Register 2



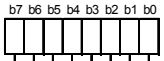
Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6 - b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit(1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when "L" is applied to the $\overline{INT0}$ pin.)	RW

NOTE:
1. Refer to **3.4 Pulse Output Forced Cutoff.**

Figure 3.7 Registers TRDOER1 to TRDOER2 in PWM3 Mode

Timer RD Output Control Register(1)

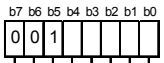


Symbol	Address	After Reset
TRDOCR	013Dh	00h

Bit Symbol	Bit Name	Function	RW
TOA0	TRDIOA0 output level select bit	0 : Active level “H”, initial output “L”, output “H” at compare match with the TRDGRA1register, output “L” at compare match with the TRDGRA0 register 1 : Active level “L”, initial output “H”, output “L” at compare match with the TRDGRA1register, output “H” at compare match with the TRDGRA0 register	RW
TOB0	TRDIOB0 output level select bit	0 : Active level “H”, initial output “L”, output “H” at compare match with the TRDGRB1register, output “L” at compare match with the TRDGRB0 register 1 : Active level “L”, initial output “H”, output “L” at compare match with the TRDGRB1register, output “H” at compare match with the TRDGRB0 register	RW
TOC0	TRDIOC0 initial output level select bit	These bits are disabled in PWM3 mode.	RW
TOD0	TRDIOD0 initial output level select bit		RW
TOA1	TRDIOA1 initial output level select bit		RW
TOB1	TRDIOB1 initial output level select bit		RW
TOC1	TRDIOC1 initial output level select bit		RW
TOD1	TRDIOD1 initial output level select bit		RW

NOTE:
1. Write to the TRDOCR register when both bits TSTART0 and TSTART1 in the TRDSTR register are set to 0 (count stops).

Timer RD Control Register 0(2)



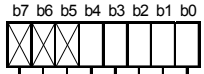
Symbol	Address	After Reset
TRDCR0	0140h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits	b2 b1b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: Do not set. 1 1 0: fOCO40M 1 1 1: Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(1)	These bits are disabled in PWM3 mode.	RW
CKEG1			RW
CCLR0	TRD0 counter clear select bits	Set to 001b (the TRD0 register cleared at compare match with TRDGRA0 register) in PWM3 mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. Bits CKEG1 to CKEG0 are enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. The TRDCR1 register is not used in PWM3 mode.

Figure 3.8 Registers TRDOCR and TRDCR0 in PWM3 Mode

Timer RD Status Register i (i = 0 or 1)(2)



Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

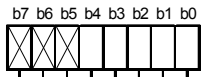
Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register(2).	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register(2).	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in PWM3 mode.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:

1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit (this bit remains 1 even if it is set to 1 from 0 after reading, and writing 0).
   - This bit remains unchanged if 1 is written to it.
2. Including when the BFji (j = C or D) bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 3.9 TRDSR0 Register in PWM3 Mode

Timer RD Interrupt Enable Register 0

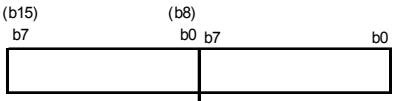


Symbol	Address	After Reset
TRDIER0	0144h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 3.10 TRDIER0 Register in PWM3 Mode

Timer RD Counter 0(1, 2)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	RW

NOTES:
1. Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
2. The TRD1 register is not used in PWM3 mode.

Figure 3.11 TRD0 Register in PWM3 Mode

Timer RD General Registers Ai, Bi, Ci, and Di (i = 0 or 1)(1)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 3.14 TRDGRji Register Functions in PWM3 mode.**	RW

NOTE:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

Figure 3.12 Registers TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi in PWM3 Mode

The following registers are disabled in PWM3 mode: TRDPMR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 3.14 TRDGRji Register Functions in PWM3 Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period. Setting range: Value set in TRDGRA1 register or above	TRDIOA0
TRDGRA1		General register. Set the changing point (the active level timing) of PWM output. Setting range: Value set in TRDGRA0 register or below	
TRDGRB0		General register. Set the changing point (the timing that returns to initial output level) of PWM output. Setting range: Value set in TRDGRB1 register or above Value set in TRDGRA0 register or below	TRDIOB0
TRDGRB1		General register. Set the changing point (active level timing) of PWM output. Setting range: Value set in TRDGRB0 register or below	
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **3.3 Buffer Operation**.) Setting range: Value set in TRDGRC1 register or above	TRDIOA0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **3.3 Buffer Operation**.) Setting range: Value set in TRDGRC0 register or below	
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **3.3 Buffer Operation**.) Setting range: Value set in TRDGRD1 register or above, setting value or below in TRDGRC0 register.	TRDIOB0
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **3.3 Buffer Operation**.) Setting range: Value set in TRDGRD0 register or below	

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

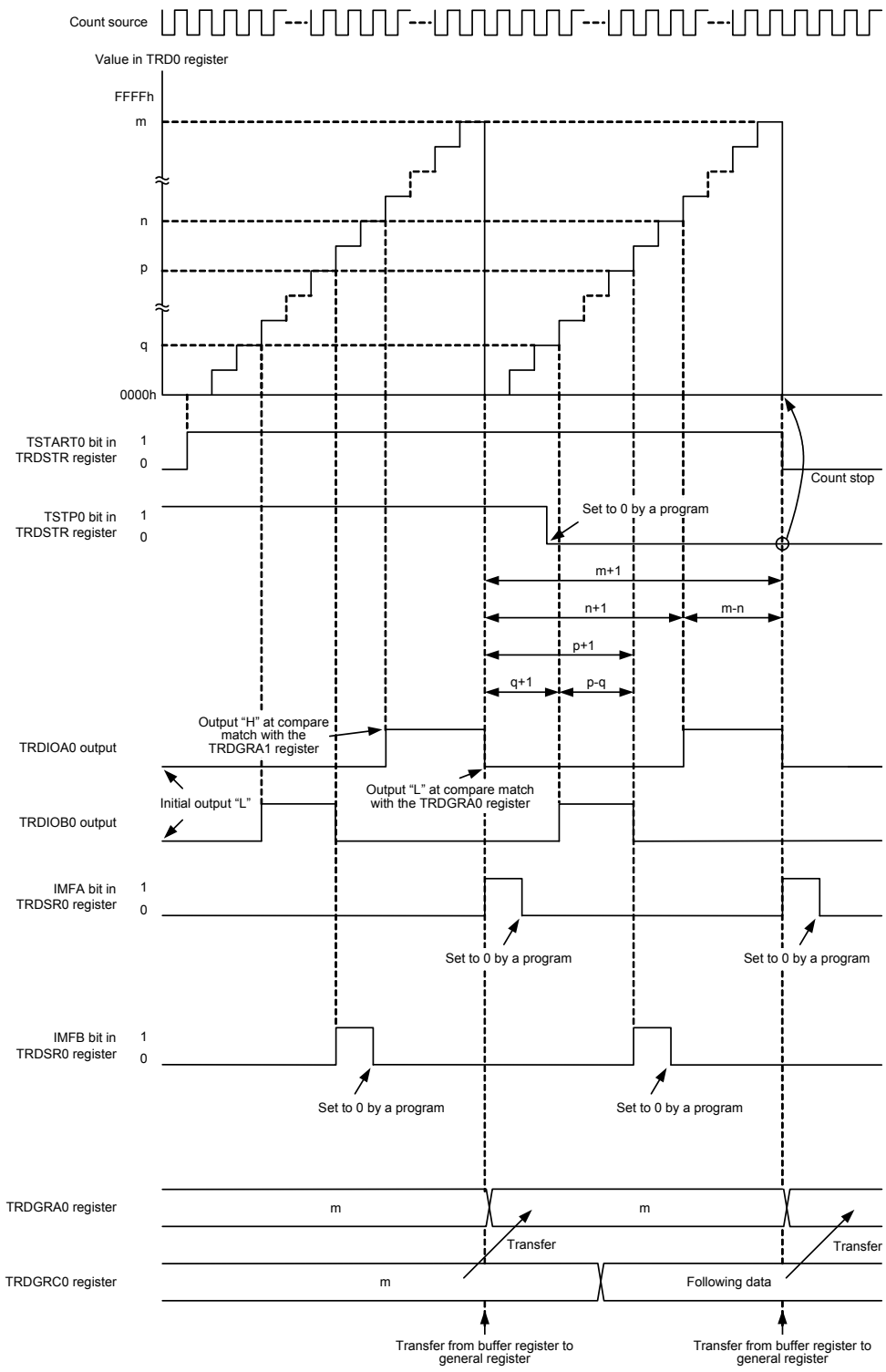


Figure 3.13 Operating Example of PWM3 Mode

3.6 Timer RD Interrupt

Timer RD generates the timer RD interrupt request based on six sources for each channel. The timer RD interrupt has one TRDiIC register (bits IR, and ILVL0 to ILVL2), and one vector for each channel. Table 3.15 lists the Registers Associated with Timer RD Interrupt, and Figure 3.14 shows a Block Diagram of Timer RD Interrupt.

Table 3.15 Registers Associated with Timer RD Interrupt

	Timer RD Status Register	Timer RD Interrupt Enable Register	Timer RD Interrupt Control Register
Channel 0	TRDSR0	TRDIER0	TRD0IC
Channel 1	TRDSR1	TRDIER1	TRD1IC

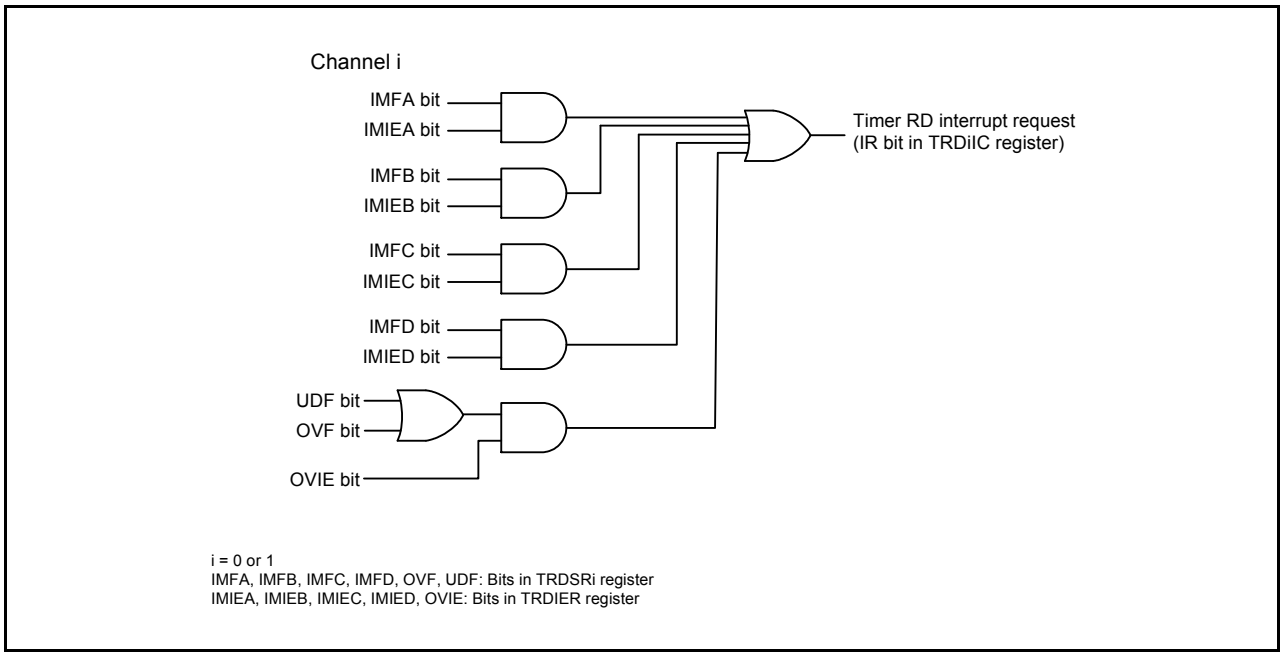


Figure 3.14 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RD interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since the interrupt source (timer RD interrupt) is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the TRDSRi register corresponding to bits set to 1 in the TRDIERi register are set to 1 (enable interrupt), the IR bit in the TRDiIC register is set to 1 (interrupt requested).
- When either bits in the TRDSRi register or bits in the TRDIERi register corresponding to bits in the TRDSRi register, or both of them, are set to 0, the IR bit is set to 0 (interrupt not requested). Therefore, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained.
- When the conditions of other request sources are met, the IR bit remains 1.
- When multiple bits in the TRDIERi register are set to 1, which request source causes an interrupt is determined by the TRDSRi register.
- Since each bit in the TRDSRi register is not automatically set to 0 even if the interrupt is acknowledged, set each bit to 0 in the interrupt routine.

For information on how to set these bits to 0, refer to **TRDSR0 Register in PWM3 Mode (Figure 3.9)**.

Refer to **TRDSR0 Register in PWM3 Mode (Figure 3.9)** for the TRDSRi register. Refer to **TRDIER0 Register in PWM3 Mode (Figure 3.10)** for the TRDIERi register.
Refer to the **R8C/25 Group Hardware Manual** for information on the TRDiIC register and the interrupt vectors.

3.7 Notes on Timer RD

3.7.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSEL0 is set to 0 (the count stops after the count is cleared at compare match of registers TRD0 and TRDGRA0), the count does not stop and the TSTART0 bit remains unchanged even if 0 (count stops) is written to the TSTART0 bit.
- Therefore, set the TSTART0 bit to 0 to change other bits without changing the TSTART0 bit when the CSEL0 bit is set to 0.
- To stop counting by a program, set the TSTART0 bit after setting the CSEL0 bit to 1. Although the CSEL0 bit is set to 1 and the TSTART0 bit is set to 0 at the same time (with one instruction), the count cannot be stopped.

- Table 3.16 lists the Timer RD Operation Clocks to use the TRDIOj0 (j = A or B) pin with the timer RD output.

Table 3.16 TRDIOj0 (j = A or B) Pin Output Level when Count Stops

Count Stop	TRDIOj0 Pin Output when Count Stops
When the CSEL0 bit is set to 1, set the TSTART0 bit to 0 and the count stops.	Hold the output level immediately before the count stops.
When the CSEL0 bit is set to 0, the count stops after the count is cleared at compare match of registers TRD0 and TRDGRA0.	Hold the output level after output changes by compare match.

3.7.2 TRD0 Register

- When writing the value to the TRD0 register by a program while the TSTART0 bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRD0 register to 0000h, and then write. If the timing for setting the TRD0 register to 0000h overlaps with the timing for writing the value to the TRD0 register, the value is not written and the TRD0 register is set to 0000h.
  These precautions are applicable when selecting the following by bits CCLR2 to CCLR0 in the TRDCR0 register.
  - 001b (Clear by the TRD0 register at compare match with the TRDGRA0 register.)
  - 010b (Clear by the TRD0 register at compare match with the TRDGRB0 register.)
  - 011b (Synchronous clear)
  - 101b (Clear by the TRD0 register at compare match with the TRDGRC0 register.)
  - 110b (Clear by the TRD0 register at compare match with the TRDGRD0 register.)

- When writing the value to the TRD0 register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Reading
```

3.7.3 TRDSR0 Register

When writing the value to the TRDSR0 register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.B   TRDSR0,DATA      ;Reading
```

3.7.4 Count Source Switch

- Switch the count source after the count stops.

Change procedure:

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

- When changing the count source from fOCO40M to another source and stopping fOCO40M, wait two or more cycles of f1 after setting the clock switch, and then stop fOCO40M.

Change procedure:

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator stops).

3.7.5 PWM3 Mode

- Do not write to the TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.

To change the PWM waveform and PWM period, transfer the values written to registers TRDGRC0, TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRA0, TRDGRB0, TRDGRA1, and TRDGRB1 using buffer operation.

3.7.6 Count Source fOCO40M

- The count source fOCO40M can be used with supply voltage VCC = 3.0 to 5.5 V. For supply voltage other than that, do no set bits TCK2 to TCK0 in registers TRDCR0 and TRDCR to 110b (select fOCO40M as the count source).

4. Program Overview

This program can be used on timer RD to output two PWM waveforms with the same period at the PWM period (200 µs).
The output signals are as follows:

TRDIOA0 pin: active level (“H”) 60 µs = 40 MHz × (TRDGRA0 – TRDGRA1)
= 25 ns × (8000 – 5600) = 25 ns × 2400
TRDIOB0 pin: active level (“H”) 60 µs = 40 MHz × (TRDGRB0 – TRDGRB1)
= 25 ns × (4000 – 1600) = 25 ns × 2400

Set TRDGRA0 to the PWM period (200 µs).
200 µs = 40 MHz × (TRDGRA0 + 1) = 25 ns × 8000

TRDIOA0 pin: PWM output change point (active level timing: TRDGRA1)
140 µs = 40 MHz × (TRDGRA1 + 1) = 25 ns × 5600
TRDIOB0 pin: PWM output change point (initial output level timing: TRDGRB0)
100 µs = 40 MHz × (TRDGRB0 + 1) = 25 ns × 4000
TRDIOB0 pin: PWM output change point (active level timing: TRDGRB1)
40 µs = 40 MHz × (TRDGRB1 + 1) = 25 ns × 1600

The setting conditions of this program are as follows:
- Select the high-speed on-chip oscillator (fOCOM40M) as count source.
- Clear timer RD counter0 (TRD0) at compare match with TRDGRA0.
- For the TRDGRA0 pin and TRDGRB0 pin, set the output levels to active “H” and the initial output levels to inactive “H”.
- Output an active level signal (“H”) from the TRDIOA0 pin at compare match between TRD0 and TRDGRA1.
- Output an active level signal (“H”) from the TRDIOB0 pin at compare match between TRD0 and TRDGRB1.
- Do not use the pulse output forced cutoff input function.

Figure 4.1 shows the Pin Used.

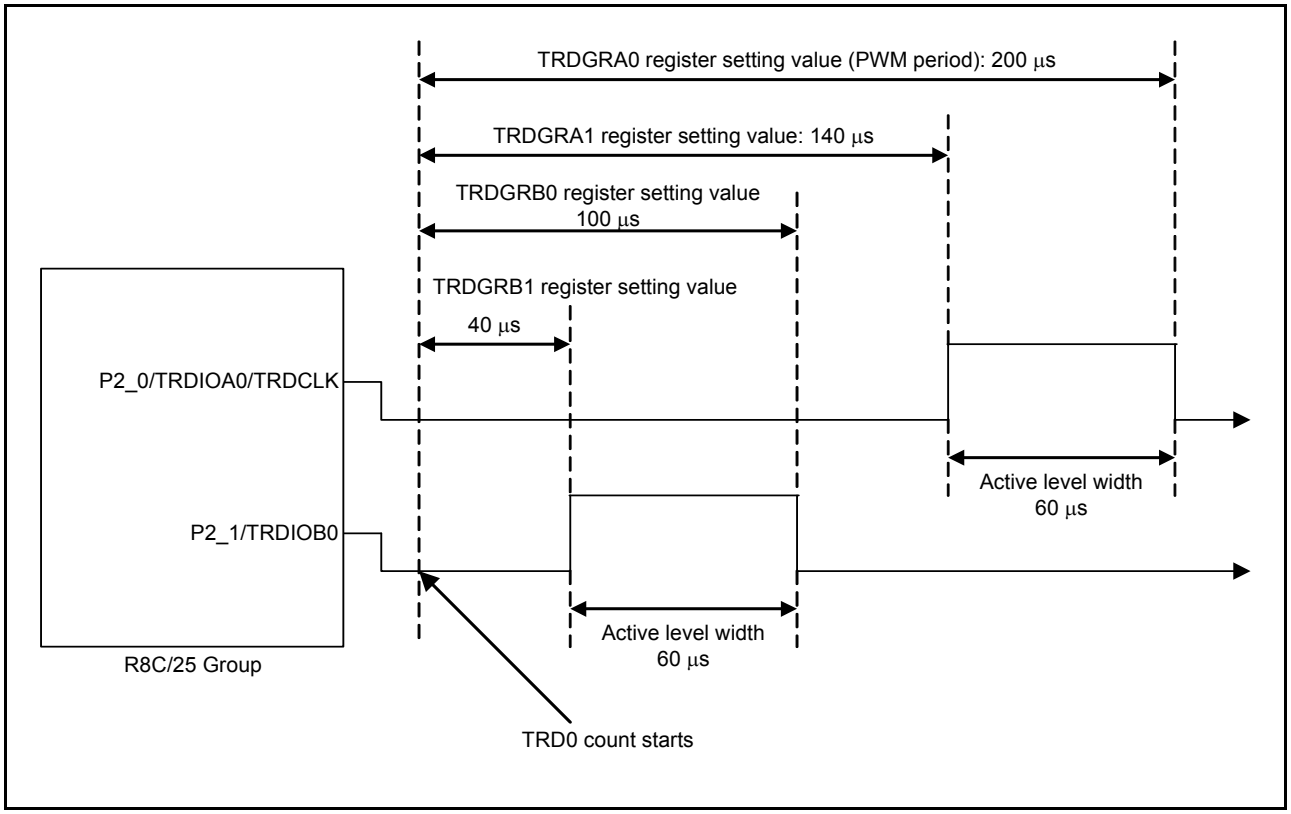


Figure 4.1 Pin Used

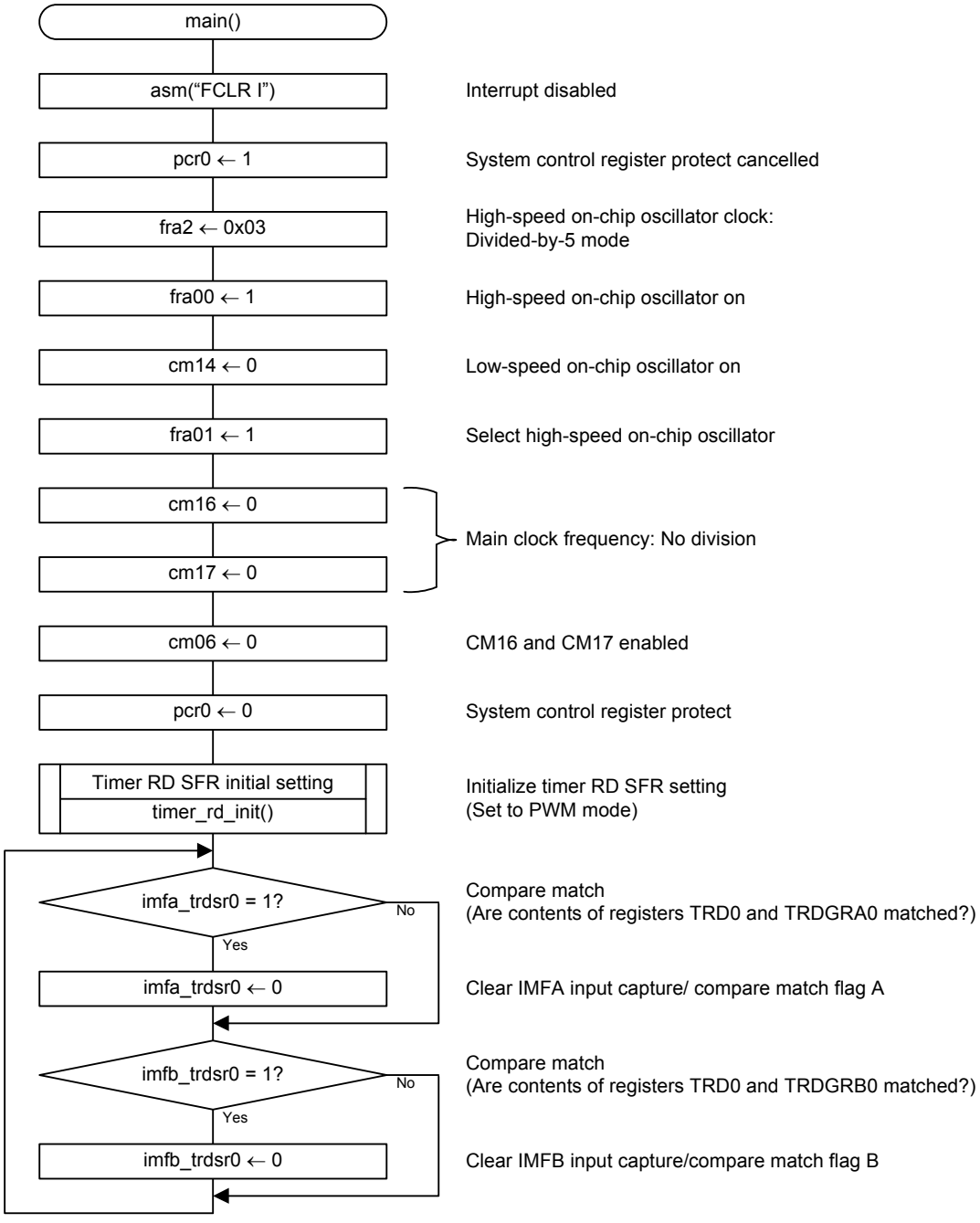
4.1 Function Table

Table 4.1

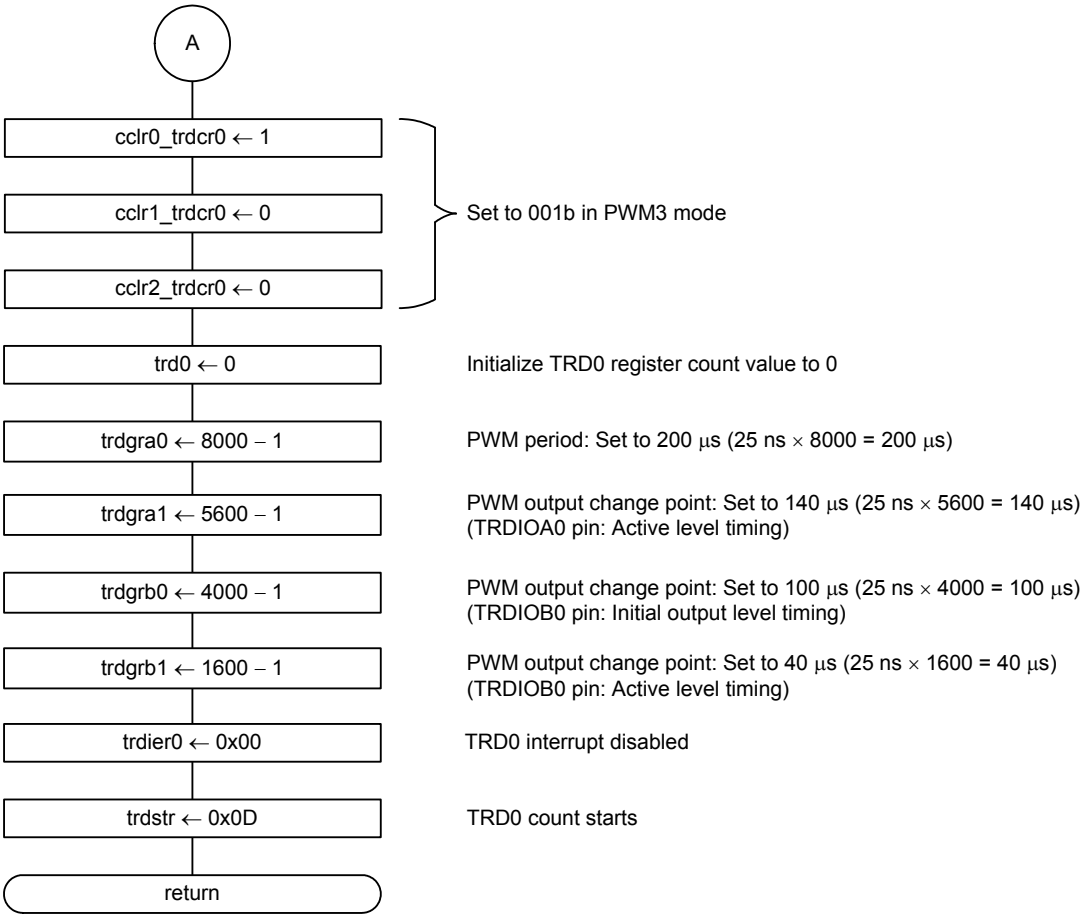
Declaration	void timer_rd_init(void)		
Overview	SFR initial setting associated with timer RD		
Argument	Argument name		Meaning
	None		
Variable used (global)	Variable name		Usage
	None		
Return value	Type	Value	Meaning
	None		
Function	Initialize the SFR registers associated with timer RD		

4.2 Flow chart

4.2.1 Main Function



4.2.2 Timer RD SER Initial Setting


A
cclr0_trdcr0 ← 1
cclr1_trdcr0 ← 0
cclr2_trdcr0 ← 0
Set to 001b in PWM3 mode
trd0 ← 0
Initialize TRD0 register count value to 0
trdgra0 ← 8000 – 1
PWM period: Set to 200 μs (25 ns × 8000 = 200 μs)
trdgra1 ← 5600 – 1
PWM output change point: Set to 140 μs (25 ns × 5600 = 140 μs)
(TRDIOA0 pin: Active level timing)
trdgrb0 ← 4000 – 1
PWM output change point: Set to 100 μs (25 ns × 4000 = 100 μs)
(TRDIOB0 pin: Initial output level timing)
trdgrb1 ← 1600 – 1
PWM output change point: Set to 40 μs (25 ns × 1600 = 40 μs)
(TRDIOB0 pin: Active level timing)
trdier0 ← 0x00
TRD0 interrupt disabled
trdstr ← 0x0D
TRD0 count starts
return

5. Sample Programming Code

A sample program can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
R8C/25 Group Hardware Manual
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
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REVISION HISTORY	R8C/25 Group Timer RD in PWM3 Mode

Rev.	Date	Description	
		Page	Summary
1.00	Dec 01, 2006	–	First Edition issued
1.10	June 1, 2012	1	Note on oscillation stabilization wait time added
		–	Previous document number: REJ05B0846

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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