R8C/1B Group and R8C/29 Group

Differences between R8C/1B Group and R8C/29 Group

REJ05B1313-0100
Rev.1.00
June 30, 2010

1. Abstract

This document is reference material for identifying differences between the R8C/1B Group and R8C/29 Group.

2. Introduction

This document applies to the following microcomputers (MCUs):

- MCUs: R8C/1B Group and R8C/29 Group

3. R8C/29 Group Replaces R8C/1B Group

Since the R8C/29C Group is an upward compatible product of the R8C/1B Group, replacing the R8C/1B Group with the R8C/29 Group is easy. For more details, refer to 4. Group Differences and the hardware user's manual.

3.1 Upward Compatibility of Functions

Upward compatible functions for the R8C/29 Group are as follows:

(1) Timer RA and timer X
(2) Timer RB and timer Z

Additional functions for the R8C/29 Group are as follows:

(1) A voltage detection 0 circuit has been added to the N and D versions.
(2) Vdet1 can be monitored.
(3) An XCIN clock oscillation circuit has been added to the N and D versions and can be selected.
(4) The digital filter function has been added for $\overline{\text{INT1}}$ input.
(5) fC32 has been added for the timer RA count source in the N and D versions.
(6) The digital filter function has been added for timer RA external input.
(7) Timer RC and timer RE have been added.
(8) The hardware LIN has been added.

4. Group Differences

4.1 Function and Specification Differences

Table 4.1 and Table 4.2 list differences in the functions and specifications.

Table 4.1 Function and Specification Differences (1) (1)

Item		R8C/1B Group	R8C/29 Group
Memory	ROM/RAM	• 4 KB/384 B • 8 KB/512 B • 12 KB/768 B • 16 KB/1 KB	• 8 KB/512 B • 16 KB/1 KB • 32 KB/1.5 KB
Reset	—	• Voltage monitor 0 reset: Not included • Flash memory start time: 11 cycles of the CPU clock	• Voltage monitor 0 reset: Included (2) • Flash memory start time: 14 cycles of the CPU clock
	Hardware reset	"L" input width to RESET pin: 500 μs (1/fRING-S × 20) or more	"L" input width to RESET pin: 10 μs or more
Voltage Detection Circuits	Voltage detection 0	• Voltage monitor 0: Not included	• Voltage monitor 0: Included (2)
	Voltage detection 1	• Monitor: Not included • Voltage monitor 1 interrupt: Not included	• Monitor: Included (2) • Voltage monitor 1 interrupt: Included (2)
	Voltage detection 2	• Voltage detection level (3.3 V ± 0.3 V)	• Voltage detection level (3.6 V ± 0.3 V)
I/O Ports	Ports for LED drive	4	8 (2)
Clock Generation Circuits		• XCIN clock oscillation circuit: Not included • Internal power low consumption control: Not included	• XCIN clock oscillation circuit: Included (2) • Internal power low consumption control: Included
High-Speed On-Chip Oscillator	Clock frequency	8 MHz (typical)	40 MHz (typical)
Low-Speed On-Chip Oscillator	Clock frequency	40 kHz (minimum)	30 kHz (minimum)
Interrupts		• Interrupt sources: 24 • External interrupt inputs: 7 ($\overline{INT}$ × 3, key input × 4) • $\overline{INT1}$ input filter: Not included • $\overline{INT3}$ input filter: Not included	• Interrupt sources: 24 (2) • External interrupt inputs: 7 ($\overline{INT}$ × 3, key input × 4) • $\overline{INT1}$ input filter: Included • $\overline{INT3}$ input filter: Included
Supply Voltage		• VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) • VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)	• VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (4) • VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (3) • VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) • VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (2)

Notes:
1. Refer to the hardware user's manual for details and electrical characteristics.
2. These only apply to the N and D versions in the R8C/29 Group.
3. This only applies to the K version in the R8C/29 Group.
4. This applies to all versions except for the K version in the R8C/29 Group.

Table 4.2 Function and Specification Differences (2) (1)

Item		R8C/1B Group	R8C/29 Group
Current Consumption		• Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz) when A/D converter stops) • Typ. 5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) when A/D converter stops) • Typ. 35 μA (VCC = 3 V, wait mode, peripheral clocks stop) • Typ. 0.7 μA (VCC = 3 V, stop mode)	• Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) (2) • Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) (2) • Typ. 2.0 μA (VCC = 3 V, wait mode, (f(XCIN) = 32 kHz)) (2) • Typ. 0.7 μA (VCC = 3 V, stop mode) (2)
Timer RA (timer X)	Count source	• fC32: Not included	• fC32: Included (2)
	Count forcible stop	Not included	Included
	Digital filter function	Not included	Included
	Pulse output mode	Pulse output stop function: Not included	Pulse output stop function: Included
	Event counter mode	Pulse output function: Not included	Pulse output function: Included
Timer RB (timer Z)	Count forcible stop	Not included	Included
Timer C		Included	Not included
Timer RC		Not included	Included
Timer RE		Not included	Included
Hardware LIN		Not included	Included
A/D Converter	A/D conversion start condition	Capture: Included	Capture: Not included
Packages		• 20-pin molded-plastic LSSOP • 20-pin molded-plastic SDIP • 28-pin molded-plastic HWQFN	• 20-pin molded-plastic LSSOP

Notes:
1. Refer to the hardware user's manual for details and electrical characteristics.
2. These only apply to the N and D versions in the R8C/29 Group.

4.2 Pin Function Differences

Table 4.3 lists pin function differences.

Table 4.3 Pin Function Differences

Peripheral Function Pin	Assigned I/O Port	
	R8C/1B Group	R8C/29 Group
XCIN	—	P4_6 (1)
XCOUT	—	P4_7 (1)
INT1	—	P1_5, P1_7
$\overline{\text{INT10}}$	P1_7	—
$\overline{\text{INT11}}$	P1_5	—
$\overline{\text{CNTR0}}$	P3_7	—
CNTR00	P1_7	—
CNTR01	P1_5	—
TRAIO	—	P1_5, P1_7
TRAO	—	P3_7
TZOUT	P1_3	—
TRBO	—	P1_3
TCIN	P3_3	—
CMP0_0	P1_0	—
CMP0_1	P1_1	—
CMP0_2	P1_2	—
CMP1_0	P3_3	—
CMP1_1	P3_4	—
CMP1_2	P3_5	—
TRCCLK	—	P3_3
TRCTRG	—	P1_1
TRCIOA	—	P1_1
TRCIOB	—	P1_2
TRCIOC	—	P3_4
TRCIOD	—	P3_5
RXD1	P4_5	P3_7, P4_5
SSI	—	P1_6, P3_3
SSI00	P3_3	—
SSI01	P1_6	—

Note:
1. These only apply to the N and D versions in the R8C/29 Group.

4.3 SFR Differences

Table 4.4 to Table 4.6 list differences in the SFRs.

Table 4.4 SFR Differences (1)

R8C/1B Group	R8C/29 Group	Remarks
—	PINSR1	
—	PINSR2	
—	PINSR3	
P1	P1	Reset values are different.
P3	P3	Reset values are different.
P4	P4	Reset values are different.
PMR	PMR	Bits 4 to 6 added
PUR0	PUR0	Reset values are different.
PUR1	PUR1	Reset values are different.
DRR	P1DRR (1)	• Register name changed • Bits 4 to 7 added
VCA2	VCA2	• Bit 0 added • Bit 5 added (1) • Reset values are different (1).
—	VW0C (1)	
VW1C	VW1C	• Bits 2 and 3 added (1) • Functions in bits 6 and 7 changed (1)
CM0	CM0	Bits 1, 3, and 4 added
CM1	CM1	Bits 1 and 2 added
OCD	OCD	Functions in bits 0 and 1 changed
HRA0	FRA0	Register name changed and allocation addresses are different.
HRA1	FRA1	Register name changed and allocation addresses are different.
HRA2	FRA2	• Register name changed and allocation addresses are different. • Functions in bits 0 to 2 changed
—	FRA4 (1)	
—	FRA6 (1)	
—	FRA7 (1)	
—	CPSRF (1)	
PRCR	PRCR	Functions in bit 3 added
—	TRCIC	
—	TREIC	
SSUAIC/IIC2AIC	SSUIC/IICIC	Register name changed and RW in bit 3 changed to RO
CMP1IC	—	
TXIC	TRAIC	Register name changed
TZIC	TRBIC	Register name changed
INT1IC	INT1IC	Reset values are different and bit 4 added
INT3IC	INT3IC	Reset values are different and bit 4 added
TCIC	—	
CMP0IC	—	
INTEN	INTEN	Allocation addresses are different and bits 2, 3, 6, and 7 added.
INT0F	INTF	• Register name changed and allocation addresses are different. • Bits 2, 3, 6, and 7 added
KIEN	KIEN	Allocation addresses are different.
AIER	AIER	Allocation addresses are different.
RMAD0	RMAD0	Reset values are different.

Note:
1. These only apply to the N and D versions in the R8C/29 Group.

Table 4.5 SFR Differences (2)

R8C/1B Group	R8C/29 Group	Remarks
RMAD1	RMAD1	Reset values are different.
TXMR	TRAMR	• Register name changed and allocation addresses are different. • Functions in bits 0, 1, and 5 moved to bits 0 to 2 • Functions in bit 2 moved to bit 0 in TRAIOC register • Functions in bit 3 moved to bit 0 in TRACR register • Functions in bit 4 moved to bit 2 in TRAIOC register • Functions in bit 6 moved to bit 4 in TRACR register • Functions in bit 7 moved to bit 5 in TRACR register • Functions in bits 4 to 6 added • Functions in bit 7 added
PREX	TRAPRE	Register name changed and allocation addresses are different.
TX	TRA	Register name changed and allocation addresses are different.
TCSS	—	• Functions in bits 0 and 1 moved to bits 4 to 6 in TRAMR register and functions added • Functions in bits 4 and 5 moved to bits 4 and 5 in TRBMR register
—	TRACR	
—	TRAIOC	
TZMR	TRBMR	• Register name changed and allocation addresses are different. • Functions in bits 4 and 5 moved to bits 0 and 1. • Functions in bit 6 moved to bit 3 • Functions in bit 7 moved to bit 0 in TRBCR register • Functions in bits 4 and 5 added • Functions in bit 7 added
PUM	TRBIOC	• Register name changed and allocation addresses are different. • Functions in bit 5 moved to bit 0 • Functions in bit 6 moved to bit 2 • Functions in bit 7 moved to bit 3 • Functions in bit 1 added
PREZ	TRBPRE	Register name changed and allocation addresses are different.
TZSC	TRBSC	Register name changed and allocation addresses are different.
TZPR	TRBPR	Register name changed and allocation addresses are different.
TZOC	TRBOCR	• Register name changed and allocation addresses are different. • Functions in bit 0 moved to bits 0 and 1 • Functions in bit 2 moved to bit 1 in TRBIOC register • Functions in bit 2 added
—	TRBCR	
TC	—	
TCC0	—	
TCC1	—	
TM0	—	
TM1	—	
TCOUT	—	
—	TRCMR	
—	TRCCR1	
—	TRCIER	
—	TRCSR	
—	TRCIOR0	
—	TRCIOR1	
—	TRC	
—	TRCGRA	

Table 4.6 SFR Differences (3)

R8C/1B Group	R8C/29 Group	Remarks
—	TRCGRB	
—	TRCGRC	
—	TRCGRD	
—	TRCCCR2	
—	TRCDF	
—	TRCOER	
—	TRESEC	
—	TREMIN	
—	TREHR (1)	
—	TREWK (1)	
—	TRECR1	
—	TRECR2	
—	TRECSR	
U0C1	U0C1	Bits 4 and 5 added
U1C1	U1C1	Bits 4 and 5 added
UCON	—	• Functions in bit 0 moved to bit 4 in U0C1 register • Functions in bit 1 moved to bit 4 in U1C1 register • Functions in bit 2 moved to bit 5 in U0C1 register • Functions in bits 4 and 5 moved to bits 0 and 1 in PINSR1 register and functions changed • Functions in bit 7 moved to bit 3 in TRAIOC register
ADCON0	ADCON0	Bit 5 deleted and reset values are different.
—	LINCR	
—	LINST	

Note:
1. These only apply to the N and D versions in the R8C/29 Group.

Table 4.7 Option Function Select Area Differences

R8C/1B Group	R8C/29 Group	Remarks
OFS	OFS	• Bits 5 and 6 added

Note:
1. The option function select area is allocated in the flash memory, not in the SFRs.

4.4 Interrupt Vector Differences

Table 4.8 lists differences in the fixed vector table and Table 4.9 lists differences in the relocatable vector table.

Table 4.8 Differences in Fixed Vector Table

Vector addresses Addresses (L) to (H)	Interrupt Source of R8C/1B Group	Interrupt Source of R8C/29 Group
0FFF0h to 0FFF3h	Watchdog timer Oscillation stop detection Voltage monitor 2	Watchdog timer Oscillation stop detection Voltage monitor 1 (1) Voltage monitor 2

Note:
1. This only applies to the N and D versions in the R8C/29 Group.

Table 4.9 Relocatable Vector Table Differences

Software Interrupt Number	Interrupt Source of R8C/1B Group	Interrupt Source of R8C/29 Group
7	—	Timer RC
10	—	Timer RE
16	Compare 1	—
22	Timer X	Timer RA
24	Timer Z	Timer RB
27	Timer C	—
28	Compare 0	—

5. Reference Documents

R8C/1B Group User's Manual: Hardware Rev.1.30
R8C/29 Group User's Manual: Hardware Rev.2.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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Revision History	R8C/1B Group and R8C/29 Group Differences between R8C/1B Group and R8C/29 Group

Rev.	Date	Description	
		Page	Summary
1.00	June 30, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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