Designing an Idle-Bus Failsafe Network for the HS-26Cxx32 Family

Introduction

This application note describes the design of an idle-bus failsafe network when using the HS-26Cxx32 family of Radiation Hardened RS-422 Receivers.

This family includes HS-26C32EH, HS-26C32RH, HS-26C32RH-T, HS-26CT32EH, HS-26CT32RH, HS-26CLV32EH, and HS-26CLV32RH.

In RS-422 data transmission, there are instances where a receiver might not receive data due to certain bus faults. In such instances, a receiver is required to indicate the fault by turning its output high. This is known as a failsafe feature.

If the connection between the bus and the receiver is broken or open, the receiver inputs float (Figure 1). To indicate this fault, the receiver inputs are internally biased, creating a differential input voltage large enough to turn the receiver output high. This is known as an open-bus failsafe.

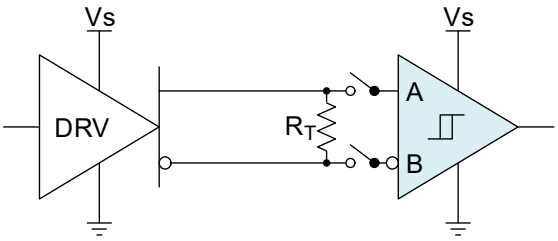


Figure 1. Open Bus: Inputs are Floating

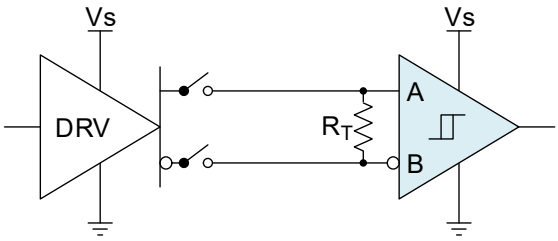


Figure 2. Idle Bus: Inputs are Shorted

Another fault is, when a receiver is connected to a terminated bus and the transmitter at the opposite end of the bus is disabled (Figure 2). In this case, the bus is not actively driven or idle, and the low-impedance termination resistor reduces the differential bus voltage to zero. This is below the input sensitivity of the receiver, making its output state undetermined. Some receiver outputs might turn high, while others turn low or even oscillate.

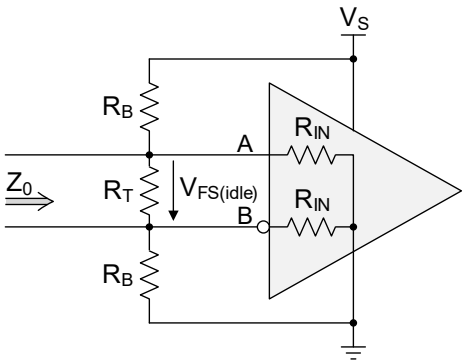
To ensure the receiver output state is high during an idle bus condition, an external resistor network is required to create the necessary input voltage that turns the output high. This is known as an idle-bus failsafe.

While the open-bus failsafe feature is incorporated in the receiver design, the idle-bus failsafe feature must be added.

Contents

1. Design Equations

This section provides design equations for an idle-bus failsafe biasing network.



$$V_{FS} = V_{TH} + V_N$$

$$R_B = \frac{Z_0}{2} \times \frac{V_{S(min)}}{V_{FS}}$$

$$R_T = \frac{2}{2/Z_0 - 1/R_B - n/R_{IN}}$$

V_{FS} = Differential failsafe voltage (≥ 450mV)
V_{TH+} = Positive receiver input threshold (+400mV for HS-26C receivers)
V_N = Noise voltage guard band (typ. 50 to 100mV)
$V_{S(min)}$ = Minimum supply voltage
R_B = Failsafe bias resistor
Z_0 = Characteristic cable impedance (e.g. 100Ω)
R_T = Termination resistor (typ. 100Ω for CAT-5)
n = Number of receivers connected to the bus
R_{IN} = Minimum input resistance (6kΩ for HS-26C receivers)
R_T = Termination resistor

Figure 3. Idle-Bus Failsafe Biasing Network using HS-26Cxx32 Receivers

Table 1 lists the recommended resistor values for R_B and R_T when using the HS-26Cxx32 receivers.

Table 1. Recommended Resistor Values for V_{FS} = 0.5V, RIN(min) = 6kΩ, Z0 = 100Ω

Parameter	Symbol	Values				UNIT
Minimum Supply Voltage	$V_{S(min)}$	3.0		4.5		V
# Bus Receiver	n	1	10	1	10	–
Failsafe Biasing Resistor	R_B	300	300	448	448	Ω
Termination Resistor	R_T	121	133	114	124	Ω

2. Receiver Input Structure

The RS-422 Standard specifies the minimum impedance between a receiver input and receiver ground with 4000Ω. The input impedance is defined as the ratio of an applied input voltage difference to the corresponding difference in measured input current: $R_{IN} = \Delta V_i / \Delta I_i$. These measurements apply with the receiver power supply in both power-on and power-off conditions (Figure 4).

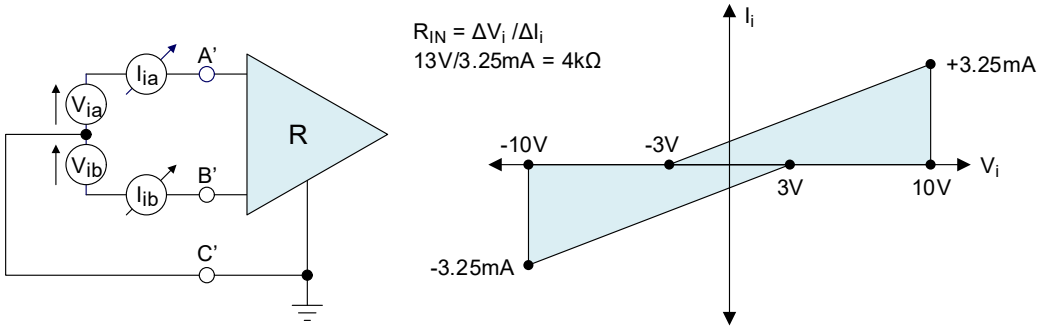


Figure 4. Receiver Input Current-Voltage Measurement

Figure 5 shows the simplified input structure of a HS-26Cxx32 receiver. Both inputs, here denoted as A and B, have identical voltage dividers. The differential failsafe voltage for a bus-open condition, $V_{FS(open)}$, is generated by connecting R_{1a} to the receiver supply and R_{1b} to receiver ground.

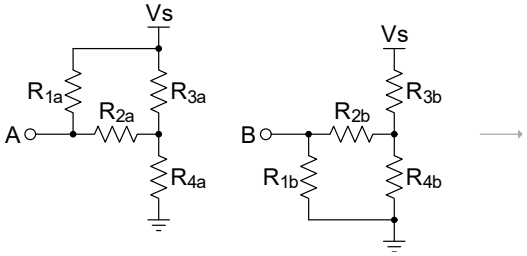


Figure 5. Receiver Input Structure

Applying simple but tedious voltage divider calculations results in the open-circuit input voltages:

$$V_A = V_S \times \left(\frac{R_2}{R_1 + R_2} + \frac{R_4}{R_4 + R_3 \parallel (R_1 + R_2)} \times \frac{R_1}{R_1 + R_2} \right) \quad \text{and} \quad V_B = V_S \times \frac{R_4 \parallel (R_1 + R_2)}{R_3 + R_4 \parallel (R_1 + R_2)} \times \frac{R_1}{R_1 + R_2}$$

Then, calculating their difference yields the open-bus failsafe voltage:

(EQ. 1) $$V_{FS(open)} = \frac{V_S}{1 + R_1 / (R_2 + R_3 \parallel R_4)}$$

In the worst-case condition, when the receiver supply is powered off, both resistors R_{3a} and R_{3b} are parallel to R_{4a} and R_{4b}, respectively. Also, R_{1a} is parallel to the remaining resistor network for input A. This results in an input impedance structure that is common to both inputs (Figure 6).

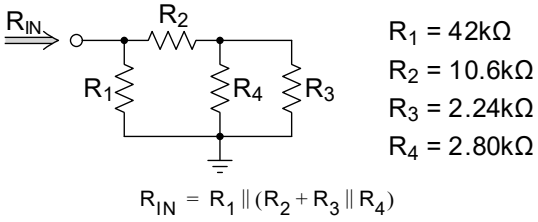


Figure 6. Effective Input Impedance of HS-26Cxx32

Therefore, the impedance is calculated with:

(EQ. 2) $$R_{IN} = R_1 \| (R_2 + R_3 \| R_4)$$

Note: The HS-26Cxx32 internal resistor values in Figure 6 are nominal, therefore, yielding an R_{IN} of 9kΩ. However, across temperature, the minimum input impedance temperature has been determined by $R_{IN(min)}$ = 6kΩ, and therefore 50% higher than the 4kΩ required by the RS-422 Standard.

3. Idle-Bus Failsafe Network

The input sensitivity of a HS-26Cxx32 receiver is specified with ±400mV. A differential input voltage of >+400mV forces the receiver output high, while a V_{ID} <-400mV turns the output low. Voltages between these thresholds cause the output to be undetermined. This condition can occur when a bus driver is disabled, and its outputs become high impedance. In this case, the low-impedance termination resistor reduces the bus voltage to zero and the bus assumes an idle state.

To ensure the receiver output turns high when the bus idles, a resistive failsafe biasing network is implemented to provide a differential voltage across R_T greater than +400mV (Figure 7).

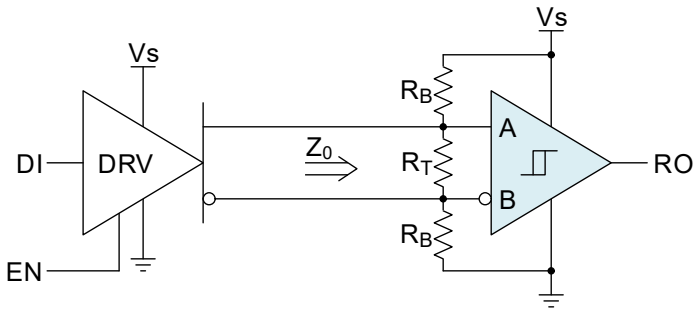


Figure 7. Idle-Bus Failsafe Biasing

Designing a robust failsafe biasing network requires that the idle-bus failsafe voltage includes a noise guard band above the positive receiver input threshold, $V_{FS(idle)} = V_{TH+} + V_N$. V_{TH+} = +400mV and V_N is the expected peak-to-peak noise.

To find an equation for the failsafe voltage, the circuit in Figure 7 is converted into the lumped equivalent circuit of Figure 8, where R_{IN}/n represents the combined input impedance of n receivers.

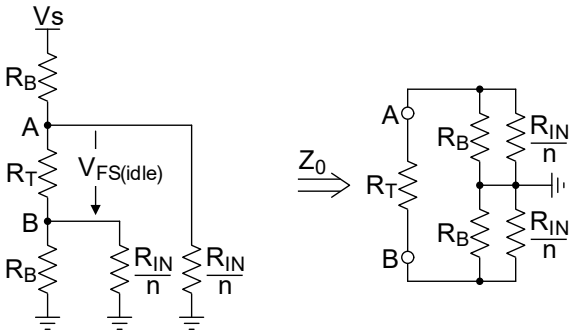


Figure 8. Lumped Equivalent Circuits

Then, establishing the node currents and voltages gives:

Node A $$\frac{V_S - V_A}{R_B} = \frac{V_A - V_B}{R_T} + \frac{V_A}{R_{IN}/n} \Rightarrow V_A = \frac{V_S/R_B + V_B/R_T}{1/R_B + n/R_{IN} + 1/R_T}$$

Node B $\frac{V_A - V_B}{R_T} = \frac{V_B}{R_B} + \frac{V_B}{R_{IN}/n} \Rightarrow V_B = \frac{V_A/R_T}{1/R_B + n/R_{IN} + 1/R_T}$

Deriving the failsafe voltage $V_{FS(idle)} = V_A - V_B$ yields:

(EQ. 3) $$V_{FS(idle)} = \frac{V_S}{1/R_B(2/R_T + n/R_{IN})}$$

And solving for R_T gives:

(EQ. 4) $$R_T = \frac{2}{(V_S/V_{FS(idle)} - 1)/R_B - n/R_{IN}}$$

The second design requirement in Figure 8 is that the impedance of the resistor network (including R_T) must match the characteristic cable impedance Z_0:

(EQ. 5) $$Z_0 = R_T \| 2(R_{IN}/n \| R_B)$$

Solving this equation for R_T gives:

(EQ. 6) $$R_T = \frac{2}{2/Z_0 - 1/R_B - n/R_{IN}}$$

Then, equating both R_T equations (Equation 4 = Equation 6) and solving for R_B provides the bias resistor value:

(EQ. 7) $$R_B = \frac{Z_0}{2} \times \frac{V_S}{V_{FS(idle)}}$$

Having established R_B, use Equation 6 to calculate R_T.

4. Other Design Considerations

At high data rates, the capacitance of the transmission cable can round the edges of the bus signal significantly. Counteract this effect by making R_{IN} slightly smaller than Z_0. This results in an underdamped termination that maintains the crisp edges of fast signal transitions.

Also, try minimizing the ground potential difference (GDP) between driver and receiver. The RS-422 Standard demands high common-mode capability for the receiver but none for the driver. However, in an idle bus condition, the GPD adds to the receiver common-mode input voltage, which can quickly exceed the absolute maximum voltage ratings of the driver's bus and supply terminals.

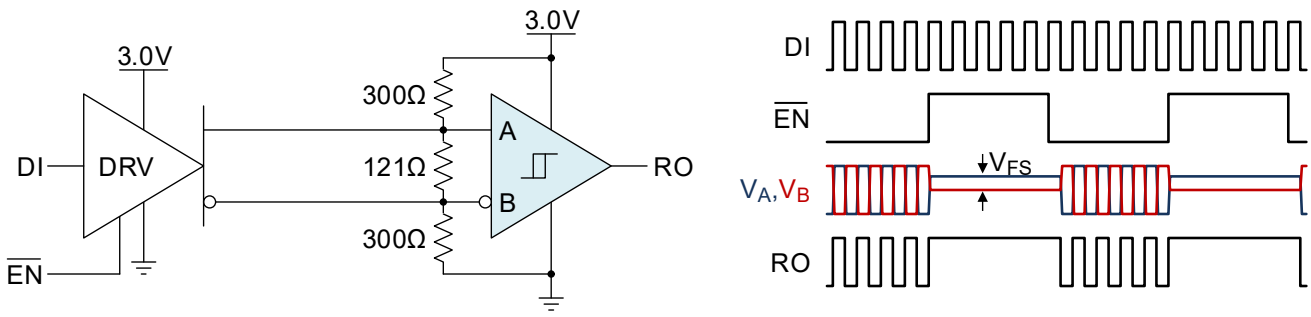


Figure 9. Idle-Bus Failsafe in Action with HS-26CLV31 Driver and HS-26CLV32 Receiver

5. Conclusion

The design methodology for implementing an idle-bus failsafe network using the HS-26Cxx32 family of RS-422 receivers is outlined in this application note. While these devices include internal mechanisms for open-bus fault detection, idle-bus conditions require an external biasing network to ensure predictable receiver behavior. Detailed design equations and resistor selection guidelines are provided to achieve the required differential input voltage and impedance matching. By following these recommendations and accounting for factors such as ground potential differences and signal integrity at high data rates, designers can ensure robust and reliable system performance in demanding environments.

6. Revision History

Revision	Date	Description
1.00	Jun 2, 2025	Initial release.

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