

ISL73847x 2-Phase Design Example with Calculations

The purpose of this document is to provide an example of how to calculate supporting components for the ISL73847x 2-phase applications. This document also introduces an Excel design calculator that automatically calculates all these values.

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1. 2-Phase Design

1.1 Initial Design Values

List out all the initial design values and any ISL73847x required parameters.

- $V_{IN} = 12V$
- $V_{OUT} = 1V$
- $V_{REF} = 0.6V$
- $I_{OUT(MAX)} = 50A$
- $n = 2$ (number of phases)
- $f_{SW} = 500kHz$
- $A_{CSA} = 8mV/mV$
- $I_{STEP} = 25A$
- $tran_{percent} = 2\%$
- $g_{m(EA)} = 4mA/V$
- $DRP_{percent} = 4\%$
- $I_{DROOP} = 19.9\mu A$
- $t_{SS} = 1ms$
- $I_{SS} = 10\mu A$

1.2 Determining the Frequency Select Resistor

The default switching frequency of the ISL73847x is 500kHz. To change the switching frequency, use a pull-down resistor from the FS pin to GND. Refer to the EC table in the datasheet for the recommended R_{FS} resistor values for 250kHz, 500kHz, 1MHz, and 1.5MHz switching frequencies, as these are tested. Use [Equation 1](#) for other frequencies to calculate R_{FS} , where f_{OSC} is twice the switching frequency (f_{SW}).

$$(EQ. 1) \quad R_{FS}[k\Omega] = \left(\frac{56497}{f_{SW}[kHz]} \right) - 20.96$$

$$R_{FS} = \left(\frac{56497}{500} \right) - 20.96$$

$$\therefore R_{FS} = 92.03k\Omega$$

The equation suggests using a 92k Ω R_{FS} resistor. However, the EC table shows that a 94.2k Ω resistor gives a 1MHz internal oscillator frequency (500kHz PWM output switching frequency).

1.3 Determining the Output Voltage Feedback Resistors

The required output voltage is 1V, the internal voltage reference is 0.6V typical, and as a starting point Renesas suggests making R_1 4.99k Ω .

$$(EQ. 2) \quad V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)$$

Rearrange the equation:

$$(EQ. 3) \quad R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_1$$

$$R_2 = \left(\frac{1}{0.6} - 1\right) \times 4.99k\Omega$$

$$\therefore R_2 = 3.327k\Omega$$

A good option for R_2 is a 3.32k Ω resistor with $\pm 0.1\%$ tolerance. Calculating the output voltage with this value gives an output voltage of 0.999V.

1.4 Determining the Current-Sense Resistor

The target current-sense amplifier input voltage is 50mV, maximum output current is 50A, the number of phases is two, and the OCP1 sense voltage is 75mV.

$$(EQ. 4) \quad R_{SEN}[\Omega] = \frac{V_{SEN}[V] \times n}{I_{OUT(MAX)}[A]}$$

$$R_{SEN} = \frac{50 \times 10^{-3} \times 2}{50}$$

$$\therefore R_{SEN} = 2m\Omega$$

$$(EQ. 5) \quad P_{RSEN}[W] = \frac{V_{OCP1}[V]^2}{R_{SEN}[\Omega]}$$

$$P_{RSEN} = \frac{(75 \times 10^{-3})^2}{2 \times 10^{-3}}$$

$$\therefore P_{RSEN} = 2.813W$$

1.5 Determining the Output Inductor

Use Equation 6 to calculate a good estimate for the output inductor based on a required ripple current, where $I_{OUT} = n \times I_{PHASE}$.

$$(EQ. 6) \quad L_{REC}[H] = \frac{(V_{IN} - V_{OUT})[V] \times D \times n}{k \times f_{SW}[Hz] \times I_{OUT(MAX)}[A]}$$

The input voltage is 12V, the calculated output voltage is 0.999V, the duty cycle is $D = 1V/12V = 0.0833$, the output switching frequency is 500kHz, the number of phases is 2, the required ripple current (k) is 30% and the max output current is 50A (2x25A).

$$\therefore L_{REC} = \frac{(12 - 0.999) \times 0.0833 \times 2}{500 \times 10^3 \times 50} = 244.5nH$$

An available inductor value is $L_{SEL} = 220nH$. This value is also close to the recommended value of 244nH. Use Equation 7 to calculate the actual inductor ripple percentage for the chosen inductor.

$$(EQ. 7) \quad ripple[\%] = \frac{(V_{IN} - V_{OUT})[V] \times D \times n}{f_{SW}[Hz] \times I_{OUT(MAX)}[A] \times L_{SEL}[H]}$$

$$\therefore ripple = \frac{(12 - 0.999) \times 0.0833 \times 2}{(500 \times 10^3) \times 50 \times (220 \times 10^{-9})} = 33.3\%$$

1.6 Determining the Current-Sense Filter

The current-sense ISEN signal must be filtered before going to the ISL73847x ISENx pins to eliminate high-frequency switching noise and extract the current signal information. In addition, the parasitic ESL of the current-sense resistor creates an inductive divider with the output inductor and adds a square wave component to the current-sense signal, which can prematurely trip overcurrent. To fix this issue, an RC filter must be placed across the ISENx traces and as close as possible to the ISL73847x device. Use Equation 12 to calculate the zero formed by the R_{SENSE} parasitic ESL and L_{OUT} . R_{SENSE} is the current-sense resistance of 2mΩ, V_{IN} is the buck input voltage of 12V, L_{OUT} is the output inductor of 220nH, and V_{ESL} is the voltage amplitude of the parasitic square wave component created by the parasitic inductance of the R_{SENSE} and L_{OUT} , which is 50mV. V_{ESL} is determined by the specific components used on the board and can be measured with oscilloscope captures of the current-sense signal without filtering.

$$(EQ. 8) \quad f_{ZERO}[Hz] = \frac{R_{SENSE}[\Omega] \times V_{IN}}{2\pi \times L_{OUT}[H] \times V_{ESL}}$$

$$(EQ. 9) \quad f_{ZERO}[Hz] = \frac{(2 \times 10^{-3}) \times 12V}{2\pi \times (220 \times 10^{-9}) \times (50 \times 10^{-3})} = 347.25kHz$$

For the ISL73847x, a bit of the ESL square-wave signal must be left to achieve short T_{ON} because the bandwidth of the current-sense amplifier itself creates filtering of the current-sense signal. Therefore, to achieve a triangular signal at the PWM input, the user must relax filtering on the CSA input. Use Equation 10 to calculate the filter resistor, so the corner-frequency of the RC filter is seven times higher than the ESL zero, where C_F is the filter capacitor of 680pF.

$$(EQ. 10) \quad R_F[\Omega] = \frac{1}{2\pi \times 7 \times f_{ZERO} \times C_F}$$

$$(EQ. 11) \quad R_F[\Omega] = \frac{1}{2\pi \times 7 \times (347.25 \times 10^3) \times (680 \times 10^{-12})} = 96.3\Omega$$

For the full possible range of V_{IN} on the ISL73847x buck supply, an R_F of 30.1Ω and C_F of 680pF are good choices for the RC filter.

1.7 Determining the Slope Compensation Resistor

Use Equation 12 to calculate the slope compensation resistor. R_{SEN} is 2mΩ, R_{FS} is 94.2kΩ, V_{OUT} is 0.999V, k is 25kV/s, L_{SEL} is 220nH. If the R_{SLOPE} calculated is less than 25kΩ, increase the L_{SEL} , and vice versa if R_{SLOPE} is greater than 100kΩ.

$$(EQ. 12) \quad R_{SLOPE}[\Omega] = \frac{R_{SEN}[\Omega] \times R_{FS}[\Omega] \times V_{OUT}[V]}{k \times L_{SEL}}$$

$$\therefore R_{SLOPE} = \frac{(2 \times 10^{-3}) \times (94.2 \times 10^3) \times 0.999}{(25 \times 10^3) \times (220 \times 10^{-9})} = 34.2k\Omega$$

The equation suggests a 34.2kΩ R_{SLOPE} value, which is between 25kΩ and 100kΩ. A good option is 34.8kΩ.

1.8 Determining the Error-Amplifier Compensation Resistor

To calculate the output capacitor and compensation values, ΔV_{OUT} and ΔI_{OUT} must be known. ΔV_{OUT} is the amount of output voltage deviation during a load step, in this example it is $2\% \times 0.999V = 19.98mV$, and ΔI_{OUT} is the load step which is 25A. With these two known values, use Equation 13 to calculate the equivalent load-line output impedance R_{LL} .

$$(EQ. 13) \quad R_{LL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$\therefore R_{LL} = \frac{19.98 \times 10^{-3}}{25} = 0.8m\Omega$$

With the load-line impedance, use Equation 14 to calculate R_{COMP} , where V_{OUT} is 0.999V, R_{SEN} is 2m Ω , A_{CSA} is 8mV/mV, n is 2, V_{REF} is 0.6V, $g_{m(EA)}$ is 4mS, and R_{LL} is 0.8m Ω .

$$(EQ. 14) \quad R_{COMP} = \frac{V_{OUT}[V] \times R_{SEN}[\Omega] \times A_{CSA}[mV/mV]}{n \times V_{REF}[V] \times g_{m(EA)}[A/V] \times R_{LL}[\Omega]}$$

$$(EQ. 15) \quad R_{COMP} = \frac{0.999 \times (2 \times 10^{-3}) \times 8}{2 \times 0.6 \times (4 \times 10^{-3}) \times (0.8 \times 10^{-3})} = 4.162k\Omega$$

A good compensation resistor is a 4.22k Ω .

1.9 Determining the Output Capacitance

Use Equation 16 to determine the minimum output capacitance. The compensation resistor is 4.22k Ω , the error amplifier transconductance is 4mA/V or 4mS, the internal voltage reference is 0.6V, f_T is the converter unity-gain frequency, which Renesas recommends setting a decade below the switching frequency ($f_T = f_{SW}/10 = 500kHz/10 = 50kHz$), A_{CSA} is 8mV/mV, and the calculated output voltage is 0.999V.

$$(EQ. 16) \quad C_{OUT(MIN)} = \frac{n \times R_{COMP}[\Omega] \times g_{m(EA)}[V/A] \times V_{REF}[V]}{2\pi \times f_T[Hz] \times A_{CSA}[mV/mV] \times R_{SEN}[\Omega] \times V_{OUT}[V]}$$

$$\therefore C_{OUT(MIN)} = \frac{2 \times (4.22 \times 10^3) \times (4 \times 10^{-3}) \times 0.6}{2\pi \times (50 \times 10^3) \times 8 \times (2 \times 10^{-3}) \times 0.999} = 4033\mu F$$

A good option is paralleling twenty-four 220 μF capacitors, or twelve per phase, which gives 5280 μF of bulk output capacitance.

With the actual total output capacitance value chosen, recalculate f_T by rearranging Equation 16 to create Equation 17.

$$(EQ. 17) \quad f_T[Hz] = \frac{n \times R_{COMP}[\Omega] \times g_{m(EA)}[V/A] \times V_{REF}[V]}{2\pi \times C_{OUT}[F] \times A_{CSA}[mV/mV] \times R_{SEN}[\Omega] \times V_{OUT}[V]}$$

$$\therefore f_T[Hz] = \frac{2 \times (4.22 \times 10^3) \times (4 \times 10^{-3}) \times 0.6}{2\pi \times (5280 \times 10^{-6}) \times 8 \times (2 \times 10^{-3}) \times 0.999} = 40kHz$$

1.10 Determining the Error-Amplifier Compensation Capacitor

Use Equation 18 to determine the error-amplifier compensation capacitor. f_z is the zero frequency of the error amplifier. Renesas recommends setting the zero formed by R_{COMP} and C_{COMP} a decade smaller than the f_T ($f_z = f_T/10 = 40\text{kHz}/10 = 4\text{kHz}$), where R_{COMP} is $4.22\text{k}\Omega$.

$$\text{(EQ. 18)} \quad C_{COMP}[F] = \frac{1}{2\pi \times f_z[\text{Hz}] \times R_{COMP}[\Omega]}$$

$$\therefore C_{COMP} = \frac{1}{2\pi \times (4 \times 10^3) \times (4.22 \times 10^3)} = 9.43\text{nF}$$

A good option for the compensation capacitor is 10nF .

1.11 Determining the Pole Capacitor

Adding a pole capacitor is recommended to cancel out the zero formed by the equivalent bulk output capacitance and ESR. To determine the pole capacitor, first determine the equivalent total ESR of the parallel combination of output capacitors. The $220\mu\text{F}$ output capacitors chosen have $6\text{m}\Omega$ of ESR individually, so the parallel combination of twenty-four of these output capacitors have an equivalent total ESR of $6\text{m}\Omega/24 = 0.250\text{m}\Omega$, as shown in Equation 19.

Note: This equation and the ones that follow apply only if all capacitors in parallel are identical with equal capacitance and ESR values.

$$\text{(EQ. 19)} \quad ESR_{TOTAL}[\Omega] = \frac{ESR[\Omega]}{\# \text{ of capacitors}}$$

$$\therefore ESR_{TOTAL} = \frac{6 \times 10^{-3}}{24} = 0.250\text{m}\Omega$$

Lastly, add a pole to the controller loop at the same frequency as the zero formed by the equivalent C_{OUT} and ESR, using Equation 20.

$$\text{(EQ. 20)} \quad C_{POLE}[F] = \frac{C_{OUT}[F] \times ESR[\Omega]}{R_{COMP}[\Omega]}$$

$$\therefore C_{POLE} = \frac{(5280 \times 10^{-6}) \times (0.25 \times 10^{-3})}{4.22 \times 10^3} = 312.8\text{pF}$$

A good option for the pole capacitor is 330pF .

1.12 Determining the Droop Regulation Resistor and Capacitor

Use Equation 21 to determine the droop resistor. The required percentage of droop regulation at full load is 4%, the internal voltage reference is 0.6V, the droop current at full load is 19.9μA, the number of phases for this design is 2, and one ISL73847x Controller.

$$(EQ. 21) \quad R_{DROOP}[\Omega] = \frac{DRP_{\text{percent}} \times V_{REF}[V]}{I_{DROOP}[\mu A] \times n} \times \# \text{ of Controllers}$$

$$\therefore R_{DROOP} = \frac{4\% \times 0.6}{(19.9 \times 10^{-6}) \times 2} \times 1 = 603\Omega$$

A good option for R_{DROOP} is 603kΩ. Use Equation 22 to determine the droop capacitor. The compensation resistor is 4.22kΩ, and the compensation capacitor is 10nF.

$$(EQ. 22) \quad C_{DROOP}[F] = \frac{R_{COMP}[\Omega] \times C_{COMP}[F]}{R_{DROOP}[\Omega]}$$

$$\therefore C_{DROOP} = \frac{(4.22 \times 10^3) \times (10 \times 10^{-9})}{604} = 69.87\text{nF}$$

A good option for C_{DROOP} is 82nF.

1.13 Determining the Soft-Start Capacitor and In-Rush Current

Use Equation 23 to determine the soft-start capacitor. The required soft-start time is 1ms, the soft-start current is 10μA and the voltage reference is 0.6V.

$$(EQ. 23) \quad C_{SS}[F] = \frac{t_{SS}[s] \times I_{SS}[A]}{V_{REF}[V]}$$

$$\therefore C_{SS} = \frac{0.001 \times (10 \times 10^{-6})}{0.6} = 16.78\text{nF}$$

A good option for C_{SS} is 22nF.

Use Equation 23 to calculate the expected soft-start time with this C_{SS} value.

$$(EQ. 24) \quad t_{SS}[s] = \frac{(22 \times 10^{-9}) \times 0.6}{10 \times 10^{-6}}$$

$$\therefore t_{SS} = 1.32\text{ms}$$

Use Equation 25 to calculate the in-rush current. The output capacitance is 5280μF, the calculated output voltage is 0.999V, and the duty cycle is 0.0833.

$$(EQ. 25) \quad I_{RUSH}[A] = \frac{D \times V_{OUT}[V] \times C_{OUT}[F]}{t_{SS}[s]}$$

$$\therefore I_{RUSH}[A] = \frac{0.0833 \times 0.999 \times (5280 \times 10^{-6})}{0.00132} = 0.333\text{A}$$

1.14 Summary of all the Calculated Component Values

- $R_{FS} = 92k\Omega \approx 94.2k\Omega$ (value pulled from the EC table)
- $R_1 = 3.327k\Omega \approx 3.32k\Omega$, with $\pm 0.1\%$ tolerance
- $R_2 = 4.99k\Omega$
- $V_{OUT} = 0.999V$
- $R_{SEN} = 2m\Omega$
- $R_{FIL} = 30.1\Omega$
- $C_{FIL} = 680pF$
- $L_{OUT} = 220nH/\text{phase}$
- $R_{SLOPE} = 34.23k\Omega \approx 34.8k\Omega$
- $R_{COMP} = 4.17k\Omega \approx 4.22k\Omega$
- $C_{OUT} = 220\mu F \times 24 = 5280\mu F$ (2640 μF /phase)
- $C_{COMP} = 9.8nF \approx 10nF$
- $R_{DROOP} = 604\Omega \approx 604\Omega$
- $C_{DROOP} = 70nF \approx 82nF$
- $C_{SS} = 17nF \approx 22nF$
- $C_{POLE} = 330pF$

Figure 1 shows an image of the ISL73847x Design Tool (Excel file) that automatically calculates all of these values for the 2-phase application design.

B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
 These cells are inputs These cells are the output														
ISL73847x Design Tool (Rev 4.0)														
Input Voltage (V_{IN})	12	V		Use DROOP?	Yes									
Output Voltage (V_{OUT})	1	V		Target ΔV_{OUT} with DROOP ($DRP_{PERCENT}$)	4	%								
Max Load Current ($I_{OUT(MAX)}$)	50	A		Output Load Step (ΔI_{OUT})	25	A								
Switching Frequency (f_{SW})	500	kHz		Target ΔV_{OUT} During Load Transient ($trans_{PERCENT}$)	2	%								
Oscillator Frequency ($f_{OSC} = 2 \times f_{SW}$)	1,000	kHz												
Number of Phases (n)	2			Recommended DROOP Resistance per Controller (R_{DROOP})	603	Ω								
Number of Controllers	1			Selected DROOP Resistor per Controller (R_{DROOP})	603	Ω								
Duty Cycle (d)	8.333	%		DROOP Capacitor (C_{DROOP})	78.77	nF								
Max ON Time (t_{ON})	166.667	ns												
Max OFF Time (t_{OFF})	1833.333	ns		Equivalent Load-Line Output Impedance (R_{LL})	0.799	m Ω								
ON/OFF Time Problem?	No			Recommended Compensation Resistor (R_{COMP})	4.669	k Ω								
Switching Frequency Problem? ($250kHz \leq f_{SW} \leq 1,500kHz$)	No			Selected Compensation Resistor (R_{COMP})	4.75	k Ω								
Use External Clock on SYNC-I ($f_{OSC} \leq 15\%$)?	No			Recommended Crossover Frequency ($f_c = f_{SW}/10$)	50.00	kHz								
Frequency Select Resistor (R_{FS})	94.2	k Ω		Minimum Output Capacitance ($C_{OUT(MIN)}$)	4,051.55	μF								
Bottom Output Feedback Resistor (R_B)	4.99	k Ω		Output Capacitance (C_{OUT})	5,280.00	μF								
Top Feedback Resistor (R_T)	3.327	k Ω		Crossover Frequency (f_c)	38.4	kHz								
Selected Top Feedback Resistor (R_T)	3.32	k Ω		Bulk Capacitor ESR Equivalent (ESR_{COUT})	0.25	m Ω								
Calculated Output Voltage (V_{OUT})	0.999	V		Bulk Output COUT/ESR Zero Frequency (f_z)	120.57	kHz								
				Recommended Pole Capacitor (C_{POLE})	277.89	pF								
Output f_{SW} on SYNC-O pin?	100k Ω SYNC-O to VCC													
Output f_{SYNC-I} or f_{OSC} on SYNC-O pin?	100k Ω SYNC-O to GND			Recommended Zero Frequency ($f_z = f_c/10$)	3.84	kHz								
				Recommended Compensation Capacitor (C_{COMP})	8.73	nF								
Recommended Current Sense Resistor (R_{SEN})	2	m Ω		Selected Compensation Capacitor (C_{COMP})	10	nF								
Selected Current Sense Resistor (R_{SEN})	2	m Ω		Zero Frequency (f_z)	3.35	kHz								
R_{SEN} Power Dissipation @ OCP1 (P_{DSEN})	2.813	W												
				Target In-rush Current (I_{RUSH})	0.333	A								
Target Ripple Current (ΔI_L)	30	%		Recommended Soft-Start Capacitor (C_{SS})	22.00	nF								
Recommended Inductor Value (L_{IND})	244.46	nH		Soft-Start Time (t_{SS})	1.32	ms								
Selected Inductor Value (L_{IND})	220	nH		Selected Soft-Start Capacitor (C_{SS})	22	nF								
Inductor (L_{IND}) Ripple Current (ΔI_L)	33.33	%		In-rush Current (I_{RUSH})	0.333	A								
Inductor (L_{IND}) Ripple Current per phase ($\Delta I_{L(PHASE)}$)	8.333	A		Soft-Start Time (t_{SS})	1.32	ms								
Slope Resistor (R_{SLOPE})	34.23	k Ω												
Slope Resistor Problem? ($25k\Omega \leq R_{SLOPE} \leq 100k\Omega$)	No													
Main DS Parameters COUT Network Design CIN Network Design Capacitor Impedance Common Resistor Values Common Capacitor Values + x														

Figure 1. Automatic Design Results for a 2-Phase ISL73847 Application Design

2. Conclusion

An Excel [ISL73847x Design Tool](#) that automatically calculates all the values derived in this document and more is available. However, it is beneficial to know how they were derived and to hand calculate some of the values.

3. Revision History

Revision	Date	Description
1.02	Jun 5, 2025	Added Determining the Current-Sense Filter section. Minor text updates throughout.
1.01	Dec 8, 2023	Updated $g_{m(EA)}$ value from 3.57 to 4 throughout. Updated Equations 11, 12, 13, 14, 16, and 18. Updated Summary of all the Calculated Component Values.
1.00	Nov 15, 2023	Initial release.

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