R32C/100 Series

Using Timer A to Output a Variable Period and Duty Ratio PWM Waveform

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Abstract

This document describes using timer A to output a PWM waveform that has a variable period and duty ratio.

Products

R32C/116 Group
R32C/117 Group
R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This document describes using timer A0 and timer A1 to output a PWM waveform that has a variable period and duty ratio. Connect timer A0 (in timer mode) to timer A1 (in one-shot timer mode). Alternate outputting PWM waveforms from port P7_2 (TA1OUT); alternate outputting a 1 ms PWM period and 0.5 ms high level width of a PWM pulse with a 0.5 ms PWM period and 0.1 ms high level width of a PWM pulse.
Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Timer Connection.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Timer A0 in timer mode	Timer A1 trigger signal
Timer A1 in one-shot timer mode	Use TA1OUT output in PWM output

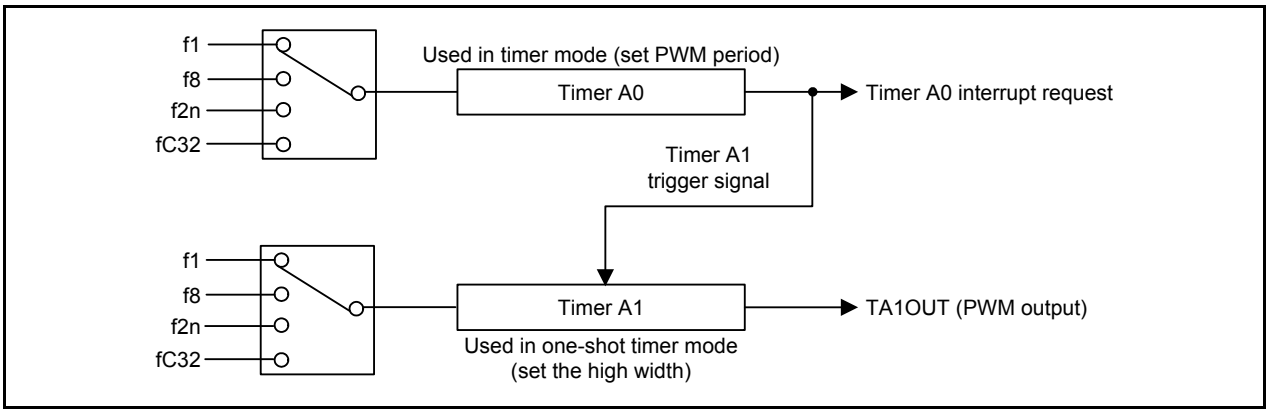

Figure 1.1 Timer Connection

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64189DFD (R32C/118 Group)
Operating frequencies	Main clock: 16 MHz PLL clock: 100 MHz Base clock: 50 MHz CPU clock: 50 MHz Peripheral bus clock: 25 MHz Peripheral function clock source: 25 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.08
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00
Renesas Starter kit	R0K564189S000BE

3. Reference Application Notes

Application notes associated with this application note are listed below. Refer to these application notes for additional information.

- R32C/100 Series Timer A Operation in Timer Mode (REJ05B1230-0100)
- R32C/100 Series Timer A Operation in One-shot Timer Mode (REJ05B1200-0100)

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

Table 4.1 Pin Used and Its Function

Pin Name	I/O	Function
P7_2	Output	TA1OUT output (outputs a PWM waveform)

5. Software

5.1 Operation Overview

(1) Initial setting
Perform initial setting for timer A0 and timer A1. Table 5.1 lists the initial setting values for timer A0 and timer A1.

Table 5.1 Initial Setting Values for Timer A0 and Timer A1

	Timer A0	Timer A1
Mode	Timer mode	One-shot timer mode
Start trigger	Set the TA0S bit in the TABSR register to 1	Timer A0 underflow
Count source	f1	f1
Port output	None	P7_2 (TA1OUT output selected)
Count value	12500 - 1 (0.5 ms)	2500 (0.1 ms)
Gate function	No gate function	No corresponding function

(2) Timer A0 count starts
When the TA0S or TA1S bit in the TABSR register is set to 1 (start counter), the timer A0 counter starts counting.

(3) Timer A0 underflows
When the timer A0 counter underflows, the value in the reload register is reloaded and the count continues. At this time, the IR bit in the TA0IC register becomes 1 (interrupt requested).

(4) Timer A1 count starts
The timer A0 underflow is the trigger that starts the timer A1 counter. At the same time, the output level of the TA1OUT pin becomes high.

(5) Count value reset
The timer A0 and timer A1 count values are reset by the timer A0 interrupt occurring. Table 5.2 lists the interrupt setting values of timer A0 and timer A1.

Table 5.2 Interrupt Setting Values of Timer A0 and Timer A1

	Timer A0	Timer A1
Count value	25000 - 1 (1 ms)	12500 (0.5 ms)

Each count value is reloaded when timer A0 underflows and timer A1 underflows, respectively. Thereafter, each time the timer A0 interrupt occurs, the count values in Table 5.1 and Table 5.2 are alternately set to timer A0 and timer A1.

(6) Timer A1 underflows
When the timer A1 counter value becomes 0, the output level of the TA1OUT pin becomes low, the counter reloads the value from the reload register and stops counting.

Figure 5.1 shows the Timing Diagram.

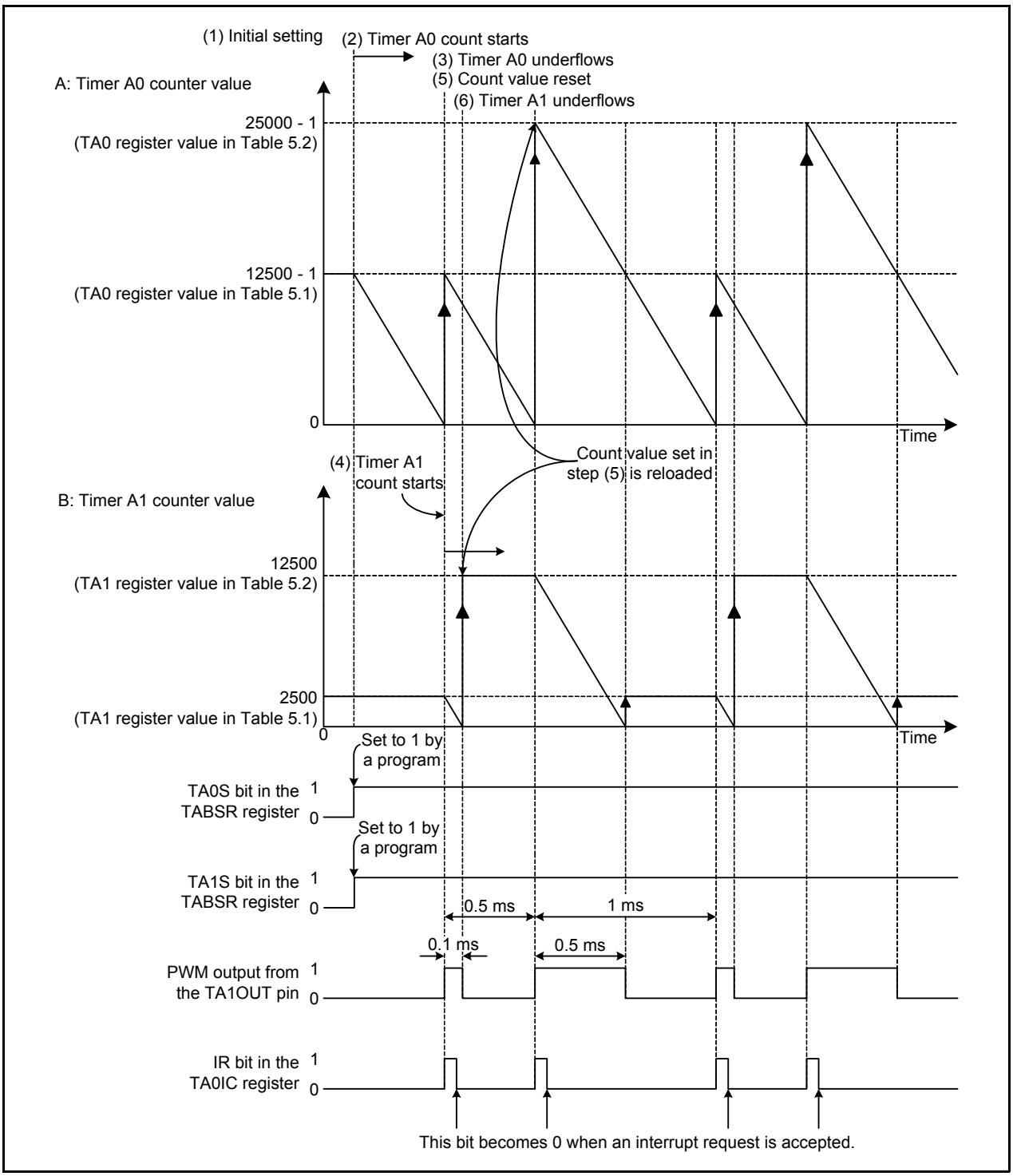

Figure 5.1 Timing Diagram

5.2 Constants

Table 5.3 lists the Constants Used in the Sample Code.

Table 5.3 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
PWM_INTERVAL	12500 - 1	PWM period (timer A0 initial setting value is 0.5 ms)
PWM_H_PERIOD	2500	High level width of PWM pulse (timer A1 initial setting value is 0.1 ms)
PWM_INTERVAL_VARIATE	12500	Variate of PWM period (0.5 ms)
PWM_H_PERIOD_VARIATE	10000	Variate of high level width of PWM pulse (0.4 ms)
MAX_INT_CNT	2	Maximum value of int_cnt

5.3 Variable

Table 5.4 lists the Global Variable.

Table 5.4 Global Variable

Type	Variable Name	Contents	Function Used
unsigned char	int_cnt	Number of timer A0 interrupt occurrences	_timer_a0

5.4 Functions

Table 5.5 lists the Functions.

Table 5.5 Functions

Function Name	Outline
timer_a0_init	Timer A0 initial setting
timer_a1_init	Timer A1 initial setting
_timer_a0	Timer A0 interrupt handling

5.5 Function Specifications

The following tables list the sample code function specifications.

timer_a0_init	
Outline	Timer A0 initial setting
Header	None
Declaration	void timer_a0_init(void)
Description	Initial setting to use timer A0 in timer mode. The count value is set to 12500 - 1 (0.5 ms), and the timer A0 interrupt is also set.
Argument	None
Returned value	None
Remark	

timer_a1_init	
Outline	Timer A1 initial setting
Header	None
Declaration	void timer_a1_init(void)
Description	Initial setting to use timer A1 in one-shot timer mode. The timer A0 underflow is set as the trigger to start the count, and the count value is set to 2500 (0.1 ms). The timer A1 interrupt is disabled.
Argument	None
Returned value	None
Remark	

_timer_a0	
Outline	Timer A0 interrupt handling
Header	None
Declaration	void _timer_a0(void)
Description	int_cnt increments and becomes 0 when it matches with MAX_INT_CNT. The count values for timer A0 and timer A1 are reset.
Argument	None
Returned value	None
Remark	

5.6 Flowcharts

5.6.1 Main Processing

Figure 5.2 shows the Main Processing.

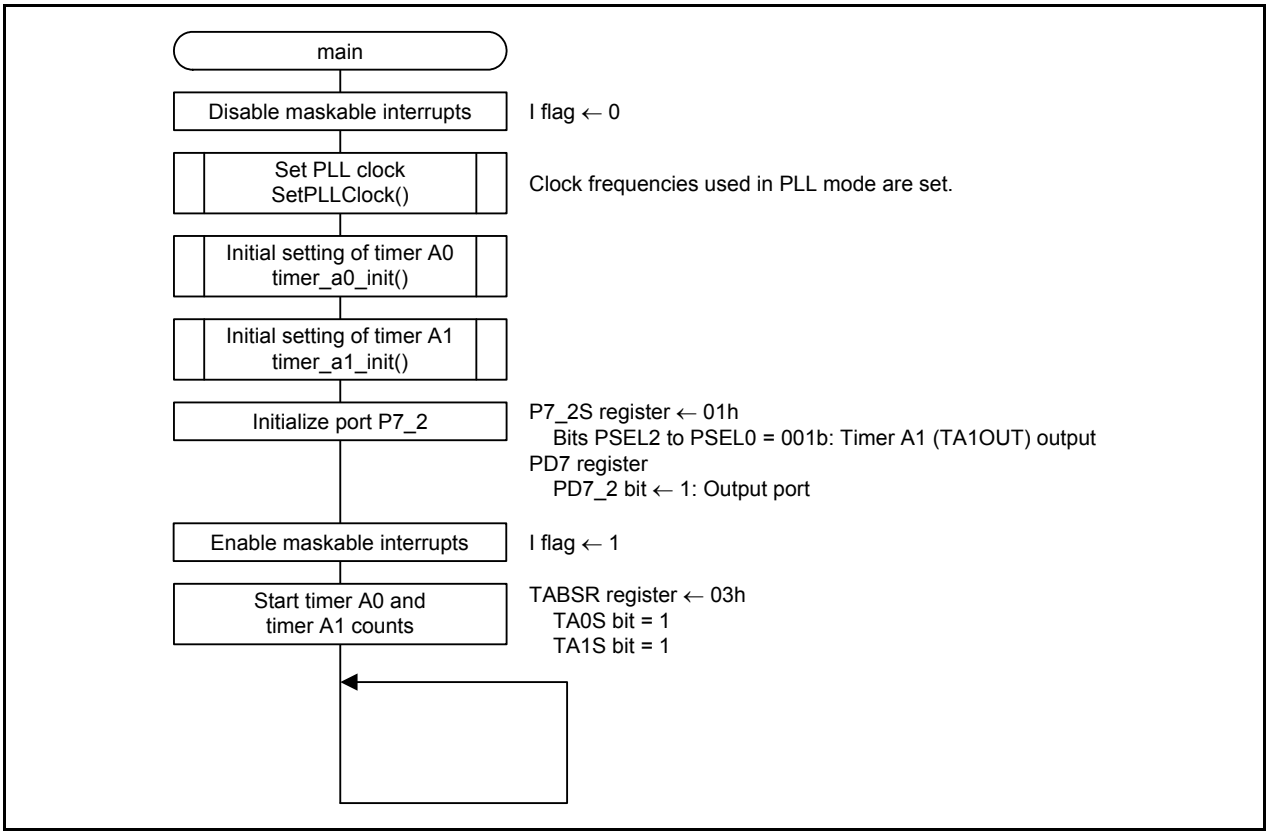

Figure 5.2 Main Processing

5.6.2 Timer A0 Initial Setting

Figure 5.3 shows the initial setting for timer A0.

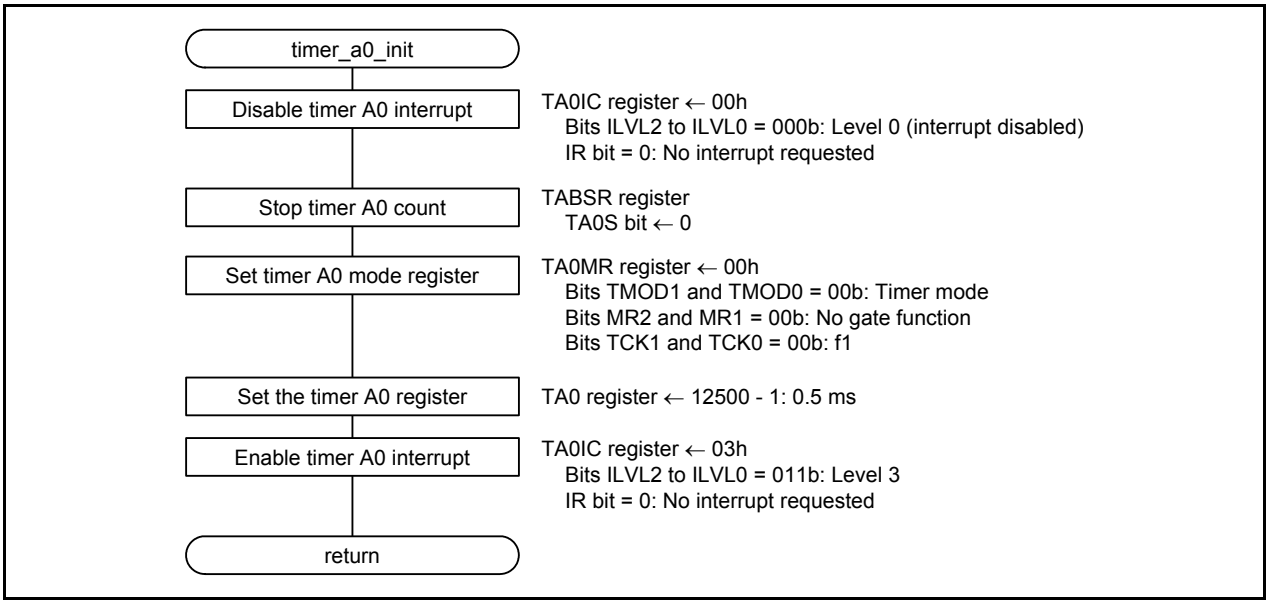

Figure 5.3 Timer A0 Initial Setting

5.6.3 Timer A1 Initial Setting

Figure 5.4 shows the initial setting of timer A1.

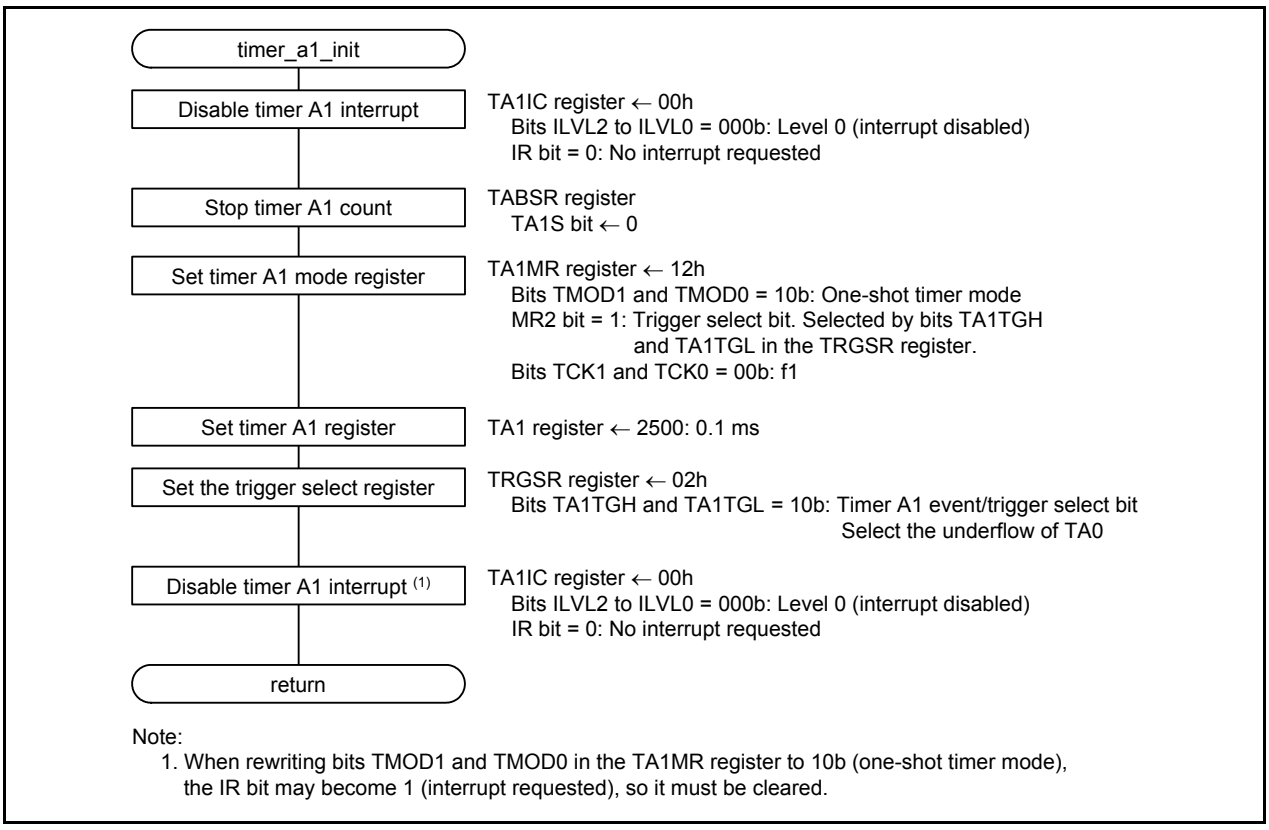

Figure 5.4 Timer A1 Initial Setting

5.6.4 Timer A0 Interrupt Handling

Figure 5.5 shows the interrupt handling for timer A0.

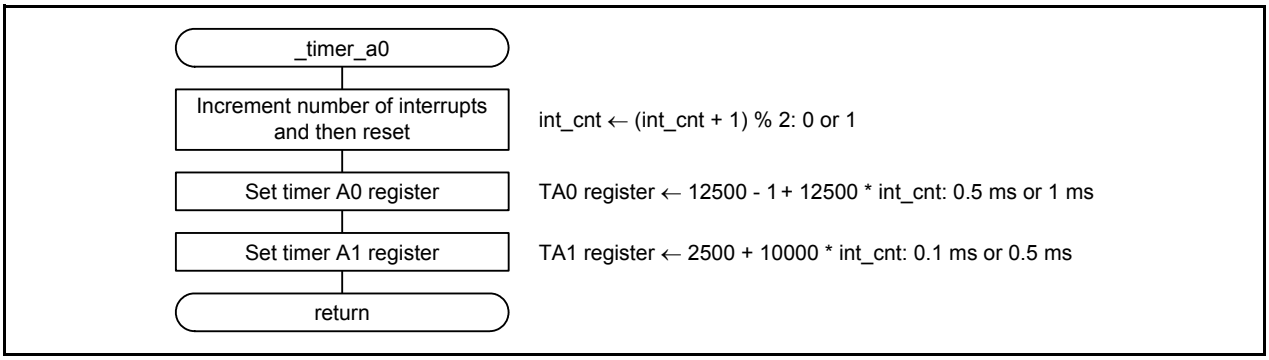

Figure 5.5 Timer A0 Interrupt Handling

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
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Revision History	R32C/100 Series Using Timer A to Output a Variable Period and Duty Ratio PWM Waveform

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 24, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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