R32C/100 Series

Transmitting/Receiving Data Using the Serial Bus Interface in Synchronous Serial Communication Mode

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Abstract

This document describes a program for transmitting/receiving data using the serial bus interface (SBI) in synchronous serial communication mode.

Products

R32C/120 Group
R32C/121 Group
R32C/145 Group
R32C/151 Group
R32C/152 Group
R32C/153 Group
R32C/156 Group
R32C/157 Group
R32C/160 Group
R32C/161 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This document explains how to transmit and receive data using the SBI in synchronous serial communication mode with two R32C/121 Group MCUs.
Transmission from the master device starts when the master device receives an INT0 interrupt request. 8-bit (one frame) data is transmitted from the master device three times and is received by the slave device. Then one frame of data is transmitted from the slave device three times and is received by the master device.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows a Connection Example.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Serial bus interface (SBI0)	Transmit and receive data

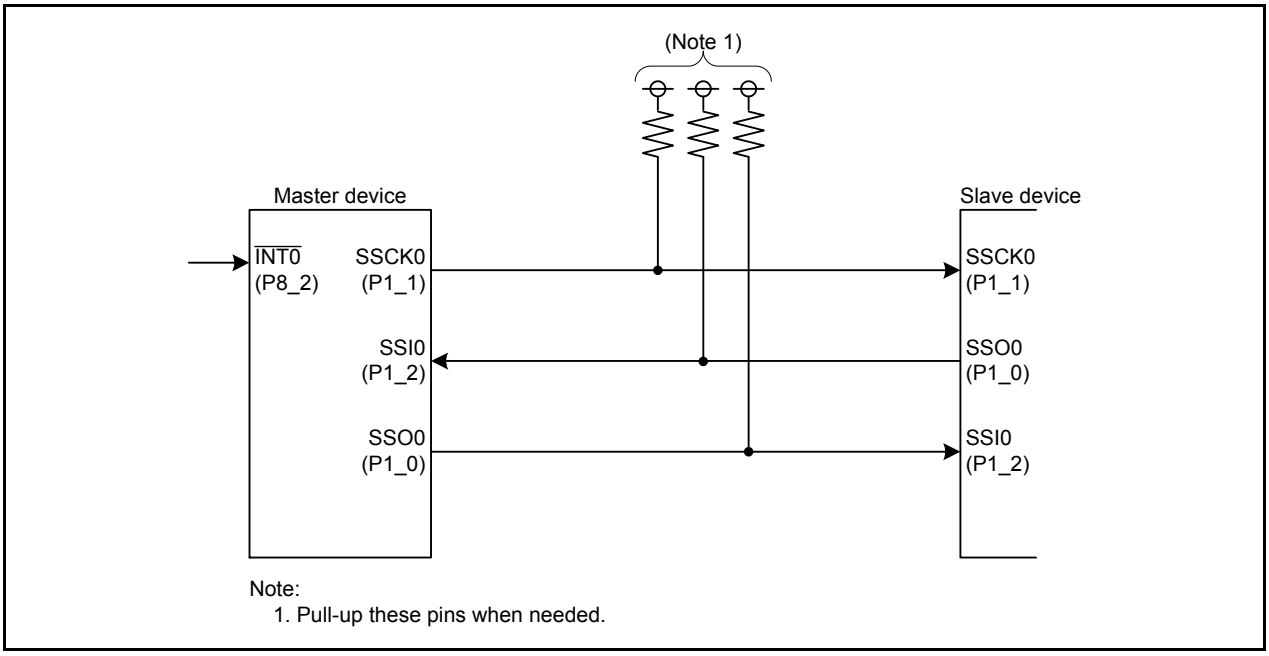


Figure 1.1 Connection Example

Figure 1.2 shows the Sample Code Outline.

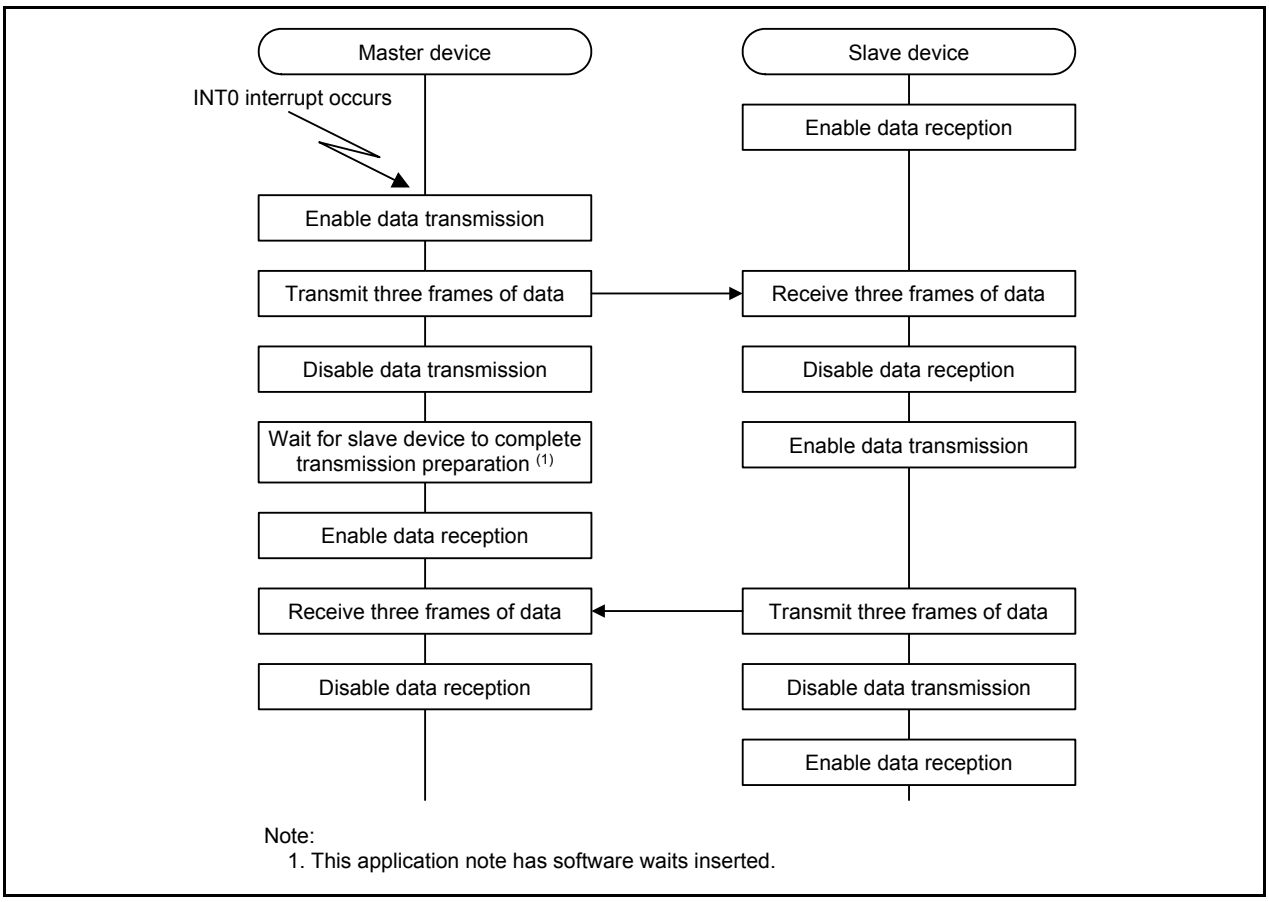


Figure 1.2 Sample Code Outline

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64219JFB (R32C/121 Group)
Operating frequencies	• Main clock: 8 MHz • PLL clock: 128 MHz • Base clock: 64 MHz • CPU clock: 64 MHz • Peripheral bus clock: 32 MHz • Peripheral function clock: 32 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.08
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)"
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Reference Application Note

The application note associated with this application note is listed below. Refer to this application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221)

4. Master Device Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P1_0/SSO0	Output	Output serial data
P1_1/SSCK0	Output	Output clock
P1_2/SSI0	Input	Input serial data
P8_2/$\overline{\text{INT0}}$	Input	Input INT0 interrupt

5. Master Device Software

Transmission from the master device starts when the master device receives an INT0 interrupt request. One frame of data is transmitted from the master device three times. Then one frame of data is transmitted from the slave device three times.
The master device settings are below.

Serial bus interface 0 settings
- Transmit/receive clock: 1 MHz (peripheral bus clock (fBCLK) divided by 32)
- Clock polarity: High when clock is stopped
- Data transfer direction: MSB first

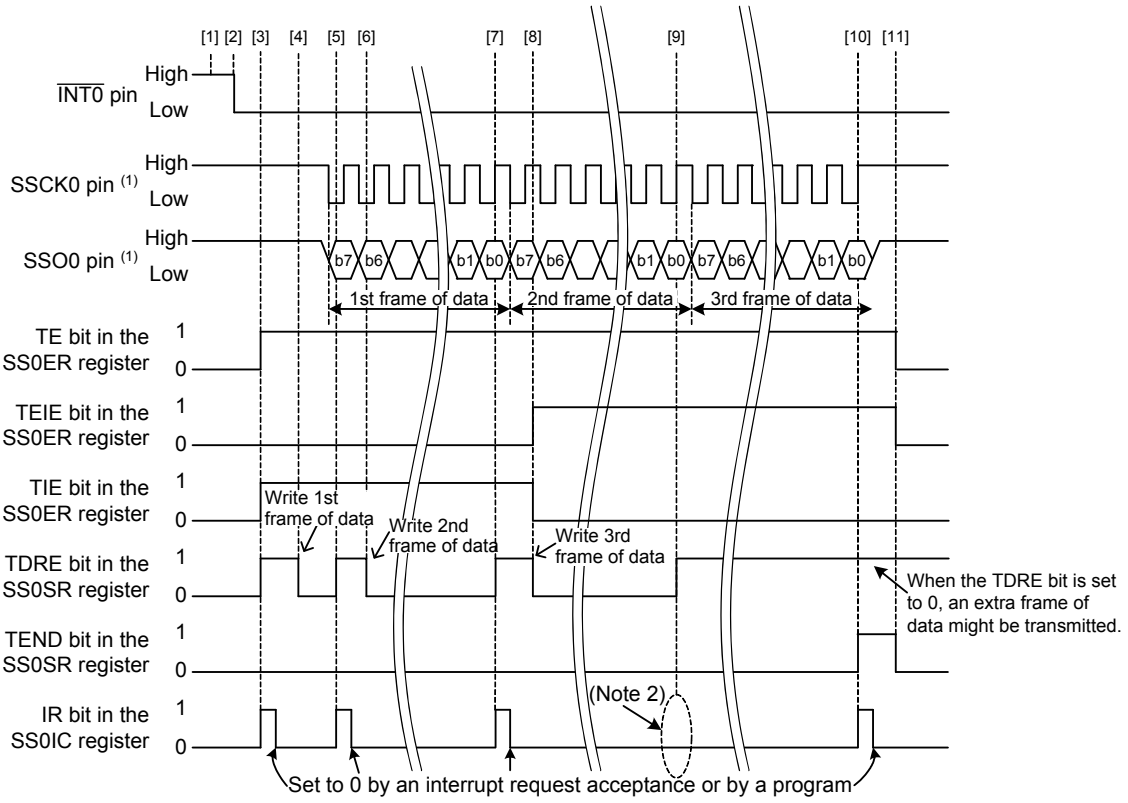
Interrupt settings
- Serial bus interface 0 interrupt
  Interrupt priority level: 2
  Interrupt request sources: Transmit data register empty, transmit end
- INT0 interrupt
  Interrupt priority level: 1
  Interrupt request source: Falling edge

5.1 Operation Overview

5.1.1 Master Transmission

(1) Perform the initial setting of the serial bus interface (SBI0).
(2) When a falling edge is input to the $\overline{\text{INT0}}$ pin, an INT0 interrupt occurs.
(3) In the INT0 interrupt handling, set the TE bit in the SS0ER register to 1 (enable data transmission) and set the TIE bit to 1 (enable transmit data register empty interrupt request). When setting these bits, the TDRE bit in the SS0SR register becomes 1 (no data left in the SS0TDR register) and a transmit data register empty interrupt occurs.
(4) In the transmit data register empty interrupt handling, write the first frame of data to the SS0TDR register. During the write operation, the TDRE bit becomes 0 (unsent data left in the SS0TDR register) and the transmit and receive clocks are output.
(5) When the first frame of data is transferred to the transmit/receive shift register, the TDRE bit becomes 1 and a transmit data register empty interrupt occurs.
(6) In the transmit data register empty interrupt handling, write the second frame of data to the SS0TDR register.
(7) When the second frame of data is transferred to the transmit/receive shift register, the TDRE bit becomes 1 and a transmit data register empty interrupt occurs.
(8) In the transmit data register empty interrupt handling, set the TIE bit in the SS0ER register to 0 (disable transmit data register empty interrupt request), set the TEIE bit to 1 (enable transmit end interrupt request), and write the last frame of data to the SS0TDR register.
(9) When the last frame of data is transferred to the transmit/receive shift register, the TDRE bit becomes 1, but the IR bit in the SS0IC register does not become 1.
(10) When the last bit is transmitted, if the TDRE bit is 1, the TEND bit in the SS0SR register becomes 1 (transmission is completed), and a transmit end interrupt occurs.
(11) In the transmit end interrupt handling, set the TEND bit to 0 (transmission continues), set the TE bit to 0 (disable data transmission), and set the TEIE bit to 0 (disable transmit end interrupt request). Then prepare for the next reception.

Figure 5.1 shows the Master Transmission Timing Diagram.



The above diagram assumes the following:

- The SSUMS bit in the SS0MR2 register is 0 (synchronous serial communication mode).
- The BIDE bit in the SS0MR2 register is 0 (standard mode).
- The MSS bit in the SS0CRH register is 1 (master mode).
- The CPHS bit in the SS0MR register is 0 (change data at odd edges (load data at even edges)).
- The CPOS bit in the SS0MR register is 0 (high when clock is stopped).
- The MLS bit in the SS0MR register is 0 (MSB first).
- Bits CSS1 and CSS0 in the SS0MR2 register are 00b (no function as chip select).

Notes:

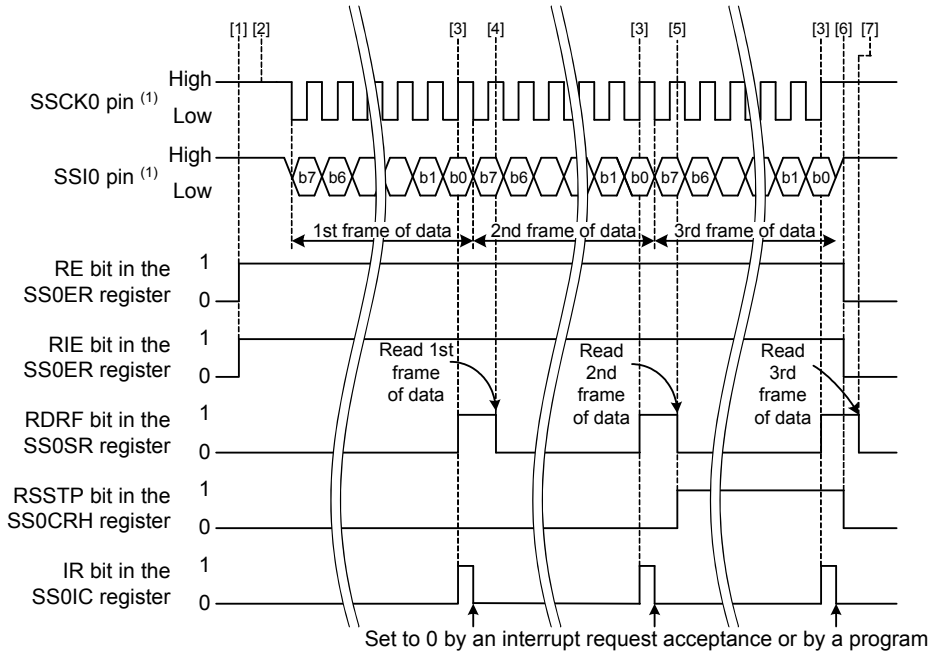
1. Example of output when pins are pulled-up.
2. The TIE bit is set to 0 (disable transmit data register empty interrupt request) in [8], so no interrupt occurs.

Figure 5.1 Master Transmission Timing Diagram

5.1.2 Master Reception

(1) At the same timing as (11) in Master Transmission, set the RE bit in the SS0ER register to 1 (enable data reception) and set the RIE bit to 1 (enable receive data register full or overrun error interrupt request).
(2) The transmit/receive clock is output by dummy reading the SS0RDR register.
(3) After receiving one frame of data, the RDRF bit in the SS0SR register becomes 1 (received data left in SS0RDR register), and the received data is stored in the SS0RDR register. When the RDRF bit becomes 1, a receive data register full interrupt occurs.
(4) In the receive data register full interrupt handling, read the received data from the SS0RDR register. When reading the received data, the RDRF bit becomes 0 (no data left in the SS0RDR register).
(5) In the receive data register full interrupt, set the RSSTP bit in the SS0CRH register to 1 (after receiving the current frame, end receive operation (stop the receive clock)) to receive the last frame of data. Read the received data from the SS0RDR register.
(6) In the receive data register full interrupt handling, before reading the last frame of data, set the RSSTP bit to 0 (after receiving the current frame, continue receive operation (output the receive clock)), the RE bit to 0 (disable data reception), and the RIE bit to 0 (disable receive data register full or overrun error interrupt request).
(7) Read the received data from the SS0RDR register.

Figure 5.2 shows the Master Reception Timing Diagram.



The above diagram assumes the following:
- The SSUMS bit in the SS0MR2 register is 0 (synchronous serial communication mode).
- The BIDE bit in the SS0MR2 register is 0 (standard mode).
- The MSS bit in the SS0CRH register is 1 (master mode).
- The CPHS bit in the SS0MR register is 0 (change data at odd edges (load data at even edges)).
- The CPOS bit in the SS0MR register is 0 (high when clock is stopped).
- The MLS bit in the SS0MR register is 0 (MSB first).
- Bits CSS1 and CSS0 in the SS0MR2 register are 00b (no function as chip select).

Note:
1. Example of output when pins are pulled-up.

Figure 5.2 Master Reception Timing Diagram

5.2 Constants

Table 5.1 lists the Constants Used in the Sample Code.

Table 5.1 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
SND	00h	Transmission
RCV	01h	Reception
D_SBI_DATA_MAX	3	Transmit data size
D_SBI_DATA_LAST_F	D_SBI_DATA_MAX-1	Constant for determining the last frame of data
D_SBI_DATA_SECOND_LAST_F	D_SBI_DATA_MAX-2	Constant for determining the second to last frame of data
ORER	0000 0100b	Mask value for the overrun error flag

5.3 Variables

Table 5.2 lists the Global Variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	snd_cnt	Transmit counter	_int0, _serial_bus_0
unsigned char	f_snd_rcv	Transmit/receive flag	_int0, _serial_bus_0
unsigned char	snd_data[]	Buffer for storing transmit data	_serial_bus_0
unsigned char	rcv_data[]	Buffer for storing receive data	_serial_bus_0
unsigned char	rcv_cnt	Receive counter	_serial_bus_0

5.4 Functions

Table 5.3 lists the Functions.

Table 5.3 Functions

Function Name	Outline
peripheral_init	Initial setting for the peripheral functions
_serial_bus_0	Serial bus interface 0 interrupt handling
_int0	INT0 interrupt handling

5.5 Function Specifications

The following tables list the sample code function specifications.

peripheral_init	
Outline	Initial setting for the peripheral functions
Header	None
Declaration	void peripheral_init(void)
Description	Setting to use the serial bus interface as the master device.
Argument	None
Returned value	None
Remark	

_serial_bus_0	
Outline	Serial bus interface 0 interrupt handling
Header	None
Declaration	void _serial_bus_0(void)
Description	Read the transmit/receive flag to determine the source of the interrupt. Perform the handling below based on the determined source of the interrupt. *When transmitting • Transmit data register empty interrupt Write data to be transmitted to the SS0TDR register. When setting the last data, disable the transmit data register empty interrupt and enable the transmit end interrupt. • Transmit end interrupt Disable the transmit end interrupt, disable transmission, and prepare for reception. *When receiving • Overrun error interrupt Disable data reception. • Receive data register full interrupt Read the receive data stored in the SS0RDR register. When receiving the second to last frame of data, set the RSSTP bit in the SS0CRH register to 1 (after receiving the current frame, end receive operation (stop the receive clock)) before reading the receive data. When receiving the last frame of data, set the RE bit in the SS0ER register to 0 (disable data reception) and set the RSSTP bit to 0 (after receiving the current frame, continue receive operation (output the receive clock)) before reading the receive data.
Argument	None
Returned value	None
Remark	

_int0	
Outline	INT0 interrupt handling
Header	None
Declaration	void _int0(void)
Description	Enable data transmission.
Argument	None
Returned value	None
Remark	

5.6 Flowcharts

5.6.1 Main Processing

Figure 5.3 shows the Main Processing.

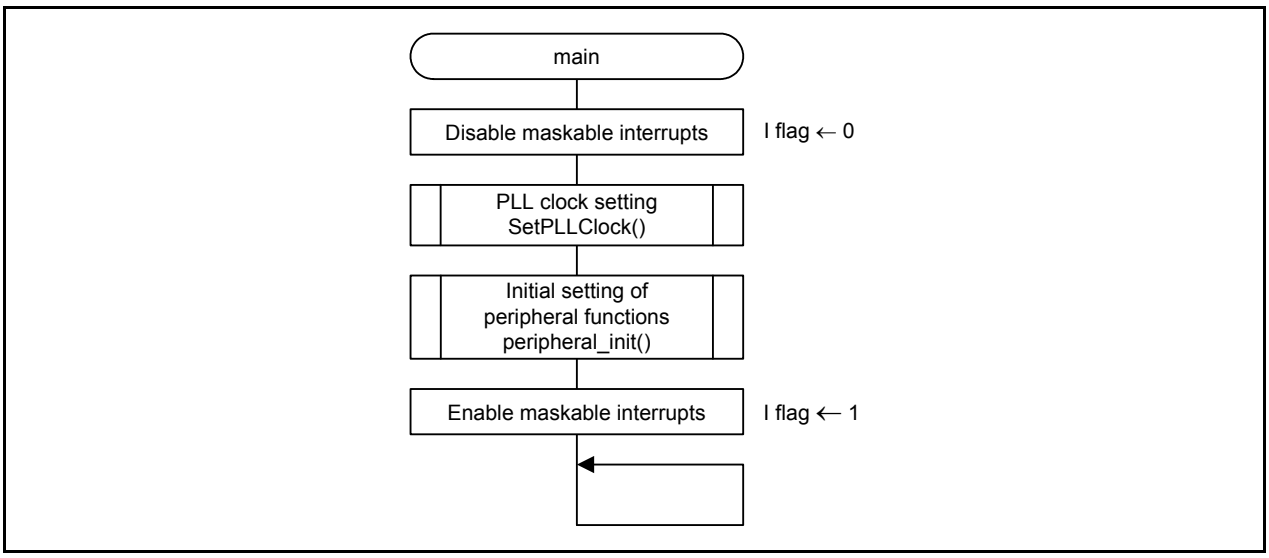


Figure 5.3 Main Processing

5.6.2 Initial Setting of the Peripheral Functions

Figure 5.4 shows the Initial Setting of the Peripheral Functions.

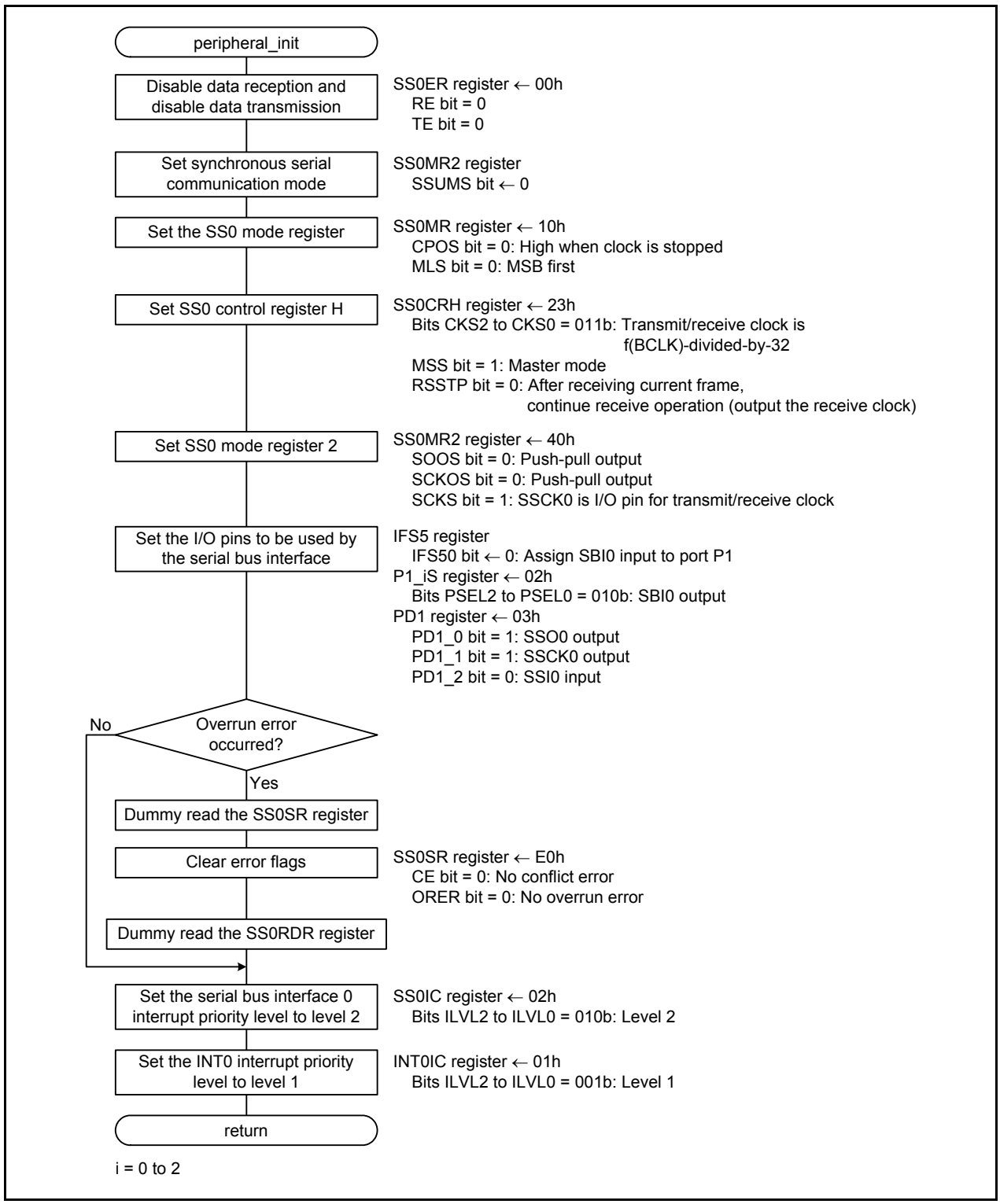


Figure 5.4 Initial Setting of the Peripheral Functions

5.6.3 Serial Bus Interface 0 Interrupt Handling

Figure 5.5 and Figure 5.6 show the Serial Bus Interface 0 Interrupt Handling.

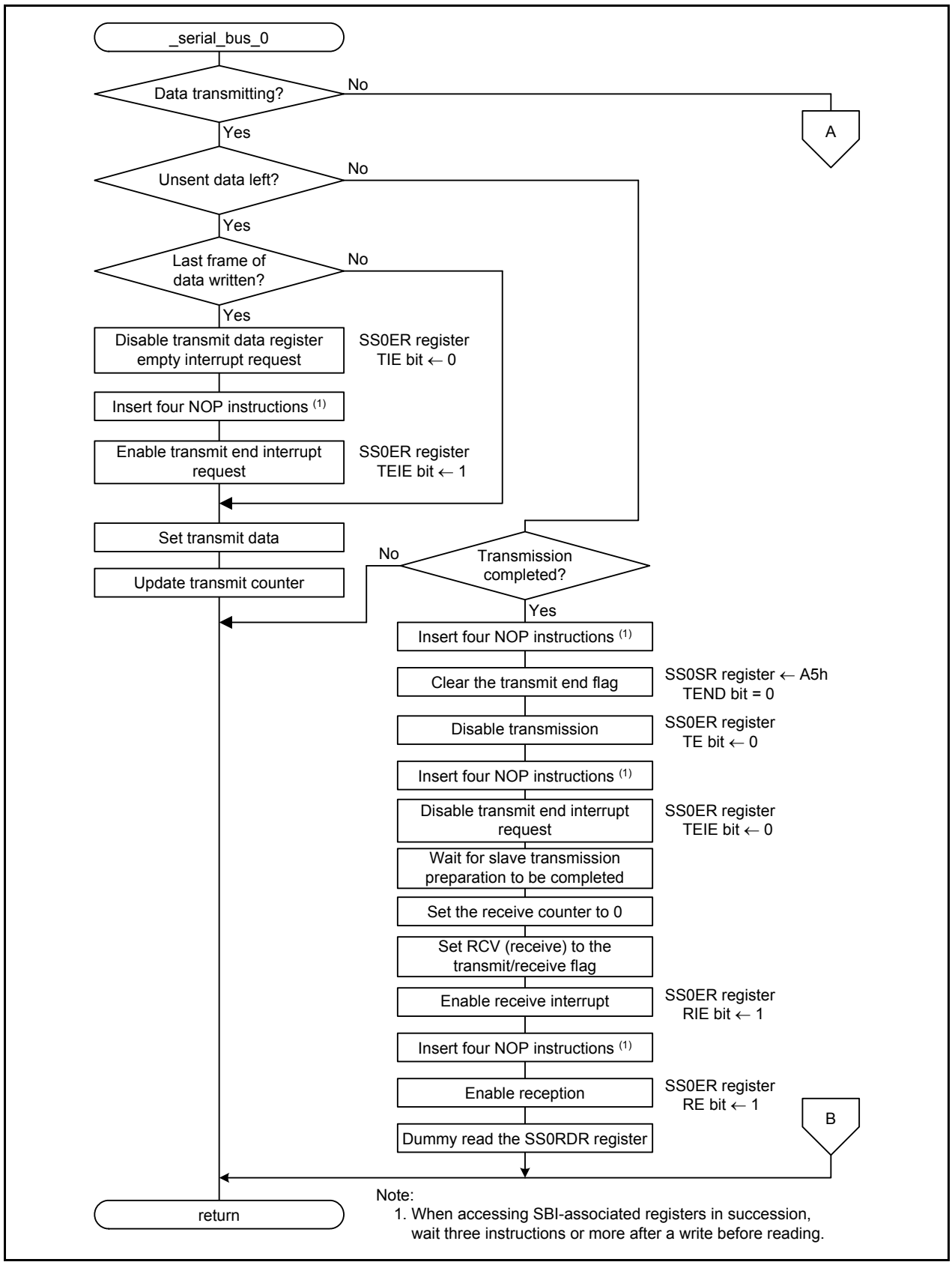


Figure 5.5 Serial Bus Interface 0 Interrupt Handling (1/2)

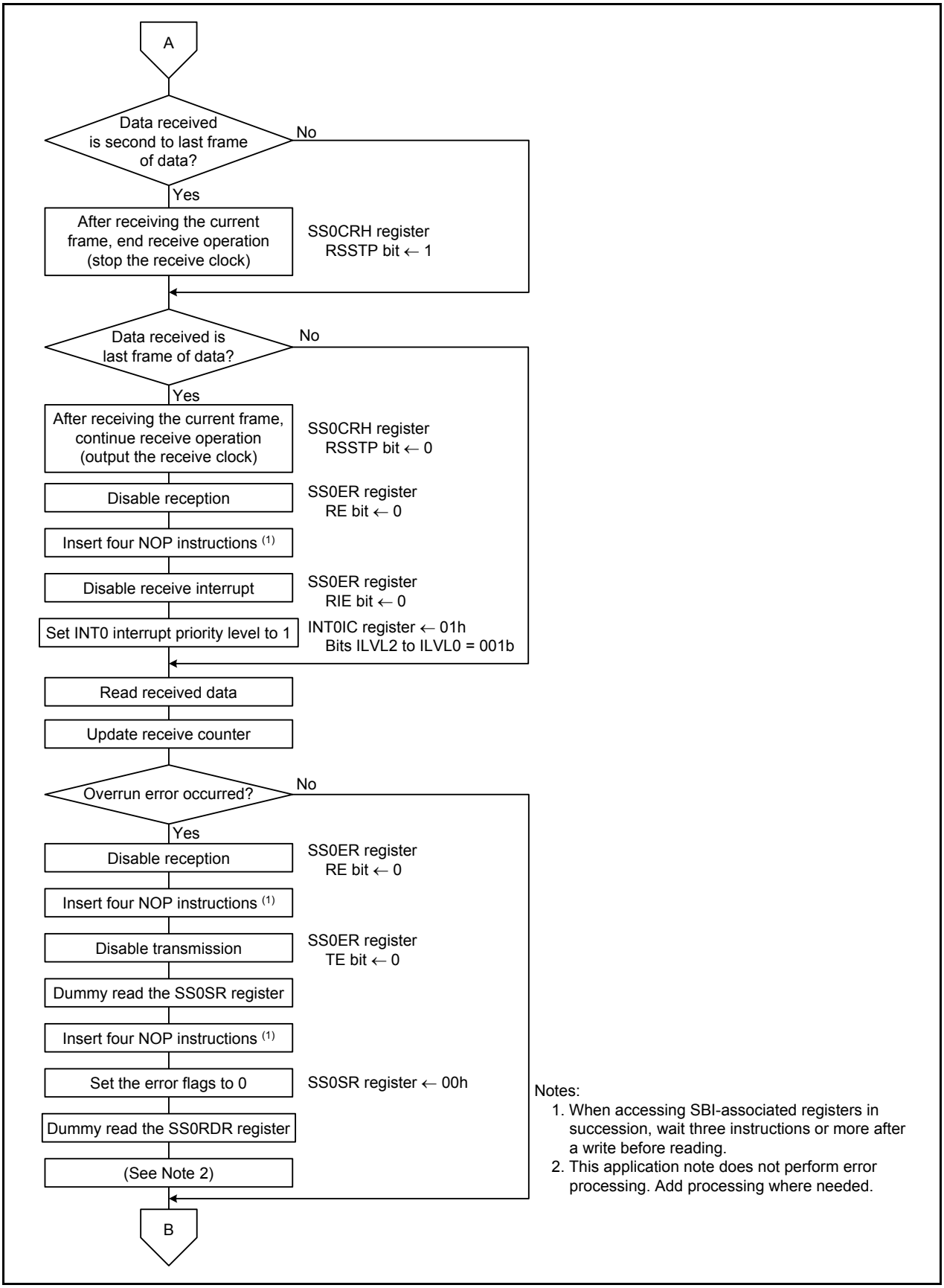


Figure 5.6 Serial Bus Interface 0 Interrupt Handling (2/2)

5.6.4 INT0 Interrupt Handling

Figure 5.7 shows the INT0 Interrupt Handling.

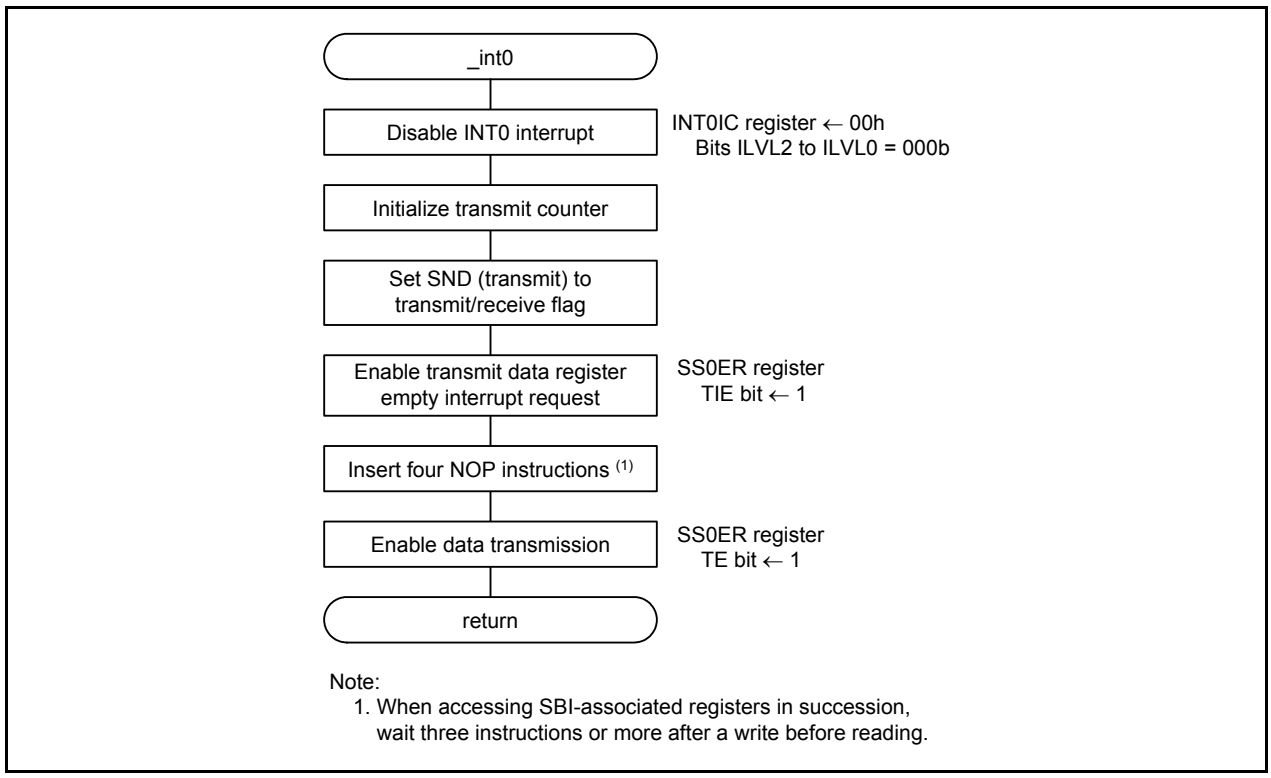


Figure 5.7 INT0 Interrupt Handling

6. Slave Device Hardware

6.1 Pins Used

Table 6.1 lists the Pins Used and Their Functions.

Table 6.1 Pins Used and Their Functions

Pin Name	I/O	Function
P1_0/SSO0	Output	Output serial data
P1_1/SSCK0	Input	Input clock
P1_2/SSI0	Input	Input serial data

7. Slave Device Software

The slave device receives one frame of data from the master device three times. Then the slave device transmits one frame of data three times. The slave device settings are below.

Settings

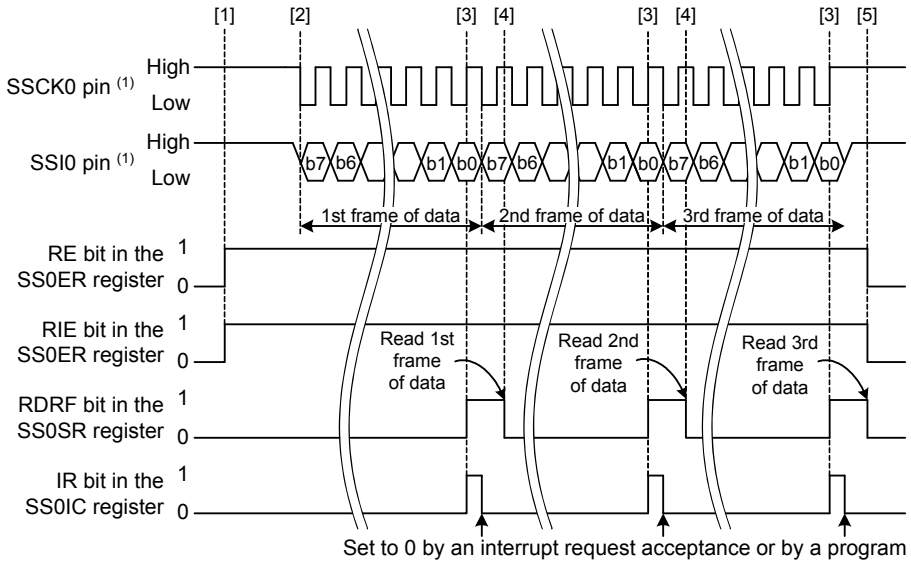
- Channel used: Channel 0
- Clock polarity: High when clock is stopped
- Data transfer direction: MSB first
- Interrupt: Serial bus interface 0 interrupt (interrupt priority level: 2)

7.1 Operation Overview

7.1.1 Slave Reception

(1) To initialize the serial bus interface, set the RE bit in the SS0ER register to 1 (enable data reception), the RIE bit to 1 (enable receive data register full or overrun error interrupt request), then dummy read the SS0RDR register.
(2) Data is received by inputting a clock to the SSCK0 pin.
(3) After receiving one frame of data, the RDRF bit in the SS0SR register becomes 1 (received data left in the SS0RDR register), and the data received is stored in the SS0RDR register. When storing the received data, a receive data register full interrupt occurs.
(4) In the receive data register full interrupt handling, read the received data from the SS0RDR register. When reading, the RDRF bit becomes 0 (no data left in the SS0RDR register).
(5) When the last frame of data is received, set the RIE bit to 0 (disable receive data register full or overrun error interrupt request), the RE bit to 0 (disable data reception), and prepare for transmission.

Figure 7.1 shows the Slave Reception Timing Diagram.



The above diagram assumes the following:
- The SSUMS bit in the SS0MR2 register is 0 (synchronous serial communication mode).
- The BIDE bit in the SS0MR2 register is 0 (standard mode).
- The MSS bit in the SS0CRH register is 0 (slave mode).
- The CPHS bit in the SS0MR register is 0 (change data at odd edges (load data at even edges)).
- The CPOS bit in the SS0MR register is 0 (high when clock is stopped).
- The MLS bit in the SS0MR register is 0 (MSB first).
- Bits CSS1 and CSS0 in the SS0MR2 register are 00b (no function as chip select).

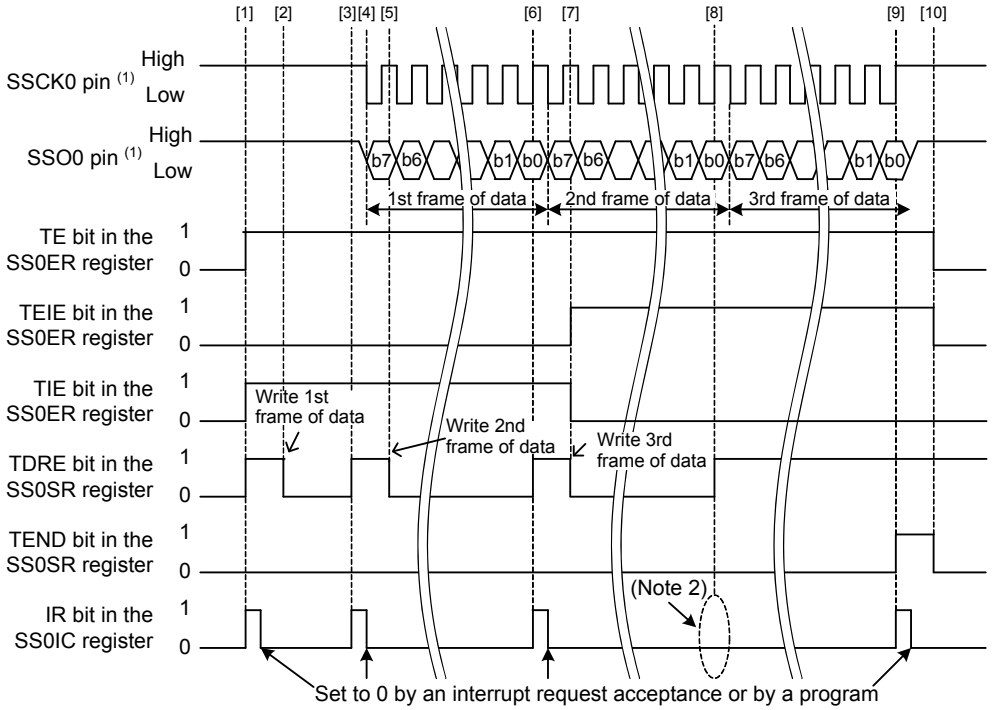
Note:
1. Example of output when pins are pulled-up.

Figure 7.1 Slave Reception Timing Diagram

7.1.2 Slave Transmission

(1) Set the TIE bit in the SS0ER register to 1 (enable transmit data register empty interrupt request) and the TE bit to 1 (enable data transmission). When setting these bits, the TDRE bit in the SS0SR register becomes 1 (no data left in the SS0TDR register), and at the same timing as (5) in Slave Reception, a transmit data register empty interrupt occurs.
(2) In the transmit data register empty interrupt handling, write the first frame of data to the SS0TDR register. When writing, the TDRE bit becomes 0 (unsent data left in the SS0TDR register).
(3) After transferring the first frame of data to the transmit/receive shift register, the TDRE bit becomes 1, and a transmit data register empty interrupt occurs.
(4) The data is transmitted when a clock is input to the SSCK0 pin.
(5) In the transmit data register empty interrupt handling, write the second frame of data to the SS0TDR register.
(6) After transferring the second frame of data to the transmit/receive shift register, the TDRE bit becomes 1, and a transmit data register empty interrupt occurs.
(7) In the transmit data register empty interrupt handling, set the TIE bit to 0 (disable transmit data register empty interrupt request) and the TEIE bit in the SS0ER register to 1 (enable transmit end interrupt request). Write the last frame of data to the SS0TDR register.
(8) After transferring the last frame of data to the transmit/receive shift register, the TDRE bit becomes 1, but because the TIE bit is 0, a transmit data register empty interrupt does not occur.
(9) When the last bit is transmitted, if the TDRE bit is 1, the TEND bit in the SS0SR register becomes 1 (transmission is completed), and a transmit end interrupt occurs.
(10) In the transmit end interrupt handling, set the TEND bit to 0 (transmission continues), the TE bit to 0 (disable data transmission), and the TEIE bit to 0 (disable transmit end interrupt request).

Figure 7.2 shows the Slave Transmission Timing Diagram.



The above diagram assumes the following:
- The SSUMS bit in the SS0MR2 register is 0 (synchronous serial communication mode).
- The BIDE bit in the SS0MR2 register is 0 (standard mode).
- The MSS bit in the SS0CRH register is 0 (slave mode).
- The CPHS bit in the SS0MR register is 0 (change data at odd edges (load data at even edges)).
- The CPOS bit in the SS0MR register is 0 (high when clock is stopped).
- The MLS bit in the SS0MR register is 0 (MSB first).
- Bits CSS1 and CSS0 in the SS0MR2 register are 00b (no function as chip select).

Notes:
1. Example of output when pins are pulled-up.
2. The TIE bit is set to 0 (disable transmit data register empty interrupt request) in [7], so no interrupt occurs.

Figure 7.2 Slave Transmission Timing Diagram

7.2 Constants

Table 7.1 lists the Constants Used in the Sample Code.

Table 7.1 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
SND	00h	Transmission
RCV	01h	Reception
D_SBI_DATA_MAX	3	Transmit data size
D_SBI_DATA_LAST_F	D_SBI_DATA_MAX-1	Constant for determining the last frame of data
ORER	0000 0100b	Mask value for the overrun error flag

7.3 Variables

Table 7.2 lists the Global Variables.

Table 7.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	rcv_cnt	Receive counter	peripheral_init, _serial_bus_0
unsigned char	f_snd_rcv	Transmit/receive flag	peripheral_init, _serial_bus_0
unsigned char	snd_cnt	Transmit counter	_serial_bus_0
unsigned char	snd_data[]	Buffer for storing transmit data	_serial_bus_0
unsigned char	rcv_data[]	Buffer for storing receive data	_serial_bus_0

7.4 Functions

Table 7.3 lists the Functions.

Table 7.3 Functions

Function Name	Outline
peripheral_init	Initial setting of the peripheral functions
_serial_bus_0	Serial bus interface 0 interrupt handling

7.5 Function Specifications

The following tables list the sample code function specifications.

peripheral_init	
Outline	Initial setting for the peripheral interrupts
Header	None
Declaration	void peripheral_init(void)
Description	Setting to use the serial bus interface as the slave device.
Argument	None
Returned value	None
Remark	

_serial_bus_0	
Outline	Serial bus interface 0 interrupt handling
Header	None
Declaration	void _serial_bus_0(void)
Description	Read the transmit/receive flag to determine the source of the interrupt. Perform the handling below based on the determined source of the interrupt. *When transmitting • Transmit data register empty interrupt Write data to be transmitted to the SS0TDR register. When setting the last frame of data, disable the transmit data register empty interrupt and enable the transmit end interrupt. • Transmit end interrupt Disable the transmit end interrupt, disable transmission, and prepare for reception. *When receiving • Overrun error interrupt Disable data reception. • Receive data register full interrupt Read the receive data stored in the SS0RDR register. When receiving the last frame of data, disable reception, disable the receive interrupts, and prepare for transmission.
Argument	None
Returned value	None
Remark	

7.6 Flowcharts

7.6.1 Main Processing

Figure 7.3 shows the Main Processing.

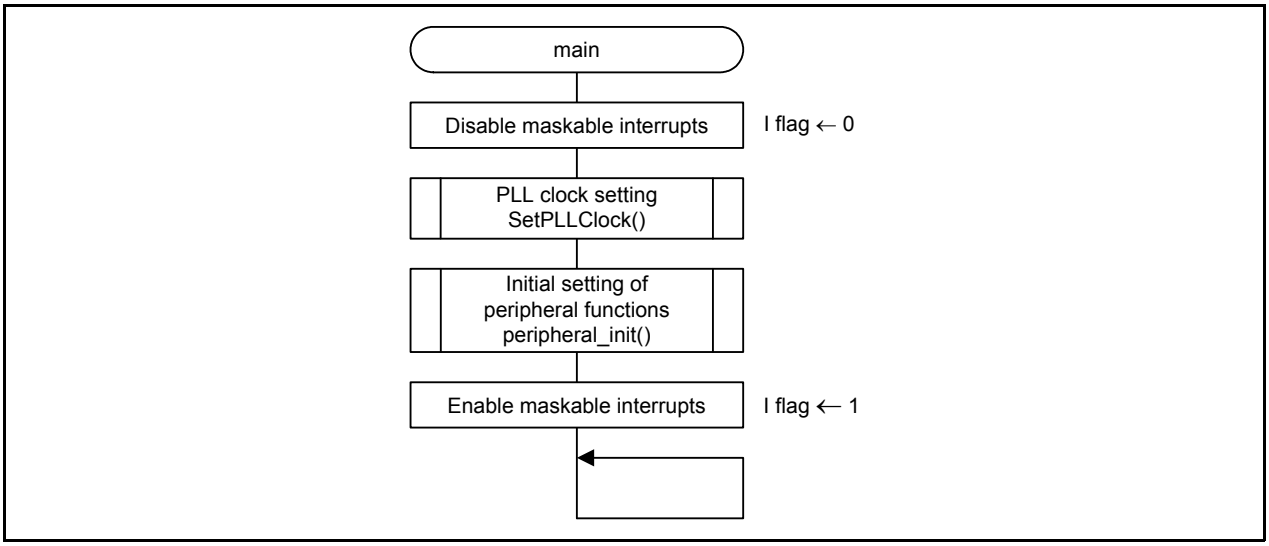


Figure 7.3 Main Processing

7.6.2 Initial Setting of the Peripheral Functions

Figure 7.4 shows the Initial Setting of the Peripheral Functions.

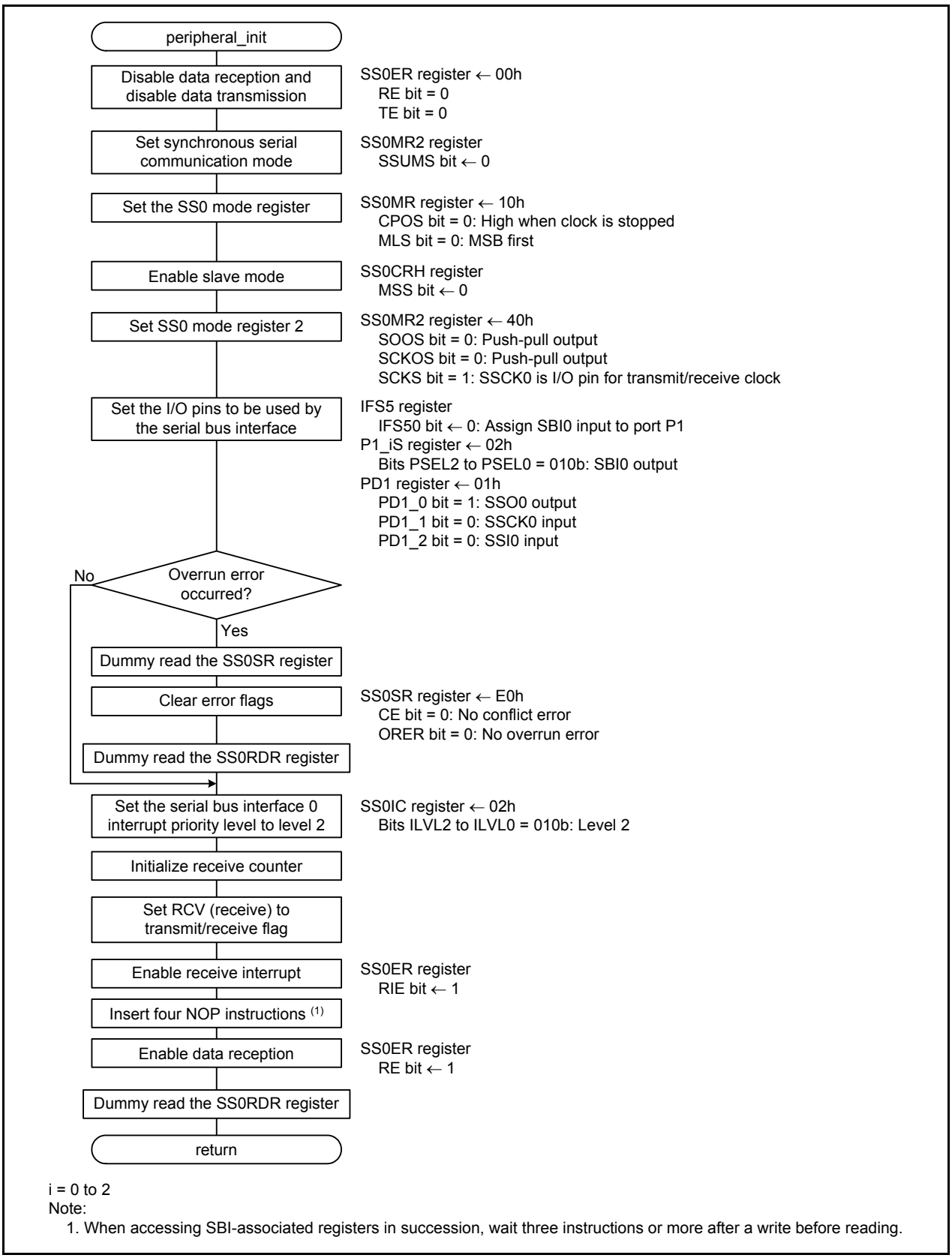


Figure 7.4 Initial Setting of the Peripheral Functions

7.6.3 Serial Bus Interface 0 Interrupt Handling

Figure 7.5 and Figure 7.6 show the Serial Bus Interface 0 Interrupt Handling.

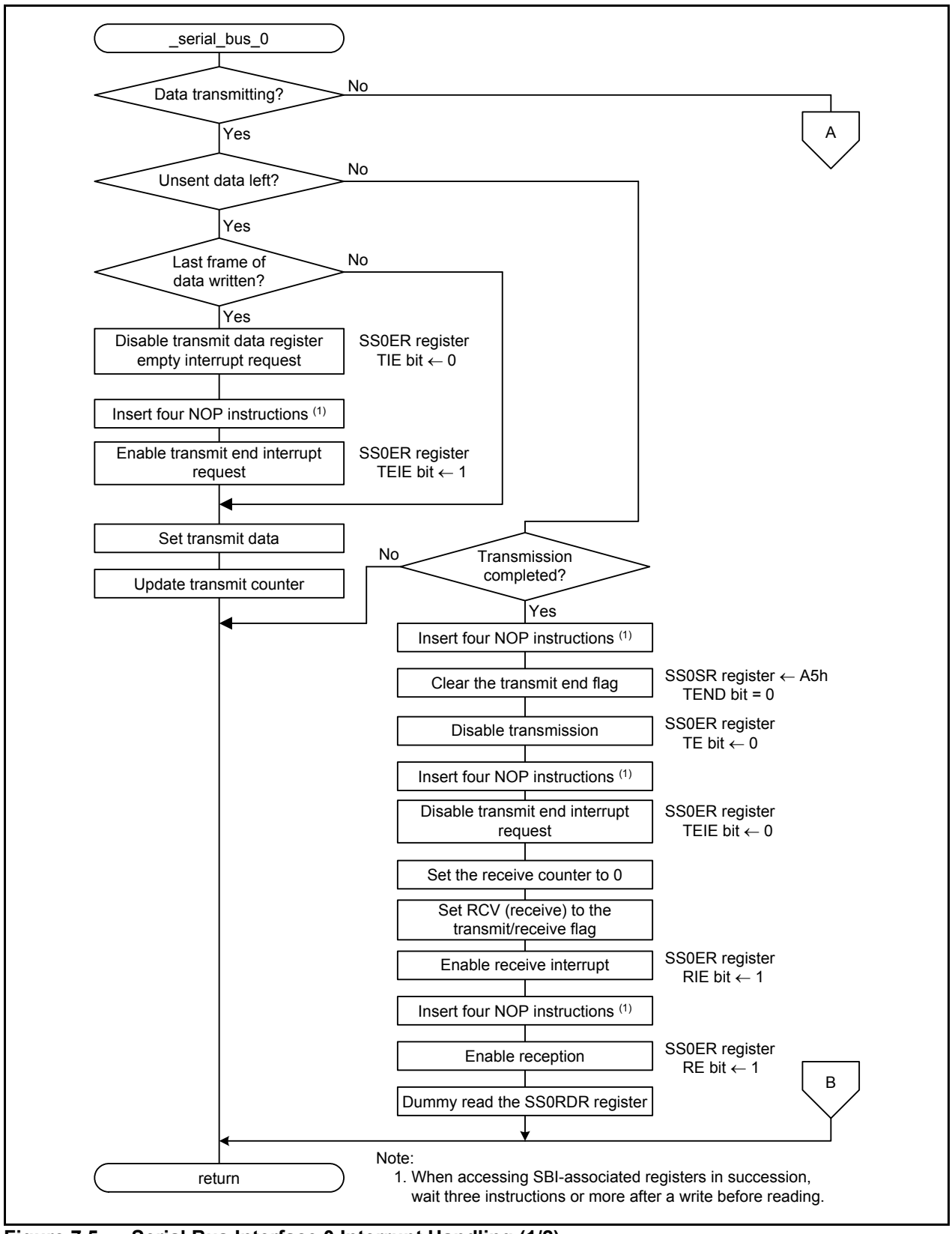


Figure 7.5 Serial Bus Interface 0 Interrupt Handling (1/2)

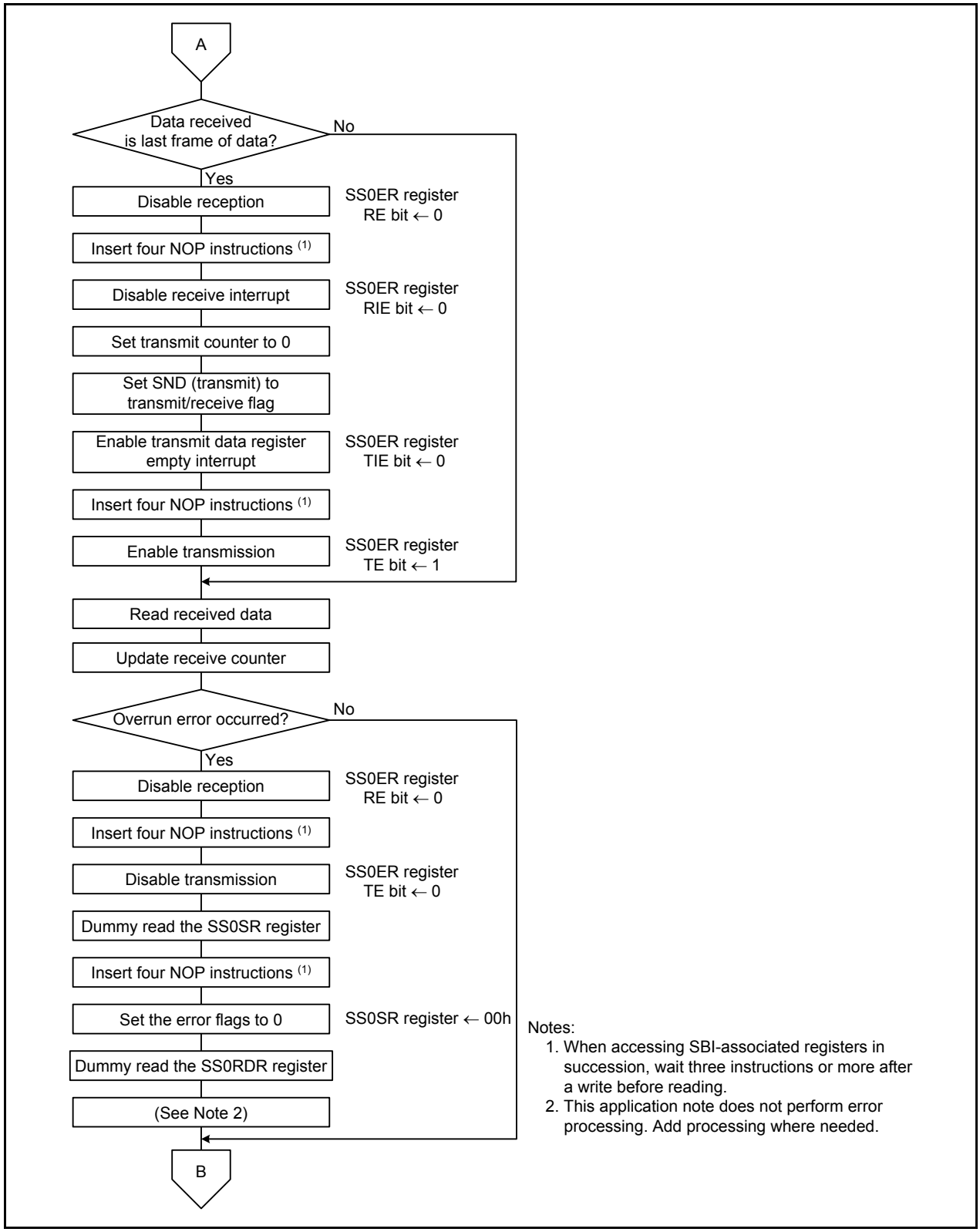


Figure 7.6 Serial Bus Interface 0 Interrupt Handling (2/2)

8. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

9. Reference Documents

R32C/120 Group User's Manual: Hardware Rev.1.20
R32C/121 Group User's Manual: Hardware Rev.1.20
R32C/151 Group User's Manual: Hardware Rev.1.10
R32C/152 Group User's Manual: Hardware Rev.1.10
R32C/153 Group User's Manual: Hardware Rev.1.10
R32C/156 Group User's Manual: Hardware Rev.1.10
R32C/157 Group User's Manual: Hardware Rev.1.10
R32C/160 Group User's Manual: Hardware Rev.1.02
R32C/161 Group User's Manual: Hardware Rev.1.02
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History	R32C/100 Series Transmitting/Receiving Data Using the Serial Bus Interface in Synchronous Serial Communication Mode

Rev.	Date	Description	
		Page	Summary
1.00	June 29, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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