R32C/100 Series

Serial Interface Operation in Special Mode 2
Using Master Transmission/Reception

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Abstract

This document describes a method of transmitting/receiving data from one master to multiple slaves using serial interface special mode 2 in the R32C/100 Series.

Products

MCUs: R32C/116 Group
R32C/117 Group
R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Transmit/receive data from one master to multiple slaves using serial interface special mode 2.
Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows Communication Control in Serial Interface Special Mode 2.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Serial interface (UART0)	Master transmission/reception using special mode 2

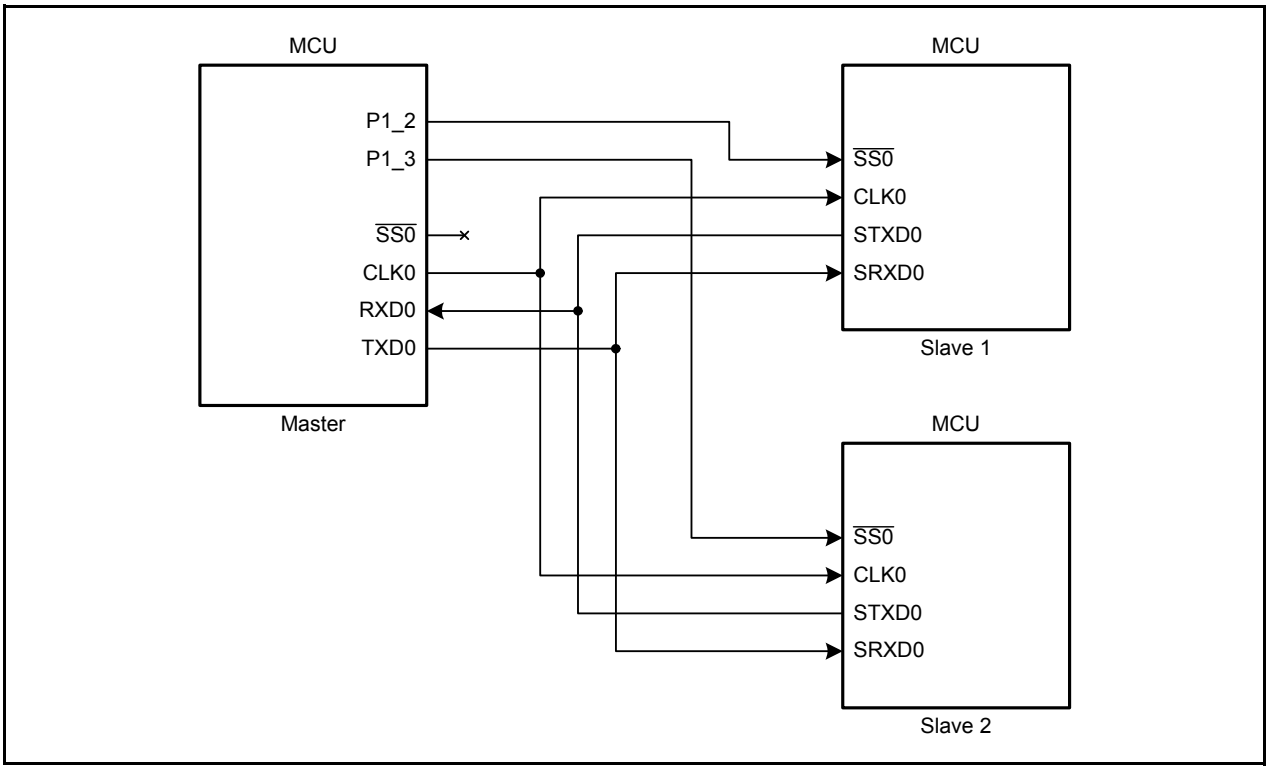


Figure 1.1 Communication Control in Serial Interface Special Mode 2

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64189DFD (R32C/118 Group)
Operating frequencies	• Main clock: 16 MHz • PLL clock: 100 MHz • Base clock: 50 MHz • CPU clock: 50 MHz • Peripheral bus clock: 25 MHz • Peripheral function clock source: 25 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for R32C/118 (product name: R0K564189S000BE)

3. Reference Application Note

The application note associated with this application note is listed below. Refer to this application note for additional information.

- R32C/100 Series
  Configuring PLL Mode (REJ05B1221-0100)

4. Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P0_0 to P0_7	Output	These pins output data received from a slave.
P1_2	Output	The SS function is used for slave 1.
P1_3	Output	The SS function is used for slave 2.
P6_0/$\overline{SS0}$	Input	This pin functions as the $\overline{SS0}$ pin.
P6_1/CLK0	Output	This pin functions as the transmit/receive clock.
P6_2/RXD0	Input	This pin receives data.
P6_3/TXD0	Output	This pin transmits data.

5. Software

The sample program uses UART0 and ports P1_2 and P1_3 to alternately transmit/receive data to/from slave 1 and slave 2. The settings are listed below.

Settings

- Use UART0 in special mode 2.
- Use an internal clock for the transfer clock.
- Use f1 for the U0BRG count source.
- For the CLK polarity, select output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge.
- Use LSB first as the transfer format.
- Select no clock delay for the clock phase setting.
- Enable the SS function.
- Do not use the UART0 transmit interrupt.
- Use the UART0 receive interrupt.
- Set the transfer rate to approximately 1 Mbps.

5.1 Operation Overview

Operation of the sample program is as follows:

(1) Initial setting
Initialize UART0 and the ports.

(2) Enable transmission/reception
Set the RE bit in the U0C1 register to 1 (reception enabled) and set the TE bit to 1 (transmission enabled).

(3) Select slave 1
Set port P1_2 to 0 and select slave 1.

(4) Start transmitting to slave 1
Write transmit data to the U0TB register.

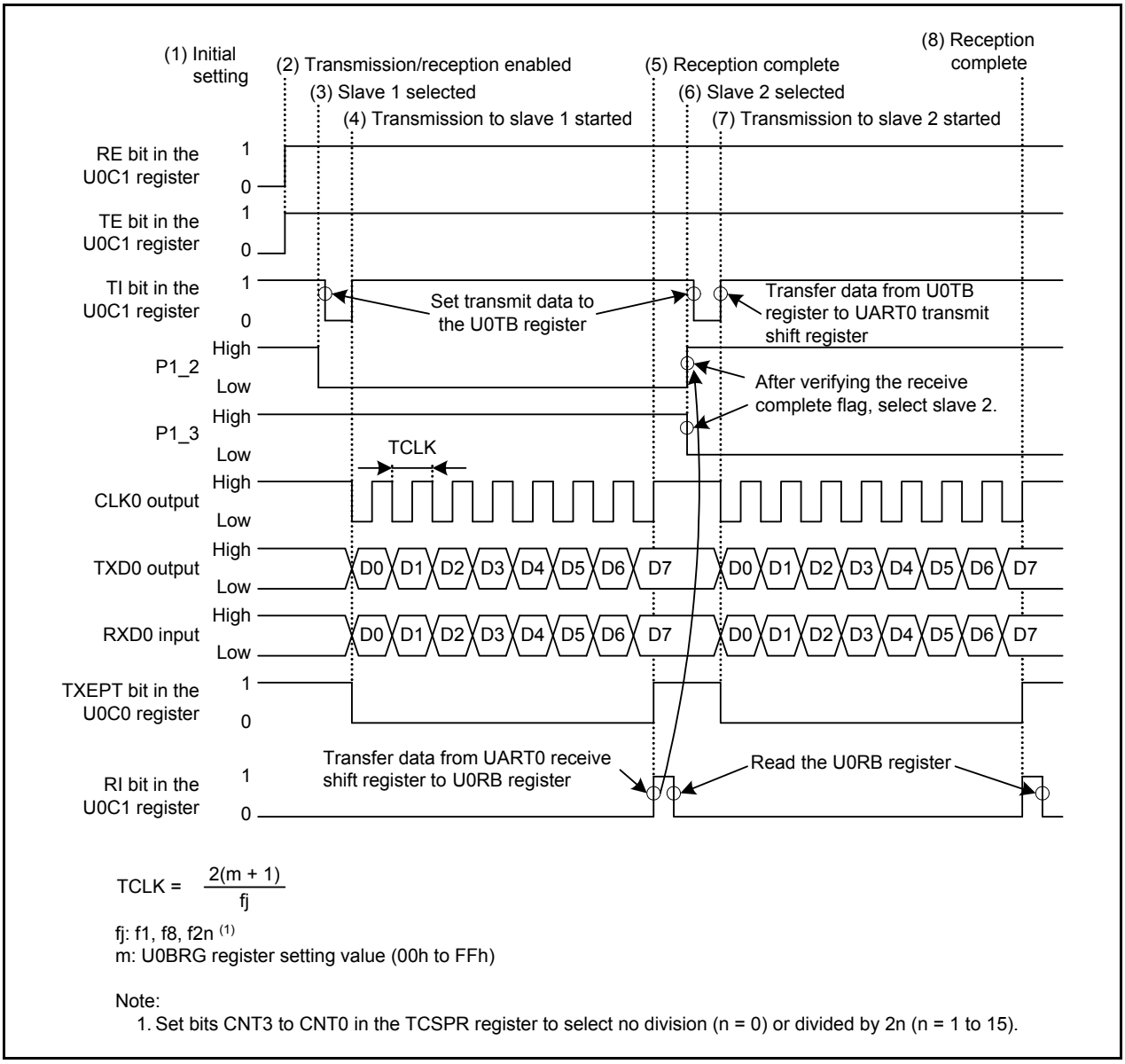
(5) Reception completed
A UART0 receive interrupt is generated when reception is completed. Read the U0RB register value in the UART0 receive interrupt handling.

(6) Select slave 2
Set port P1_3 to 0 and select slave 2.

(7) Start transmitting to slave 2
Write transmit data to the U0TB register.

(8) Reception completed
A UART0 receive interrupt is generated when reception is completed. Read the U0RB register value in the UART0 receive interrupt handling.

Figure 5.1 shows the Timing Diagram.



$$TCLK = \frac{2(m + 1)}{fj}$$

fj: f1, f8, f2n (1)
m: U0BRG register setting value (00h to FFh)

Note:
1. Set bits CNT3 to CNT0 in the TCSPR register to select no division (n = 0) or divided by 2n (n = 1 to 15).

Figure 5.1 Timing Diagram

5.2 Constants

Table 5.1 lists the Constants Used in the Sample Code.

Table 5.1 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
OVR_ERROR_MASK	1000h	Mask value of the overrun error
OVR_ERROR	1000h	Comparative value of the overrun error
TRANS_DATA1	55h	Slave 1 transmit data
TRANS_DATA2	AAh	Slave 2 transmit data
STATUS_TRANS	00h	Transmit wait status
STATUS_RECEIVE	01h	Receive wait status
STATUS_FINISH	02h	Transmit/receive complete status
STATUS_OVERRUN	03h	Overrun error status
SLV1_SELECT	00h	Use slave 1
SLV2_SELECT	01h	Use slave 2

5.3 Variable

Table 5.2 lists the Global Variable.

Table 5.2 Global Variable

Type	Variable Name	Contents	Function Used
unsigned char	status	Status	main(), _uart0_receive()

5.4 Functions

Table 5.3 lists the Functions.

Table 5.3 Functions

Function Name	Outline
uart0_init	UART0 initial setting
_uart0_receive	UART0 receive interrupt handling

5.5 Function Specifications

The following tables list the sample code function specifications.

uart0_init	
Outline	UART0 initial setting
Header	None
Declaration	void uart0_init(void)
Explanation	Perform initial setting on UART0.
Argument	None
Returned value	None
Remark	None

_uart0_receive	
Outline	UART0 receive interrupt handling
Header	None
Declaration	void _uart0_receive(void)
Explanation	When there is an overrun error, change the status to overrun. In all other cases, display the receive data to port P0, and set the status to transmit/receive complete.
Argument	None
Returned value	None
Remark	None

5.6 Flowcharts

5.6.1 Main Processing

Figures 5.2 and 5.3 show the main processing.

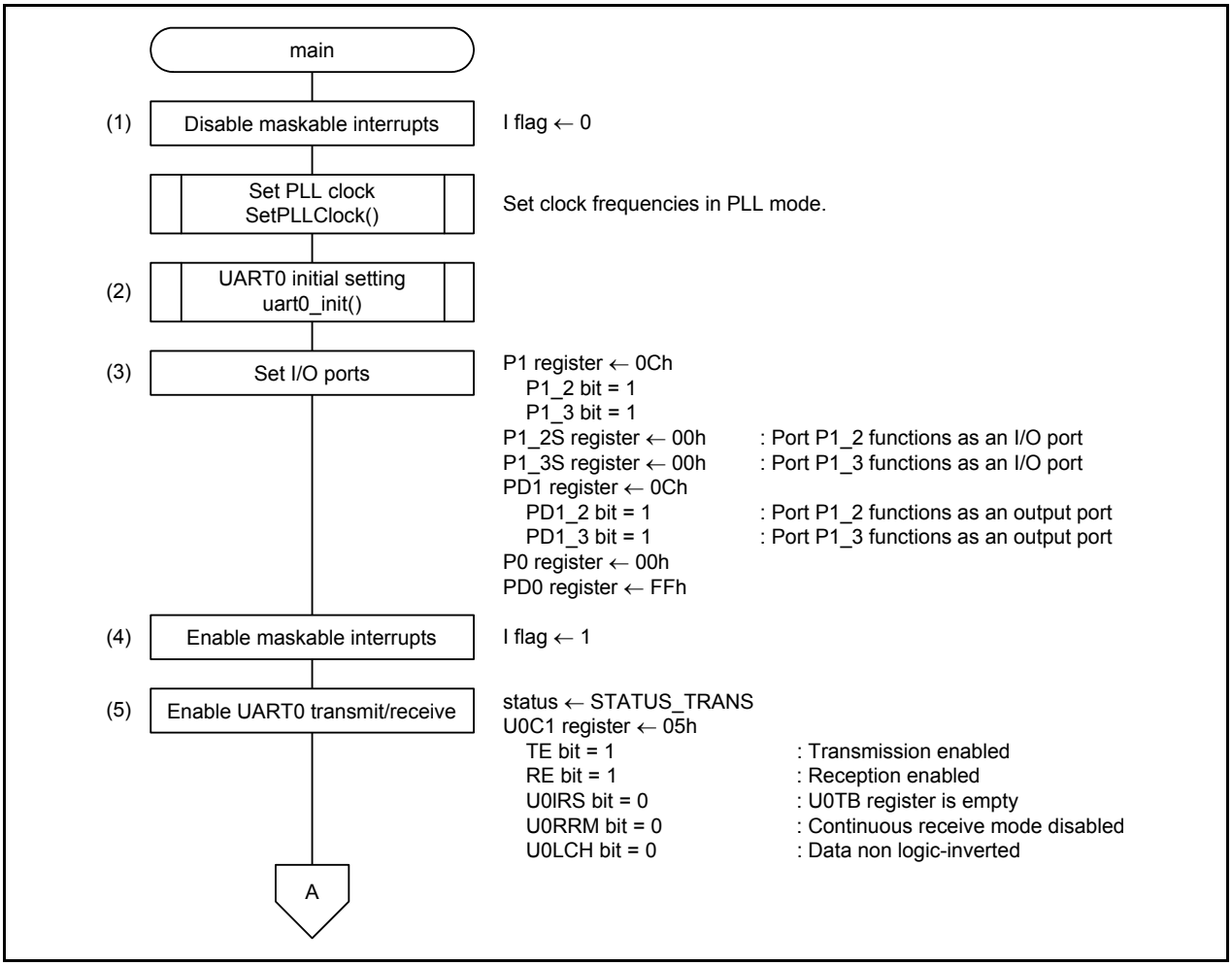


Figure 5.2 Main Processing (1/2)

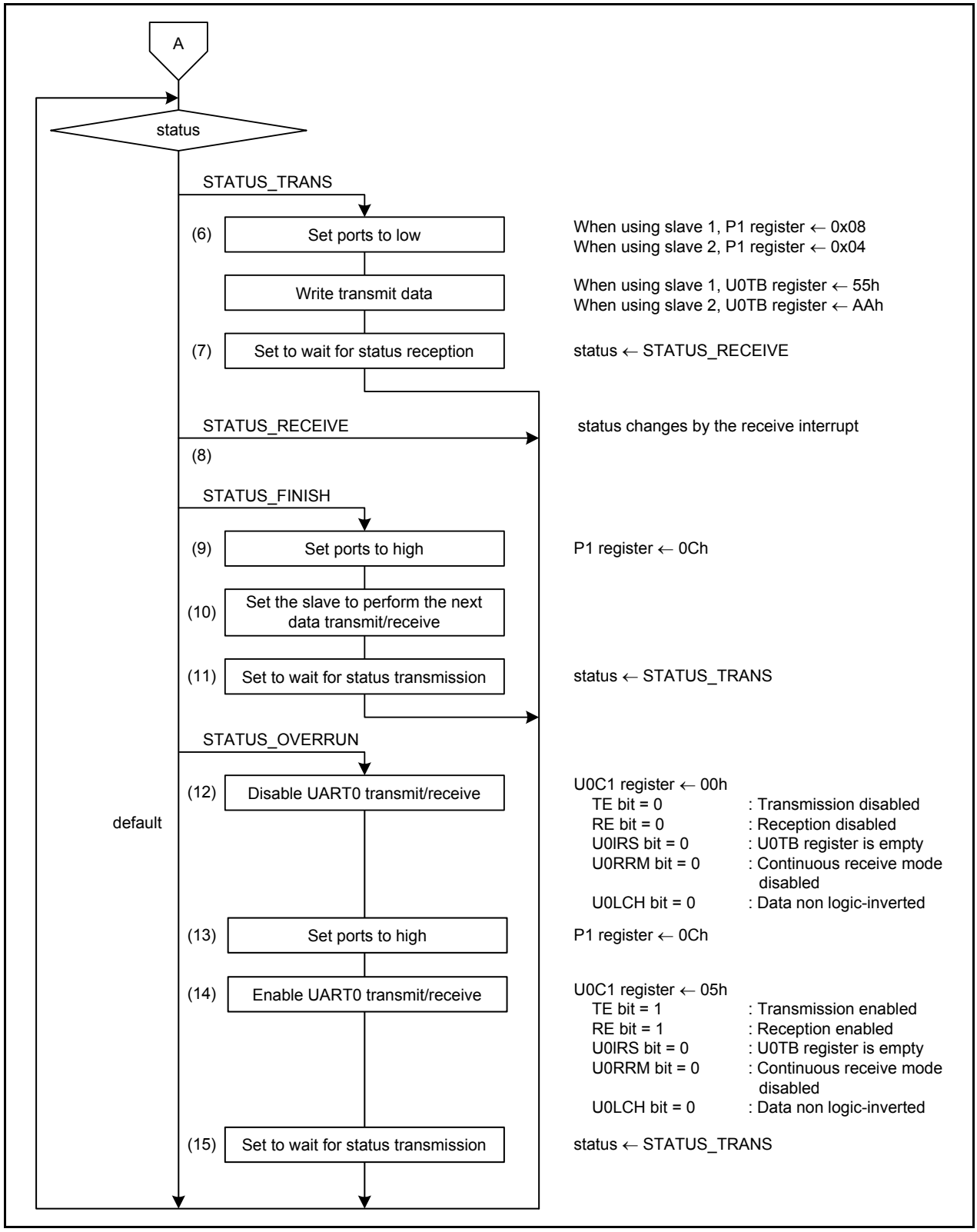


Figure 5.3 Main Processing (2/2)

5.6.2 UART0 Initial Setting

Figure 5.4 shows the initial setting for UART0.

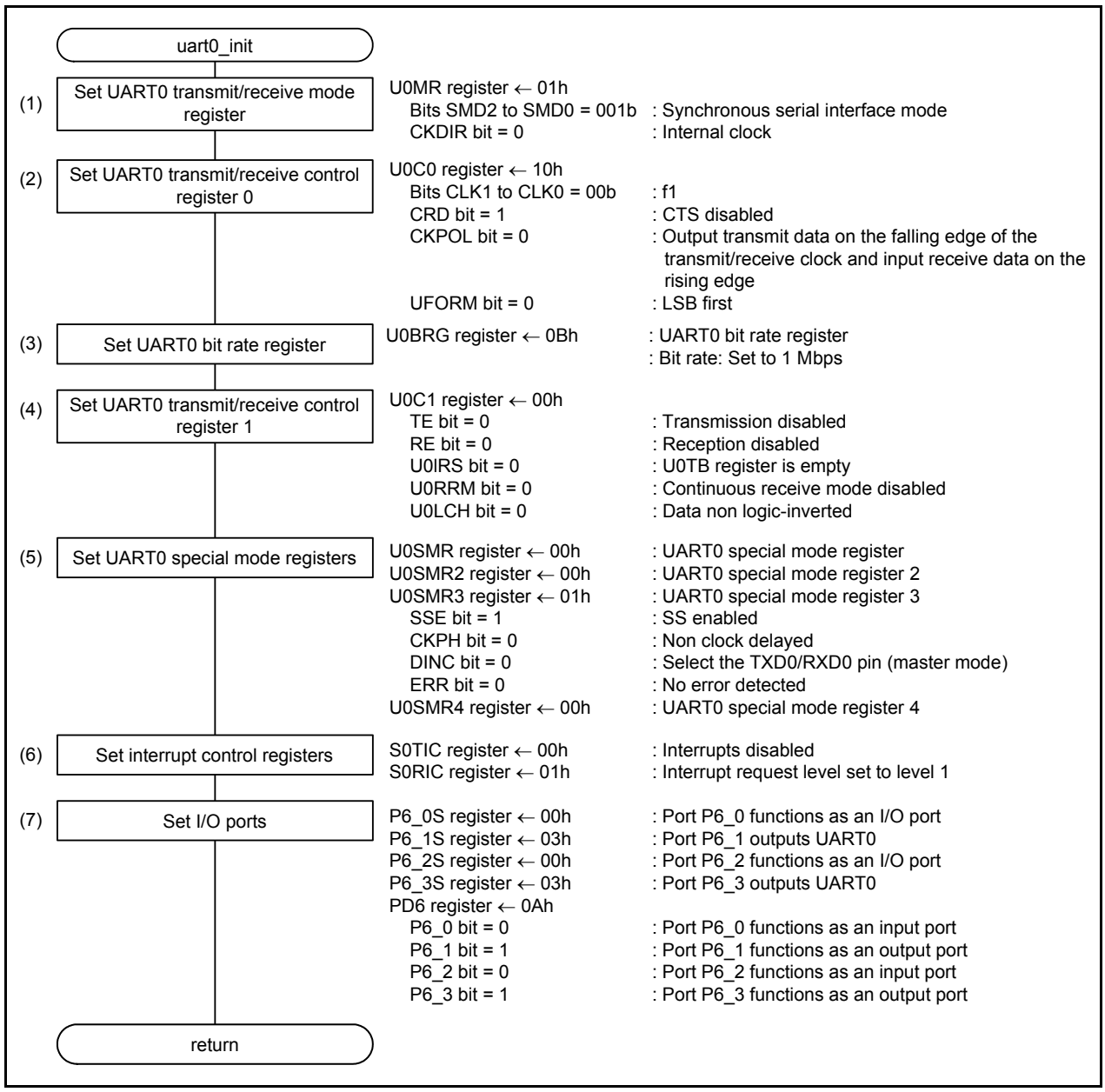


Figure 5.4 UART0 Initial Setting

5.6.3 UART0 Receive Interrupt Handling

Figure 5.5 shows the handling for the UART0 receive interrupt.

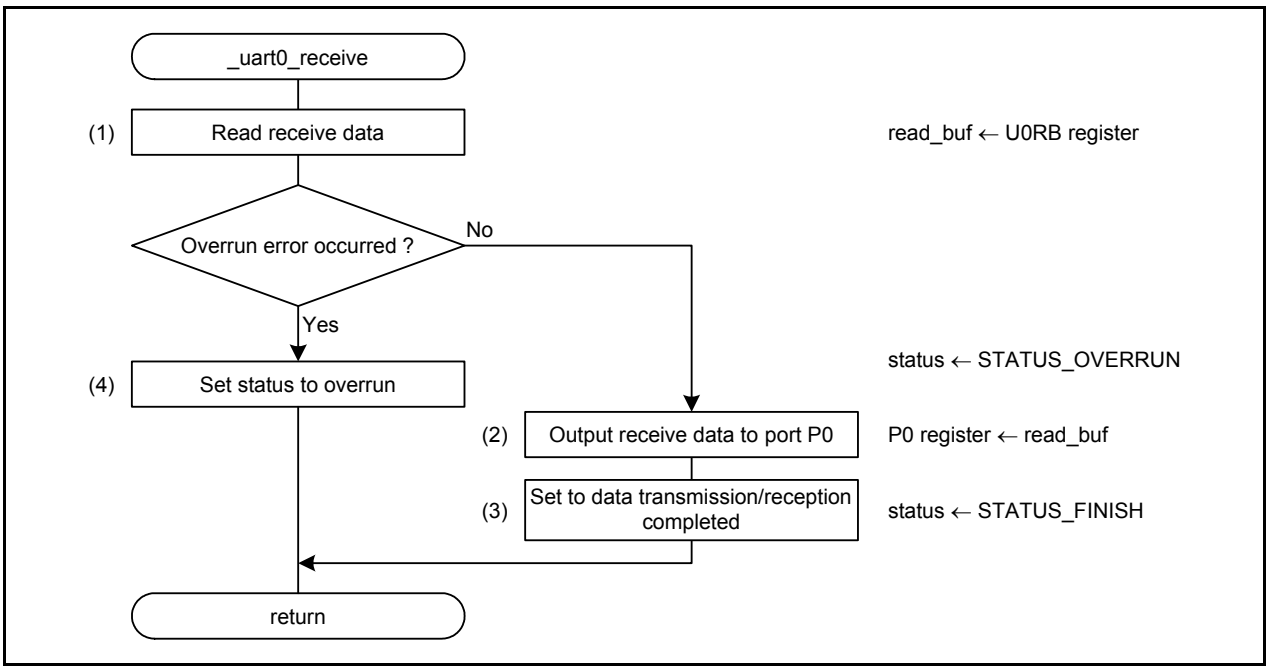


Figure 5.5 UART0 Receive Interrupt Handling

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	R32C/100 Series Serial Interface Operation in Special Mode 2 Using Master Transmission/Reception

Rev.	Date	Description	
		Page	Summary
1.00	July 22, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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