D2-4/D2-4P

API Register Specification (SRS WOW/HD™ Support)

Abstract

This document describes the Applications Programming Interface (API) for control, register addressing and audio processing data parameters of the D2-4 (D2-41151), and the D2-4P (D2-45157) devices. This document accompanies the IC product datasheets for the D2-4 and D2-4P devices.

Signal flow and audio path architecture are internally-defined within the D2-4. However, the audio processing blocks within the signal path are programmable, and their parameters are adjusted by the register control described in this document.

Only the specific register addresses defined in this document are valid. All other addresses are reserved and no data should be written to any of these reserved addresses.

The D2-4/D2-4P devices support either the D2 Audio DSP Sound Enhancement Algorithm or SRS WOW/HD audio enhancement algorithms. These device-specific functions are integrated within the firmware as part of the standard audio processing signal flow, and algorithm support is device part-number specific.

This document describes the signal flow and audio enhancement processing for the D2-41151 (D2-4) and D2-45157 (D2-4P) devices that support SRS WOW/HD processing.

Unless otherwise noted, all references to D2-4 within this document also apply to the D2-4P device, and except for the enhancement algorithms, all other audio processing functions and register control are identical for all devices.

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Related Literature

For a full list of related documents, visit our website:

- D2-41151, D2-45157 device pages

1. Registers and Control

Registers are accessed through the I2C control interface, where the D2-4 operates as an I2C slave device that receives communication and control from a system controller operating as the I2C master.

1.1 Hexadecimal Addresses and Data

Unless otherwise noted, all address and data values in this document are 24-bit hexadecimal numbers.

1.2 Round-Off Discrepancies in Calculations

Equations in this document represent the reference design's firmware algorithm calculations for defining the data parameters. Often the values displayed from the D2 Audio DSP Customization GUI user interface screen may appear in error by a very small difference from the true calculated equation values. This is due to round-off of internal calculations for presentation on the user screen and is not an error in actual parameter value.

1.3 Default Settings and Parameter Values

Default parameter settings listed in this document are the default settings internally defined by the D2-4 firmware. Additional parameter settings can be stored in a parameter table within an on-board EEPROM, where upon booting from that EEPROM, its data defines register settings within this address range. Parameter settings can also be written from a system controller during booting or during operation.

1.4 Storing Parameters to EEPROM

An EEPROM can be installed in the application, where the D2-4 device can read saved parameter settings from the EEPROM upon reset or power-up, loading the programmable audio processing registers with the settings previously saved to EEPROM. The firmware within the D2-4 supports writing audio processing register parameter settings to this EEPROM to save setting changes.

To store parameters to EEPROM:

- Write This Default Value: 000000
- To Register Address: 800000

This initiates the sequence for the D2-4 to write all of its programmable audio processing data parameters to EEPROM.

1.5 Reading and Writing Registers

All reads or writes to registers begin with a Start Condition, followed by the Device Address byte, three Register Address bytes, three Data bytes, and a Stop Condition. The I2C channel address is defined internal to D2-4 at a single address:

- I2C device address for D2-4/D2-4P is 0xB2.

1.5.1 Writing to Registers

Figure 1 shows the write sequence. Table 1 on page 4 describes each byte of the write sequence. Initiate a write by setting the read/write bit (R/W bit) within the device address byte.

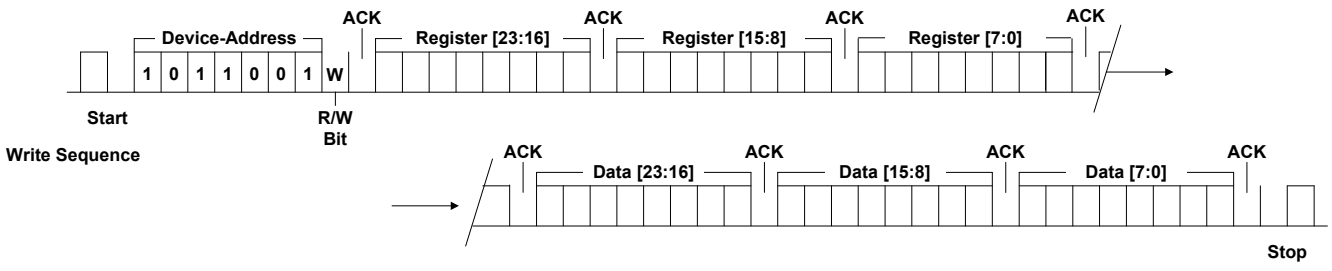

Figure 1. I2C Write Sequence Operation

Table 1. I²C Write Sequence

Byte	Name	Description
0	Device Address	Device Address, with R/W bit set
1	Register Address [23:16]	Upper 8 bits of address
2	Register Address [15:8]	Middle 8 bits of address
3	Register Address [7:0]	Lower 8 bits of address
4	Data [23:16]	Upper 8 bits of write data
5	Data [15:8]	Middle 8 bits of write data
6	Data [7:0]	Lower 8 bits of write data

1.5.2 Reading from Registers

All reads to registers, shown in Figure 2 on page 4, require two steps. First, the master must send a write command consisting of the device address with the read/write bit (R/W bit) set to indicate a write, followed by three register address bytes. However, instead of following the address with three data bytes as in a write command, the master must then send a repeated Start, this time with the R/W bit set to read. The master then reads the next three data bytes. The master must “ACK” the first two read bytes and send a “NACK” on the third byte received, and finally a Stop condition to complete the transaction. The device's control interface acknowledges each byte by pulling SDA low on the bit immediately following each write byte. These bytes are described in Table 2 on page 4.

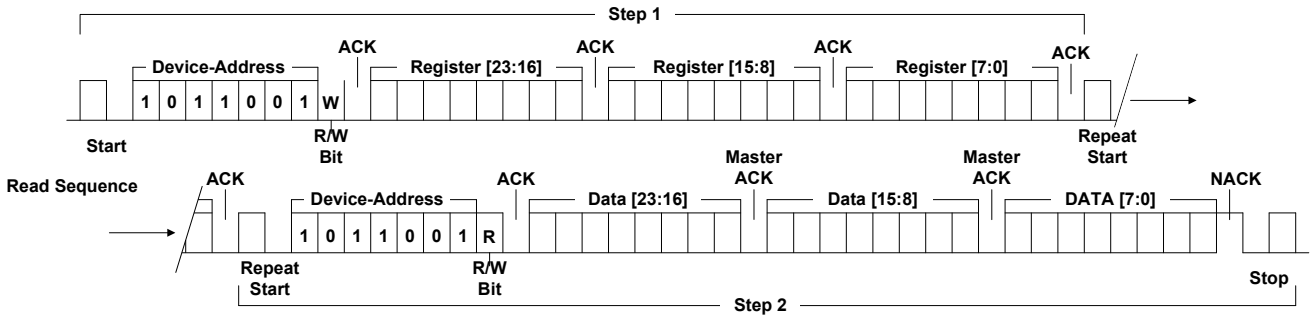

Figure 2. I²C Read Sequence Operation

Table 2. I²C Read Sequence

Byte	Name	Description
0	Device Address	Device Address, with Write bit set
1	Register Address [23:16]	Upper 8 bits of address
2	Register Address [15:8]	Middle 8 bits of address
3	Register Address [7:0]	Lower 8 bits of address
4	Device Address	Device Address, with Read bit set
5	Data [23:16]	Upper 8 bits of write data
6	Data [15:8]	Middle 8 bits of write data
7	Data [7:0]	Lower 8 bits of write data

1.6 Register Address Table Map

Assigned register locations are shown in Table 3. See the specific audio processing block's individual register address assignment for specific register function definition.

Only the specific register addresses defined in this document are valid. All other addresses are reserved and no data should be written to any of these reserved addresses.

Table 3. Register Addresses

Address Ranges (hex)		Function
From	To	
000000		Master Volume Adjustment Control
020001		Input Select Write Address
020002		Input Select Read Address
000001	000005	Output Volume Trim Controls
000006	000009	2x2 Input Mixer
00000A	000011	Tone Controls
000012		Stereo Router
000013	00001E	Input Compressors (Limiters)
00001F	00003C	5-Band Equalizers
00003D	000060	3-Band Equalizers
000061	00007E	Speaker Equalizers
00007F	0000AE	High-Pass and Low-Pass Filters (Output Channels 1-4)
0000AF	0000B0	Stereo Mixer
0000B1	0000BC	High-Pass and Low-Pass Filters (Output Channel 5)
0000BD	0000DA	Output Compressors (Limiters)
0000DB	0000E9	Loudness Contour Controls
000148	000165	SRS WOW/HD Processing Controls
000166		Signal Flow Option Register
000167		Hardware Option Register
-		All Other Addresses Reserved

2. Audio Processing

The audio processing and signal flow within the D2-4 devices is defined by the internal ROM firmware and executed by the device's internal DSP. This firmware defines the audio flow architecture and the processing blocks used in that definition, but also provides for programmable parameters for those processing blocks.

Figure 3 on page 6 shows the signal flow for the D2-4 devices. Signal flow and programmable audio processing for the D2-4P devices, shown in Figure 4 on page 7, is identical. Table 3 lists the programmable audio processing blocks described in this document.

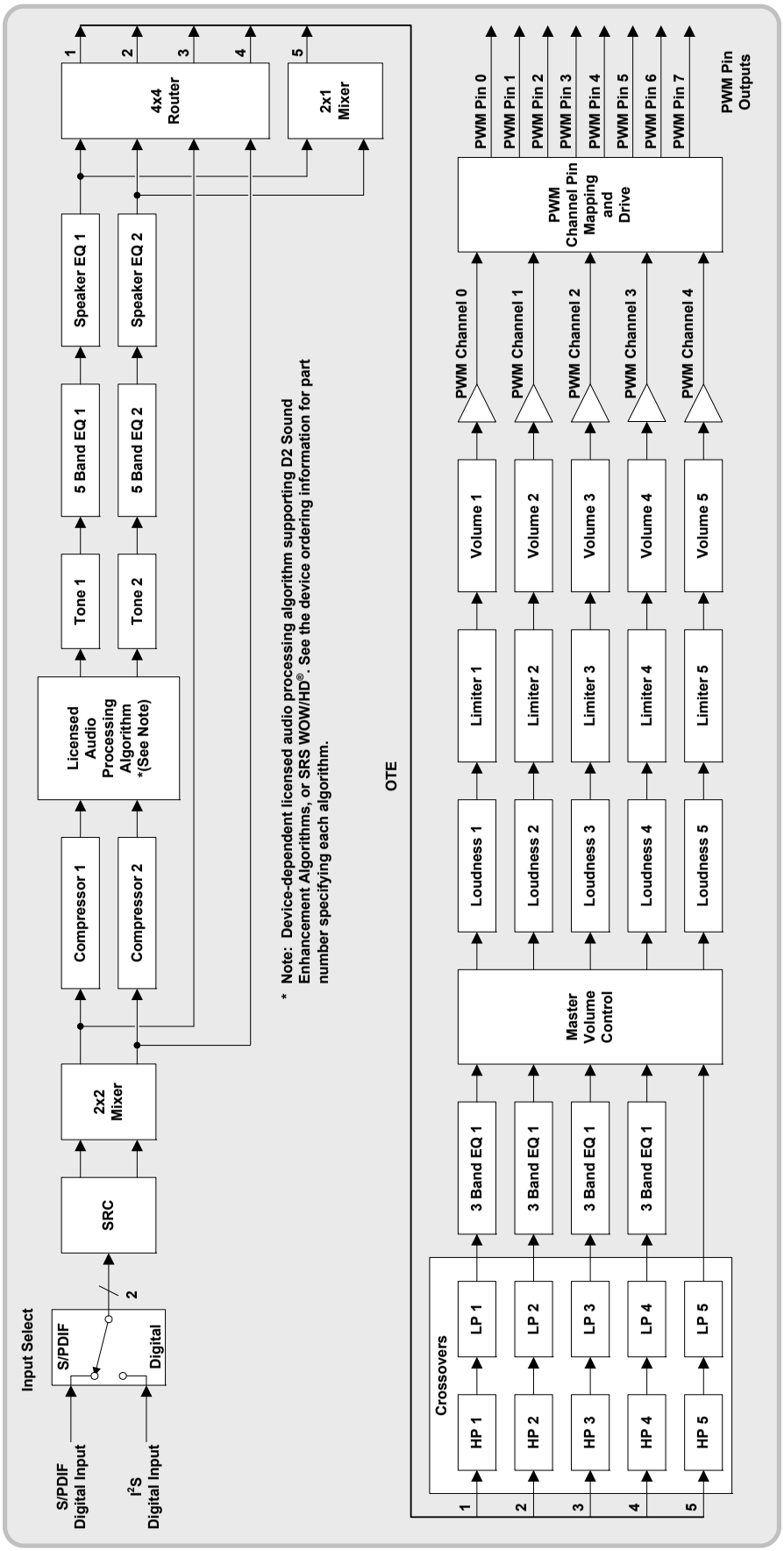

Figure 3. D2-4 Family D2-41151 Audio Processing Signal Flow

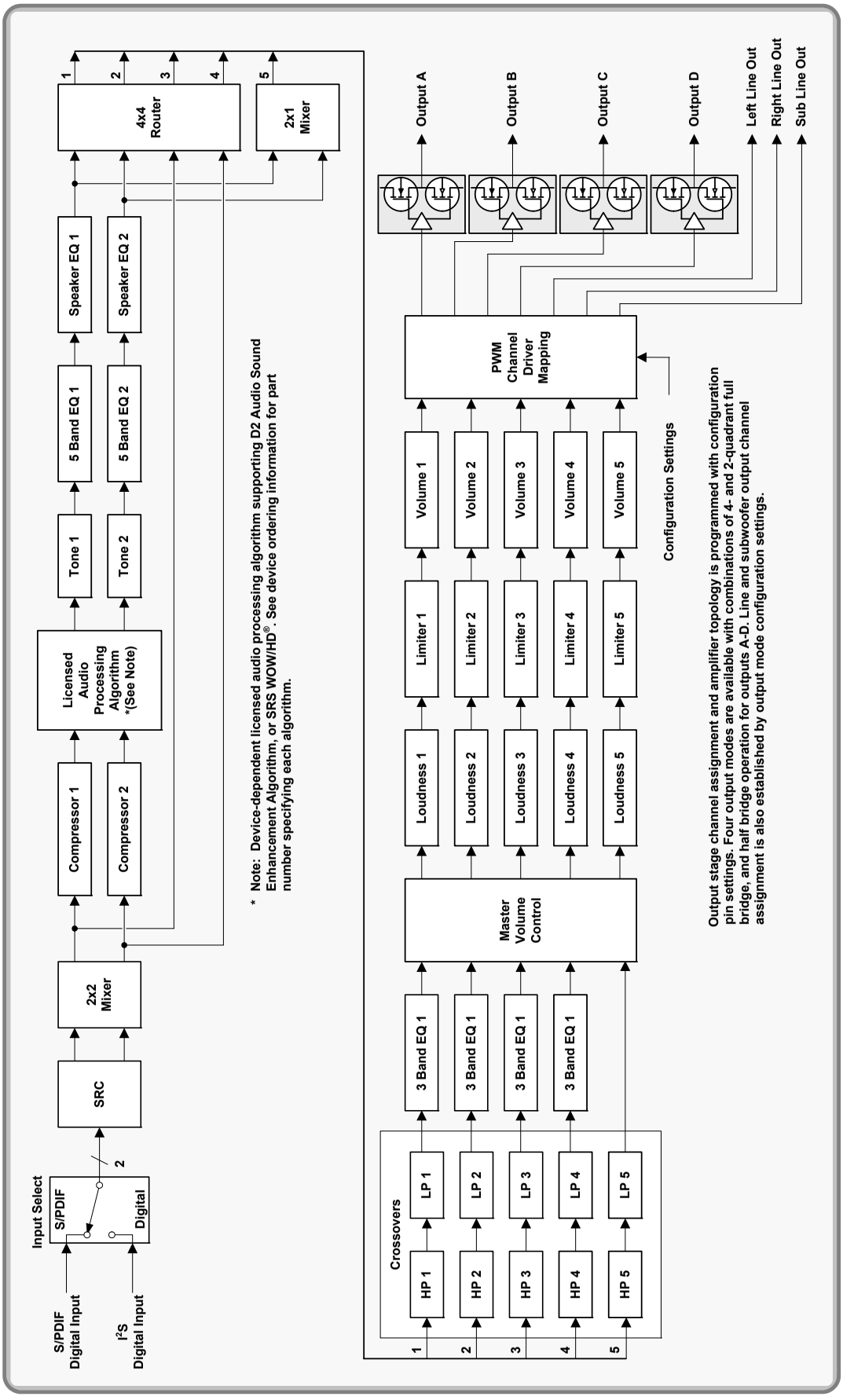

Figure 4. D2-4P Family D2-45157 Audio Processing Signal Flow

2.1 Channel Number Reference

Channel number designations that are either zero-based or one-based are used interchangeably in documents or software tools supporting the D2-4/D2-4P devices. References of “Channels 1 through 5” therefore correlate to similar references of “Channels 0 through 4.” A “one-based” reference is used in this document. (For example, Input channels are referenced as 1 and 2, and output channels are referenced as 1, 2, 3, 4, and 5.)

2.2 Enhancement Audio Processing Options

The D2-4/D2-4P devices support either the D2 Audio DSP Sound Enhancement Algorithms or SRS WOW/HD audio enhancement algorithms. These device-specific functions are integrated within the firmware as part of the standard audio processing signal flow, and are supported per device as:

- D2 Audio DSP Sound Enhancement algorithm (Wide Sound, Deep Bass, Audio Align, and Clear Voice) Audio Processing
  - Supported in the D2-41051 and D2-45057 devices.
- SRS WOW/HD Audio Processing
  - Supported in the D2-41151 and D2-45157 devices.

Each of these enhancements uses its own algorithms, where choice of enhancement is specified by the D2-4 device’s part number. The D2-41051 and D2-45057 include only D2 Audio DSP Sound Enhancement Algorithm support. The D2-41151 and D2-45157 include only SRS WOW/HD support. These enhancements also have their own unique set of programmable parameters to control their operation. The location of these enhancement blocks within the signal flow is shown as the “Licensed Audio Processing Algorithm” block in Figures 3 and 4.

Each enhancement algorithm support is unique only to devices referenced by its particular part number, and operates only within the devices of that part number. To avoid conflict with any software writes to address locations used by each of the enhancement algorithms, any read/write instructions to register locations of algorithms not included or supported within each part number device are ignored. Only the instructions to addresses included for the device’s supported algorithms are acknowledged.

This document describes register assignments for only the SRS WOW/HD. Register assignments for D2 Audio DSP Sound Enhancement Algorithms operation are provided separately.

3. Input Select Register

The Input Select register assigns the source input that is presented to the audio processing path. The D2-4 devices support two input choices of S/PDIF Digital, or Serial Audio Input (SAI) Digital inputs. The default firmware setting is to use SAI inputs.

The input sources specified by the Input Select register route to the on-chip Sample Rate Converters (SRC) where they are then presented to the on-chip audio processing.

The input select register operates at two different register addresses:

- Address 020002 is read-only.
- Address 020001 is write only.

The first two data bits (bits [23:22]) of the Input Select register must be set to “1”. Bit zero (0) defines the input selection. All other bits of this register are reserved and must be set to “0”.

The input to the audio processing path is assigned by writing this data to address 020001:

- C00001 assigns S/PDIF as the input.
- C00000 assigns SAI as the input.

Table 4. D2-4 Input Select Register

Register Bits [23:0]																							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																				Input Channel Source			
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Always 0xCx				All bits = 0																Assigns SAI to Input Channels			
																				0	0	0	1
																				Assigns S/PDIF Digital to Input Channels			

4. Master Volume Control

A software-controlled Master Volume control adjusts the global volume for all audio processing channels. A single register is used for the Master Volume adjustment.

Volume level is represented as attenuation, and does not introduce additional gain (Note 1).

- The Master Volume control register address is:
  - 000000
- The default value is:
  - 800000, which corresponds to 0dB, or no attenuation

4.1 Volume and Trim Control Parameters

The Master Volume controls and Channel Volume Trim controls are both implemented to provide attenuation, and do not introduce additional gain (Note 1). Maximum level with no attenuation is 0dB, and maximum attenuation is 100dB. Setting their register parameter values to 000000 causes full cut off (infinite attenuation) of the signal.

The Volume Control gain parameter is a signed, 24-bit number. Signal polarity can be inverted through the volume gain control block, where the magnitude of the signal attenuation is identical, but the signal polarity is inverted in phase. The Most Significant Bit (MSB) of the 24-bit parameter defines this signal polarity. In normal (non-inverted) application, the 24-bit gain parameter is represented as a negative number, and its MSB is set. Clearing this MSB (representing a positive number) inverts the polarity. Calculations for both normal and inverted parameters are shown in Equations 1 and 2, which is accomplished simply removing the negative sign from the gain formula and recalculating the gain parameter. This yields a positive instead of negative 24-bit parameter value, but represents the same attenuation level.

Regardless of the sign of the 24-bit hex parameter value, the magnitude of the gain (attenuation) adjustment does not change. Only the signal polarity changes with the corresponding sign change of the parameter. A negative 24-bit hex parameter therefore represents normal polarity, whereas a positive 24-bit hex parameter represents inverted polarity but with the same magnitude.

Maximum level with no attenuation is 0dB, and maximum attenuation is 100dB. **Note:** It is possible to enter parameter values correlating to attenuation beyond this 100dB limit, but only values within the specified range are valid.

Setting the register parameter value to 000000 causes full cut off (infinite attenuation) of the signal.

4.2 Master Volume Gain Parameter Calculations

(EQ. 1) $$\text{Volume Gain Parameter} = -\left[2^{23} \times 10^{\left(\frac{\text{Gain}}{20}\right)}\right]$$ Normal Polarity, Non-Inverted

(EQ. 2) $$\text{Volume Gain Parameter} = \left[2^{23} \times 10^{\left(\frac{\text{Gain}}{20}\right)}\right]$$ Inverted Polarity

where: Gain is in dB, and is a negative (or zero) term.(Note 1)

	Minimum		Maximum	
Valid Range (Note 2)	-100dB		0dB	
	FFFFAC		800000	Normal Polarity, Non-Inverted
	000054		7FFFFF	Inverted Polarity
		000000		Signal Path Cut-Off
Default Setting	0dB		800000	

Notes:
1. The term “Gain” is often used to indicate level adjustment, and within general discussions, can actually represent either increase or attenuation of level. In this terminology, positive gain is an increase in signal level, while negative gain is attenuation. The Master Volume control implements attenuation and does not introduce gain. As such, the “Gain” term used in the equations is a negative value that actually represents an attenuation.
2. The maximum parameter value of 800000 may be appear as 800001 from the D2 Audio DSP Customization GUI user interface screen. This is due to round-off of internal calculations for presentation on the user screen and is not an error in actual parameter value.

5. Output Trim Volume Controls

A dedicated per-channel output volume level adjustment provides individual channel gain or attenuation as a final adjustment to trim signal levels at each of the outputs.

These output level settings provide a gain (Note 1) from +12dB to -88dB. Each of the output volume adjustments has its own register address and level setting.

The Output Volume gain parameter is a signed 24-bit number. Signal polarity can be inverted through the gain control blocks, where the magnitude of the signal attenuation or gain is identical, but the signal polarity is inverted in phase. The MSB of the 24-bit parameter is used to define this signal polarity. In normal (non-inverted) application, the 24-bit gain parameter is represented as a negative number, and its MSB is set. Clearing this MSB (representing a positive number) inverts the polarity. Calculations for both normal and inverted parameters are shown in Equations 3 and 4, which is simply removing the negative sign from the gain formula and recalculating the gain parameter. This yields a positive instead of negative parameter value.

Regardless of the sign of the 24-bit hex parameter value, the magnitude of the gain (attenuation) adjustment does not change. Only the signal polarity changes with the corresponding sign change of the parameter. A negative 24-bit hex parameter therefore represents normal polarity, whereas a positive 24-bit hex parameter represents inverted polarity but with the same magnitude.

Maximum level (gain) is +12dB, and minimum level (attenuation) is -88dB. **Note**: It is possible to enter parameter values correlating to attenuation beyond these limits, but only values within the specified range are valid.

Setting the register parameter value to 000000 causes full cut off (infinite attenuation) of the signal.

5.1 Output Trim Volume Parameter Calculation

(EQ. 3) $$\text{Output Trim Gain Parameter} = -\left[2^{23} \times 10^{\left(\frac{\text{Gain}-12}{20}\right)}\right]$$ Normal Polarity, Non-Inverted

(EQ. 4) $$\text{Output Trim Gain Parameter} = \left[2^{23} \times 10^{\left(\frac{\text{Gain}-12}{20}\right)}\right]$$ Inverted Polarity

where: Gain is in dB (positive for gain; negative for attenuation)

	Minimum		Maximum	
Valid Range Note 2	-88dB		+12dB	
	FFFFAC		800000	Normal Polarity, Non-Inverted
	000054		7FFFFF	Inverted Polarity
		000000		Signal Path Cut-Off
Default Setting	0dB		E00000	

5.2 Output Trim Volume Register Addresses

Register Parameter	Output Trim Addresses
Channel 1 Address	000001
Channel 2 Address	000002
Channel 3 Address	000003
Channel 4 Address	000004
Channel 5 Address	000005

6. Mixers

The D2-4 audio processing path includes two mixers.

- A 2-input by 2-output (2x2) Mixer routes the input sources to each of the two audio processing input paths.
- A 2-input Stereo Mixer routes the outputs of the two input channels to drive the fifth output processing channel.

The Input Mixer contains four registers and the Stereo Mixer contains two registers. Each register defines the gain of its specific input channel that is mixed into its specific output channel.

Either input of the Input Mixer can be mixed at adjustable gains into either or both of its two outputs. The default setting is 0dB for the Channel 1 input to Channel 1 output, and for the Channel 2 input to Channel 2 output. Gains across channels are set at defaults of cut-off.

The two stereo inputs from Channel 1 and Channel 2 can be mixed and/or routed to Channel 5 through the Stereo Mixer. This configuration typically provides a mix of both stereo input channels for crossover processing and becomes the source for the subwoofer channel. Gains for both input channels are adjustable to feed the single stereo mixer output.

Operation and calculations for the mixer parameters are identical for both mixer blocks.

6.1 Mixer Gain

The mixer gain parameter is a signed, 24-bit number. Signal polarity can be inverted through the gain control blocks, where the magnitude of the signal attenuation is identical, but the signal polarity is inverted in phase. The MSB of the 24-bit parameter defines this signal polarity. In normal (non-inverted) application, the 24-bit gain parameter is represented as a negative number, and its MSB is set. Clearing this MSB (representing a positive number) inverts the polarity. Calculations for both normal and inverted parameters are shown in Equations 5 and 6, which is simply removing the negative sign from the gain formula and recalculating the gain parameter. This yields a positive instead of negative parameter value.

Regardless of the sign of the 24-bit hex parameter value, the magnitude of the gain (attenuation) adjustment does not change. Only the signal polarity changes with the corresponding sign change of the parameter. A negative 24-bit hex parameter therefore represents normal polarity, whereas a positive 24-bit hex parameter represents inverted polarity but with the same magnitude.

The valid range for gain is 0dB for maximum level with no attenuation, and -100dB at lowest (maximum attenuation) level. Setting the register parameter value to 000000 causes full cut off (infinite attenuation) of the signal.

Default gain settings for the Stereo Mixer are -6dB, allowing for summation of both input channels. The default parameter value of C00000 produces this -6dB gain. Note however, that due to round-off effects during calculation when using the D2 Audio DSP Customization GUI software, entering a value of -6dB produces a parameter of BFD919 (for -6.00000049dB) and entering a value of -6.0206dB, for a more precise representation of 50% signal attenuation, actually produces C00000.

6.1.1 Mixer Gain Parameter Calculation

(EQ. 5) $$\text{Mixer Gain Parameter} = -\left[2^{23} \times 10^{\left(\frac{\text{Gain}}{20}\right)}\right]$$ Normal Polarity, Non-Inverted

(EQ. 6) $$\text{Mixer Gain Parameter} = \left[2^{23} \times 10^{\left(\frac{\text{Gain}}{20}\right)}\right]$$ Inverted Polarity

where: Gain is in dB and is a negative (or zero) term.

	Minimum		Maximum	
Valid Range Note 2	-100dB		0dB	
	FFFFAC		800000	Normal Polarity, Non-Inverted
	000054		7FFFFF	Inverted Polarity
		000000		Signal Path Cut-Off
Default Settings Note 2	0dB		800000	For pass-through channels (such as In 1 to Out 1, and In 2 to Out 2)
	(cut-off)		000000	For non-connected channels (such as In 1 to Out 2, and In 2 to Out 1)
	-6dB		C00000	For Stereo Mixer (C00000 actually represents -6.0206dB)

6.2 Mixer Register Addresses

6.2.1 2x2 Input Matrix Mixer Register Addresses

Register Parameter	Input Channel 1	Input Channel 2
Output Channel 1	000006	000007
Output Channel 2	000008	000009

6.2.2 Stereo Mixer Register Addresses

Register Parameter	Input Channel 1	Input Channel 2
Output Channel	0000AF	0000B0

7. Stereo Router

A 4x4 stereo router assigns any one of the four input channel paths to each of the four output paths. The router performs path assignment only. It does not have provision for gain or signal level adjustment.

The lower 8 bits at a single address location (000012) are used for the router path assignment. These 8 bits are divided into four groups of 2 bits each, where each group corresponds to the router's output channel. The contents of each 2 bits within these groups defines the input channel that is assigned to that particular output.

7.1 Router Register Parameter Data and Addresses

	Reserved	Output Channel 4	Output Channel 3	Output Channel 2	Output Channel 1
Register Bits	[23:8]	[7:6]	[5:4]	[3:2]	[1:0]
Default Value	0x000	11	10	01	00

7.1.1 Input Channel Value Definitions

The bit values correspond to the input channel that is assigned to the output channel:

Bit Value	Input Channel
00	1
01	2
10	3
11	4

The default data value for the router is 0000E4, which corresponds to:

Input Channel	Output Channel
1	1
2	2
3	3
4	4

8. Compressors (Limiters)

Audio compressors are provided in both the input and output audio processing paths. Both audio input channels have one compressor, and each of the five output channels also has one compressor. Each compressor has configurable Compression Ratio, Threshold, Attack and Release Time, and Makeup Gain. The compressors operate and are implemented independently. Their audio processing operation (compressor or limiter function) is determined by their programmable settings.

8.1 Threshold

The compressor/limiter function operates to reduce the gain of its output signals when its input exceeds a given threshold. The Threshold parameter is a signed, 24-bit number. The threshold value is entered in dB. The valid range for Threshold is -90dB to 0dB.

8.1.1 Limiter Threshold Parameter Calculation

(EQ. 7) $$\text{Limiter Threshold Parameter} = 2^{23} \times \frac{1}{32}\left[\left(\frac{\text{Threshold}}{10 \times \log_{10}(2)}\right) + 31\right]$$

where: Threshold is in dB (-90dB to 0dB)

	Minimum	Maximum
Valid Range	-90dB	0dB
	000000	7C0000
Default Setting	0dB	7C0000

8.2 Ratio

The Limiter Ratio is the number of dB above the threshold that the input level must increase to increase the output level by 1dB. The Ratio parameter is a signed, 24-bit number. The Ratio value is entered as a ratio-to-one number. The valid range for the Ratio parameter is 1 to 100. **Note**: A ratio of 1 disables the limiter, and values above 10 are typically used to provide a limiting function.

8.2.1 Limiter Ratio Parameter Calculation

(EQ. 8) $$\text{Limiter Ratio Parameter} = 2^{23} \times \left[1 - \frac{1}{\text{Ratio}}\right]$$

	Minimum	Maximum
Valid Range	1:1	100:1
	000000	7EB852
Default Setting	100:1	7EB852

8.3 Attack and Release Time

The Attack Time is the rate at which the gain is reduced when the input exceeds the threshold. The Release Time is the rate at which the gain is increased when the input falls below the threshold. Calculations and parameters for both Attack and Release times are identical.

The Attack and Release time parameters are signed, 24-bit numbers. The time value is entered as milliseconds. Valid ranges for both the attack and release times are 1ms to 1000ms.

8.3.1 Limiter Attack and Release Time Parameter Calculation

(EQ. 9) $$\text{Attack or Release Time Parameter} = 2^{23} \times \left[a + \sqrt{a^2 - 2a}\right]$$

Where:

$$a = \left[\cos\left(\frac{1}{3 \times T}\right) - 1\right]$$

T is in milliseconds

	Minimum	Maximum	
Valid Range	1ms	1000ms	
	24011D	000AEC	
Default Settings	10ms	04322A	Attack time
	100ms	006D08	Release time

8.4 Makeup Gain

Depending on the settings for Threshold and Compressor Ratio, additional Makeup Gain may be necessary to reach a full-scale output.

The Makeup Gain parameter is a signed, 24-bit number. The Makeup Gain value is entered in dB. The valid range for Makeup Gain is -70dB to +36dB.

8.4.1 Limiter Makeup Gain Parameter Calculation

(EQ. 10) $$\text{Makeup Gain Parameter} = 2^{23} \times \left[\frac{10^{\left(\frac{\text{Gain}}{20}\right)}}{64}\right]$$

where Gain is in dB

	Minimum	Maximum
Valid Range	-70dB	+36dB
	000029	7FFDBD
Default Settings	0dB	020000

8.5 Compressor Register Addresses

8.5.1 Input Channel Compressor Register Addresses

Register Parameter	Channel 1	Channel 2
Threshold	000014	00001A
Ratio	000015	00001B
Attack Time	000016	00001C
Release Time	000017	00001D
Makeup Gain	000018	00001E

8.5.2 Output Channel Compressor Register Addresses

Register Parameter	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Threshold	0000BE	0000C4	0000CA	0000D0	0000D6
Ratio	0000BF	0000C5	0000CB	0000D1	0000D7
Attack Time	0000C0	0000C6	0000CC	0000D2	0000D8
Release Time	0000C1	0000C7	0000CD	0000D3	0000D9
Make Up Gain	0000C2	0000C8	0000CE	0000D4	0000DA

9. Tone Controls

A tone control block is included for each of the audio processing channels. Each of the filters (bass or treble) is implemented with a first-order (6dB/octave) roll-off that uses programmable corner frequency and a boost or attenuating gain. The signal flow processing automatically provides a smooth transition between tone control changes.

9.1 Tone Control Parameters and Registers

Each bass and treble filter includes its own frequency register and gain register and provides a total of four registers per tone control block.

9.1.1 Tone Control Register Addresses

Register Parameter	Channel 1	Channel 2
Bass Corner Frequency Parameter	00000A	00000E
Bass Gain Parameter	00000B	00000F
Treble Corner Frequency Parameter	00000C	000010
Treble Gain Parameter	00000D	000011

9.2 Tone Control Corner Frequency Calculation

The Corner Frequency of the Tone Control is defined as the frequency at which the gain of the filter is -3dB. The Corner Frequency parameter is a signed, 24-bit number.

9.2.1 Tone Control Corner Frequency Parameter Calculation

(EQ. 11) $$\text{Corner Frequency Parameter} = 2^{23} \times \left[\frac{\sin\left(\frac{\pi \times F}{24000}\right) - 1}{\cos\left(\frac{\pi \times F}{24000}\right)} \right]$$

where F = Frequency in Hz

	Minimum	Maximum	
Valid Range	10Hz	22kHz	
	802ADD	FFFFFF	For 10Hz to 11.999kHz
	000000	6237C4	For 12kHz to 30kHz
Default Settings	200Hz	834ED4	Bass Default
	2000Hz	9DC83B	Treble Default

9.3 Tone Control Gain Calculation

The gain parameter is a signed, 24-bit number. Gain is entered in dB. The valid range for Tone Control Gain is -14dB to +14dB. A setting of 000000 sets gain to unity (0dB) for no boost or cut.

9.3.1 Tone Control Gain Parameter Calculation

(EQ. 12) $$\text{Tone Control Gain Parameter} = 2^{23} \times \left[\frac{10^{\left(\frac{\text{Gain}}{20}\right)} - 1}{4} \right]$$

where Gain is in dB

	Minimum		Maximum	
Valid Range	-14dB		+14dB	
	E6667A		7FFE1D	
		000000		0dB, no boost or cut
Default Settings	0dB		000000	Bass Default
	0dB		000000	Treble Default

10. Multi-Band Equalizers

Three sets of Multi-Band Parametric Equalizers are provided in the audio signal processing path.

Two sets of 5-Band Equalizers are provided in each of the two input channels, and four 3-Band Equalizers are located in the four output channels. These equalizers operate identically and provide separate equalization blocks, such as EQs that are adjustable by the end user, and EQs for implementing end product presets that are defined during production.

The equalizer blocks are implemented from individual identical cascaded stages (three stages for the 3-Band, and five stages for the 5-Band Equalizers). Each stage operates completely independently, but all are configured identically. Each equalizer band stage uses three register parameters to define its operation. These parameters are Center Frequency, Quality-Factor (Q), and Gain. All parameters are calculated identically for each of the equalizer stages.

10.1 Equalizers Center Frequency

The Center Frequency parameter is a signed, 24-bit number. The frequency value is entered in Hz. The valid range for the frequency parameter is 10Hz to 22000Hz.

10.1.1 Equalizer Center Frequency Parameter Calculation

(EQ. 13) $$\text{Frequency Parameter} = 2^{23} \times \left[\frac{F}{24} \times 10^{-3} \right]$$

where F = Frequency in Hz

	Minimum	Maximum
Valid Range	10Hz	22kHz
	000DA7	755555
Default Settings	400Hz	022222

10.2 Equalizers Quality Factor

The Quality Factor (Q) parameter is a signed, 24-bit number. The valid range for the Q parameter is >0.5 to 10.
Note: A setting of 0.5, producing a parameter value of 800000 is invalid.

10.2.1 Equalizer Q-Factor Parameter Calculation

(EQ. 14) $$\text{Q-Factor Parameter} = 2^{23} \times \left[\frac{1}{2 \times Q}\right]$$

	Minimum	Maximum
Valid Range	0.5+	10
	7FFFFF	066666
	(Q>0.5; a value of 0.5 creates a hex value of 800000 which is invalid)	
Default Settings	Q = 4.323	0ECE1F

10.3 Equalizers Gain

Gain is defined at the equalizer block stage's center frequency. The gain parameter is a signed, 24-bit number. Gain is entered in dB. The valid range for gain is -30dB to +6dB.

10.3.1 Equalizer Gain Parameter Calculation

(EQ. 15) $$\text{Equalizer Gain Parameter} = -2^{23} \times \left[1 - 10^{\left(\frac{\text{Gain}}{20}\right)}\right]$$

where Gain is in dB

	Minimum		Maximum	
Valid Range	-30dB		+6dB	
	840C37		7FFF3F	
		000000		Bypasses EQ filter stage element
Default Settings	0dB		000000	

10.4 Multi-Band Parametric Equalizer Register Addresses

10.4.1 3-Band Parametric Equalizer Addresses

Register Parameter	Channel 1 Address	Channel 2 Address	Channel 3 Address	Channel 4 Address
Band 1 Frequency	00003D	000046	00004F	000058
Band 1 Damping/Bandwidth	00003E	000047	000050	000059
Band 1 Gain/Bypass	00003F	000048	000051	00005A
Band 2 Frequency	000040	000049	000052	00005B
Band 2 Damping/Bandwidth	000041	00004A	000053	00005C
Band 2 Gain/Bypass	000042	00004B	000054	00005D
Band 3 Frequency	000043	00004C	000055	00005E
Band 3 Damping/Bandwidth	000044	00004D	000056	00005F
Band 3 Gain/Bypass	000045	00004E	000057	000060

10.4.2 5-Band Parametric Equalizer Addresses

Register Parameter	Channel 1 Address	Channel 2 Address
Band 1 Frequency	00001F	00002E
Band 1 Damping/Bandwidth	000020	00002F
Band 1 Gain/Bypass	000021	000030
Band 2 Frequency	000022	000031
Band 2 Damping/Bandwidth	000023	000032
Band 2 Gain/Bypass	000024	000033
Band 3 Frequency	000025	000034
Band 3 Damping/Bandwidth	000026	000035
Band 3 Gain/Bypass	000027	000036
Band 4 Frequency	000028	000037
Band 4 Damping/Bandwidth	000029	000038
Band 4 Gain/Bypass	00002A	000039
Band 5 Frequency	00002B	00003A
Band 5 Damping/Bandwidth	00002C	00003B
Band 5 Gain/Bypass	00002D	00003C

10.4.3 Speaker (5-Band) Equalizer Addresses

Register Parameter	Channel 1 Address	Channel 2 Address
Band 1 Frequency	000061	000070
Band 1 Damping/Bandwidth	000062	000071
Band 1 Gain/Bypass	000063	000072
Band 2 Frequency	000064	000073
Band 2 Damping/Bandwidth	000065	000074
Band 2 Gain/Bypass	000066	000075
Band 3 Frequency	000067	000076
Band 3 Damping/Bandwidth	000068	000077
Band 3 Gain/Bypass	000069	000078
Band 4 Frequency	00006A	000079
Band 4 Damping/Bandwidth	00006B	00007A
Band 4 Gain/Bypass	00006C	00007B
Band 5 Frequency	00006D	00007C
Band 5 Damping/Bandwidth	00006E	00007D
Band 5 Gain/Bypass	00006F	00007E

11. Loudness Contour

An individual software-controlled Loudness Contour is included for each of the five output channels. The Loudness Contour curve is customized to allow for dynamically and automatically enhancing the frequency response of the audio program material relative to the Master Volume Level setting. The Loudness Contour models the frequency response correction as defined by the Fletcher/Munson audio response curve. It provides for amplitude or volume changes to those signals to which the ear does not respond equally at very low listening levels.

This Loudness Contour feature is disabled by default, but can be enabled through its register control. Contact Renesas Applications support for additional information about the implementation of this algorithm.

11.1 Loudness Contour Register Data

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Address					
Enable Loudness	0000DB	0000DE	0000E1	0000E4	0000E7
Tone Low Pass	0000DC	0000DF	0000E2	0000E5	0000E8
Tone High Pass	0000DD	0000E0	0000E3	0000E6	0000E9
Default Value					
Enable Loudness	000000	000000	000000	000000	000000
Tone Low Pass	81AA26	81AA26	81AA26	81AA26	81AA26
Tone High Pass	EF2603	EF2603	EF2603	EF2603	EF2603

11.1.1 Enable Loudness Settings

	Enable Loudness	Bypass Loudness
Loudness Mode	000001	000000

12. High-Pass and Low-Pass Crossover Filters

High-Pass and Low-Pass filter blocks are provided for each of the output channels. These provide a flexible Crossover function for all the output channels, including provision for defining the subwoofer channel's frequency response, if applicable.

Four cascaded filter blocks are available for each channel. Each filter can be configured for low-pass or high-pass operation with adjustable slope and Q. Higher order slopes and bandpass functions can be achieved by using multiple low or high pass filters.

The High and Low Pass blocks operate together, and are implemented as a total of four cascaded elements. Two of the elements are allocated for High Pass, and the other two elements are allocated for Low Pass functionality. However, complete flexibility allows each element to be defined for either High or Low Pass. Each element is selectable for a slope of 6dB, 12dB, 18dB, or 24dB, or can be bypassed. Any or all of the parameters can be defined independently based on system requirements.

The D2 Audio DSP Customization GUI software includes preset options for choosing Butterworth, Bessel, or Linkwitz-Riley filter implementations, and sets the parameters appropriately for these implementations.

Each element within the filter block uses three different parameters, for a total of 12 parameters for the channel's filter function. These three per-element parameter definitions are identical for all elements. These parameters are Filter Configuration, Corner Frequency, and Quality Factor.

Combinations of settings for the individual elements within the filter block determine the block's overall characteristics.

12.1 Corner Frequency

The Corner Frequency parameter is a signed, 24-bit number. The frequency value is entered in Hz. The valid range for the frequency parameter is 10 to 22000Hz.

Note: While it is possible to enter parameter values beyond the specified valid range, only values within this range are actually used during audio processing operation. Values beyond the range specified are not used, and if entered, the processing uses the value shown for the maximum range. For example, the default parameter value is 7FFFFF, corresponding to 24kHz. This is beyond the operational range, and if entered beyond the specified range, audio processing uses the maximum (22kHz) value limit.

12.1.1 Filter Corner Frequency Parameter Calculation

(EQ. 16) $$\text{Frequency Parameter} = 2^{23} \times \left[\frac{F}{24} \times 10^{-3}\right]$$

where F = Frequency in Hz

	Minimum	Maximum
Valid Range	10Hz	22kHz
	000DA7	755555
Default Settings	24kHz	7FFFFF

Note: The default setting of 7FFFFF is beyond maximum operational range of 755555, or 22kHz. Although entry beyond valid range is possible, operation is within valid range. The maximum valid range (22kHz) is assumed for operation. Values beyond this range are ignored and use the maximum 22kHz value instead.

12.2 Quality Factor

The Quality Factor (Q) parameter is a signed, 24-bit number. The valid range for the Q parameter is >0.5 to 10. (Note that a setting of 0.5, producing a parameter value of 800000 is invalid.)

12.2.1 Filter Q-Factor Parameter Calculation

(EQ. 17) $$\text{Q-Factor Parameter} = 2^{23} \times \left[\frac{1}{2 \times Q}\right]$$

	Minimum	Maximum	
Valid Range	0.5^{+}	10	
	7FFFFF	066666	
	(Q>0.5; A value of 0.5 creates a hex value of 800000 which is invalid)		
Default Settings	Q = 0.5412	7641AF	First Biquad Block
	Q = 1.3066	30FBC5	Second Biquad Block

12.3 Configuration Settings

Bit assignments within the Configuration parameter determine whether the block's filter element is active, bypassed, or unused; selects whether the block is a high pass or low pass configuration; and whether it implements a first or second order function. These bit combinations are shown in High/Low Pass Filter Register Addresses.

12.3.1 Filter Configuration Mode Definition

Each High-Pass and Low-Pass filter block is implemented as two biquad elements. The filter slope shown (6dB or 12dB/octave) is for each biquad element only. The total filter block slope of 6dB, 12dB, 18dB, or 24dB/octave is accomplished through combinations of slope selections of each biquad element within the complete filter block.		
Mode Settings	x00000	Low-Pass, Second-Order, 12dB/octave slope
	x00001	Low-Pass, First-Order, 6dB/octave slope
	x00002	High-Pass, Second-Order, 12dB/octave slope
	x00003	High-Pass, First-Order, 6dB/octave slope
	8xxxxx	Bypass
Default Settings	800000	Filter Bypassed.

12.3.2 High/Low Pass Filter Register Addresses

Register Parameter	Channel 1 Address	Channel 2 Address	Channel 3 Address	Channel 4 Address	Channel 5 Address
Low-Pass Biquad 1 Configuration	00007F	00008B	000097	0000A3	0000B1
Low-Pass Biquad 1 Frequency	000080	00008C	000098	0000A4	0000B2
Low-Pass Biquad 1 Damping/Q-Factor	000081	00008D	000099	0000A5	0000B3
Low-Pass Biquad 2 Configuration	000082	00008E	00009A	0000A6	0000B4
Low-Pass Biquad 2 Frequency	000083	00008F	00009B	0000A7	0000B5
Low-Pass Biquad 2 Damping/Q-Factor	000084	000090	00009C	0000A8	0000B6
High-Pass Biquad 1 Configuration	000085	000091	00009D	0000A9	0000B7
High-Pass Biquad 1 Frequency	000086	000092	00009E	0000AA	0000B8
High-Pass Biquad 1 Damping/Q-Factor	000087	000093	00009F	0000AB	0000B9
High-Pass Biquad 2 Configuration	000088	000094	0000A0	0000AC	0000BA
High-Pass Biquad 2 Frequency	000089	000095	0000A1	0000AD	0000BB
High-Pass Biquad 2 Damping/Q-Factor	00008A	000096	0000A2	0000AE	0000BC

13. SRS WOW/HD

The D2-4 (D2-41151) and D2-4P (D2-45157) devices support the SRS WOW/HD audio enhancement algorithms.

For these devices, there are 30 registers supporting SRS WOW/HD. One register initiates change control, and 29 registers control parameter data.

13.1 Configuration Change Register Control

Use the Configuration Change register to initiate changes made by any of the TruSurround registers. At completion of any writes to any of the TruSurround registers, the Configuration Change register must be set to 1. It is cleared and reset to 0 by the SRS WOW/HD algorithms at completion of the change initiation. Any number of registers can be changed in any order. Their changes are not passed to the internal algorithms until after initiated by the Change Configuration register change bit.

When any of the 29 parameter data registers for SRS WOW/HD are written with new data, that data is not immediately passed to the SRS algorithms and no audio processing change occurs. Because of the need for synchronous and controlled updating of inter-related parameters, they update only when triggered by setting the Configuration Change register. This configuration allows smooth and uninterrupted audio flow when any change occurs to the SRS WOW/HD functionality.

Any writes to any of the SRS WOW/HD registers must be followed by setting the Change Control register bit as the last write instruction of the sequence. It is not necessary to write this bit after every change, only that it occurs after completion of all the changes made at that time.

13.2 Mode Enable Registers

Use these registers to enable or disable operating modes.

Function	Register Address	Parameter Setting		Parameter Default Setting	
		Enabled	Disabled	Value	Setting
Configuration Change Control	000148	Parameter Change Initiated With Bit0 = 1			
SRS WOW/HD Enable	000149	000001	000000	000000	Disabled
SRS TruBass Front Enable	00014C			000000	Disabled
SRS TruBass Subwoofer Enable	00014D			000000	Disabled
Definition Front Enable	00014E			000000	Disabled
Definition Center Enable	00014F			000000	Disabled
Dialog Clarity Enable	000150			000000	Disabled
SRS WOW/HD 3D Enable	000151			000000	Disabled
SRS WOW/HD 3D High Bit Rate Enable	00015E			000000	Disabled
SRS WOW/HD 3D Focus Enable	00015F			000000	Disabled
SRS WOW/HD 3D Limiter Enable	000160			000000	Disabled

13.3 SRS Adjustment Registers

Use these registers to make variable adjustments.

Function	Address	Minimum Setting		Maximum Setting		Default Setting	
		Value	Data	Value	Data	Value	Data
SRS WOW/HD Surround Level Control	000152	-100dB	000054	0 dB	7FFFFF	-4.5dB	4CCCCD
SRS WOW/HD Input Gain Control	000153	-100dB	000054	0 dB	7FFFFF	-6dB	400000
SRS WOW/HD Output Gain Control	000154	-100dB	000054	0 dB	7FFFFF	0dB	7FFFFF
SRS WOW/HD Bypass Gain Control	000155	-100dB	000054	0 dB	7FFFFF	-3dB	5AE148
Definition Front Adjustment Control	000156	0	000000	1	7FFFFF	0.3	266666
Definition Center Adjustment Control	000157	0	000000	1	7FFFFF	0.3	266666
Dialog Clarity Adjustment Control	000158	0	000000	1	7FFFFF	0.5	400000
SRS TruBass Front Adjustment Control	000159	0	000000	1	7FFFFF	0.3	266666
SRS TruBass Subwoofer Adjustment Control	00015A	0	000000	1	7FFFFF	0.3	266666
SRS WOW/HD 3D Space Adjustment Control	000162	0	000000	1	7FFFFF	0.8	666666
SRS WOW/HD 3D Center Adjustment Control	000163	0	000000	1	7FFFFF	0.5	400000
SRS WOW/HD 3D Focus Adjustment Control	000164	0	000000	1	7FFFFF	0.4	333333
SRS WOW/HD 3D Limiter Adjustment Control	000165	0	000000	1	7FFFFF	0.75	600000

13.3.1 SRS Gain Adjustment Parameter Calculations

Applies to: SRS WOW/HD Surround Level Control
SRS WOW/HD Input Gain Control
SRS WOW/HD Output Gain Control
SRS WOW/HD Bypass Gain Control

(EQ. 18) $$\text{Gain Adjustment Parameter} = \left[2^{23} \times 10^{\left(\frac{\text{Gain}}{20}\right)}\right]$$

where Gain is in dB and is a negative (or zero) term.

	Minimum	Maximum	
Valid Range	-100dB	0dB	
	FFFFAC	800000	
	000000		Signal Path Cut-Off

13.3.2 SRS Adjustment Parameter Calculations

Applies to: Definition Front Adjustment Control
Definition Center Adjustment Control
Dialog Clarity Adjustment Control
SRS TruBass Front Adjustment Control
SRS TruBass Subwoofer Adjustment Control
SRS WOW/HD 3D Space Adjustment Control
SRSWOW/HD 3D Center Adjustment Control
SRS WOW/HD 3D Focus Adjustment Control
SRS WOW/HD 3D Limiter Adjustment Control

(EQ. 19) $$\text{Adjustment Parameter} = [2^{23} \times (\text{Setting Adjustment})]$$

where:“Setting Adjustment” is a numerical adjustment value from 0 to 1.

	Minimum	Maximum
Valid Range	0	1
	000000	7FFFFF

13.4 SRS WOW/HD 3D Mode Select Register

Setting Selection	Register Address	Parameter Setting	
	000161		
3d Stereo		000002	(Default)
Extreme		000003	

13.5 SRS WOW/HD Input Mode Select Register

Input Mode	Register Address	Parameter Setting	
	00014A		
1-0-1		000000	
2-0-1		000001	(Default)
2-1-1		000002	
2-2-1		000003	
3-0-1		000004	
3-1-1		000005	
3-2-1		000006	
3-3-1		000007	
Lr Rt		000008	
3-2-1 BS Digital		000009	
PL2 Music		00000A	
CSII		00000B	

13.6 SRS WOW/HD Output Mode Select Register

Output Mode	Register Address	Parameter Setting	
	00014B		
Headphone		000043	
2-0-0		000003	(Default)
2-0-1		000023	
2-2-0		00000F	
2-2-1		00002F	
3-0-0		000013	
3-1-0		000033	
3-2-0		00001F	
3-2-1		00003F	

13.7 SRS TruBass Speaker Size Select Register

Speaker Size (Frequency, Hz)	Register Address	Parameter Setting	
	00015B	Front Speaker	
	00015C	Subwoofer Speaker	
40		000000	(Subwoofer Default)
60		000001	
100		000002	
150		000003	(Front Default)
200		000004	
250		000005	
300		000006	
400		000007	

13.8 SRS TruBass Crossover Frequency Select Register

Crossover Frequency (Hz)	Register Address	Parameter Setting	
	00015D		
80		000000	(Default)
120		000001	
160		000002	
200		000003	

14. Signal Flow Option Register

The Signal Flow Option register is a single 24-bit control word that controls optional signal flow components. The register and its bit assignments are described below.

Defined Bits: Only 9 bits (bits 8:0) are defined and implemented in normal device operation.

Unused Bits: Bits 23:9 are not used and reserved. The unused bits should always be written as (0) zero.

Bit Function Definitions: Each of the 9 defined bits specify whether their assigned function is active. If the bit is zero, the function is bypassed, and if the bit is a one, the function is active.

Signal Flow Option Default Setting: The Signal Flow Option register default bit settings are:

- 0x0000FF (hex)

Signal Flow Option Register Address: The Signal Flow Option register is located at address:

- Address 0x000166 (hex)

Table 5. D2-4 Signal Flow Register

Register Bits [23:0]																							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved Bits; Default = all 0															Default Bit Settings of defined bits:								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
															See Table 6 for bit definitions.								

Table 6. Signal Flow Register Bit Definitions

Bit	Name	Function
0	Sound Enhancement Algorithms	Enables Sound Enhancement algorithms when = 1. When set = 0, bypasses all Sound Enhancement Algorithm functions. (Regardless of bit setting, these Sound Enhancement Algorithms are only enabled on the Sound Enhancement Algorithm -specific (D2-4/D2-41051 and D2-4P/D2-45057) hardware-enabled licensed assignment of those specific device part number.)
1	SRS Algorithms	Enables SRS algorithms when = 1. When set = 0, bypasses all SRS functions. (Regardless of bit setting, these SRS algorithms are only enabled on the SRS-specific (D2-4/D2-41151 and D2-4P/D2-45157) hardware- enabled licensed assignment of those specific device part number.)
2	(Reserved)	Reserved. Default = 1. However, function is not enabled within any production D2-4 or D2-4P hardware. Writing of either 0 or 1 is ignored.
3	(Reserved)	Reserved. Default = 1. However, function is not enabled within any production D2-4 or D2-4P hardware. Writing of either 0 or 1 is ignored.
4	Input Compressors	Enables audio processing path Input Compressors when = 1. Bypasses Input Compressors when = 0.
5	Speaker EQ	Enables Speaker EQs in audio processing path when = 1. Bypasses Speaker EQs when = 0.
6	Output EQ	Enables Output EQs in audio processing path when = 1. Bypasses Output EQs when = 0.
7	Green Function	Enables Green Function when = 1. Disables Green Function when = 0.

Table 6. Signal Flow Register Bit Definitions (Continued)

Bit	Name	Function
8	Master Volume Off	Master Volume zero-setting PWM shutdown. When set = 1, setting the Master Volume to minimum invokes PWM shutdown, through Green Function. When = 0, PWM shutdown not affected by Master Volume.

15. Hardware Option Register

The Hardware Option register is a single 24-bit control word that enables hardware features on the device. The register and its bit assignments are described below.

Defined Bits: Only 13 bits (bits 12:0) are defined and implemented in normal device operation.

Unused Bits: Bits 23:13 are not used and reserved. The unused bits should always be written as (0) zero.

Bit Function Definitions: Each of the 13 defined bits control their respective feature. If the bit is zero, the feature is disabled, and if the bit is a one, the feature is active.

Hardware Option Default Setting: The Hardware Option register default bit settings are:

- 0x00027F (hex)

Hardware Option Register Address: The Hardware Option register is located at address:

- Address 0x000167 (hex)

Table 7. D2-4 Hardware Register

Register Bits [23:0]																							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved Bits; Default = all 0											Default Bit Settings of defined bits:												
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1
											See Table 8 for bit definitions.												

Table 8. Hardware Option Register Bit Definitions

Bit	Name	Function
0	Master Volume	Enables Master Volume control when = 1. When set = 0, Master Volume setting ignored.
1	Mute Input	Enables Mute Input when = 1. When set = 0, Mute Input ignored.
2	SPDIF TX	Enables SPDIF Transmit output when = 1. When set = 0, SPDIF Transmit disabled.
3	Host Error	Enables Host Error output when = 1. When set = 0, Host Error output disabled.
4	Temperature Sense	Enables Temperature Sensor when = 1. When set = 0, Temperature Sensor ignored.
5	PSSYNC	Enables Power Supply Sync (PSSYNC) output when = 1. When set = 0, PSSYNC disabled.
6	Master Clock	Enables Master Clock (MCLK) output when = 1. When set = 0, MCLK disabled.
7	SPDIF Pass	Enables SPDIF Pass Through when = 1. When set = 0, SPDIF Pass Through disabled. (The SPDIF Pass Through function overrides the SPDIF input source selection.)
8	PSSYNC Rate 0	When set = 1, and when bit 5 (PSSYNC) is also enabled set = 1, PSSYNC operates at 2x the PWM switch rate. (Only 1 of these 3 PSSYNC rate bits should be set = 1 at one time, and the other 2 should be set = 0.)
9	PSSYNC Rate 1	When set = 1, and when bit 5 (PSSYNC) is also enabled set = 1, PSSYNC operates at 1x the PWM switch rate. (Only 1 of these 3 PSSYNC rate bits should be set = 1 at one time, and the other 2 should be set = 0.)
10	PSSYNC Rate 2	When set = 1, and when bit 5 (PSSYNC) is also enabled set = 1, PSSYNC operates at 1/2 (half) the PWM switch rate. (Only 1 of these 3 PSSYNC rate bits should be set = 1 at one time, and other 2 should be set = 0.)
11	PSSYNC Duty	When set = 0 PSSYNC output (when enabled) operates at 50% duty cycle. When set = 1, (and when enabled) PSSYNC operates at a 10% duty cycle.

Table 8. Hardware Option Register Bit Definitions (Continued)

Bit	Name	Function
12	DspStop	Setting = 1 stops DSP clocks in the background wait loop. When set = 0, DSP clocks operate normally.

16. Revision History

Rev.	Date	Description
0.00	Jun.4.19	Initial release

Notice

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