R2A20114A Series

Application Note

R03AN0007EJ0300
Rev.3.00
May 15, 2014

1. Introduction

R2A20114A series is a boost converter control IC with PFC (Power Factor Correction).
Especially in case that the difference in input and output voltage is small, R2A20114A will improve harmonic current characteristics compared to conventional R2A20114.

Employing continuous conduction mode (CCM) interleaving PFC, it performs higher efficiency and lower switching noise even for high power mode. So that, it can be applicable for a variety of applications. Interleaving control of the boost converters, namely, producing 180 degrees phase shift between the output signals (GD1,2) driving the boost converters, enables the system to perform high conversion efficiency and low switching noises and, at the same time, to reduces ripple currents in input and output current and then this allows use of smaller components such as boost inductors, input filters and output capacitors.

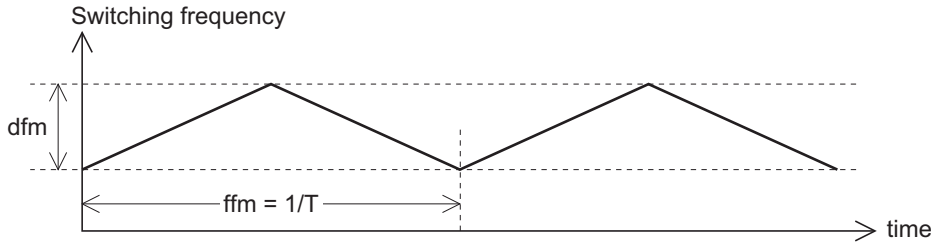
The R2A20114A is a type of the current sensing by shunt resistor. The shunt resistor is suitable for the application in the air conditioner field.
The two mode over voltage protection, over current protection are built in the R2A20114A, and can constitute a power supply system of high reliability with few external parts.

2. Product Lineup and Feature

Table 1 R2A20114A Product Lineup and Function List

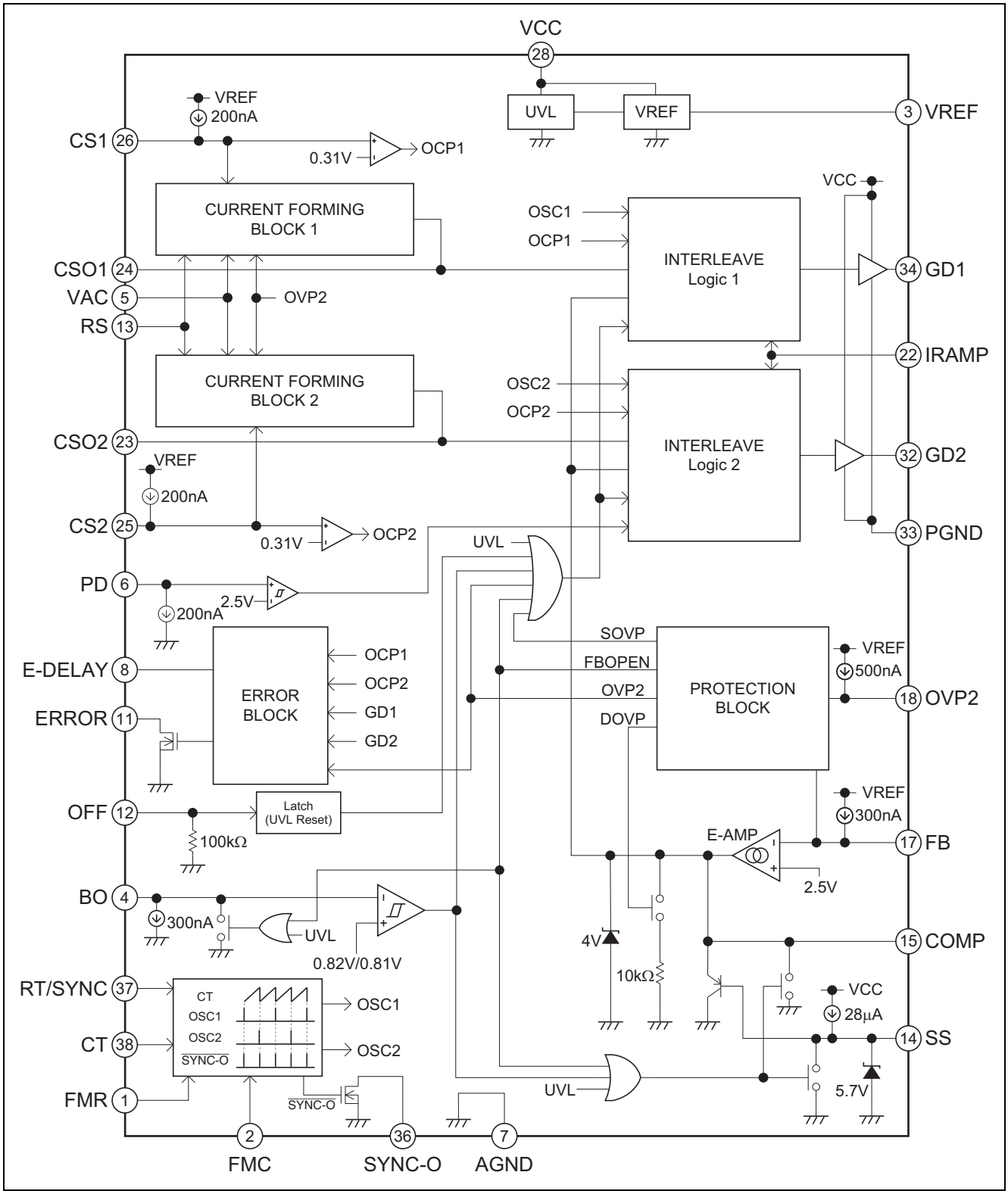
Item		R2A20114ASP	R2A20114AFP
PFC control		Continuous conduction mode interleaving	
Current detection method		Shunt resistor	
Package		SOP-20	LQFP-40
Protection circuits	Brownout detection	Supported	Supported
	2nd OVP	Not supported	Supported
	Phase error	Not supported	Supported
Noise reduction	Jitter generation (frequency modulation)	Supported (But, frequency modulation period (dfm)*1 is fixed)	Supported
Synchronization with external signal	Input	Supported	Supported
	Output	Not supported	Supported
Efficiency improvement	Phase drop	Not supported	Supported

Note: *1 Refer to the figure depicted below:

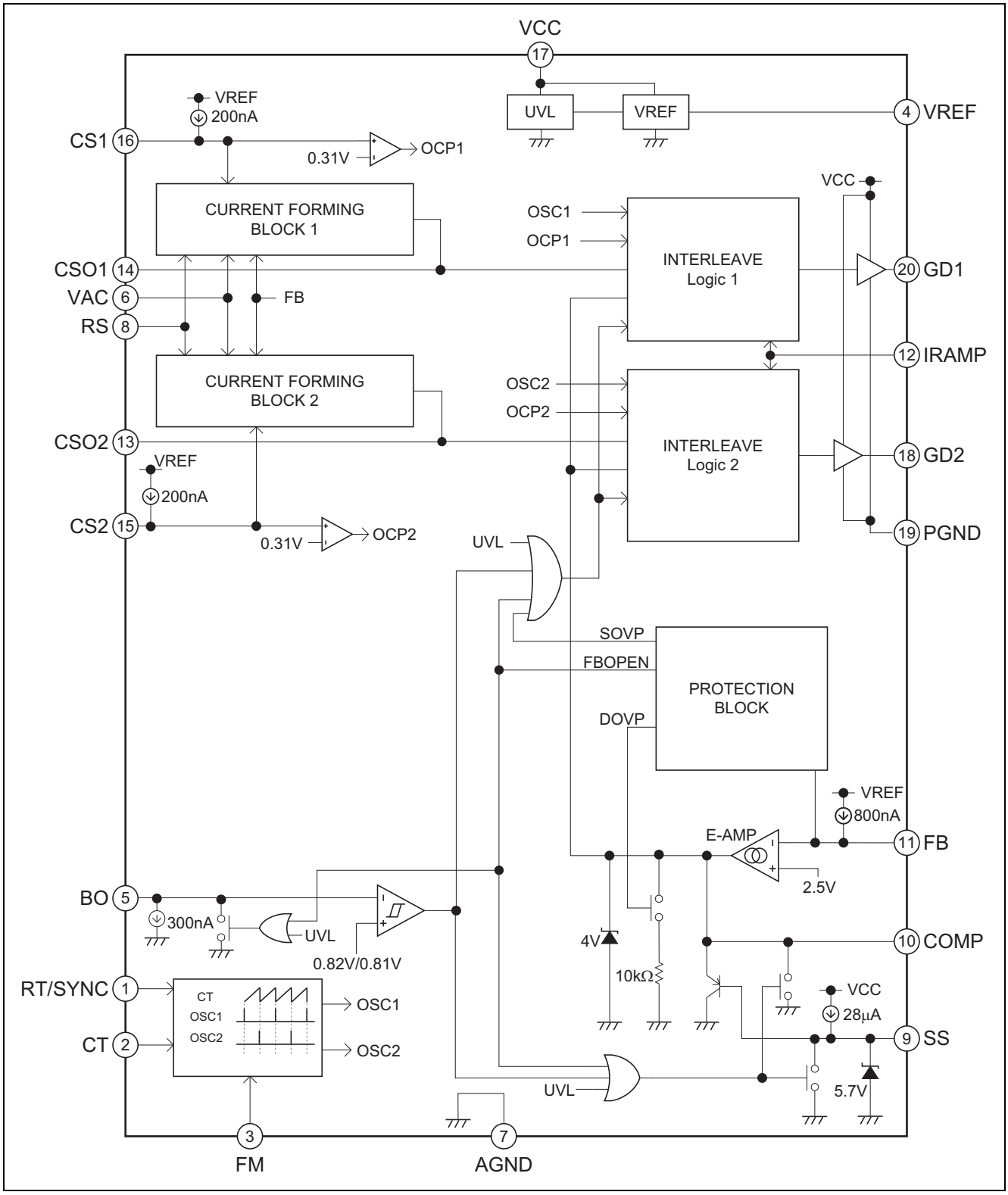


3. Block Diagram

3.1 R2A20114AFP Block Diagram (LQFP-40)



3.2 R2A20114ASP Block Diagram (SOP-20)



4. Descriptions of the R2A20114A Functional Blocks

4.1 Protection

The over voltage protection, the over voltage protection 2, the over current protection and the feedback open loop protection are available.

4.1.1 Over Voltage Protection (OVP)

The over voltage protection has two step protections. Dynamic over voltage protection (D-OVP) discharges COMP pin voltage when FB pin voltage reaches 1.04 × VFB (2.5 V typ). The Power MOSFET on time is limited gradually, therefore the audio noise is avoided because an inductor current does not stop suddenly. Static over voltage protection (S-OVP) stops an GD signal when FB pin voltage reaches 1.08 × VFB (2.5 V typ). A Power MOSFET turns off quickly and S-OVP keeps stopping an GD signal till FB pin voltage reaches 1.08 × VFB (2.5 V typ) – 0.08.

4.1.2 Over Voltage Protection 2 (OVP2)

The special pin that is individual from OVP senses the PFC output voltage.

When OVP2 pin becomes 1.08 × VFB (2.5 V typ), a switching stops.

4.1.3 Feed Back Open Loop Detection

The feedback open-loop protection discharges COMP pin voltage during FB pin voltage is under 0.5 V.

Therefore an GD signal does not appears in this case. There is 0.2 V hysteresis.

4.1.4 Over Current Protection (OCP)

CS pin senses the each Power MOSFET drain current by using an external sense resistor. In case of R2A20114A, when CS1 or CS2 pin reaches 0.31 V, an GD signal is disable.

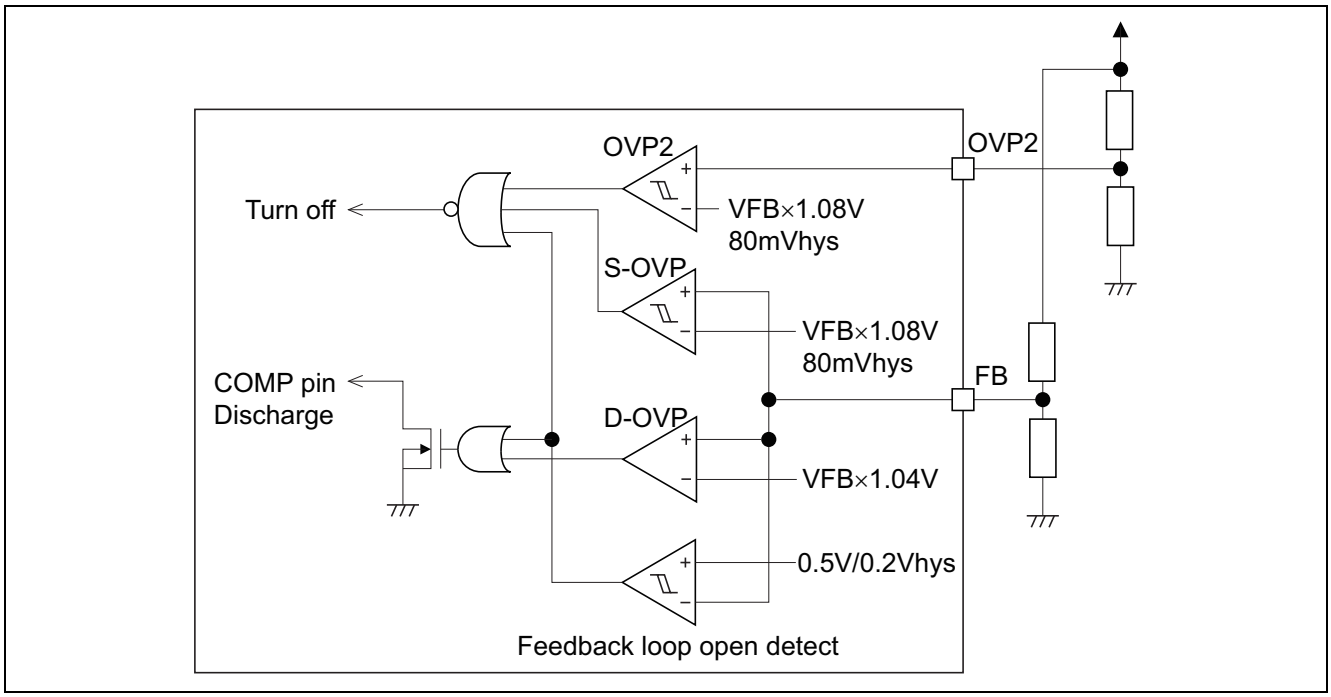


Figure 1

4.2 Drive Stage

The R2A20114A contains two totem-pole output stages for phase1 and phase2.
The source drivability is 100 mA peak and the sink drivability is 1.0 A peak.
If the Qg of Power MOSFET is large or the distance between IC and Power MOSFET is long, please adjust a drive ability according to the characteristics of using Power MOSFET.

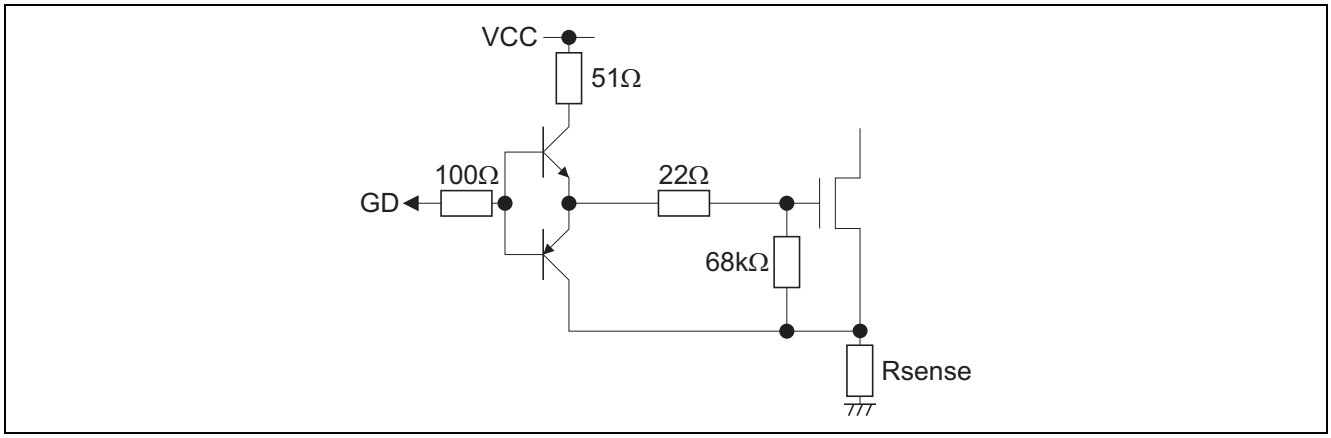


Figure 2 Driver Example

4.3 Soft Start

ON time increase gradually by connecting capacitor between SS pin and GND.
SS pin charge current is 28 µA constant current , and SS time is adjustable by changing capacitor value.
SS pin discharge the capacitor when VCC is under UVLO threshold voltage or FB voltage is under 0.5 V or BO voltage is under 0.81 V.

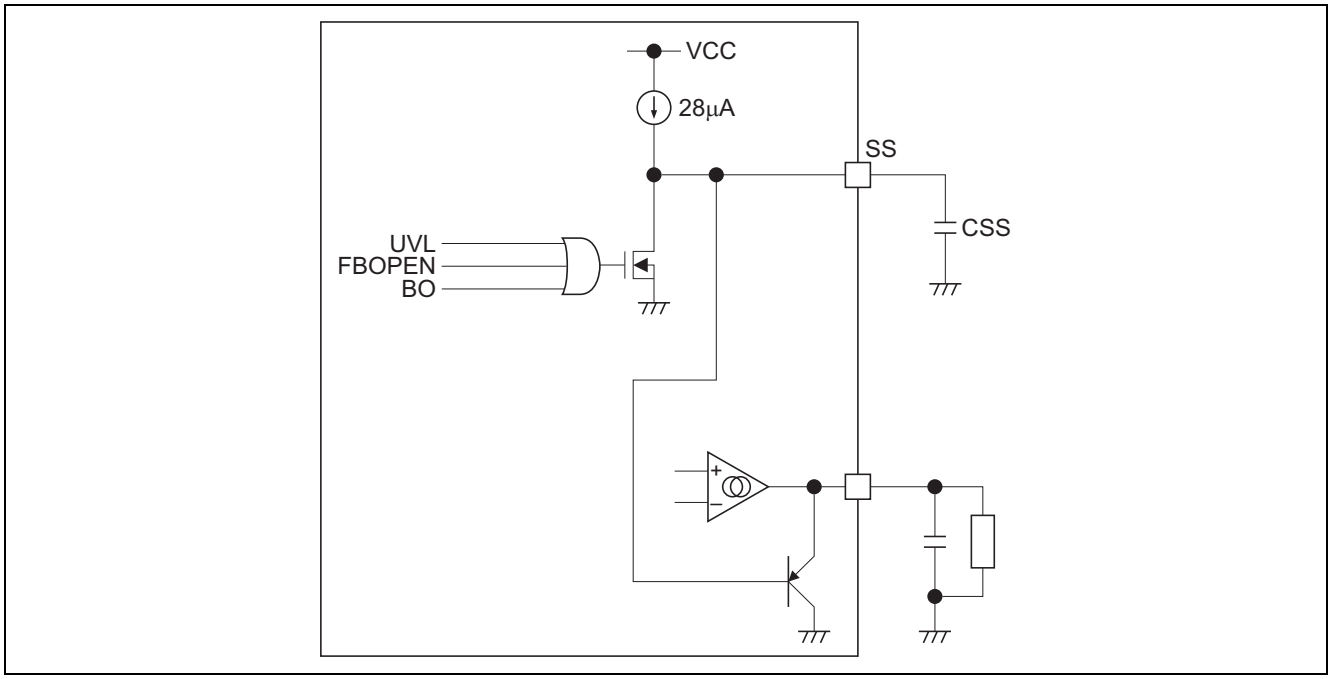


Figure 3

4.4 Phase Drop (R2A20114AFP)

When the PD signal becomes 2.5 V or more, GD2 stops in order to improve efficiency at light load.

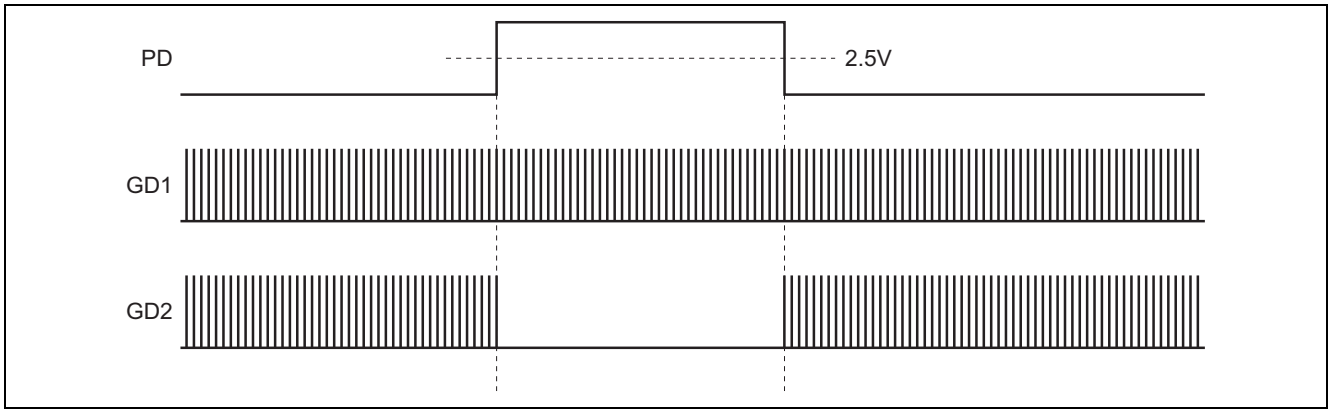


Figure 4

R2A20114A prevents output voltage from overshooting / undershooting by controlling slope of internal RAMP signal.

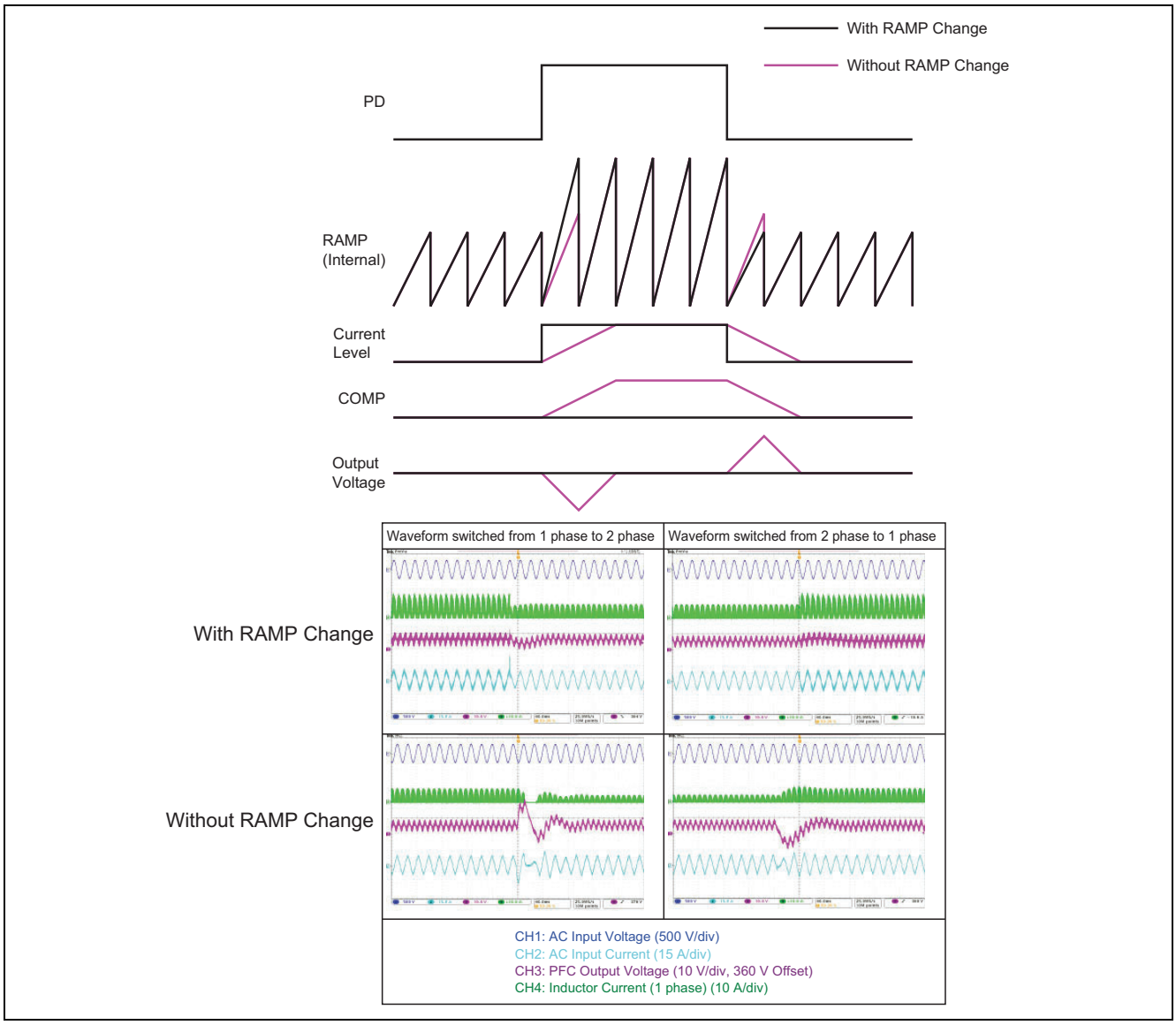


Figure 5

4.5 ERROR Function (R2A20114AFP)

The block diagram of the ERROR pin is shown as follows.
The IC latch can operate when the error occurs by connecting 'ERROR' pin with 'OFF' pin.
When the ERROR pin detects E-DELAY, Phase Error, and OVP2, the ERROR pin is high.

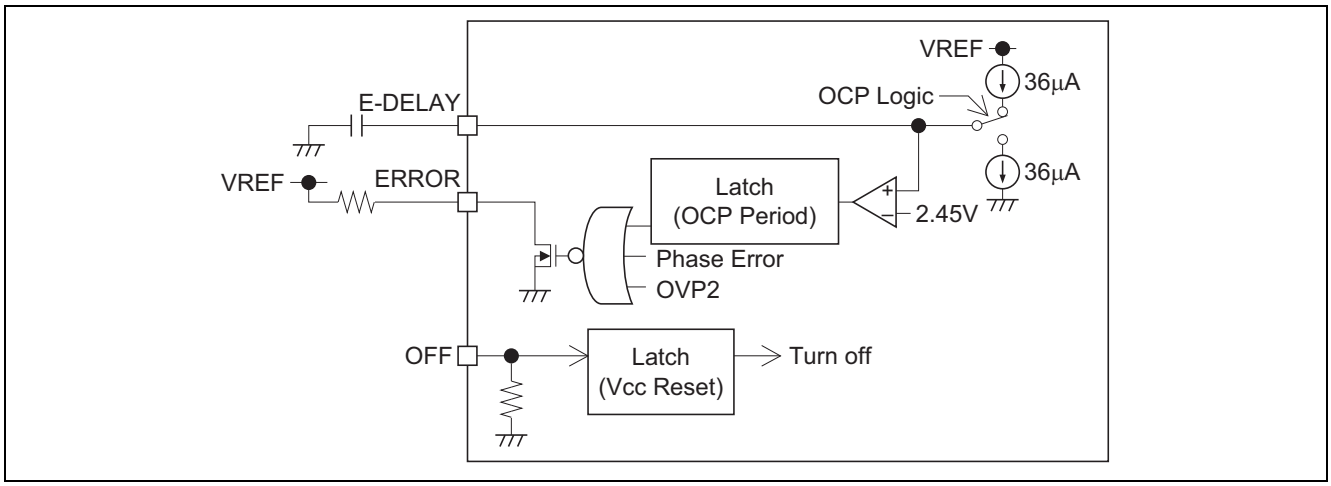


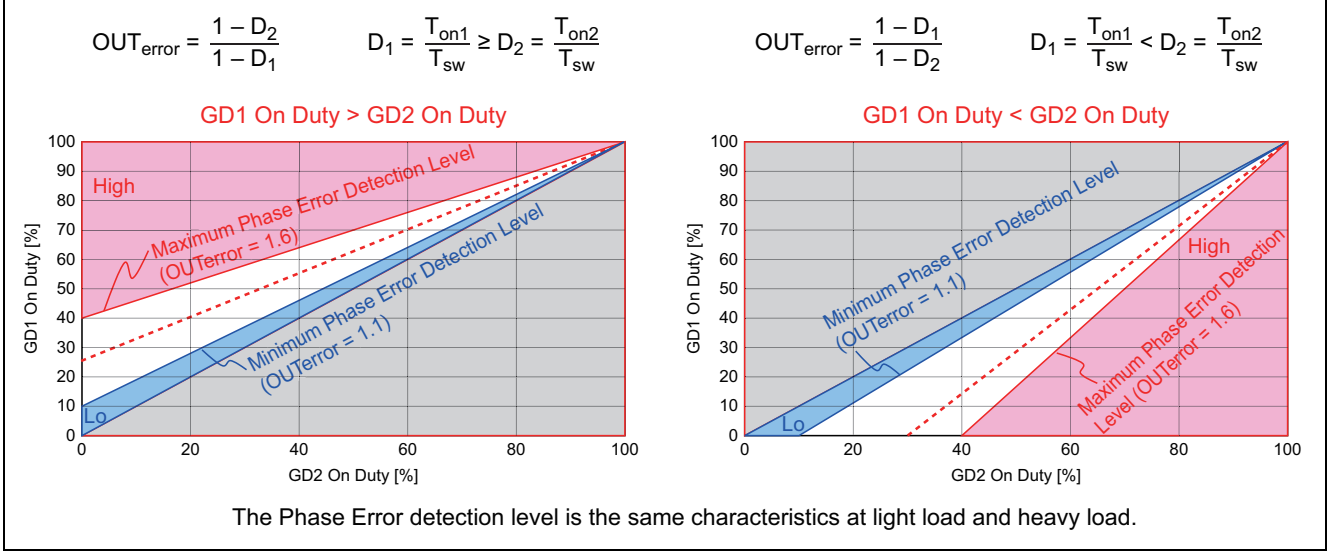
Figure 6

4.5.1 Error Pin Movement by Overvoltage Protection Detection 2 (OVP2)

When an OVP2 pin voltage becomes it than 1.08 × VFB[V], the output of GD1,2 stops. The ERROR pin outputs High meaning abnormality at the same time. When an OVP2 pin voltage becomes less than 1.08 × VFB (2.5 V typ) – 0.08[V], GD1,2 is output again, and the ERROR pin becomes Lo from Hi.

4.5.2 Error Pin Movement by the Phase Error Detection

When the duty ratio of GD1,2 becomes large by abnormal movement such as the open/short destruction of the power element, the ERROR pin detects the duty ratio and outputs High meaning abnormality (a phase error). The ERROR pin changes from Hi to Lo again, when the duty ratio of GD1,2 becomes small. The change area of the phase error is shown below.

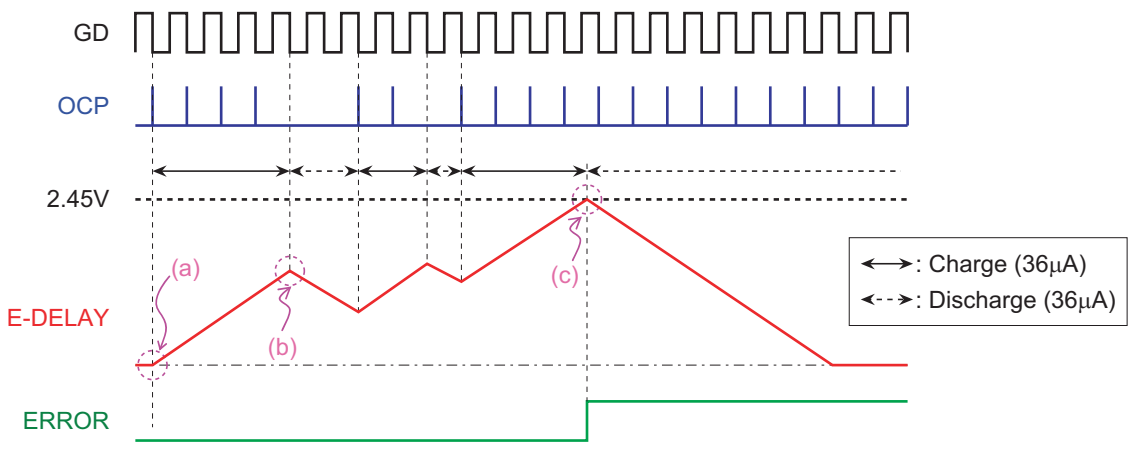


The Phase Error detection level is the same characteristics at light load and heavy load.

Figure 7

4.5.3 Error Pin Movement by the OCP Timer Latch (E-Delay) Detection

When an E-DELAY pin reaches 2.45 V because an over current protection circuit continues working, the ERROR terminal outputs High. After released from over current condition, the error signal becomes Low.



(a) The E-DELAY starts charge mode when OCP is detected.
(b) If OCP will not be detected by GD is turned off, the E-DELAY change from charge to discharge mode.
(c) The error signal becomes 'High' when reaching the threshold 2.45V of the E-DELAY.
The E-DELAYstarts discharge mode.

Figure 8

4.6 OFF Function (R2A20114AFP)

When OFF terminal is pulled up over 4 V (typ.), GD pulse is stop in latch mode. This latch mode is reset Vcc terminal voltage when Vcc voltage is under UVLO Turn-off Threshold voltage.

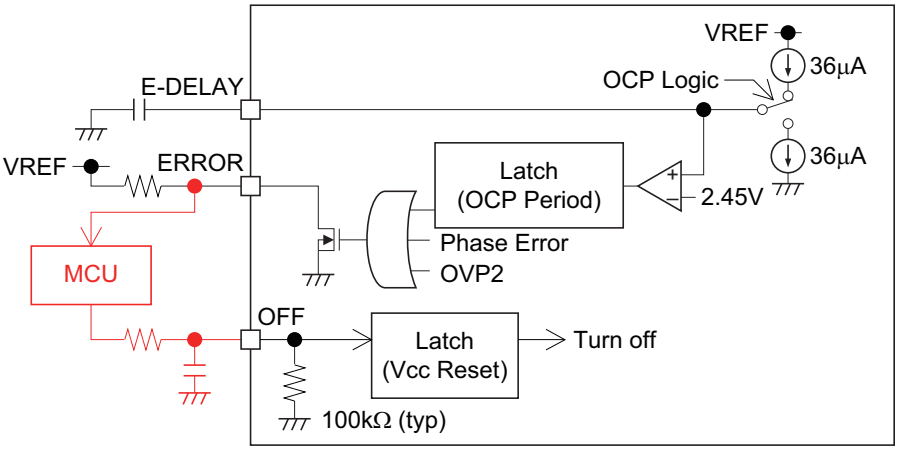


Figure 9

It is possible to stop in the latch mode when the ERROR signal is output by using the ERROR function and OFF function. However, ERROR signal may occur during transient operation (starting up, changing load and Instantaneous Voltage Drop, etc.). IC may stop in the latch mode by the transient ERROR signals when directly connecting between the OFF and ERROR pin. Please mask the ERROR signal by using the microcontroller or the like.

Because OFF function responds with signal of about 10 ns, please use noise filter to prevent malfunction. However, because OFF pin is pulled down by resistor of 100 kΩ(typ), please note the resistance value of the external noise filter to be operated OFF function.

4.7 Synchronous Function

R2A20114A switches synchronous mode by inputting Synchronous Signal into RT/SYNC terminal. Synchronous signal is rise edge trigger operation and GD becomes low by rise edge trigger.

Synchronous mode is latch mode. This latch mode is reset Vcc terminal voltage when Vcc voltage is under UVLO Turn-off Threshold voltage.

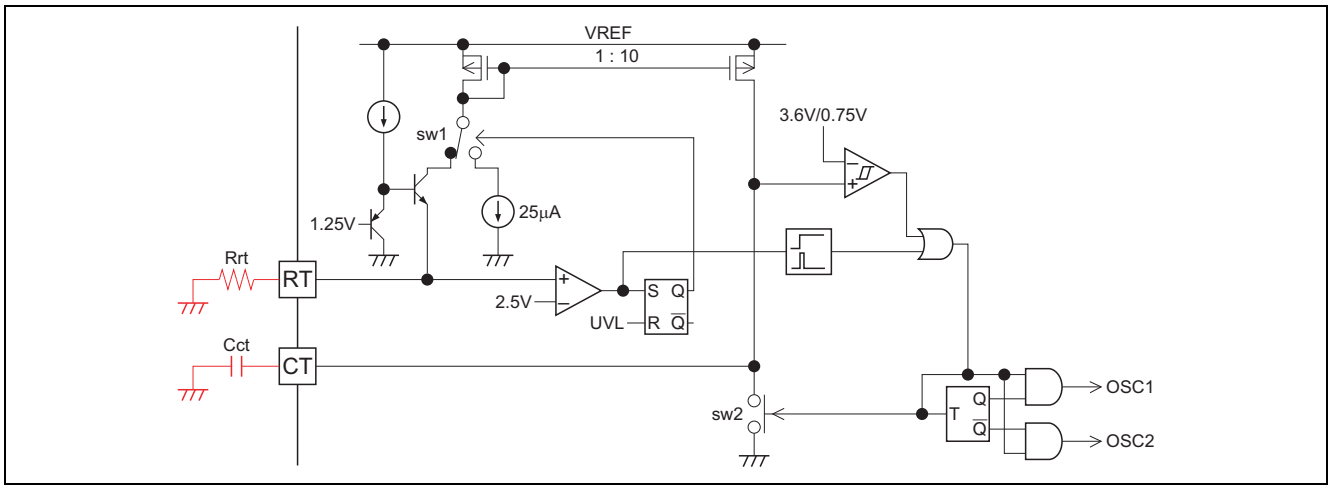


Figure 10 Synchronous Block Diagram

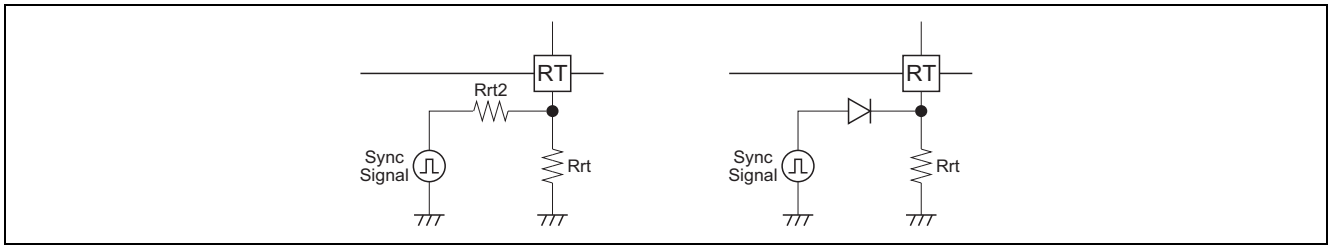


Figure 11 Example of Synchronous Circuits

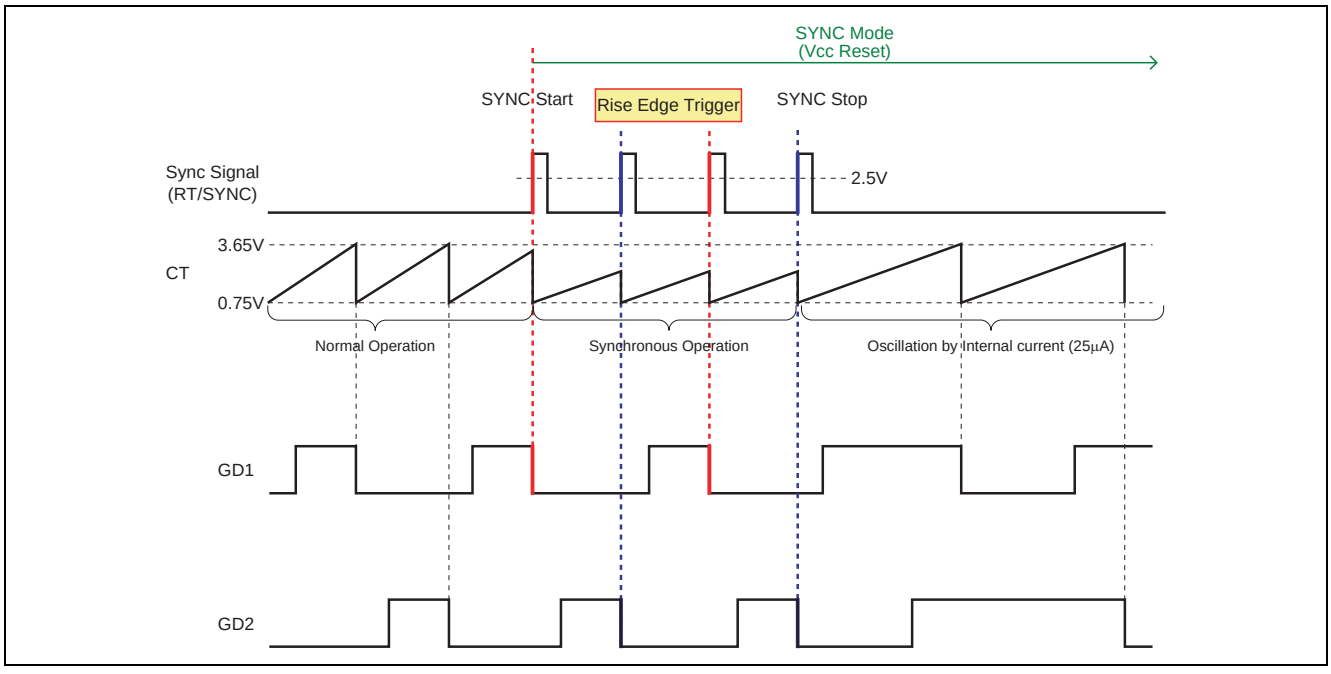


Figure 12 Synchronous Operation

4.8 Synchronous Output Function (R2A20114AFP)

SYNC-O terminal outputs signal to synchronize CT terminal voltage.

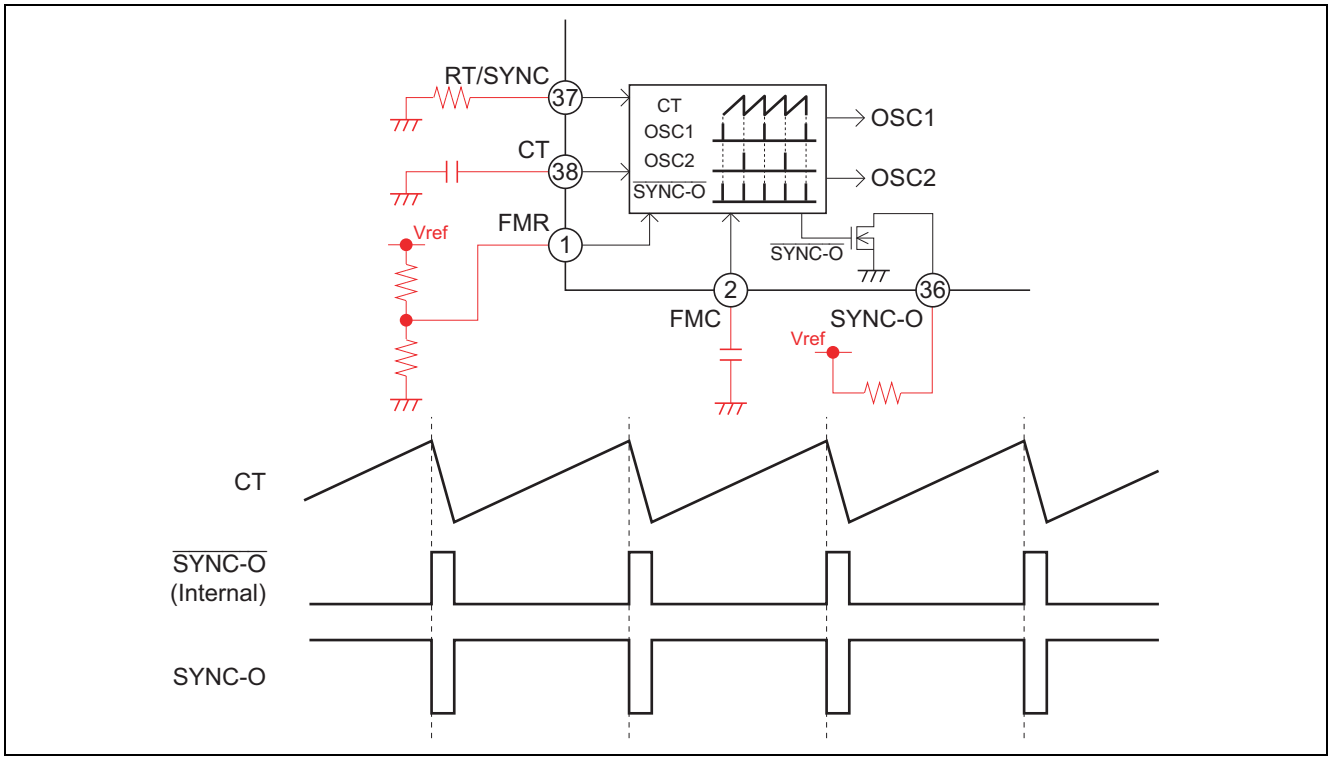


Figure 13

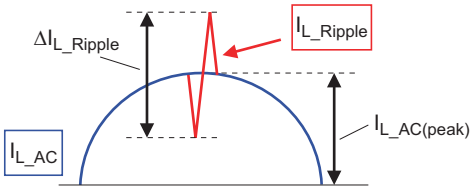
5. Design Guide

Note: * Calculation sheet of excel is available.

5.1 Boost Inductor

The boost inductor value is determined by an output power and a fixed switching frequency.
A switching frequency must become over 20 kHz which is audio frequency to avoid audio noise of an inductor or an input capacitor. Generally it is around 50 kHz.
The boost inductor value is obtained by Equation 1. A conduction loss η input around 0.9.

$$L = \frac{2 \times V_{AC(min)}^2 \times (V_{out} - \sqrt{2} \times V_{AC(min)}) \times \eta \times F_{PFC}}{\gamma \times f_{GD} \times P_{out(max)} \times V_{out}} \quad (1)$$



$$\gamma = \frac{\Delta I_{L\_Ripple}}{I_{L\_AC(peak)}} \quad (2)$$

$V_{AC(min)}$: Effective value of minimum input voltage [V(rms)]
V_{out}: Output voltage [V]
$P_{out(max)}$: Maximum output power [W]
η: Efficiency
F_{PFC}: Power Factor
f_{GD}: fixed switching frequency[Hz]

ΔI_{L_Ripple}: Maximum ripple current of Boost inductor
$I_{L\_AC(peak)}$: Peak current of Boost inductor

5.2 Output Capacitor

The necessary capacitor value to guarantee voluntary hold-up time is expressed in the next equation.

$$C_{out}\ [F] \geq \frac{2 \times P_{out} \times t_{hold}}{V_{out}^2 - V_{out(min)}^2} \quad (3)$$

t_{hold} [s]: Hold-up time
$V_{out(min)}$ [V]: Minimum output voltage

5.3 Power MOSFET (IGBT) and Boost Diode

A peak current flowing on a Power MOSFET (IGBT) or a boost diode is expressed in the next equation. A conduction loss η input around 0.9.

$$I_{in} = \frac{P_{out}}{V_{AC(min)} \times \eta \times F_{PFC}} \quad (4)$$

$$I_{L(peak)} = (1 + \gamma/2) \times I_{in} / \sqrt{2} \quad (5)$$

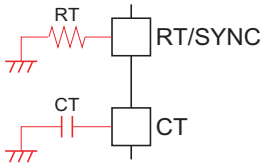
I_{in}: Effective value of Maximum input current
$I_{L(peak)}$: Peak current of Boost inductor

5.4 Operating Frequency

5.4.1 Operating Frequency Setting

The R2A20114A operating frequency f_{GD} is determined by adjusting the timing resistor R_T (the R_T pin, pin 1 of SOP-20 or pin 37 of LQFP-40) and the timing capacitance C_T (the C_T pin, pin 2 of SOP-20 or pin 38 of LQFP-40). The operating frequency is approximated by the following expression.
The expression (6) is the formula that was similar so that an error of the range of each capacity value and the resistance value of figure 14.
Therefore, the calculation result of the expression (6) does not completely accord with the real frequency.
More correct value is calculated by Excel Calculation Sheet, because Excel Calculation Sheet use more complex formula.

$$f_{GD} = \frac{2.5}{R_T \times C_T} \quad (6)$$



It is necessary to select a 7 kΩ or more resistance because of the maximum rating of the RT-pin, due to meet Maximum RT current is less than 200 µA. If it use FM function, RT current will be large. It is necessary to check RT current specification. Also, use a 100 pF or more for the timing capacitance to reduce effects from parasitic capacitance and noise.
As a reference, the operating frequency data when the timing resistor and the timing capacitance are changed is shown in the figure below.

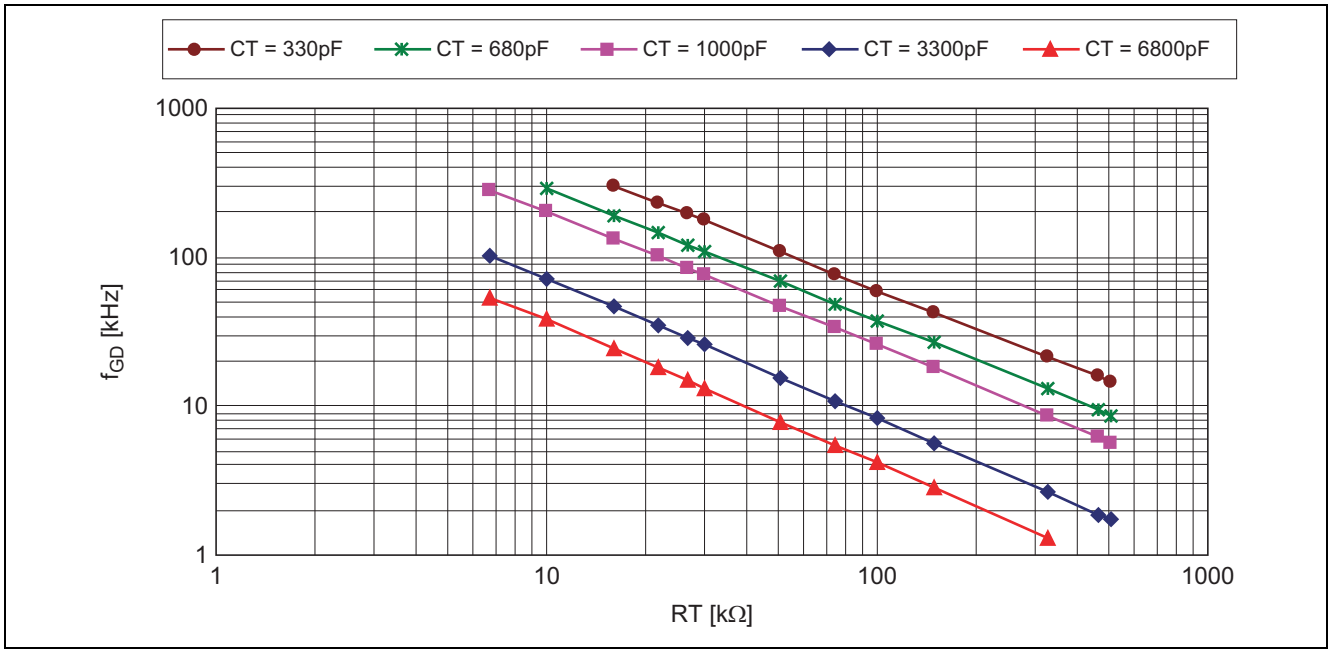


Figure 14 Operating Frequency Characteristics

5.4.2 A Method to Limit Max Duty of GD

By the setting of the drive circuit, On Duty becomes a little less than 100% value in zero cross of input voltage for the delay of the MOS gate. As a result, there is the case that the input current of zero cross is not normal like figure 15. When such a waveform occurred, Max Duty is limited by connecting resistance between Vref and CT, and an input current waveform is improved.

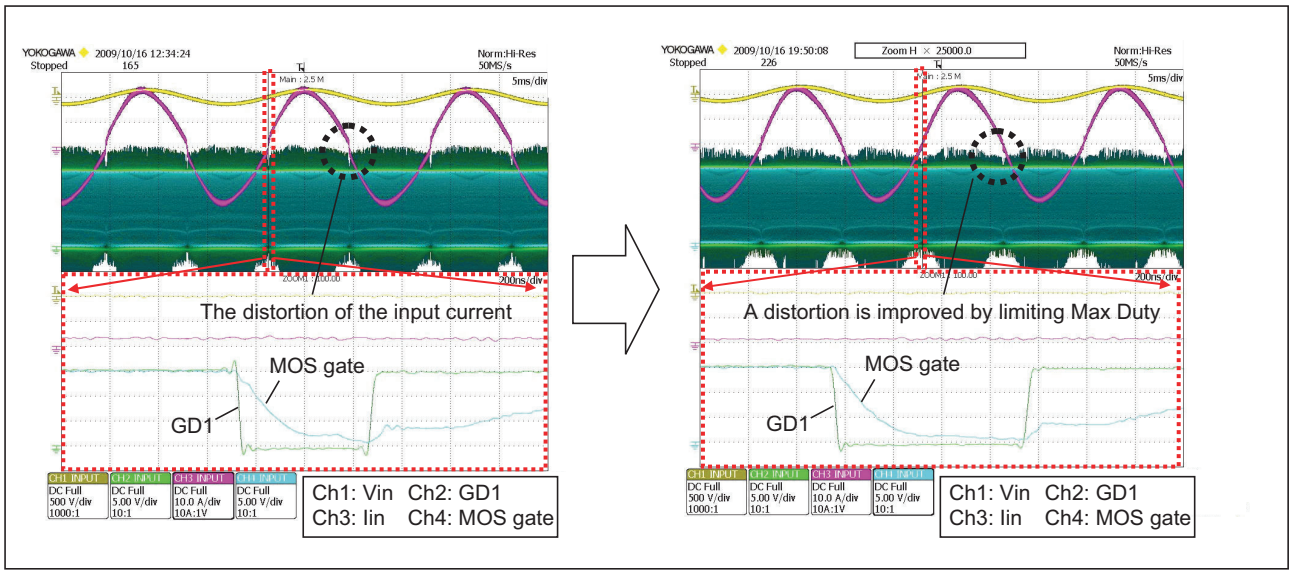


Figure 15-1 The input current waveform with the distortion

Figure 15-2 An input current waveform after Max Duty limit

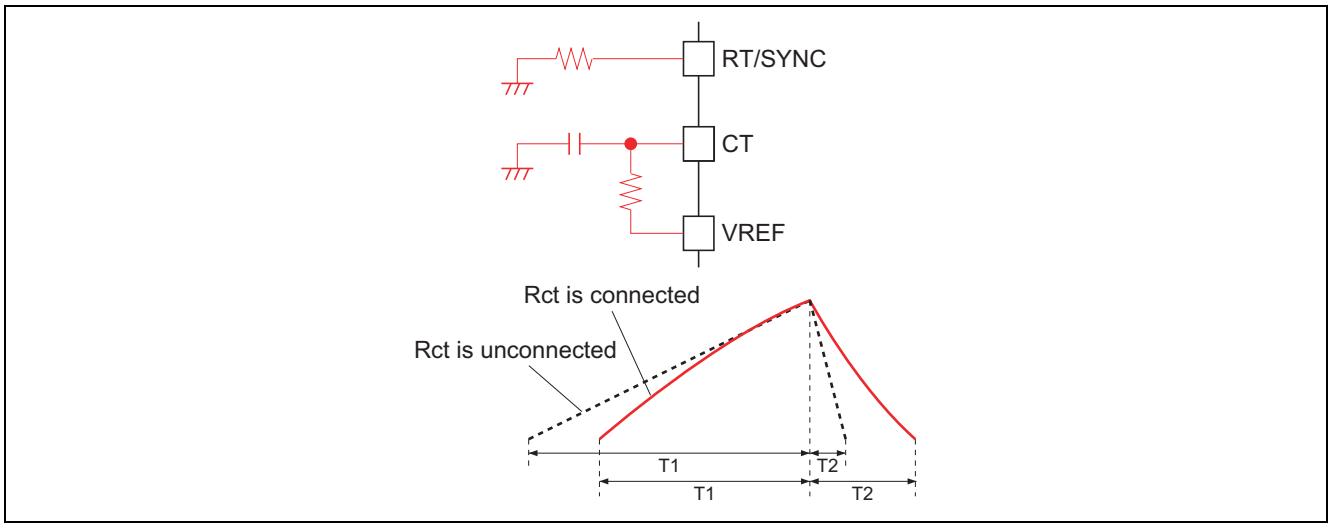


Figure 16 The Circuit which Limits Max Duty

This IC controls an on pulse of GD by comparing CSO with RMAP. If fall time of the CT is adjusted because resistance is connected between Vref and CT, the off time for gate drive is adjusted. But Rt and Ct must be adjusted because the oscillation frequency changes only by adding Rct.
When the fixed number is decided, Please decide the fixed number with the Excel sheet prepared for.

5.5 Frequency Modulation (FM)

FM function recommends to use only in case that noise trouble occurs.

a) R2A20114AFP

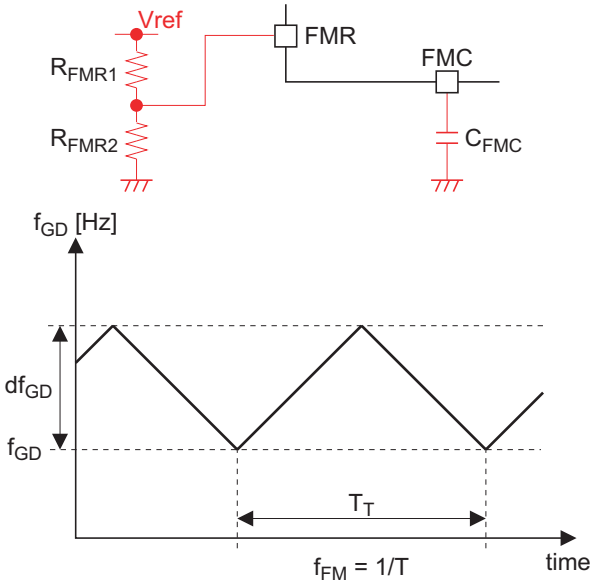
The R2A20114A Frequency Modulation function is determined by adjusting the resistor R_{FMR1}, the resistor R_{FMR1} and the timing capacitor C_{FMC}. The operating frequency is approximated by the following expression:

$$f_{FM} = \frac{5.6 \times 10^{-6}}{C_{FMC} \times (V_{FMR} - 0.2)} \quad (7)$$

$$df_{GD} = 0.3 \times \frac{V_{FMR} - 0.2}{2.3} \times f_{GD} \quad (8)$$

$$V_{FMR} = 5 \times \frac{R_{FMR2}}{R_{FMR1} + R_{FMR2}} \quad (9)$$

f_{FM}: Modulation Frequency [Hz]
df_{GD}: Modulation Frequency Width of operation frequency [Hz]



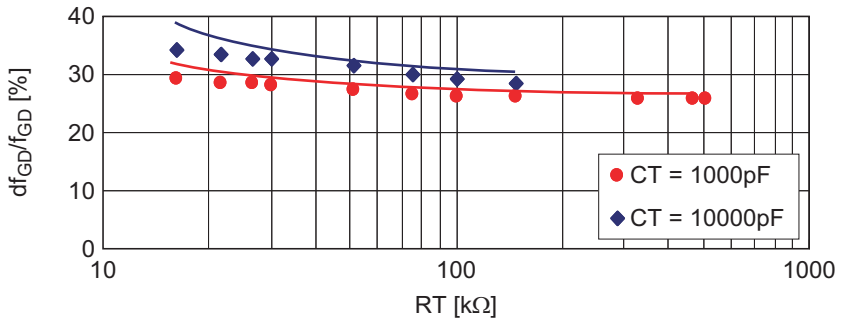


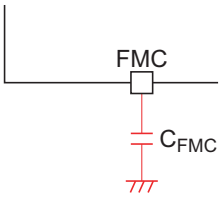
Figure 17 RT Resistor vs. df_{GD}/f_{GD} (VFMR = 2.5 V)

b) R2A20114ASP

The frequency modulation function of R2A20114ASP can adjust only modulation frequency f_{FM}. The modulation frequency f_{FM} is determined by adjusting the capacitor C_{FMC}. The f_{FM} is approximated by the expression (10). In addition, the Modulation Frequency Width of operation frequency df_{GD} is determined only by switching frequency f_{GD}. The df_{GD} is approximated by the expression (11).

$$f_{FM}\,[\mathrm{Hz}] = \frac{5.6 \times 10^{-6}}{C_{FMC} \times 2.3} \quad (10)$$

$$df_{GD}\,[\mathrm{Hz}] = 0.3 \times f_{GD} \quad (11)$$

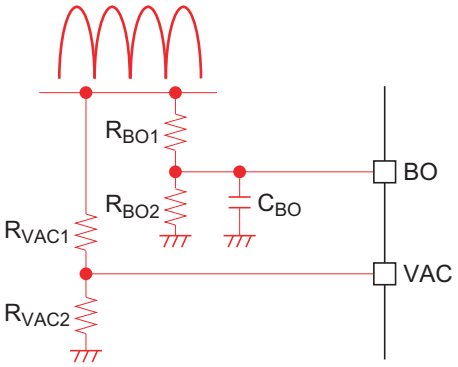


5.6 Input AC Voltage Sensing

The Full-bridge rectification wave is smoothed by capacitor, applied to the BO pin.
The voltage similar to the Full-bridge rectification wave applied to the VAC pin.

$$V_{BO} = \frac{2\sqrt{2} \times R_{BO2} \times V_{ac}}{\pi \times (R_{BO1} + R_{BO2})} \quad (12)$$

$$C_{BO} = \frac{1}{2\pi \times f_c + \left(\frac{R_{BO1} \times R_{BO2}}{R_{BO1} + R_{BO2}}\right)} \quad (13)$$



Vac: Effective value of minimum input voltage [V(rms)]
f_C: Cutoff frequency [Hz]

a) R2A20114AFP

Please defend the following conditions. After decide OVP2 terminal resistors, please decide the values of R_{VAC1} and R_{VAC2}.

$$\frac{R_{VAC1}}{R_{VAC2}} = \frac{R_{OVP2\_1}}{R_{OVP2\_2}} \quad (14.1)$$

b) R2A20114ASP

Please defend the following conditions. After decide FB terminal resistors, please decide the values of R_{VAC1} and R_{VAC2}.

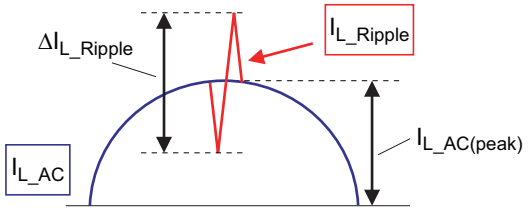
$$\frac{R_{VAC1}}{R_{VAC2}} = \frac{R_{FB1}}{R_{FB2}} \quad (14.2)$$

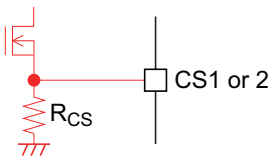
5.7 Resistor of Current Sensing

a) R2A20114AFP

$$R_{CS} \leq \frac{0.3\sqrt{2} \times V_{ac} \times \eta \times F_{PFC}}{P_{out} \times (2 + \gamma)} \quad (15.1)$$

$$\gamma = \frac{\Delta I_{L\_Ripple}}{I_{L\_AC(peak)}} \quad (15.2)$$





<Current sense of R2A20114ASP/AFP>

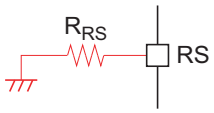
V_{ac}: Effective value of input voltage [V]
P_{out}: Maximum output power [W]
η: Efficiency
F_{PFC}: Power Factor
γ: Ripple of boost inductor current
ΔI_{L_Ripple}: Maximum ripple current of Boost inductor [A]
$I_{L\_AC(peak)}$: Peak current of Boost inductor [A]

5.8 Phase Compensation Circuit of Current Amplifier

5.8.1 RS Pin

a) R2A20114ASP/AFP

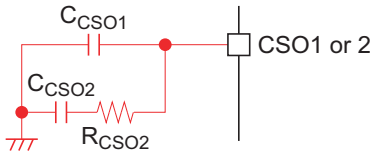
$$R_{RS}\,[\Omega] = \frac{L \times 10^9}{2.5 \times R_{CS}} \times \frac{R_{ovp2\_2}}{R_{ovp2\_1} + R_{ovp2\_2}} \qquad (16)$$



L: Boost inductor [H]
Rcs: Resistor of Current sense [Ω]
Vout: Output voltage[V]
n: Current-sense Transformer turns ratio

5.8.2 CSO Pin

Current loop frequency characteristics should have set below conditions.
It has enough gain at twice of AC input frequency.
It has enough lower gain at switching frequency.
As a recommendation,
Over 40 dB at twice of AC input frequency
Set zero cross frequency of current loop around 1/10 of switching frequency.
Around –30 dB at switching frequency
How to adjust refers to 5.12.2.



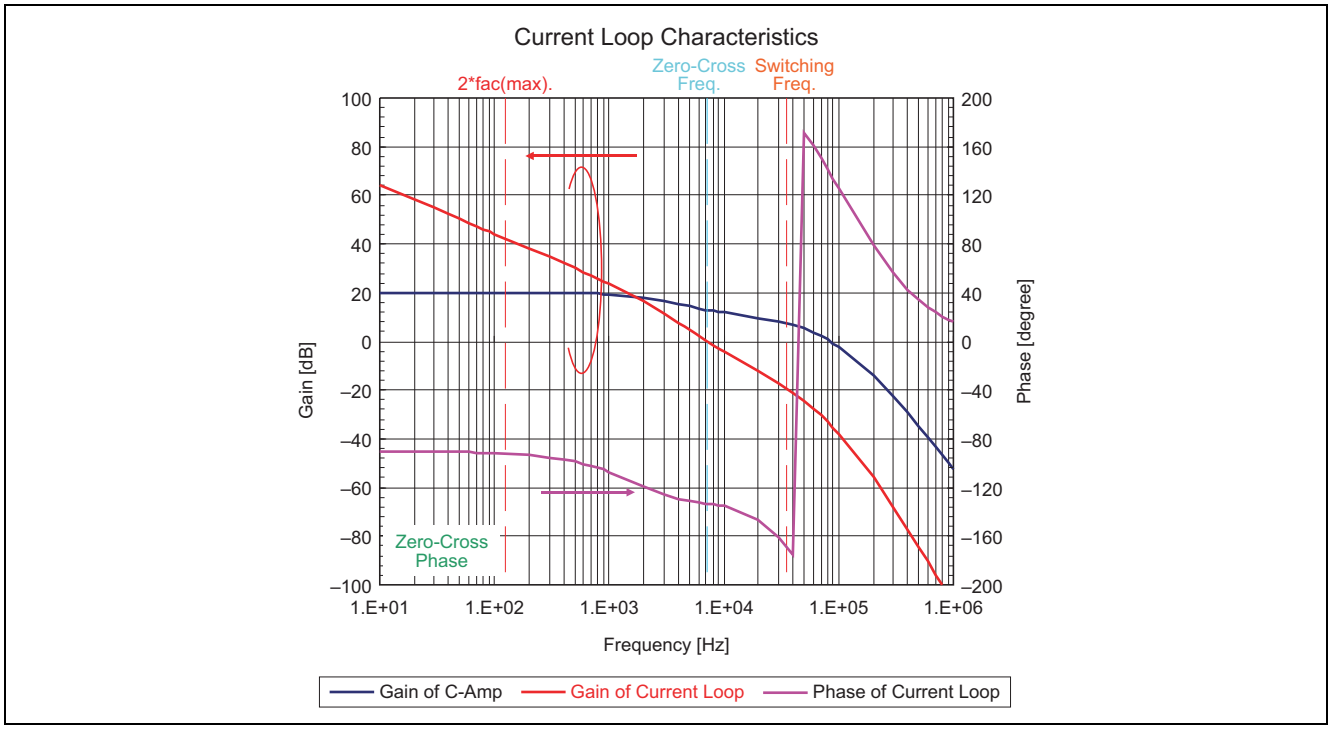
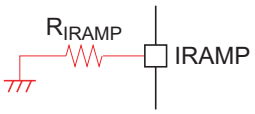


Figure 18

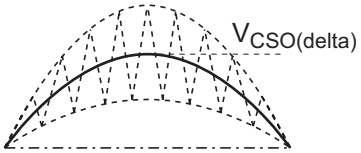
5.9 Resistor of IRAMP Pin

The R_{IRAMP} must be adjusted to be able to output max power with the minimum input voltage. The R_{IRAMP} is approximated by the expression (17) on the condition that it is operated with CCM in the minimum input voltage and the max power.

$$R_{IRAMP}\ [\Omega] = 4 \times 10^9 \times \left(\frac{\sqrt{2} \times V_{AC(min)}}{V_{OUT} \times f_{GD}} - 2 \times 10^{-6} \right) \times \frac{1}{V_{CSO(delta)}} \quad (17)$$

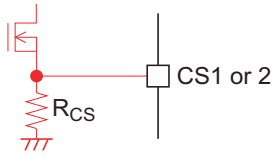


$V_{CSO(delta)}$: Peak voltage of the CSO pin [V]
f_{GD}: operating frequency [Hz]



a) R2A20114ASP/AFP

$$V_{CSO(delta)}\ [V] = \frac{4.5\sqrt{2} \times P_{out} \times R_{cs}}{V_{AC} \times \eta} \quad (18)$$

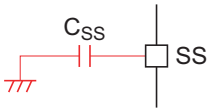


<Current sense of R2A20114ASP/AFP>

5.10 Capacitor of Soft-start

If tss is time when an SS pin voltage reaches Vss, capacity Css is expressed in the expression (19). Please input 2 V into Vss in the beginning.
But startup time tss is different by load and an input and output condition. Therefore, please decide the fixed number after adjusting it while confirming the evaluation board.

$$C_{SS}\ [\mu F] = \frac{28 \times 10^{-6}}{V_{SS}} \times t_{ss} \quad (19)$$



Vss: SS pin voltage [V]
tss: soft-start time [sec]

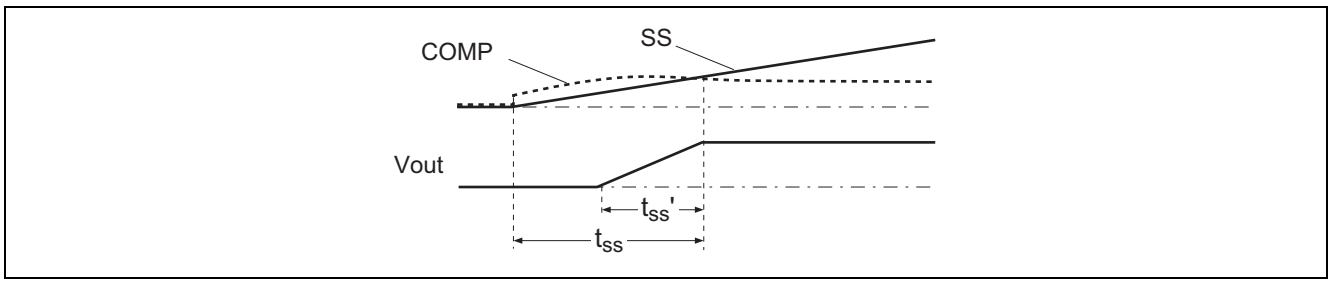


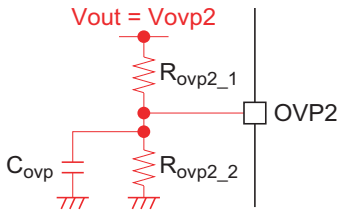
Figure 19 Each Pin Waveform at the Soft-start

5.11 Protection Functions

5.11.1 OVP2 Voltage Setting

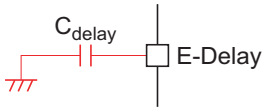
The capacitor(Covp) has the possibility to need as a noise filter.

$$V_{OVP2}\,[\mathrm{V}] = \frac{R_{ovp2\_1} + R_{ovp2\_2}}{R_{ovp2\_2}} \times 2.5 \times 1.08 \qquad (20)$$



5.11.2 E-Delay Setting

$$C_{delay} = \frac{36 \times 10^{-6}}{2.54} \times t_{delay} \qquad (21)$$

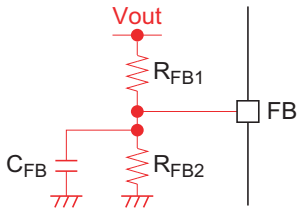


5.12 Output Voltage Setting and Frequency Characteristics of Voltage Loop Mode

5.12.1 Output Voltage Setting

FB pin will be controlled to 2.5 V. So, please choose resistors to meet it.
The capacitor (C_{FB}) has the possibility to need as a noise filter.

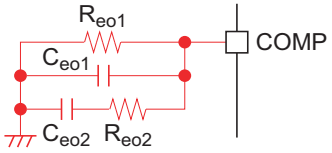
$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times 2.5 \qquad (22)$$



5.12.2 COMP Parameter Setting

Voltage and current amplifier are transconductance (gm) amplifier. It does not need to feedback for input side. Therefore, it is possible to minimize influence on input circuit by feedback circuit. Gain of gm amplifier is calculated by product of transconductance and output impedance. For example of voltageamplifier, it's shown with formula. Gm-v is transconductance of voltage amplifier. Rvo is output resistor of voltage amplifier itself.

$$G_V = G_{m\text{-}v} \times \frac{1}{\frac{1}{R_{vo}} + \frac{1}{R_{eo1}} + j\omega C_{eo1} + \frac{1}{R_{eo2} + \frac{1}{j\omega C_{eo2}}}} \qquad (23)$$



Gm-v: transconductance of voltage amplifier [S]
Rvo: 500kΩ total output resistance of voltage amplifier

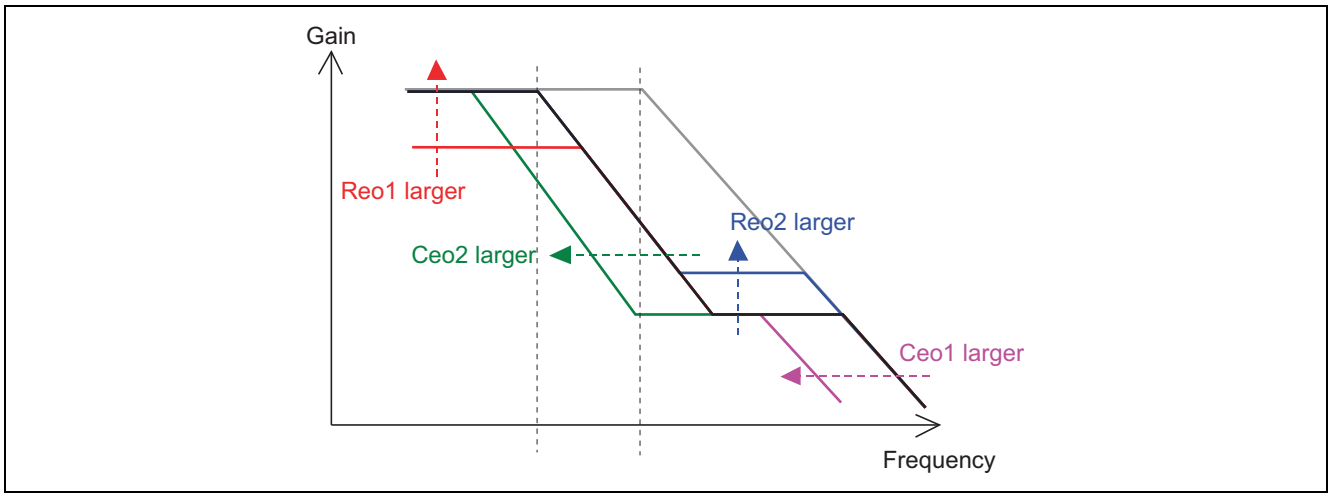
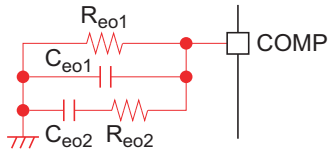


Figure 20 Outline of Gain Characteristics

Voltage loop frequency characteristics should have set below conditions.
It has enough lower gain at twice of AC input frequency.
Zero-cross frequency is lower than AC input frequency
As a recommendation,
Over –30 dB at twice of AC input frequency
Set zero cross frequency of voltage loop around 1/5 of AC input frequency.
How to adjust refers to 5.12.2.



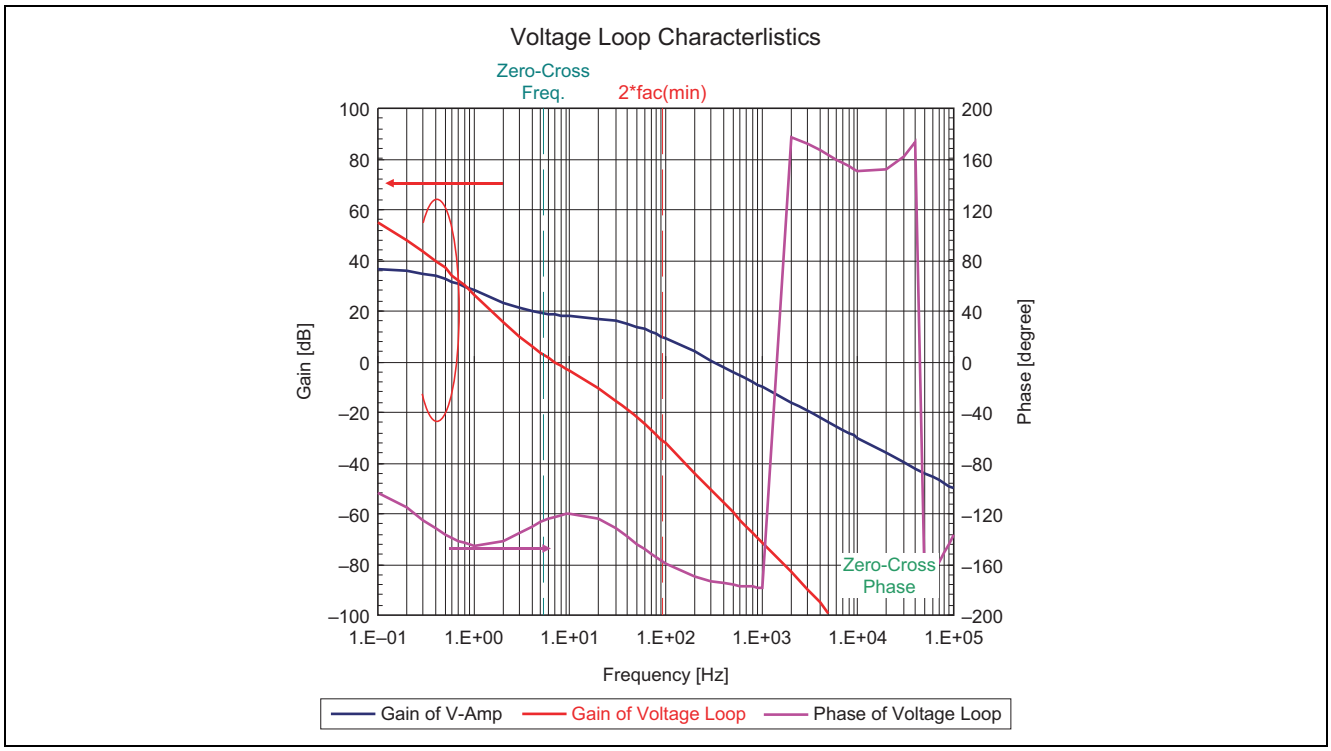


Figure 21

5.13 An used Pin

The state of the unused pin to recommend of the R2A20114A series is shown by below. All pins except the list shown below are used.

Table 2 The State of the Unused Pin to Recommend of the R2A20114A

R2A20114AFP		R2A20114ASP		
LQFP-40		SOP-20		
Pin No.	Pin Name	Pin No.	Pin Name	The State of the Unused Pin to Recommend
1	FMR	—	—	Open
2	FMC	3	FM	GND
4	BO	5	BO	Connect to the VREF
6	PD	—	—	GND
8	E-DELAY	—	—	Open
11	ERROR	—	—	Open
12	OFF	—	—	GND
14	SS	—	—	Open
18	OVP2	—	—	GND
36	SYNC-O	—	—	Open
—	N.C.	—	—	Open

Note: The pin except the above is not made unused.

5.14 Notice for PCB Layout

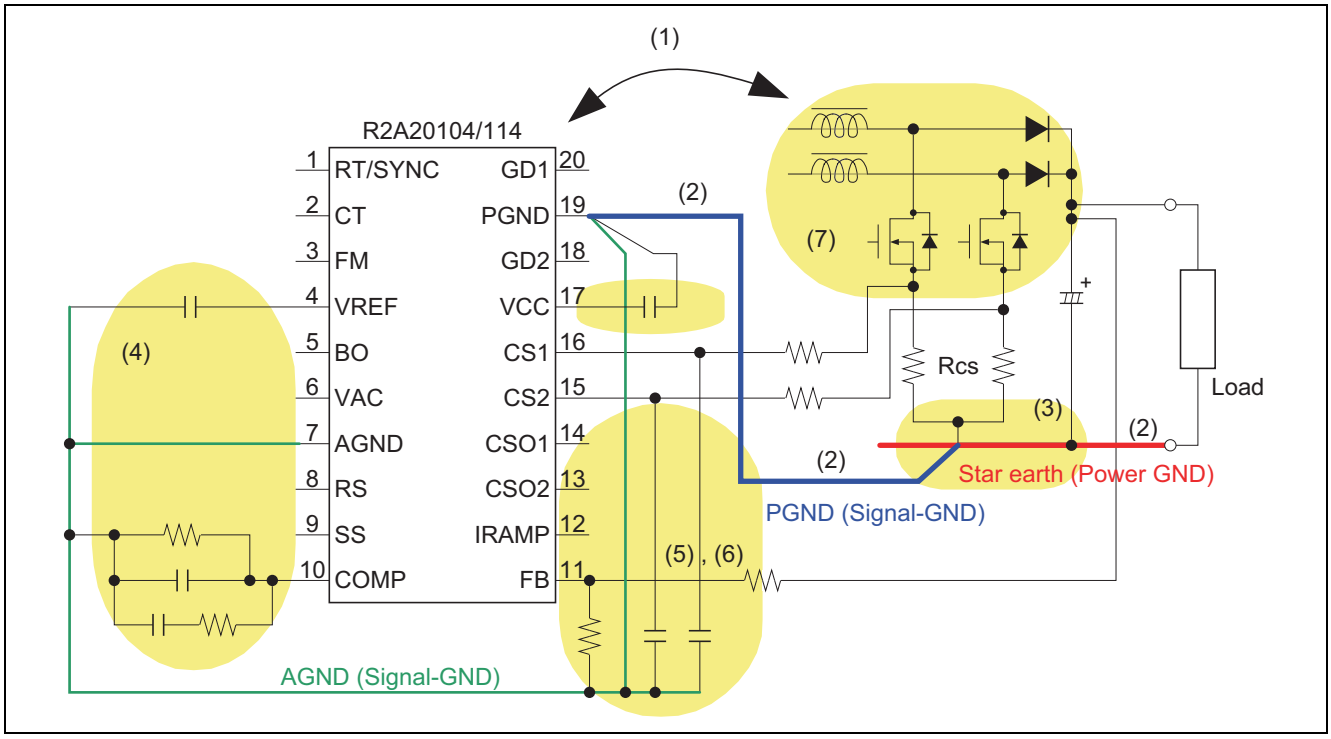


Figure 22

(1) Please make sure PFC IC be located as apart from power stage (MOSFET, DIODE, Boost L) as possible. Specially please be careful to MOSFET drain line layout to avoid radiation noise.

(2) Please separate Power-GND and Signal-GND pattern surely and make both GNDs be connected under the output CAP. The pattern for Power-GND is widely from output CAP to PGND.
And please place the capacitor between Vcc and AGND.

(3) The pattern for resistance RCS of current detection is made an even phase as short as possible, and it connects it under the output CAP.

(4) Please place COMP/VREF external Parts as close to the IC pin as possible.

(5) Please place the filter for CS1, CS2 and as close to the IC as possible for avoiding radiation noise.

(6) Please place the FB resistor as close to the IC as possible for avoiding radiation noise.

(7) The pattern for power stage (MOSFET, DIODE, Boost L) parts is shortened as much as possible.

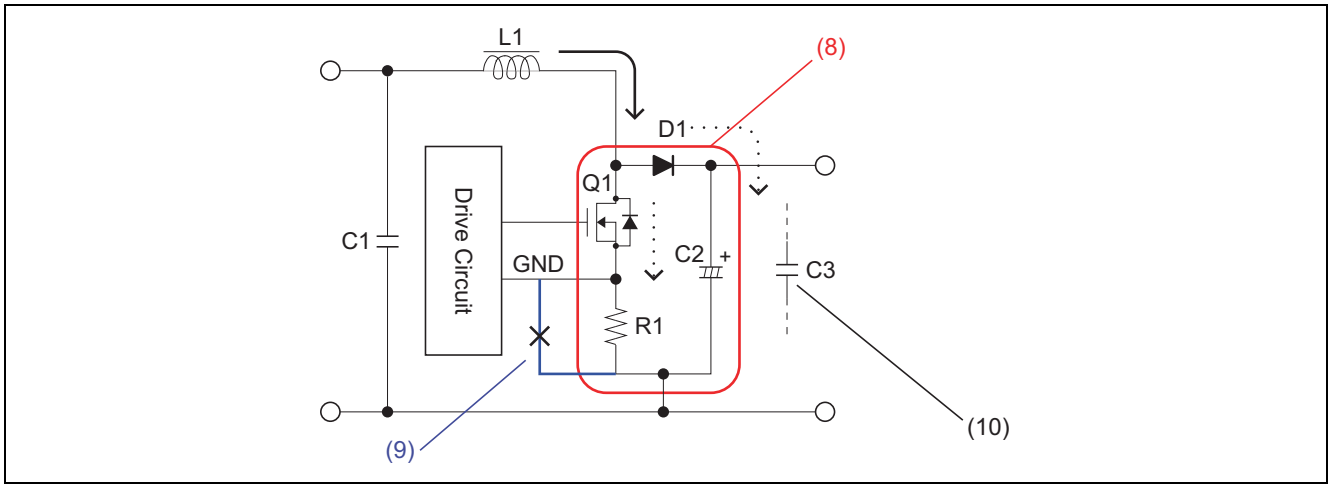


Figure 23

(8) It is possible to reduce MOSFET drain overshoot by widely shortening the pattern, which flows discontinuous current.

(9) The return-GND of drive circuit should be connect with source of MOSFET(Q1).
The current of return-GND separate with large current(for power circuit) and small current(for drive circuit).

(10) If switching ripple voltage of output is too large, please place the film capacitor (C3) near diode (D1). The film capacitor selects the good one of the high frequency characteristic.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep 08, 2011	—	First edition issued
2.00	Apr 02, 2014	4, 7, 8, 15, 21	Second edition issued
3.00	May 15, 2014	7	Figure 7

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