RZ/A1H Group

QE for Video Display Controller 5 Sample Program

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Summary

This application note describes a sample application for Video Display Controller 5 (VDC5), which interoperates with QE for Video Display Controller 5, a plugin for the e^2 studio integrated development environment with support for Renesas microcontrollers. QE for Video Display Controller 5 is a tool that provides a graphical interface for display control to support the development of embedded systems incorporating display devices.

Target Device

RZ/AH Group

Contents

1. Overview

As shown in Figure 1.1, VDC5 comprises multiple blocks, so simply checking display attributes requires an understanding of the VDC5 specifications and several settings. However, by using the sample program and QE for Video Display Controller 5, it is possible to prepare an environment in which display device connections can be checked quickly, without the need to understand the VDC5 specifications. QE for Video Display Controller 5 is a tool that provides a graphical interface for display control. The user inputs information on the display device to be used, and the tool outputs a header file containing the information necessary for display control. Using the header file as a basis, the sample program makes settings to VDC5. The tool also provides a function that adjusts the timing in real time, making it possible to first make fine adjustments with the display device connected, and then to output the header file. The sample program is described below.

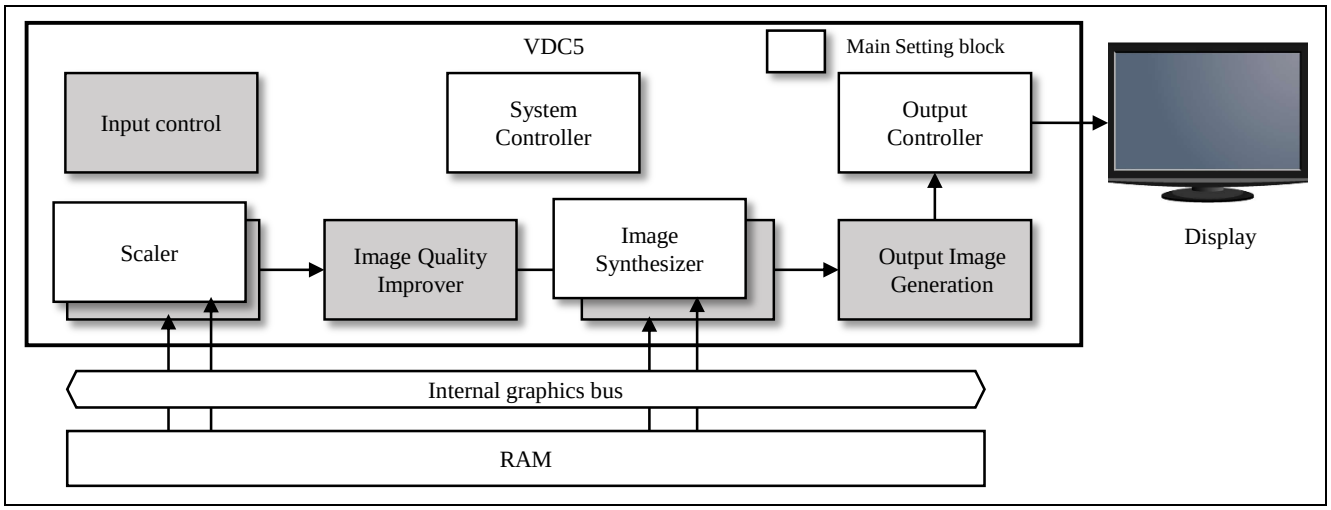


Figure 1.1 VDC5 Block Configuration

2. Operation Confirmation Conditions

The sample program accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	RZ/A1H
Operating frequency	CPU clock (Iϕ): 400 MHz Image processing clock (Gϕ): 266.67 MHz Internal bus clock (Bϕ): 133.33 MHz Peripheral clock 1 (P1ϕ): 66.67 MHz Peripheral clock 0 (P0ϕ): 33.33 MHz
Operating voltage	Power supply (I/O): 3.3 V Power supply (internal): 1.18 V
Development environment	Development environment Renesas “e^2 studio” Version: 4.3.1.0001
Compiler	GNUARM-NONE-EABI Toolchain v14.02
Operating mode	Boot mode 0*1 (CS0 space, 16-bit boot)
Board to be used	Board • RSK CPU board (YR0K77210C000BE) • RSK TFT APP board (YROK77210C000BE)
Emulator	J-Link LITE ARM debugger
Board settings (Jumper/switch)	• RSK CPU board (YR0K77210C000BE) SW4-1 OFF, SW4-2 OFF, SW4-3 OFF, SW4-4 OFF, SW4-5 OFF, SW4-6 OFF, SW4-7 OFF, SW4-8 OFF SW6-1 ON, SW6-2 ON, SW6-3 ON, SW6-4 ON, SW6-5 ON, SW6-6 ON JP11 2-3, JP12 1-2, JP21 1-2, JP18 1-2 • RSK TFT APP board (YROK77210C000BE)

Note 1. The sample program is loaded into the on-chip RAM and run from there. It does not use the CS0 space.

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the hardware configuration used by the sample program.

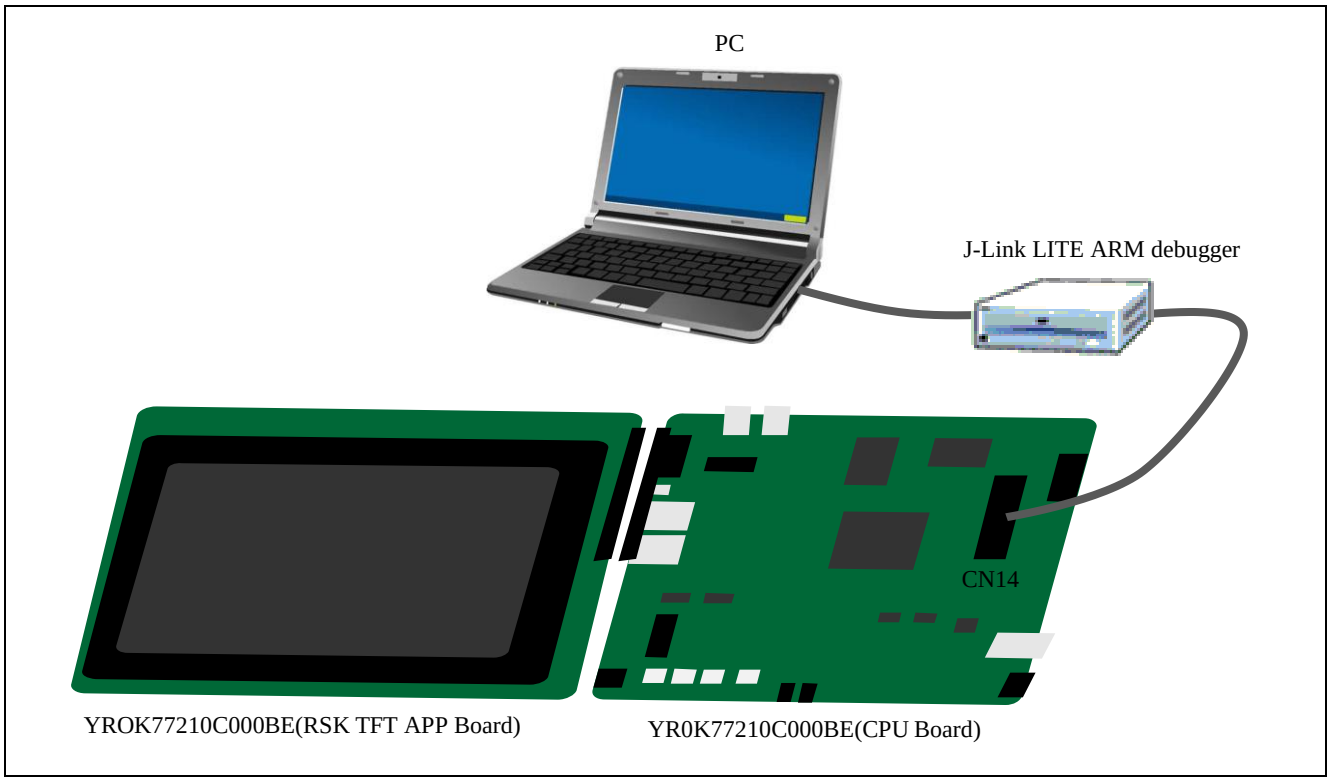


Figure 3.1 Hardware Configuration of Sample Program

4. Software

4.1 Operation Overview

As shown in Figure 4.1, the sample program initializes clocks, interrupts, the MMU, etc., on the CPU; initializes the bus settings for connecting to external memory, etc., on the board; and makes VDC5 operation settings based on the header file output by Video Display Controller 5. Then it makes GPIO settings used for display control.

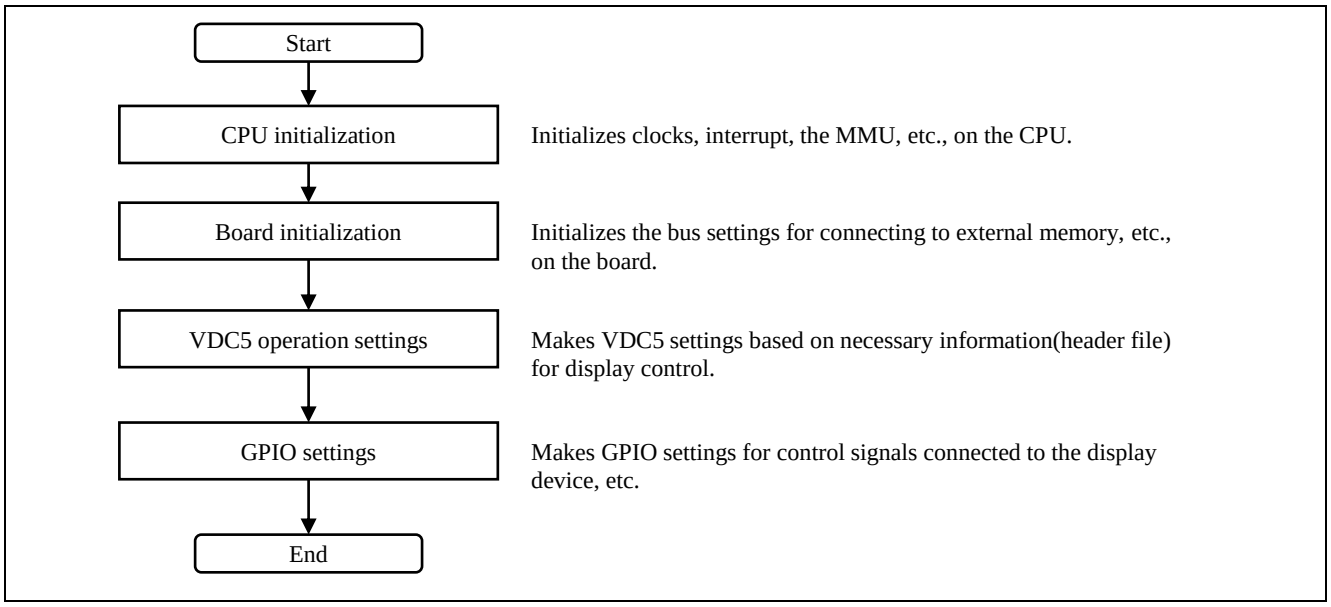


Figure 4.1 Sample Program Operation Overview

4.2 Sample Software Details

Figure 4.2 lists the VDC5 operation settings in detail. The VDC5 operation settings are based on the header file output by QE for Video Display Controller 5.

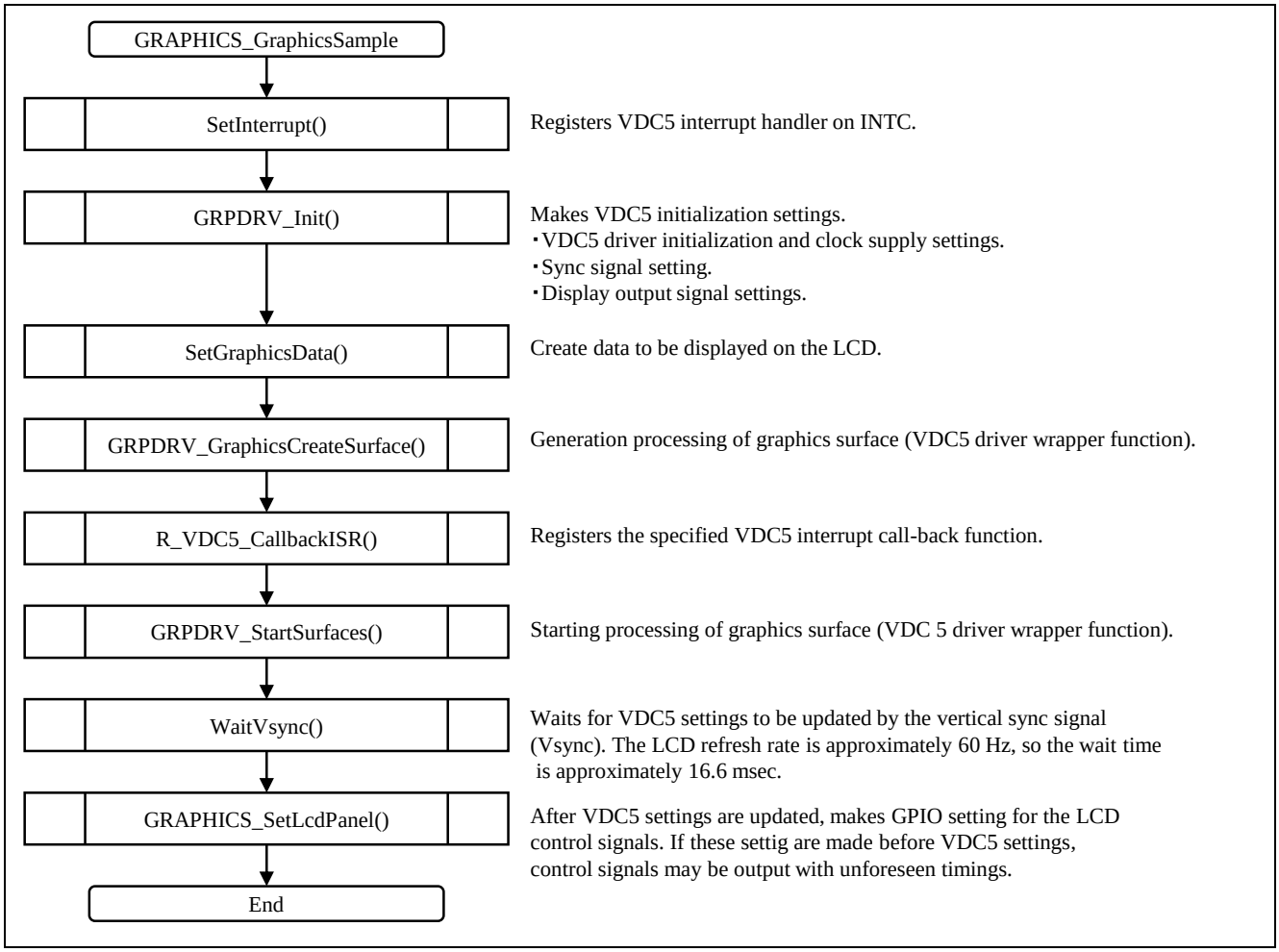


Figure 4.2 Flowchart of VDC5 Operation Settings

If the display device settings are made correctly, the screen shown in Figure 4.3 is displayed.

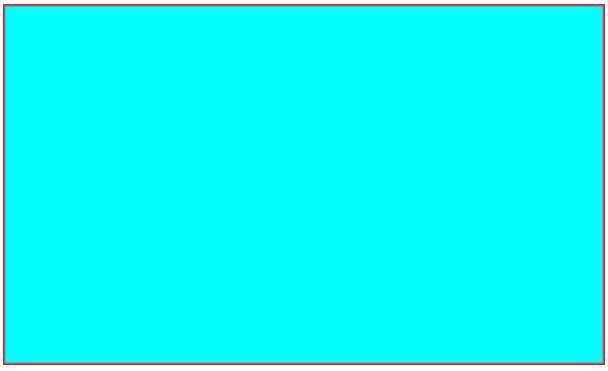


Figure 4.3 Display Screen

4.3 Memory Map

The specific section used by the sample program is as shown below.

Table 4.1 Specific Section Used by Sample Program

Name of Area	Type	Description
VRAM_SECTION_1	ZI Data	Buffer for storing display data Assigned to an uncached area at a fixed address (0x60500000) in the large-capacity on-chip RAM.

4.4 Peripheral Functions Used

Table 4.2 lists the peripheral functions used by the sample program and their applications.

Table 4.2 Peripheral Functions Used and Their Applications

Peripheral Function	Application
Video display controller 5 (VDC5) Channel 0	Display • Uses graphics 2. • Color format: RGB888
Interrupt controller (INTC)	VDC5 channel 0 interrupt control • Waiting for register update
Large-capacity on-chip RAM	VRAM • On-chip RAM is used as a display buffer.

4.5 Interrupt Used

Table 4.3 lists the interrupt used by the sample program. The VDC5 register settings are updated by the vertical sync signal (Vsync), and this interrupt is used to wait for the update to occur. The LCD refresh rate is approximately 60 Hz, so the interrupt interval is approximately 16.6 msec.

Table 4.3 Interrupt Used by Sample Program

Interrupt (Source ID)	Priority	Source Description
VDC5 channel 0 (GR3_VLINE0: 78)	5	Specified line signal of graphics 3 panel output (synchronized with line 0 of the video signal output by the image synthesis block)

4.6 Function Specifications

For information on the functions used by the sample program, refer to the related application note RZ/A1H Group: Video Display Controller 5 Sample Driver (R01AN1822JJ/EJ).

5. Using the Sample Program and QE for Video Display Controller 5

The sample program is intended to be run in the environment provided by the RSK CPU board (YR0K77210C000BE). The procedure for confirming connection of the RSK TFT APP board (YROK77210C000BE) with QE for Video Display Controller 5 when using this environment is described below. For instructions for installing e^2 studio and QE for Video Display Controller 5, refer to the manuals of each of these tools.

5.1 Procedure for Confirming Display with a Header File Generated by QE for Video Display Controller 5

5.1.1 Importing the Sample Project

After launching e^2 studio, right-click with the mouse and select **Import**, as shown in Figure 5.1, to display the **Import** dialog box.

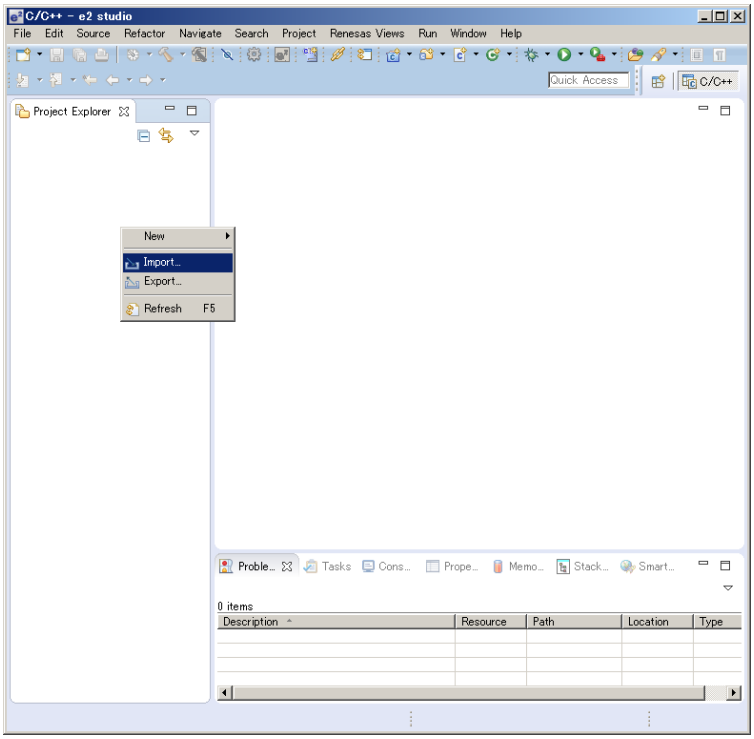


Figure 5.1 Importing the Project

In the **Import** dialog box (Figure 5.2), select **Existing Projects into Workspace** and click the **Next** button.

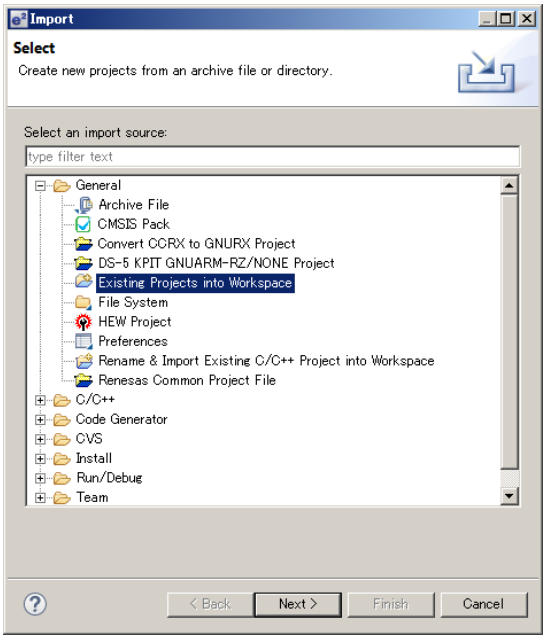


Figure 5.2 Import Dialog Box

In the **Browse Folders** dialog box (Figure 5.3), select the folder containing the sample program and click the **OK** button.

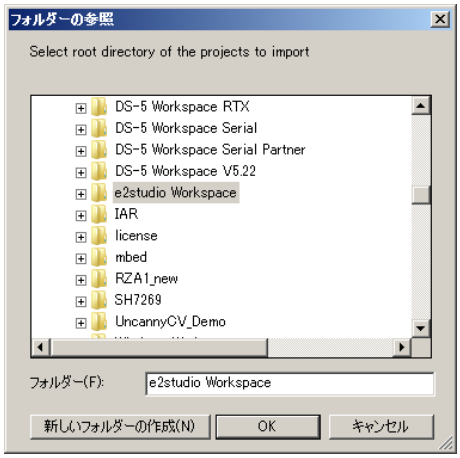


Figure 5.3 Browse Folders

When the sample project is found, **RZ_A1H_QE_for_VDC5_sample** is displayed in the **Project** field, as shown in Figure 5.4. Check the box and then click the **Finish** button.

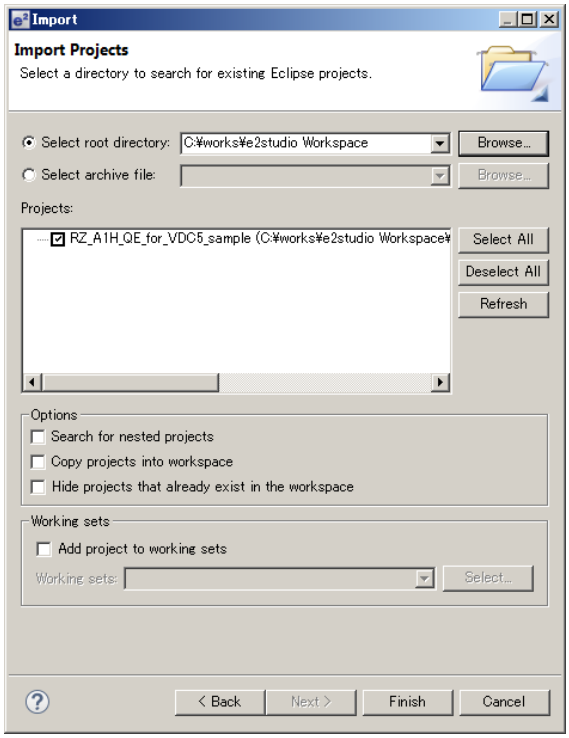


Figure 5.4 Import Project Confirmation Dialog Box

When the above steps are completed, the sample program is imported into e^2 studio (Figure 5.5).

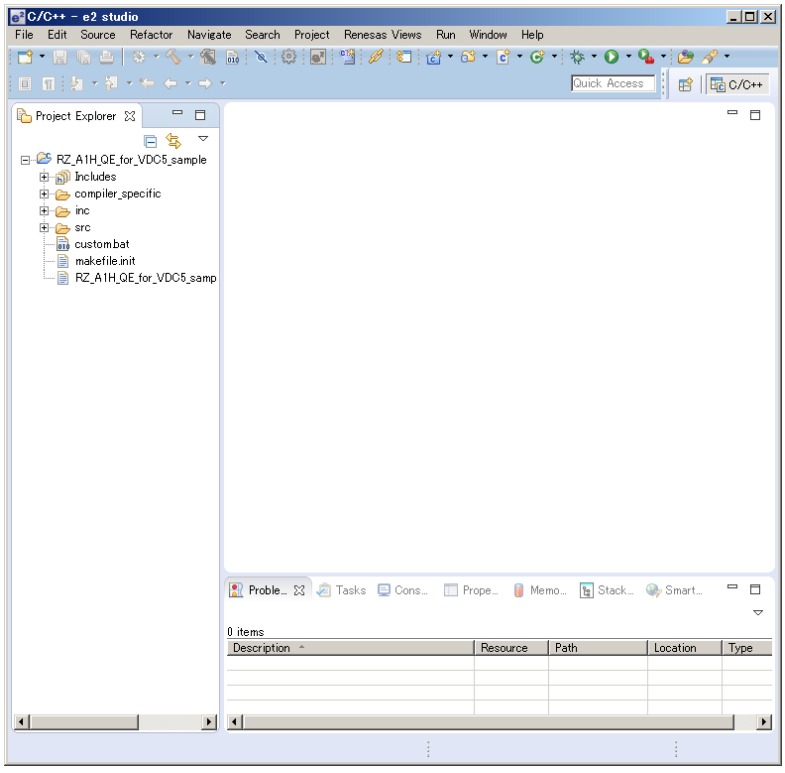


Figure 5.5 Imported Sample Project

5.1.2 Launching QE for Video Display Controller 5

From the e^2 studio menu select **Renesas Views → Renesas QE → Display Timing Tuning(QE)** to launch QE for Video Display Controller 5 (Figure 5.6).

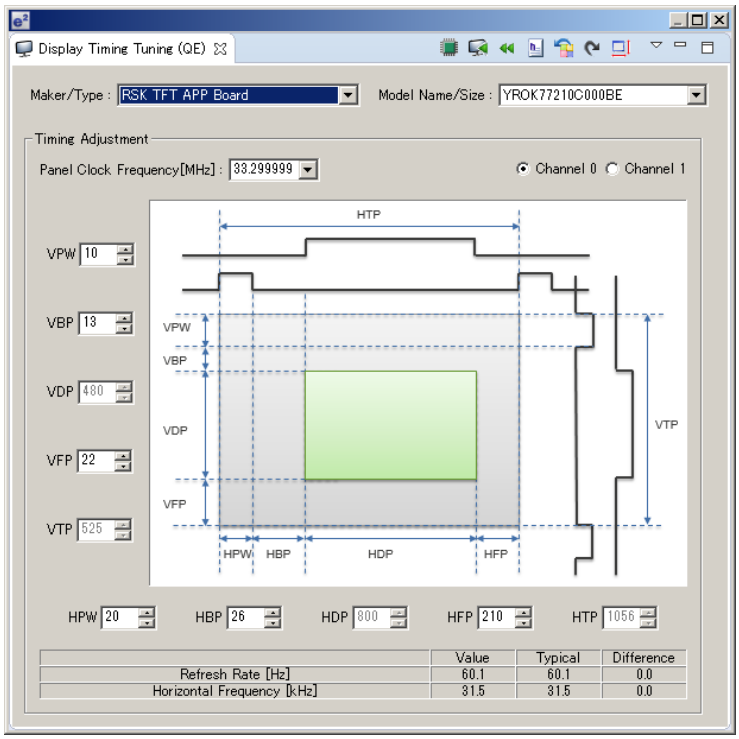


Figure 5.6 QE for Video Display Controller 5 Launch Screen

5.1.3 Display Device Information Settings

Select **Custom** from the **Maker/Type** pull-down list at the top of the dialog box shown in Figure 5.6 to display the **Edit Custom Display Data** dialog box (Figure 5.7). The display device information is input into this dialog box. The TFT LCD (GWP0700CNWV04) from GW Opto is mounted on the RSK TFT APP board (YROK77210C000BE) used in the present case, and information matching the specifications of this TFT LCD will be input.

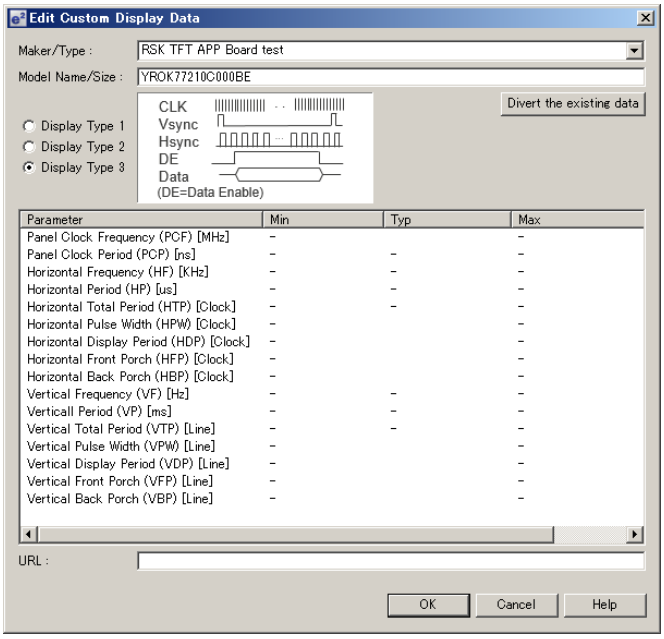


Figure 5.7 Edit Custom Display Data Dialog Box

(a) Entering a Registered Name

Enter any name you wish in the **Maker/Type** and Model/Size fields of the **Edit Custom Display Data** dialog box (Figure 5.8). This name will be registered in the drop-down list and will become selectable.

Figure 5.8 Name Registration

(b) Selecting the Display Type

Table 5.1 lists the main control signals required when connecting a display device. In the present case, three display device types combining these control signals are supported by QE for Video Display Controller 5.

Table 5.1 Main Control Signals

Name	Function Summary
Horizontal sync signal (Hsync)	Signal that creates timing for displaying one line
Vertical sync signal (Vsync)	Signal that creates timing for displaying one screen
Panel clock (CLK)	Pixel-level display frequency
Display enable (DE)	Signal indicating that valid data is being output
Data (Data)	Display data

The user must select from the three display types listed in Table 5.2 to determine which control signals are required by the specifications of the display device used.

Table 5.2 Control Signals Used

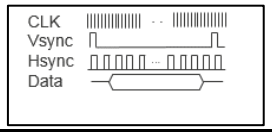
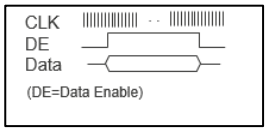
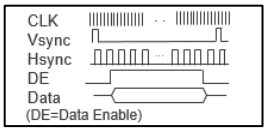
Name	Display Type 1 	Display Type 2 	Display Type 3 
Horizontal sync signal (Hsync)	Used	Not used	Used
Vertical sync signal (Vsync)	Used	Not used	Used
Panel clock (CLK)	Used	Used	Used
Display enable (DE)	Not used	Used	Used
Data (Data)	Used	Used	Used

Figure 5.9 and Figure 5.10 show horizontal and vertical input timing charts for the RSK TFT APP board (YROK77210C000BE) used in the present case. The horizontal sync (Hsync) signal, vertical sync (Vsync) signal, and display enable (DE) signal shown in these timing charts are required, so select display type 3 (Figure 5.11).

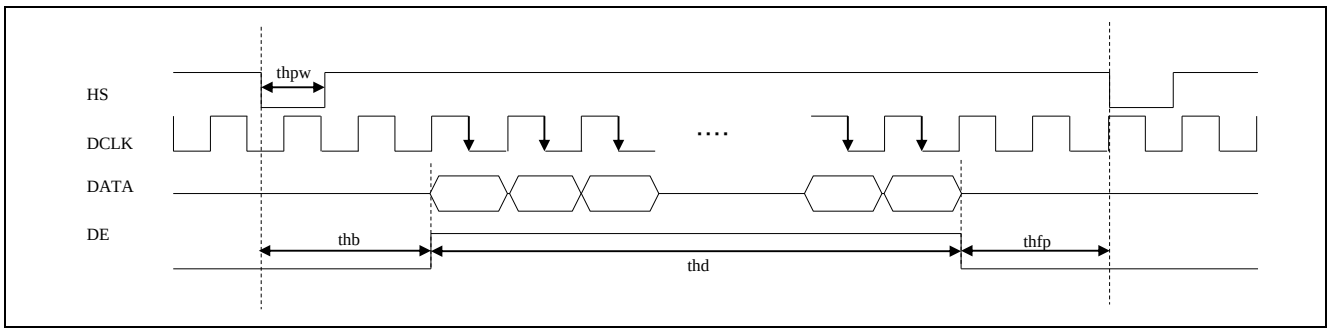


Figure 5.9 Horizontal Input Timing Diagram

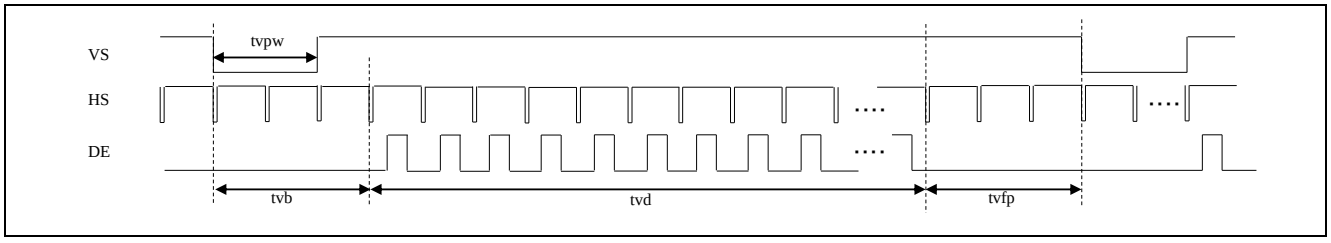


Figure 5.10 Vertical Input Timing Diagram

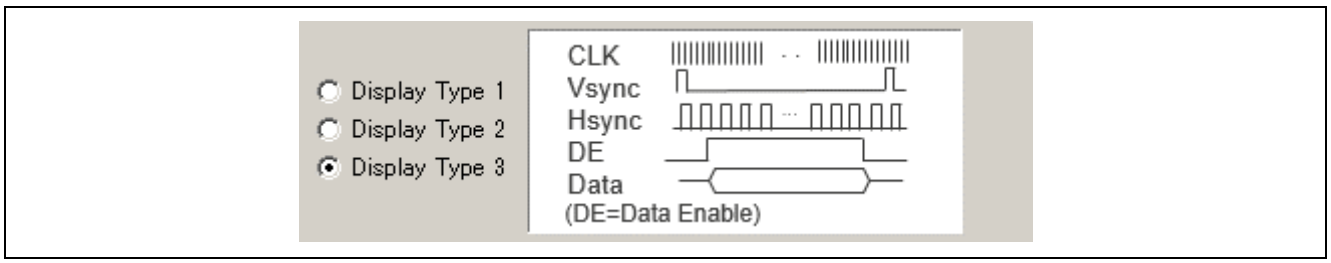


Figure 5.11 Display Type Selection

(c) Inputting Control Timing Values

Figure 5.9 and Figure 5.10 show horizontal and vertical input timing charts for the RSK TFT APP board (YROK77210C000BE) used in the present case. Table 5.3 and Table 5.4 list the input timing of the horizontal and vertical sync signals. After inputting these control timing values, the result is as shown in Figure 5.12. The values input under **Typ** are used for timing control, and the values input under **Min** and **Max** are used to confirm that values are within the allowable range when the GUI is used for timing adjustment in QE for Video Display Controller 5.

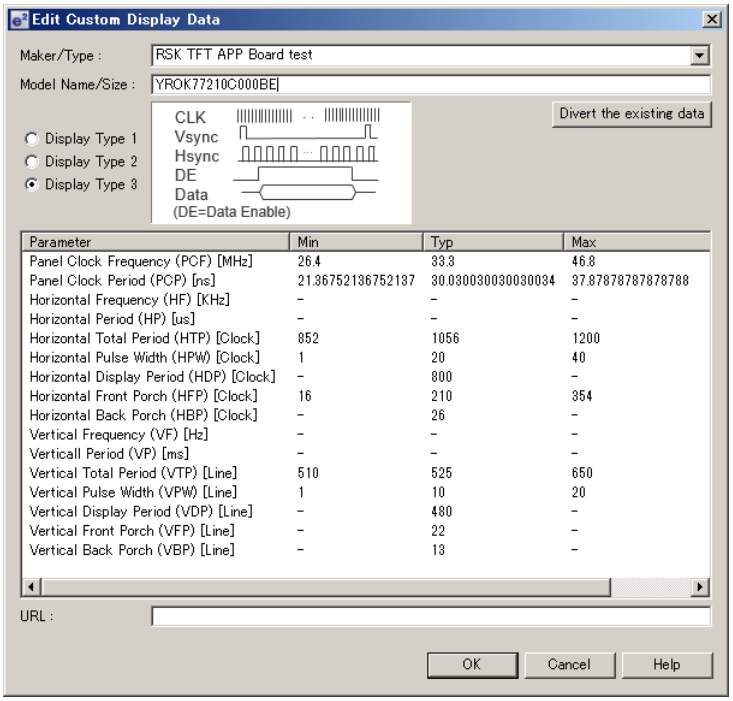


Figure 5.12 Result Inputting Control Timing Values

Refer to Table 5.3 when inputting the following items:

- Panel clock frequency
- Horizontal total period
- Horizontal pulse width
- Horizontal display period
- Horizontal front porch
- Horizontal back porch

Refer to Table 5.4 when inputting the following items:

- Vertical total period
- Vertical pulse width
- Vertical display period
- Vertical front porch
- Vertical back porch

Note: In Figure 5.12 the **Typ** values for Horizontal Pulse Width and Vertical Pulse Width are midway between the **Min** and **Max** values. Also, the values listed in Table 5.3 and Table 5.4 should be input for HS Blanking and VS Blanking, but since these HS Blanking and VS Blanking values include the HS pulse width and VS pulse width, respectively, the **Typ** values for Horizontal Pulse Width and Vertical Pulse Width are subtracted and the resulting values are input as the **Typ** values for Horizontal Back Porch and Vertical Back Porch, respectively.

Table 5.3 Horizontal Input Timing

Item	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Horizontal display area	thd	—	800	—	DCLK	
DCLK frequency	fclk	26.4	33.3	46.8	MHz	
One horizontal line	th	852	1056	1200	DCLK	
HS pulse width	thpw	1	—	40	DCLK	
HS blanking	thb	46	46	46	DCLK	
HS front porch	thpf	16	210	354	DCLK	

Table 5.4 Vertical Input Timing

Item	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd	—	480	—	TH	
VS period time	Tv	510	525	650	TH	
VS pulse width	tvpw	1	—	20	TH	
VS blanking	tvb	23	23	23	TH	
VS front porch	tvpf	7	22	147	TH	

(d) **Control Signal Output Settings**

Click the display controller and LCD settings icon (Figure 5.13) in QE for Video Display Controller 5 to display the **Display Controller and LCD Settings** dialog box (Figure 5.14).

Figure 5.13 Display Controller and LCD Settings Icon

In this dialog box, make output settings for the control signals listed below.

[Panel driver signal (TCON) output selection]

- Output pin selection:
  Output to pins LCD_TCON0 to LCD_TCON6 (TCON0 to TCON6)
- Control signal polarity:
  Positive polarity (high active)
  Negative polarity (low active)

[LCD setting]

- Output data format selection:
  24-bit RGB888 output (24-bit (VDC5_LCD_OUTFORMAT_RGB888))
  18-bit RGB666 output (18-bit (VDC5_LCD_OUTFORMAT_RGB666))
  16-bit RGB565 output (16-bit (VDC5_LCD_OUTFORMAT_RGB565))
- Data output timing:
  Output at rising edge of panel clock (Rising (VDC5_EDGE_RISING))
  Output at falling edge of panel clock (Falling (VDC5_EFGE_FALLING))

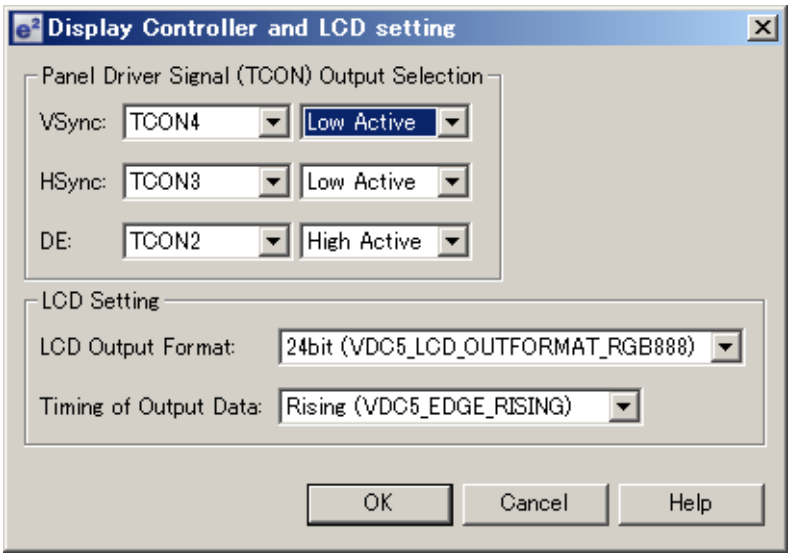


Figure 5.14 Display Controller and LCD Settings Dialog Box

The output pin selection items matching the specifications of the RSK TFT APP board (YROK77210C000BE) used in the present case are listed below.

- Output pin selection
  - Vsync: TCON4
  - Hsync: TCON3
  - DE: TCON2

Based on Figure 5.9 and Figure 5.10, the polarity of the control signals is listed below.

- Polarity of the control signals
  - Vsync: Negative polarity (low active)
  - Hsync: Negative polarity (low active)
  - DE: Positive polarity (high active)

The output data format matching the board specifications is listed below.

- Output data format selection:
  24-bit RGB888 output (24-bit (VDC5_LCD_OUTFORMAT_RGB888))

Regarding the data output timing, since sampling occurs at the falling edge of the DCLK signal, according to Figure 5.9, the timing of data output on the VDC5 side is at the rising edge of the panel clock.

- Data output timing:
  Output at rising edge of panel clock (Rising (VDC5_EDGE_RISING))

This completes the display device information settings.

5.1.4 Generating a Header File

You can generate a header file reflecting the control timing settings by clicking the generate header file icon (Figure 5.15) in QE for Video Display Controller 5. The header file name and output destination can be specified by the user.

Figure 5.15 Generating a Header File

The sample program references the generated header file and makes settings to VDC5. Save the header file using the folder name and file name shown below.

[Folder]

- RZ_A1H_QE_for_VDC5_sample\inc\lcd

[File name]

- RSK_TFT_ch0.h

5.1.5 Building the Sample Project

After completing the display device information settings and outputting the header file in QE for Video Display Controller 5, right-click the imported project, as shown in Figure 5.16, and select **Build Project**.

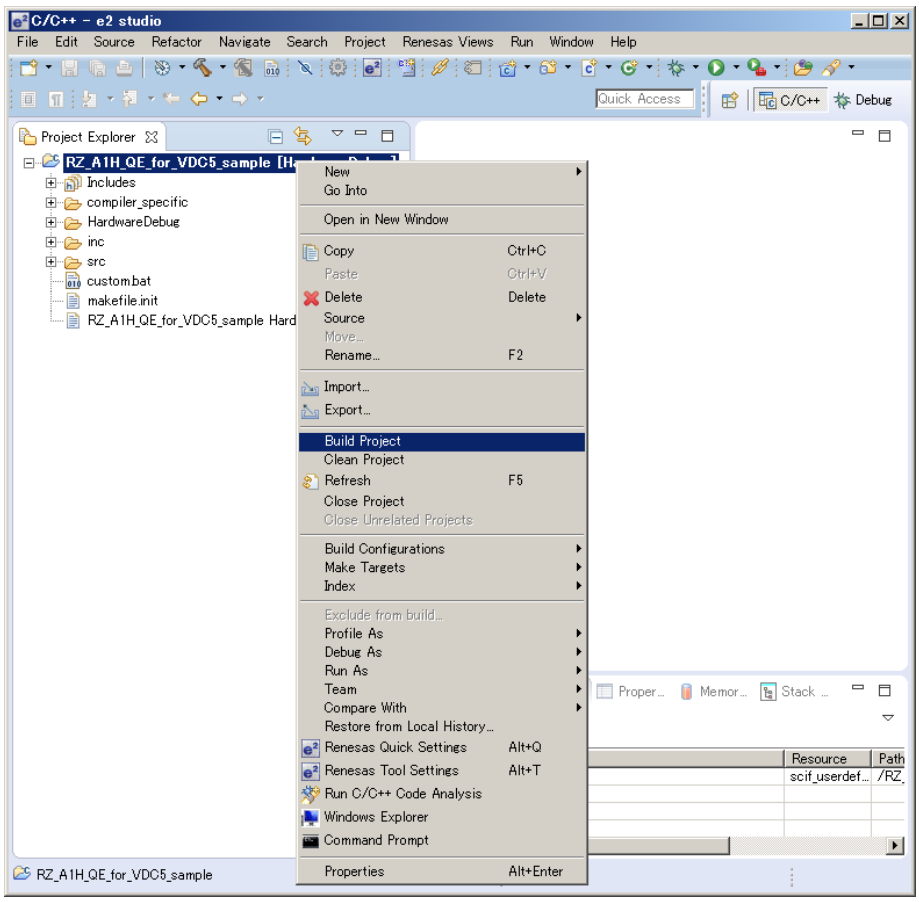


Figure 5.16 Building the Project

You can confirm that building the project has completed successfully when the console output shown in Figure 5.17 is displayed.

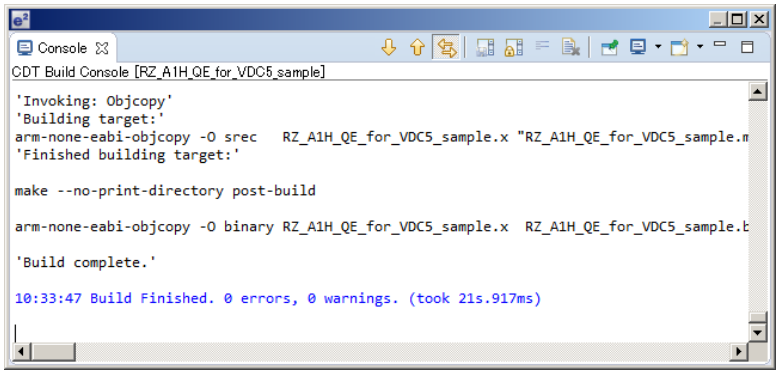


Figure 5.17 Console Output of Result

5.1.6 Confirming Debugger Settings and Display

The RSK CPU board (YR0K77210C000BE) is used to confirm the display on the RSK TFT APP board (YROK77210C000BE). The debugger used is the JLINK LITE ARM debugger bundled with the RSK CPU board (YR0K77210C000BE). The debugger settings are described below.

From the e^2 studio menu, select **Run → Debug Configurations** to display the **Debug Configurations** dialog box (Figure 5.18). Select **Renesas GDB Hardware Debugging**, right-click with the mouse, and select **New**.

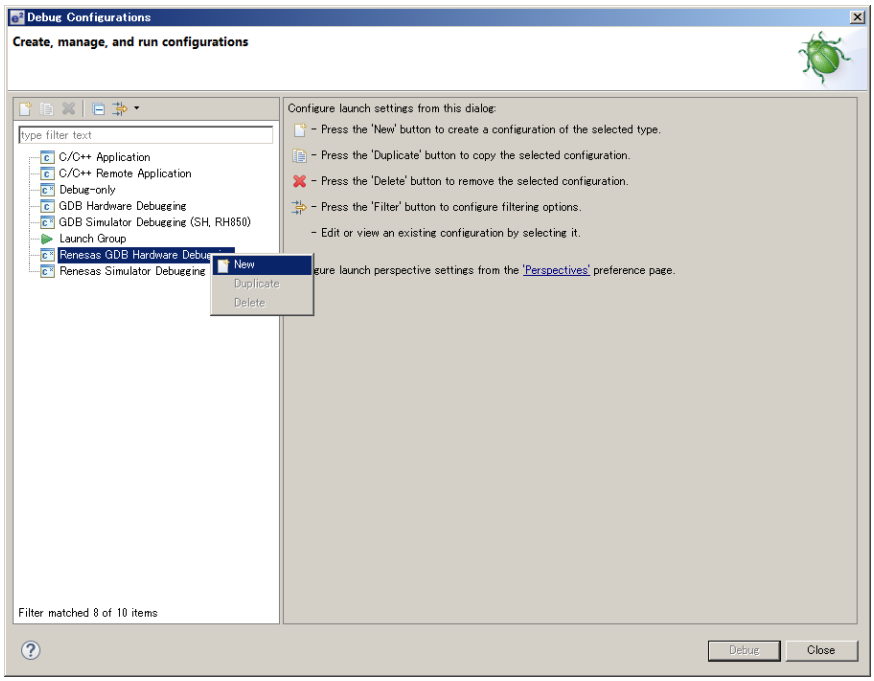


Figure 5.18 Debug Configuration Dialog Box

Figure 5.19 shows a newly created debug configuration. Click the **Browse…** button under **Project**, and select **RZ_A1H_QE_for_VDC5_sample**.

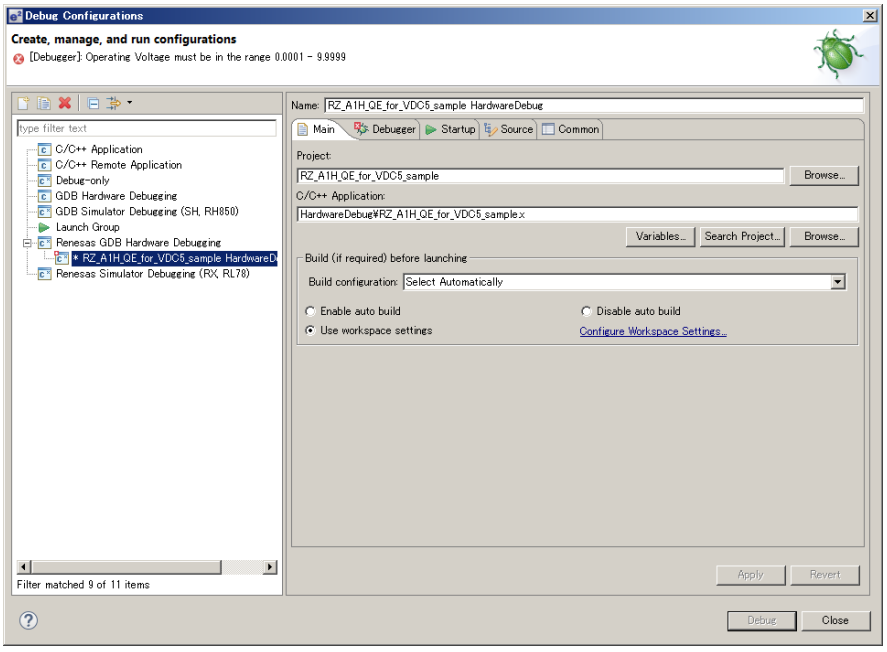


Figure 5.19 Newly Created Debug Configuration

Next, select the **Debugger** tab, make the settings listed below (Figure 5.20), and click the **Apply** button.

[Debug hardware]: J-Link ARM

[Target Device]: R7S721001

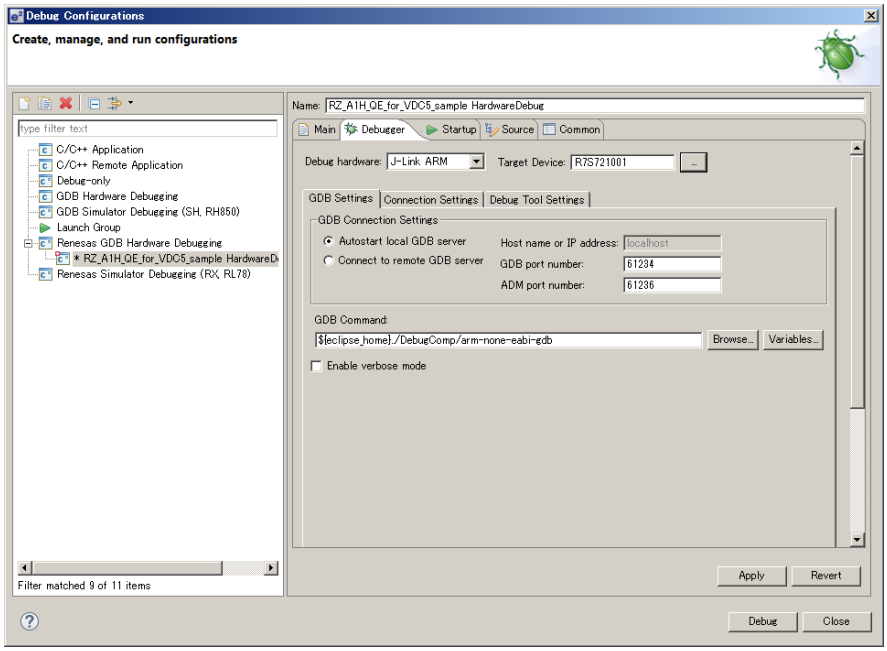


Figure 5.20 Debugger Settings

Next, select the **Startup** tab, and remove the break point that is set by default. Uncheck the box shown in Figure 5.21. If this box it not unchecked, execution will always stop once at main.

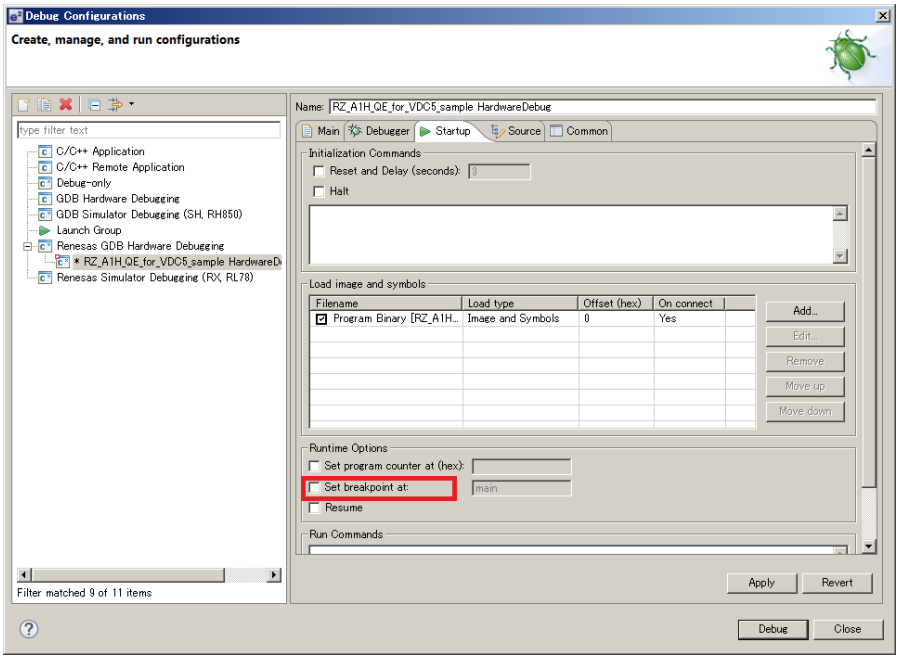


Figure 5.21 Removing Break Point

After making the above settings, if the debugger is not connected, click the **Debug** button to start loading the program and launch the debugging environment (Figure 5.22).

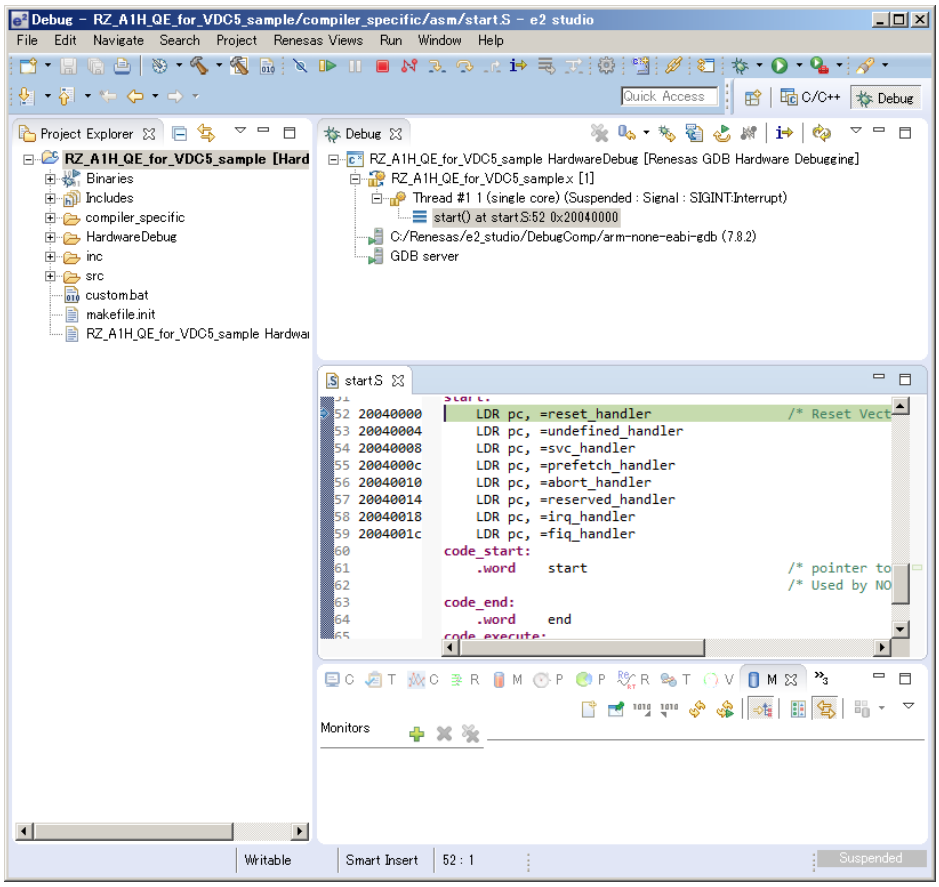


Figure 5.22 Startup Screen of Debugging Environment

After the debugger starts, if the display device settings have been entered correctly, a line one pixel thick is drawn around the outer edge of the screen, as shown in Figure 5.23. This screen is generated by the program according to the display size in the header information generated by QE for Video Display Controller 5. If you cannot confirm that this screen was displayed correctly, for example if it is shifted to the left or to the right, use QE for Video Display Controller 5 to adjust the control signal timing.

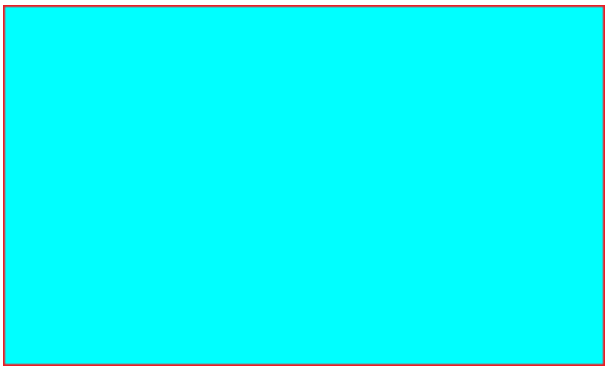
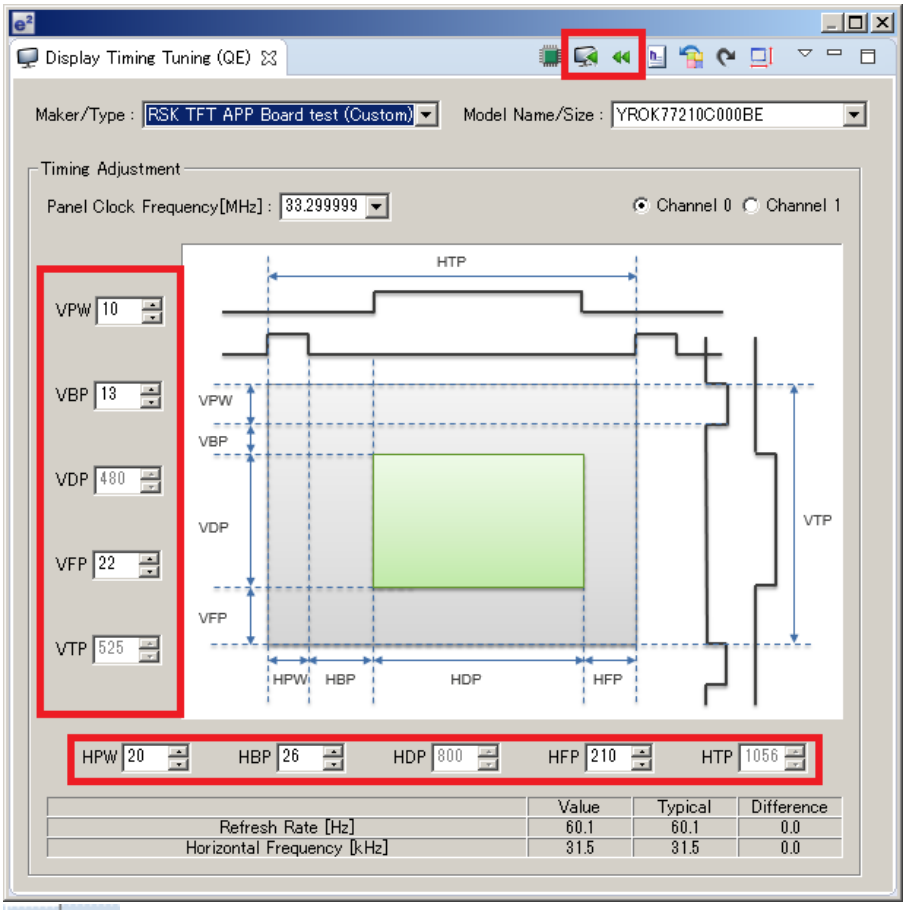


Figure 5.23 Startup Screen

5.2 Real-Time Adjustment Function Using QE for Video Display Controller 5

After connecting the debugger and launching the sample program, you can alter the control signal timing by changing the setting values shown in Figure 5.24. Make adjustments while viewing the results on the connected display device, then re-output the header file.



Left button : Set setting values in registers.
Right button : Set changes in registers in real time.

Figure 5.24 Debugging the Control Signal Timing

Note: When debugging the control signal timing, the contents of the registers of VDC5 are changed directly via the debugger. The sample program assumes the VDC5 graphics plane graphics 2 will be used. If the user makes changes to use other graphics planes, such as graphics 0, graphics 1, or graphics 3, the anticipated operation may not be possible.

5.3 Image Download Function of QE for Video Display Controller 5

After checking the screen shown in Figure 5.23, you can use the image download function of QE for Video Display Controller 5 to display any image you wish. Click the icon shown in Figure 5.25 to display the **Send the Image** dialog box (Figure 5.26).

Figure 5.25 Image Download Icon

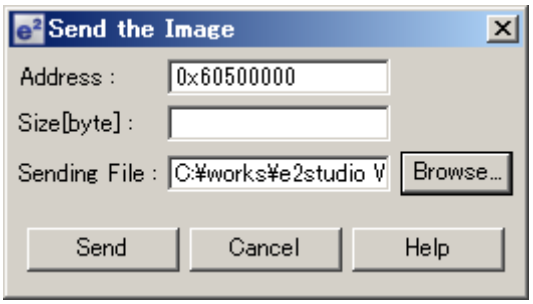


Figure 5.26 Send Image Dialog Box

Address: Specify the address of the buffer for storing display data.

Size [bytes]: Image file size (When not specified, the file size is used.)

Sending File: Image file (binary format)

For **Address**, specify 0x60500000. The sample program reserves the buffer for storing display data with an array variable (FrameBuffer_1[]) and allocates it to VRAM_SECTION_1 section (0x60500000).

For **Sending File**, use a binary image that matches the display data format set in the sample program. The display data format is set to RGB888 in the sample program. Note that you can use ImagePackager,*[1] which is bundled with the sample program, to generate image files for downloading.

Note 1. For details of ImagePackager, refer to the related application note RZ/A1H Group: Graphics Library RGA (R01AN2162JJ/EJ).

6. Adapting the Sample Program to the User Environment

The sample program was created in conjunction with the RSK CPU board (YR0K77210C000BE) and RSK TFT APP board (YROK77210C000BE). In order to use it for checking LCD displays in the user environment, the sample program must modified to match that environment. The locations to be modified are listed below.

6.1 CPU and Board Initialization

The sample program performs initialization to match the RSK CPU board (YR0K77210C000BE). It is therefore necessary to make modifications to match the user environment. The sample program makes settings for external memory such as SDRAM, although external memory is not used. These settings should be modified to match the user environment.

6.2 VDC5 Operation Settings

Some items related to display device control can be specified using QE for Video Display Controller 5 and some cannot. The settings that cannot be made using QE for Video Display Controller 5 are specified by the sample program instead. Therefore, the following three items need to be modified to match the user environment.

- Display device timing control
  The sample program references RSK_TFT_ch0.h when making settings to VDC5. This header file is generated by QE for Video Display Controller 5.
- Panel clock settings
  The sample program references RSK_TFT_panel_clk.h. This file must be modified to match the user environment. Note that this item cannot be specified using QE for Video Display Controller 5.
- GPIO settings
  The sample program uses GRAPHICS_SetLcdPanel_Ch0() in lcd_display_ch0.c to make these settings. This function must be modified to match the user environment. Note that this item cannot be specified using QE for Video Display Controller 5.

The panel clock settings are GPIO that cannot be specified using QE for Video Display Controller 5 are described below.

6.2.1 Panel Clock Settings

VDC5 allows a variety of input clocks to be used as the source clock to generate the panel clock. The selectable source clocks are listed below. Note that the selected source clock is then frequency divided (1/1 to 1/32).

[Source clocks]

- Video clock (VIDEO_X1)
- Video clock (DV_CLK)
- External clock 0 (LCD0_EXTCLK)
- External clock 1 (LCD1_EXTCLK)
- Peripheral clock 1 (P1ϕ)
- LVDS PLL clock
- LVDS PLL clock × 1/7

The sample program uses the selections listed below to produce a “Panel Clock Frequency” of 33.3 MHz, as set in Figure 5.12, to match the specifications of the RSK TFT APP board (YROK77210C000BE).

- Peripheral clock 1 (P1ϕ) 66.6 MHz
- 1/2 division ratio

These settings are located in RSK_TFT_panel_clk.h.

- #define LCD_CH0_PANEL_CLK (VDC5_PANEL_ICKSEL_PERI)
- #define LCD_CH0_PANEL_CLK_DIV (VDC5_PANEL_CLKDIV_1_2)

6.2.2 Using the LVDS PLL to Generate the Panel Clock

The preceding item described how a selection is made among the multiple source clocks to generate the panel clock. It is possible to gain additional flexibility by selecting the LDCS PLL clock as the source clock. The LDCS PLL clock can be used even when not using the LVDS LCD. Some setting examples are provided below.

Appended to the sample program are headers for settings to select the LDCS PLL clock, use the 66.6 MHz peripheral clock 1 (P1ϕ) as the source clock, and generate a 40 MHz clock.

These settings are located in RSK_HDMI_800x600_panel_clk.h. The source clock is the clock generated by the LVDS PLL, which is then frequency divided (1/1).

- #define LCD_CH0_PANEL_CLK (VDC5_PANEL_ICKSEL_LVDS)
- #define LCD_CH0_PANEL_CLK_DIV (VDC5_PANEL_CLKDIV_1_1)

The LVDS PLL settings are shown below. The 66.6 MHz peripheral clock 1 (P1ϕ) is selected as the source clock of the LVDS PLL.

- #define LVDS_PLL_INPUT_CLK (VDC5_LVDS_INCLK_SEL_PERI)

The settings for the LVDS PLL are listed below. For details on the setting values, see 40.5.1, LVDS PLL Settings, in RZ/A1H Group, RZ/A1M Group User's Manual: Hardware.

- #define LVDS_PLL_NIDV (VDC5_LVDS_NDIV_4)
- #define LVDS_PLL_NODIV (VDC5_LVDS_NDIV_4)
- #define LVDS_PLL_NFD (384u)
- #define LVDS_PLL_NRD (5u-1u)
- #define LVDS_PLL_NOD (VDC5_LVDS_PLL_NOD_8)

Table 6.1 lists example settings for other panel clocks.

Table 6.1 Example Panel Clock Settings Using the LVDS PLL

Generated Panel Clock	25.175 [MHz]	40.0 [MHz]	65.0 [MHz]	83.5 [MHz]	85.5 [MHz]
LCD_CH0_PANEL_CLK	VDC5_PANEL_ICKSEL_LVDS				
LCD_CH0_PANEL_CLK_DIV	VDC5_PANEL_CLKDIV_1_1				
LVDS_PLL_INPUT_CLK	VDC5_LVDS_INCLK_SEL_PERI				
LVDS_PLL_NIDV	VDC5_LVDS_NDIV_4				
LVDS_PLL_NODIV	VDC5_LVDS_NDIV_4				
LVDS_PLL_NFD	145	384	312	481	82
LVDS_PLL_NRD	(3u-1u)	(5u-1u)	(5u-1u)	(6u-1u)	(1u-1u)
LVDS_PLL_NOD	8	8	4	4	4

6.3 GPIO Settings

The ports of the RZ/A1 are multiplexed with pins of peripheral modules. The functions of multiplexed pins (alternative functions) are selected by means of register settings. In the present case the pins listed below are set as display device output pins, but multiple pins are multiplexed. The multiplexed RZ/A1H ports are listed below.

Output pin selections (multiplexed ports)

- Vsync: TCON4 (P3_5, P11_10, P11_13)
- Hsync: TCON3 (P3_4, P11_11)
- DE: TCON2 (P3_3, P11_12)

The following port selections are made in the sample program to match the RSK CPU board (YR0K77210C000BE) and RSK TFT APP board (YROK77210C000BE).

Output pin selections (selected ports)

- Vsync: TCON4 (P11_10)
- Hsync: TCON3 (P11_11)
- DE: TCON2 (P11_12)

GRAPHICS_SetLcdPanel_Ch0() in lcd_display_ch0.c is used to make these settings. In addition, settings are made in like manner for the following pins needed for display device control.

Output pin selections (selected ports)

- Panel clock: LCD0_CLK (P11_15)
- Data: LCD DATA23 to LCD DATA0 (P11_7 to P11_0, P10_15 to P10_0)

Modify these settings are necessary to match the display device you are using. Making the appropriate modifications will make it possible to confirm the operation of the display device you are using.

7. Reference Documents

User's Manual

- RZ/A1H Group User's Manual: Hardware
- RZ/A1H Group Renesas Starter Kit+ User's Manual For e^2 studio
  (The latest information can be downloaded from the Renesas Electronics website.)

Application Notes

- RZ/A1H Group Example of Initialization (R01AN1864JJ/EJ)
- RZ/A1H Group Video Display Controller 5 Sample Driver (R01AN1822JJ/EJ)
- RZ/A1H Group Graphics Library "RGA" (R01AN2162JJ/EJ)
  (The latest information can be downloaded from the Renesas Electronics website.)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Oct. 17, 2016	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

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   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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