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H8/300H Tiny Series

PWM Output using Timer W PWM Mode

Introduction

The PWM mode of timer W is used to output PWM waveforms from the FTIOB pin.

Target Device

H8/3664

Contents

1. Specifications

1. The PWM mode of timer W is used to output a PWM waveform from the FTIOB pin.
2. In this sample task, the output PWM waveform has a pulse period of 30.72 ms with a high-level width of 22.5 ms.

2. Description of Functions

1. In this sample task, a PWM waveform is output by using the PWM mode of timer W. Figure 2.1 is a block diagram of timer W PWM mode. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer counter (TCNT) is a 16-bit readable/writable counter that is incremented by either the internal or external clock input. In this sample task, a clock generated by dividing the system clock by 8 is selected as the input clock of TCNT.
- Timer control register W (TCRW) selects the input clock of TCNT and specifies the initial output values of the FTIOA to FTIOD pins. In this sample task, the initial output value of FTIOB is specified as 1.
- Timer mode register W (TMRW) controls starting of the TCNT counter operation and selects the output mode of FTIOB to FTIOD. In this sample task, the PWM mode is specified for the FTIOB pin.
- Timer I/O control register 0 (TIOR0) controls the GRA and GRB. In this sample task, GRA and GRB are specified as output-compare registers, timer W outputs 0 on a compare-match with GRA, and outputs 1 on a compare-match with GRB.
- General register A (GRA) is a 16-bit readable/writable register. In PWM mode (PWMB bit of TMRW is set to 1), this register holds the period of the output PWM waveform.
- General register B (GRB) is a 16-bit readable/writable register. In PWM mode (PWMB bit of TMRW is set to 1), this register holds the duty cycle of the output PWM waveform. When the TIO bit of TCRW is cleared to 0, the GRB specifies the high-level width of the PWM waveform.
- The period of the PWM waveform is calculated by the following equation:

$$\text{Period of PWM waveform} = \frac{1}{\text{System clock}/\ 8} \times 0\text{xF000} = 30.72\ \text{ms}$$

High-level width of the PWM waveform is calculated by the following equation:

$$\text{High-level width of PWM waveform} = \frac{1}{\text{System clock}/\ 8} \times 0\text{xB000} = 22.5\ \text{ms}$$

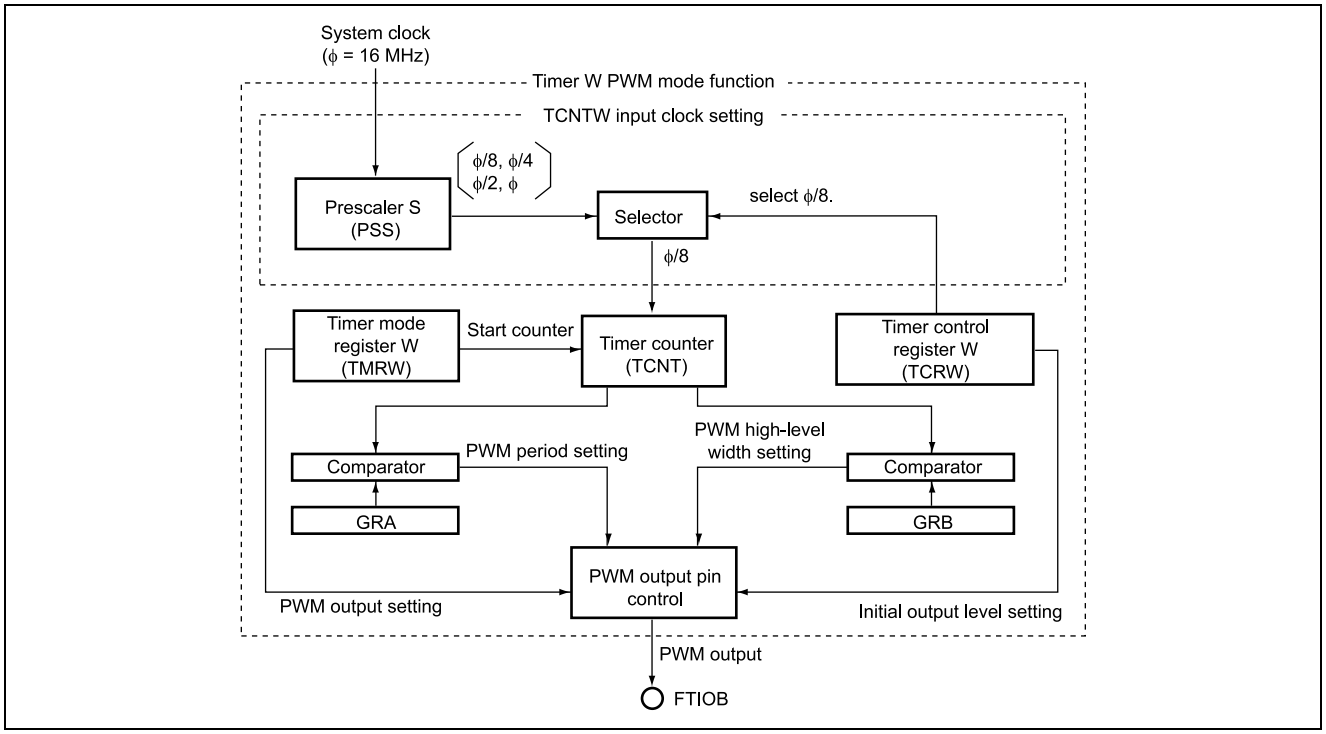


Figure 2.1 Block Diagram of Timer W PWM mode

Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so that the PWM waveform is output by using the PWM mode of timer W.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit up-counter with system clock (16 MHz) input
TCNT	Timer counter W
TCRW	Specifies the input clock of TCNT and initial output level of FTIOB.
TMRW	Controls starting of TCNT counter operation and specifies PWM mode.
GRA	Holds the PWM period.
GRB	Holds the PWM duty cycle (in terms of high-level width of the PWM waveform).
FTIOB pin	PWM output pin

3. Description of Operation

Figure 3.1 illustrates the operation of this sample task. The hardware and software processing is applied in the manner shown in figure 3.1 to produce PWM output by using the PWM mode of timer W.

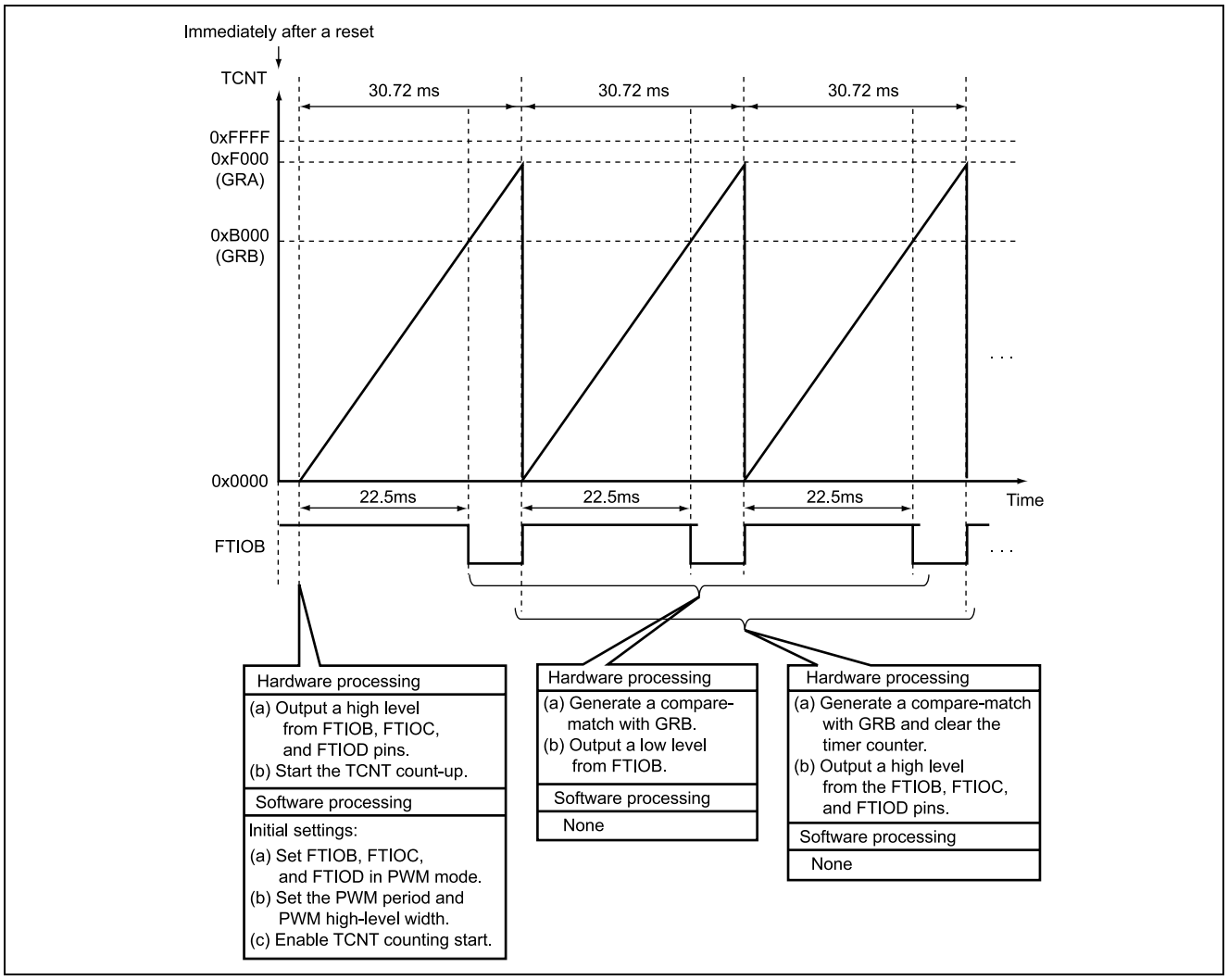


Figure 3.1 Principle of Operation: Output of PWM Waveform by Using PWM Mode of Timer W

4. Description of Software

4.1 Module

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of the Module

Module Name	Label Name	Function
Main routine	main	Initializes the 8-bit counter and sets up for PWM output.

4.2 Description of Arguments

This sample task uses no arguments.

4.3 Description of Internal Registers

The internal registers used in this sample task are described below.

- TMRW Timer mode register W Address: 0xFF80

Bit	Bit Name	Setting	Function
7	CTS	1	Counter start CTS = 0: TCNT counter operation is stopped. CTS = 1: TCNT counter operation has been started.
5	BUFEB	0	Buffer operation B BUFEB = 0: GRD functions as an input-capture/output-compare register. BUFEB = 1: GRD functions as a buffer register for GRB.
4	BUFEA	0	Buffer operation A BUFEA = 0: GRC functions as an input-capture/output-compare register. BUFEA = 1: GRC functions as a buffer register for GRA.
0	PWMB	0	PWM mode B PWMB = 0: Sets the FTIOB pin in the output-compare output mode. PWMB = 1: Sets the FTIOB pin in the PWM output mode.

- TCRW Timer control register W Address: 0xFF81

Bit	Bit Name	Setting	Function
7	CCLR	1	Counter clear CCLR = 0: Specifies the TCNT to operate as the free-running timer. CCLR = 1: Clears TCNT on compare-match A.
6	CKS2	CKS2 = 0	Clock select 2 to 0
5	CKS1	CKS1 = 1	CKS2 = 0, CKS1 = 1, CKS0 = 1: Specifies the input clock for TCNT as $\phi/8$
4	CKS0	CKS0 = 1	
1	TOB	0	Timer output level set B TOB = 1: Specifies the FTIOB pin to output a high level until a compare-match B is generated. TOB = 0: Specifies the FTIOB pin to output a low level until a compare-match B is generated.

- TIERW Timer interrupt enable register W Address: 0xFF82

Bit	Bit Name	Setting	Function
7	OVIE	0	Timer overflow interrupt enable OVIE = 0: Disables interrupts by the OVF flag of TSRW. OVIE = 1: Enables interrupts by the OVF flag of TSRW.
3	IMIED	0	Output compare interrupt D enable IMIED = 0: Disables IMFD interrupts. IMIED = 1: Enables IMFD interrupts.
2	IMIEC	0	Output compare interrupt C enable IMIEC = 0: Disables IMFC interrupts. IMIEC = 1: Enables IMFC interrupts.
1	IMIEB	0	Output compare interrupt B enable IMIEB = 0: Disables IMFB interrupts. IMIEB = 1: Enables IMFB interrupts.
0	IMIEA	0	Output compare interrupt A enable IMIEA = 0: Disables IMFA interrupts. IMIEA = 1: Enables IMFA interrupts.

- TSRW Timer status register W Address: 0xFF83

Bit	Bit Name	Setting	Function
1	IMFB	0	Output compare flag B IMFB = 0: Indicates that no compare-match has occurred between TCNT and GRB IMFB = 1: Indicates that a compare-match has occurred between TCNT and GRB
0	IMFA	0	Output compare flag A IMFA = 0: Indicates that no compare-match has occurred between TCNT and GRA IMFA = 1: Indicates that a compare-match has occurred between TCNT and GRA

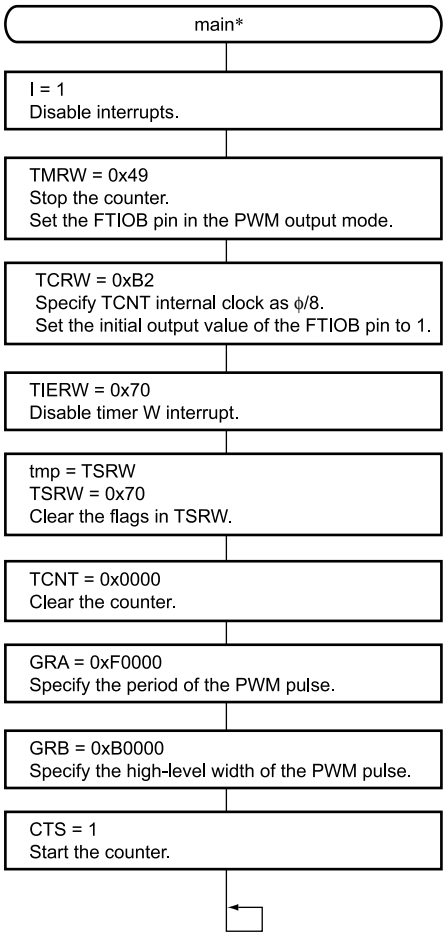
- TCNT Timer counter Address: 0xFF86
  Function: A 16-bit up-counter with an input clock generated by dividing the system clock by 8.
  Setting: 0xFF86
- GRA General register A Address: 0xFF88
  Function: Generates a compare-match A when the value in the GRA matches the TCNT counter value.
  Setting: 0xF000
- GRB General register B Address: 0xFF8A
  Function: Generates a compare-match B when the value in the GRB matches the TCNT counter value.
  Setting: 0xB000

4.4 Description of RAM

This sample task does not use RAM.

5. Flowchart

Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3664-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'PWM Output Function'                                                                                              */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer W PWM Output                                                                                               */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TMRW           *(volatile unsigned char *)0xFF80                  /* Timer Mode Register W                */
#define        TMRW_BIT       (*(struct BIT *)0xFF80)                            /* Timer Mode Register W                */
#define        CTS            TMRW_BIT.b7                                        /* Counter Start                        */
#define        TCRW           *(volatile unsigned char *)0xFF81                  /* Timer Control Register W             */
#define        TIERW          *(volatile unsigned char *)0xFF82                  /* Timer Interrupt Enable Register      */
#define        TSRW           *(volatile unsigned char *)0xFF83                  /* Timer Status Register W              */
#define        TCNT           *(volatile unsigned int *)0xFF86                   /* Time Counter                         */
#define        GRA            *(volatile unsigned int *)0xFF88                   /* General Register A                   */
#define        GRB            *(volatile unsigned int *)0xFF8A                   /* General Register B                   */

/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                       /* SP Set                               */
void main ( void );
```

```
/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                  /* VECTOR SECTOIN SET                        */
void (*const VEC_TBL1[])(void) = {                                      /* 0x00 - 0x0f                               */
     INIT                                                               /* 00 Reset                                  */
};

#pragma section                                                         /* P                                         */

/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                                  /* Interrupt Disable                         */

     TMRW = 0x49;                                                       /* FTIOB Port is PWM Output Mode             */
     TCRW = 0xB2;                                                       /* Set phi/8                                 */
     TIERW = 0x70;                                                      /* Interrupt Disable                         */
     tmp = TSRW;
     TSRW = 0x70;                                                       /* Clear Interrupt Flag                      */

     TCNT = 0x0000;                                                     /* Clear TCNTV                               */
     GRA = 0xF000;                                                      /* Set PWM period                            */
     GRB = 0xB000;                                                      /* Set PWM high level width                  */
     CTS = 1;                                                           /* Counter start                             */

     while(1);
}
```

Link address specifications

Section Name	Address
CV1	0x0000
P	0x0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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