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April 1st, 2010
Renesas Electronics Corporation

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APPLICATION NOTE

Pulse Frequency Measurements Using Event Counter Function

Introduction

Measurement of the frequency of the applied pulse stream input from Timer B1 event input pin (TMIB) using the 8-bit event counter function of Timer B1.

Target Device

H8/300H Tiny Series H8/3687

Contents

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1. Specification

1. Measurement of the frequency of the applied pulse stream input from Timer B1 event input pin (TMIB) using the 8-bit event counter function of Timer B1.
2. The number of rising-edge events of the pulse stream applied from the TMIB input pin is counted during one-second, and the event count for the one-second time-interval is stored in RAM.
3. Measurement of the one-second time-interval is performed using the timebase function of Timer A time clock.

2. Description of Functions Used

1. In this task example, the frequency of the pulse stream input at the TMIB input pin is measured using the Timer B1 event counter function.
   A. Figure 2.1 shows the block diagram of the Timer B1 event counter function which is described as follows:
      — Timer Mode Register B1 (TMB1) is an 8-bit read/write register used to select the interval function and select the input clock.
      — Timer Counter B1 (TCB1) is an 8-bit readable up counter that is incremented by means of the applied internal clock and/or external events. The applied input clock can be selected from a total of eight clocks, seven of which are derived from the system clock divided by 8192, 2048, 512, 256, 64, 16 and 4, and one external clock. In this task example, the edge detection of the TMIB input pin is selected as the TCB1 input clock.
      — Timer B1 Interrupt Request Flag (IRRTB1) is set to 1 by a TCB1 overflow event. If, on the provision that IRRTB1 has been set to 1, Timer B1 Interrupt Enable (IENTB1) of the Interrupt Enable Register (IENR1) is set to 1, and the I bit of the Condition Code register (CCR) is cleared to 0, the Timer B1 interrupt sequence will start on reception of the Timer B1 interrupt.
      — Timer B1 Event Input pin (TMIB) functions as the input pin for the pulse stream that will be subject to the frequency measurements. In this task example, a Timer B1 interrupt will be generated every 160 µs using the Timer B1 auto reload function.

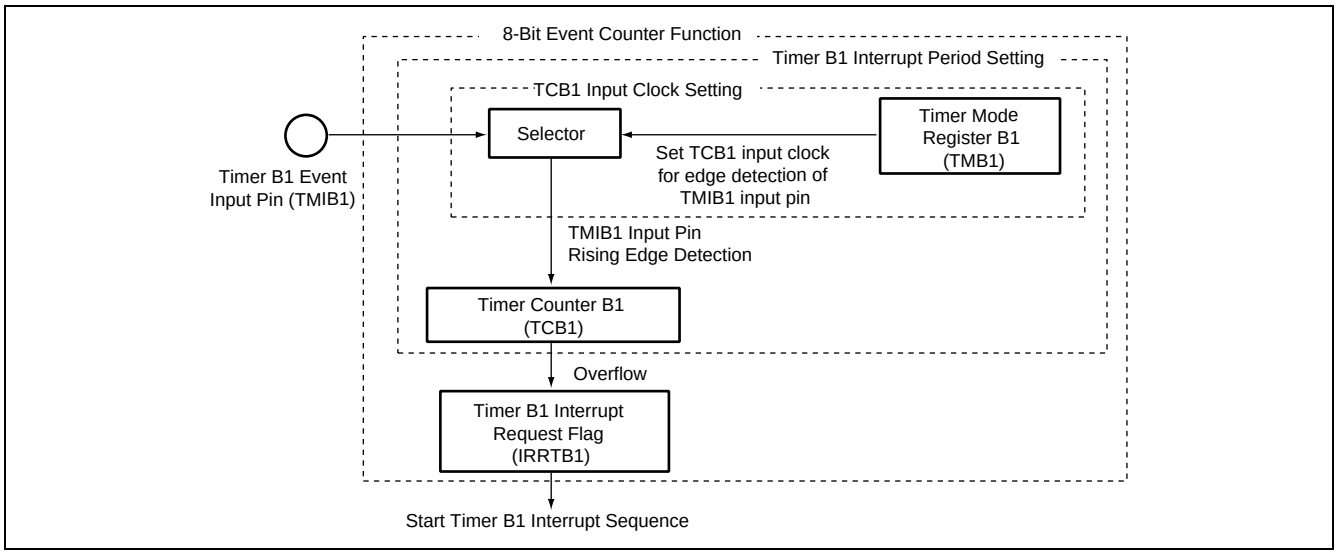


Figure 2.1 Timer B1 Event Counter Function Block Diagram

B. The following is brief description of the method of frequency measurement.
   - When 256 rising-edge input pulse events have been applied to the TMIB input pin, TCB1 overflows and a Timer B1 interrupt is generated.
   - The 8-bit counter set by cnt_1 is incremented during the Timer B1 interrupt sequence,
   - The count value in TCB1 is read out and stored in cnt_2 after an interval of one second has elapsed, at which point the TCB1 increment sequence by the signal applied from the TMIB input pin is stopped.
   - The frequency of the pulse stream applied to the TMIB input pin can be found using the following expression:

     Input Pulse Frequency (Hz) = (Timer B1 Interrupt Event Count) x 256 + (Count Value in TCB1 after a one-second time lapse)
     = (Value in cnt) x 256 +(Value in cnt_1)

   - Since counter (cnt), used to count the Timer B1 interrupt events, is an 8-bit counter, the maximum frequency of the input pulse stream that can be measured is 65.535 kHz.
   - When the 8-bit counter (cnt) that counts the number of Timer B1 interrupt events overflows, frequency measurements are stopped at that instant and the sequence finishes by writing H'00 to cnt and the register (cnt_1) that stores the TCB1 count value after the 1 sec time lapse.

2. Table 2.1 lists the function assignments applicable to this task example. The functions are assigned as indicated in table 1. Frequency measurement is performed by timer B1 event counter function.

Table 2.1 Function Assignment

Function	Function Assignment
TCB1	This is an 8-bit counter to which edge detection for the TMIB input pin is input
TMB1	This register sets the interval function and sets the TCB1 input clock to edge detection for the TMIB input pin
IRRTB1	This reflects the presence/absence of a Timer B1 interrupt request
TMIB	This is the input pin of the pulse stream subject to frequency measurements
IEG1	This sets the input sense of the TMIB pin for rising edge detection
TCNTV	This is an 8-bit counter to which an input clock, derived by dividing the 16 MHz internal operating frequency by 128, is applied
TCRV0	This sets selection of TCNTV input clock, and clears the counter by Compare Match A
TCSRV	This selects PSW and sets the TCA overflow period
TCORA	This sets the compare match value for TCNTV
TCRV1	This selects the TGRV input edge, starts the TCNV input count up, and selects the TCNTV input clock

3. Operational Description

1. Figure 3.1 illustrates the principle of operation described by way of waveform diagrams. As shown in figure 3.1, pulse stream frequency measurements by means of the Timer B1 event counter function are facilitated by both hardware and software operations.

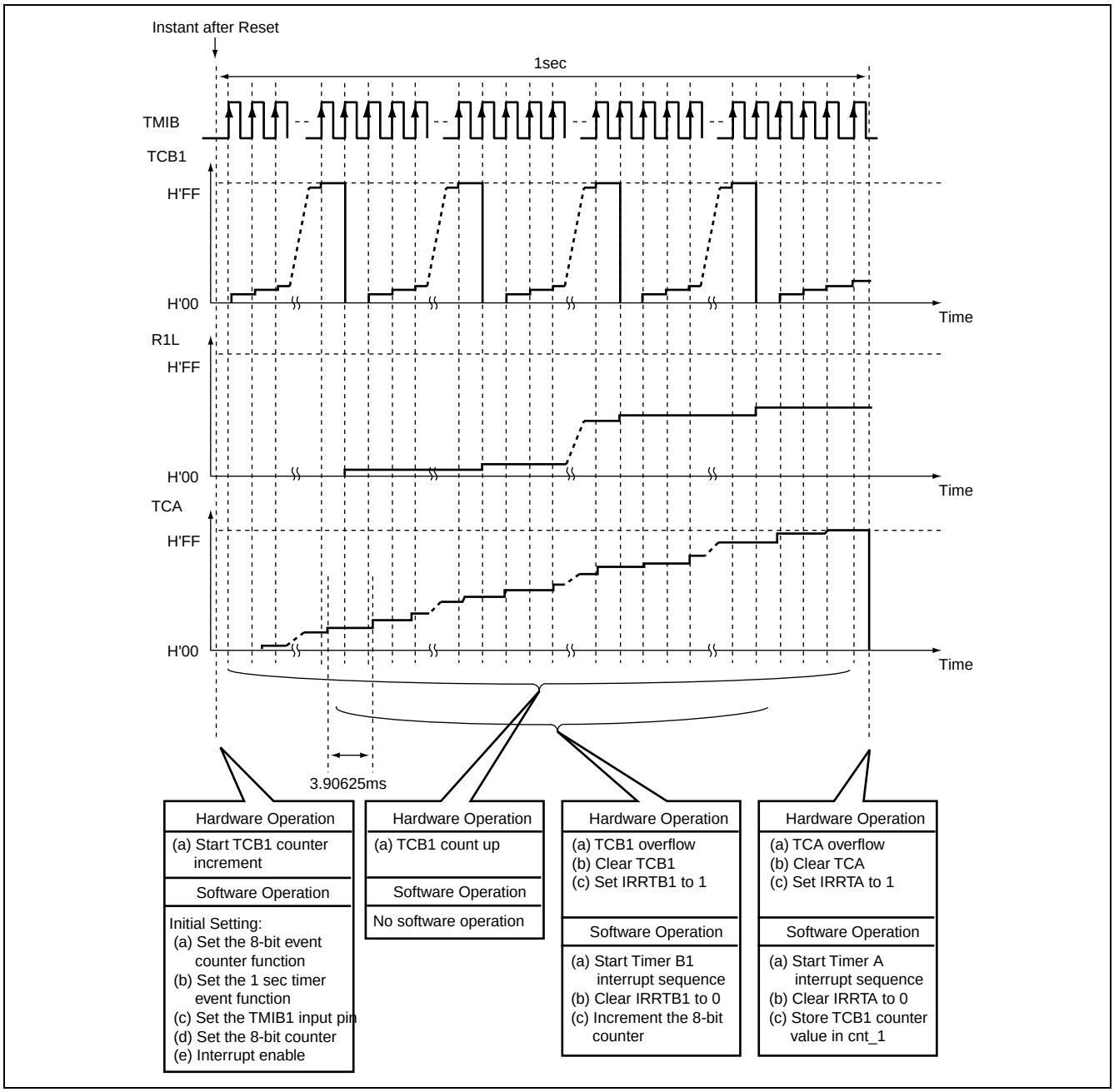


Figure 3.1 Operating Principle of Frequency Measurement by Timer B1 Event Counter Function

4. Software Description

4.1 Module Description

The modules applicable to this task example are listed in table 4.1.

Table 4.1 Module Description

Module Name	Label Name	Function
Main Routine	main	The main routine initializes the stack pointer, sets the event counter function, sets the timebase function, sets the 8-bit counter, enables the interrupts, and initializes Timer B1 on completion of measurements.
8-Bit Counter	TB1INT	In the Timer B1 interrupt sequence, increments the 8-bit counter and performs the process operations when cnt overflows.
1 Sec Time Lapse	TVCMA	In the Timer A interrupt sequence, disables the interrupts by a time lapse of 1 sec and stores the TCB1 count value in cnt_1

4.2 Argument Description

Table 4.2 lists the arguments applicable to this task example.

Table 4.2 Argument Description

Argument Name	Function	Used in	Data Size	I/O
cnt	Stores the 8-bit counter count value after 1-sec time lapse	8-bit counter	1 byte	Output
8-bit counter	Stores TCB1 counter value after 1-sec time lapse	1-sec time lapse	1 byte	Output
1 sec time lapse	Stores counter value that discriminates whether one second has lapsed	1-sec time lapse	2 bytes	Output

4.3 Description of Applicable Internal Registers

Table 4.3 lists the internal registers used in this task example.

Table 4.3 Description of Applicable Internal Registers

Register Name		Functional Description	Address	Setting
IRR2	IRRTB1	Interrupt Request Register 1 (Timer B1 Interrupt Request Flag) : When IRRTB1 is 0, a Timer B1 interrupt is not requested : When IRRTB1 is 1, a Timer B1 interrupt is requested	H'FFF7 Bit 5	0
IENR2	IENTB1	Interrupt Enable Register 1 (Timer B1 Interrupt Enable) : When IENTB1 is 0, Timer B1 interrupt request is disabled : When IENTB1 is 1, Timer B1 interrupt request is enabled	H'FFF5 Bit 5	1

Table 4.3 Description of Applicable Internal Registers (cont)

Register Name		Functional Description	Address	Setting
IEGR2	IEG1	Interrupt Enable Edge Select Register 2 (INT1 Edge Select) : When IEG1 is 1, TMIB input pin edge detection is set for rising-edge detection	H'FFF2 Bit 1	1
TCRV0	CMIEA	Timer Control Register V0 (Timer V Interrupt Enable) : When CMIEA is 0, Timer V interrupt request is disabled : When CMIEA is 1, Timer V interrupt request is enabled	H'FFA0 Bit 6	1
TCRV0 TCRV1	CKS0 to CKS2 ICSK1	Timer Control Register V0 (Clock Select) Timer Control Register V1 (clock Select) : Sets the clock to 1/128 of the internal clock and counts up on the falling edge.	H'FFA0 H'FFA5	CKS0 to CKS2 = 1, 1, 0 ICSK1 = 1
TCSRV	CMFA	Timer Control Status Register V (Timer V Interrupt Request Flag) : When CMFA = 0, Timer V compare match interrupt is not requested : When CMFA = 1, Timer V compare match interrupt is requested	H'FFA1 Bit 6	1
TMB1		Timer Mode Register B1 : When TMB1 is H'7F, the Timer B1 function is set as the interval function and the TCB1 input clock is set for edge detection of TMIB input clock	H'F760	H'7F
TCB1		Timer Counter B1 : This is an 8-bit up counter to which the input edge detection for the TMIB1 pin is applied	H'F761	H'00
TCNTV		Timer Counter V : This is an 8-bit up counter to which the input clock, derived by dividing the 16 MHz clock by 128, is applied	H'FFA4	H'00
TC0RA		Time Constant Register A : When the setting value of TCORA and the count value in TCNTV match, a compare match V is generated	H'FFA2	H'20

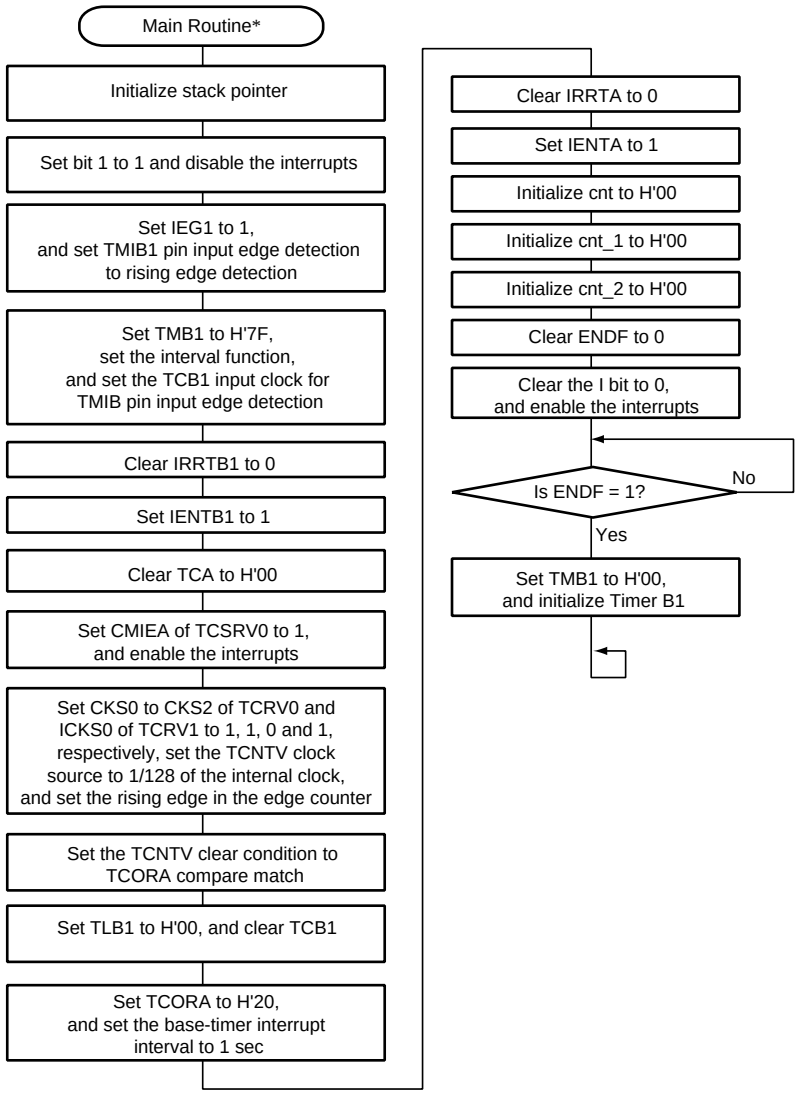
4.4 Description of RAM Used

Table 4.4 lists and describes the RAM used in this task example.

Table 4.4 Description of Applicable RAM

Label Name		Function	Address	Used in
USRF	ENDF	Flag that determines whether or not the input pulse frequency measurements have ended	H'FB80 Bit 0	Main routine 8-bit counter 1-sec time lapse

5. Flowcharts



Note: * In this example, the stack pointer is set by INIT.SRC (assembly language)

Figure 5.1 Main Routine

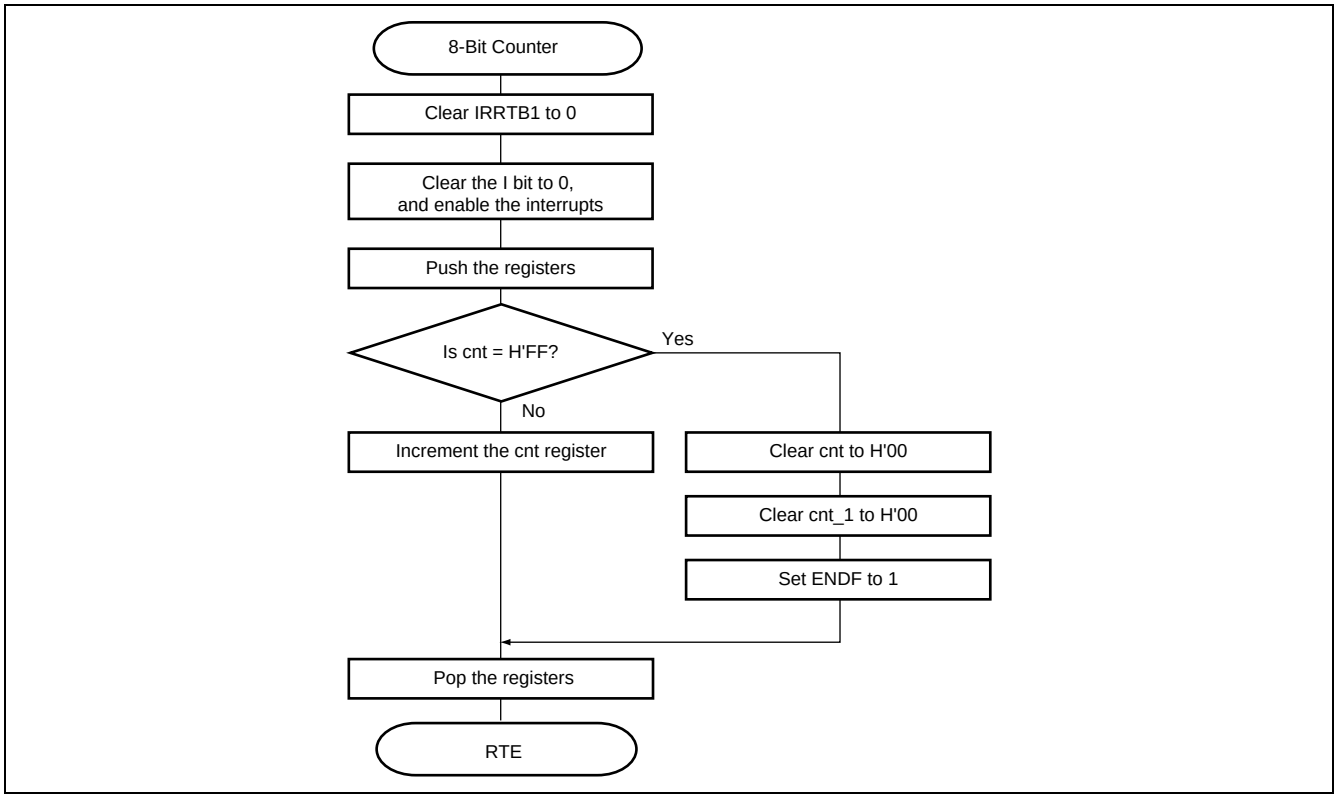


Figure 5.2 Timer B1 Interrupt Service Routine

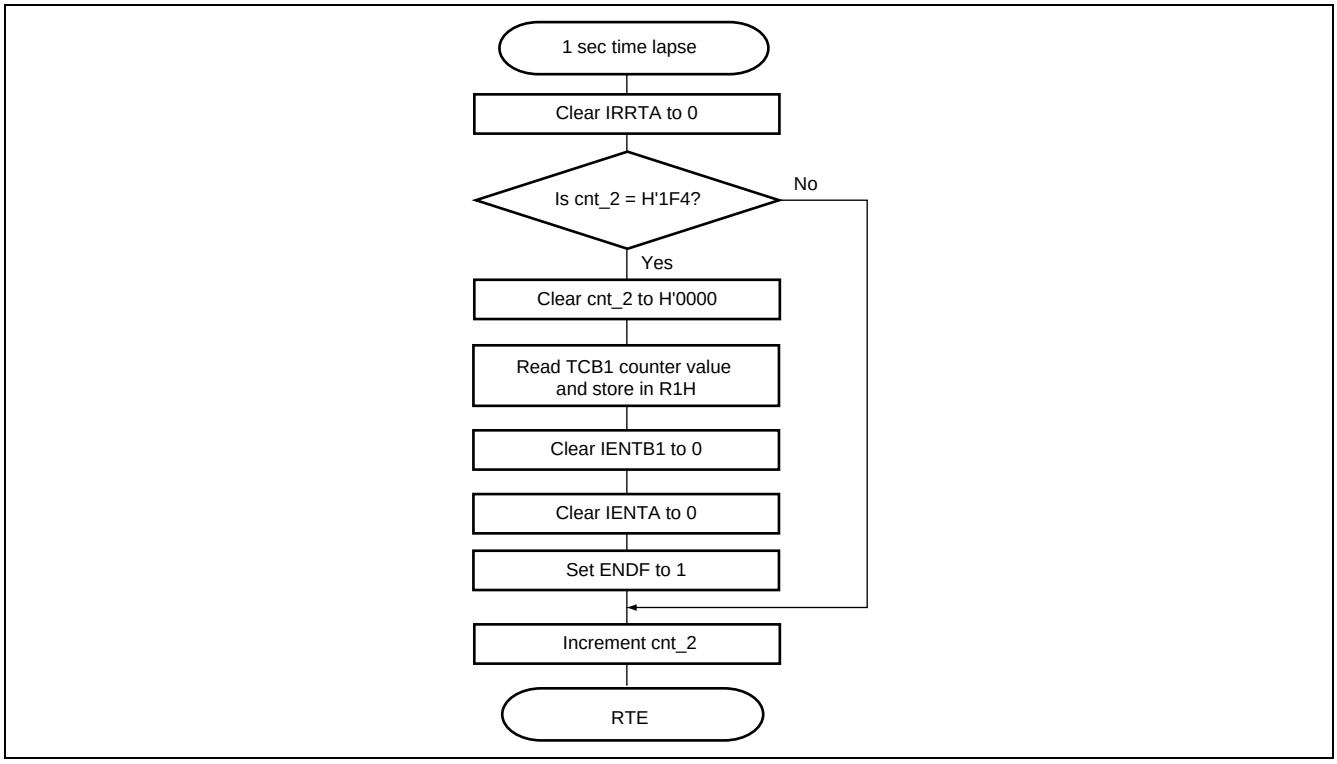


Figure 5.3 Timer V Interrupt Service Routine

6. Program Listing

INIT.SRC (Program List)

```
      .EXPORT   _INIT
      .IMPORT   _main
 ;
      .SECTION  P,CODE
 _INIT:
     MOV.W     #H'FF80,R7
     LDC.B     #B'10000000,CCR
     JMP       @_main
 ;
     .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300HN Series -H8/3687-                             */
/*    Application Note                                      */
/*                                                          */
/* 'Pulse Frequency Measurement by Event Counter Function' */
/*                                                          */
/*    Function                                              */
/*    :Timer B1 8 Bit Event Counter                         */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <C:\ch38\include\machine.h>
```

```
/*******************************************************/
/*    Symbol Definition                                */
/*******************************************************/

struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define        TMB1      *(volatile unsigned char *)0xF760 /* Timer B1 Mode register                    */
#define        TCB1      *(volatile unsigned char *)0xF761 /* Timer B1 Counter Register                 */

#define        TCRV0     *(volatile unsigned char *)0xFFA0 /* Timer Control Rgister V                   */
#define        TCRV0_BIT (*(struct BIT *)0xFFA0)           /* Timer Control Rgister V                   */
#define        CMIEB     TCRV0_BIT.b7                      /* Compare Match Interrupt Enable B          */
#define        CMIEA     TCRV0_BIT.b6                      /* Compare Match Interrupt Enable A          */
#define        OVIE      TCRV0_BIT.b5                      /* Timer Over Flow Interrupt Enable          */
#define        CCLR1     TCRV0_BIT.b4                      /* Counter Clear Bit 1                       */
#define        CCLR0     TCRV0_BIT.b3                      /* Counter Clear Bit 0                       */
#define        CKS2      TCRV0_BIT.b2                      /* Clock Select 2                            */
#define        CKS1      TCRV0_BIT.b1                      /* Clock Select 1                            */
#define        CKS0      TCRV0_BIT.b0                      /* Clock Select 0                            */
#define        TCSRV      *(volatile unsigned char *)0xFFA1/* Timer Control/Status Register             */
#define        TCSRV_BIT   (*(struct BIT *)0xFFA1)         /* Timer Control Rgister V                   */
#define        CMFB      TCSRV_BIT.b7                      /* Compare Match Interrupt Flag B            */
#define        CMFA      TCSRV_BIT.b6                      /* Compare Match Interrupt Flag A            */
#define        OVFTCSRV_BIT.b5                             /* Timer Over Flow Interrupt Enable          */
#define        OS3TCSRV_BIT.b3                             /* Output Select3                            */
#define        OS2TCSRV_BIT.b2                             /* Output Select2                            */
#define        OS1TCSRV_BIT.b1                             /* Output Select1                            */
#define        OS0TCSRV_BIT.b0                             /* Output Select0                            */
#define        TCORA     *(volatile unsigned char *)0xFFA2 /* Time Constant Register A                  */
#define        TCORB     *(volatile unsigned char *)0xFFA3 /* Time Constant Register B                  */
#define        TCNTV     *(volatile unsigned char *)0xFFA4 /* Timer Counter V1                          */
```

```
#define        TCRV1     *(volatile unsigned char *)0xFFA /* Timer Control Register V1                */
#define        TCRV1_BIT   (*(struct BIT *)0xFFA5)        /* Timer Control Rgister V                  */
#define        TVEG1     TCRV1_BIT.b4                     /* TRGV Input Edge Select 1                 */
#define        TVEG0     TCRV1_BIT.b3                     /* TRGV Input Edge Select 0                 */
#define        TRGE      TCRV1_BIT.b2                     /* TCNTV Count Up TCNTV Count Up Disable    */
#define        ICKS0     TCRV1_BIT.b0                     /* Internal Clock Select                    */

#define        IEGR1     *(volatile unsigned char *)0xFFF2 /* Interrupt Edge Select Register 1        */
#define        IEGR1_BIT (*(struct BIT *)0xFFF2)          /* Interrupt Edge Select Register 1        */
#define        IEG3      IEGR1_BIT.b3                     /* IRQ3 Edge Select                        */
#define        IEG2      IEGR1_BIT.b2                     /* IRQ2 Edge Select                        */
#define        IEG1      IEGR1_BIT.b1                     /* IRQ1 Edge Select                        */
#define        IEG0      IEGR1_BIT.b0                     /* IRQ0 Edge Select                        */
#define        IENR1     *(volatile unsigned char *)0xFFF4  /* Interrupt Enable Register 1            */
#define        IENR1_BIT (*(struct BIT *)0xFFF4)          /* Interrupt Enable Register 1             */
#define        IEN3      IENR1_BIT.b3                     /* IRQ3 Interrupt Enable                   */
#define        IEN2      IENR1_BIT.b2                     /* IRQ2 Interrupt Enable                   */
#define        IEN1      IENR1_BIT.b1                     /* IRQ1 Interrupt Enable                   */
#define        IEN0      IENR1_BIT.b0                     /* IRQ0 Interrupt Enable                   */
#define        IENR2     *(volatile unsigned char *)0xFFF5 /* Interrupt Enable Register 2            */
#define        IENR2_BIT (*(struct BIT *)0xFFF5)          /* Interrupt Enable Register 2             */
#define        IENTB1    IENR2_BIT.b5                     /* Timer B1 Interrupt Enable               */
#define        IRR1      *(volatile unsigned char *)0xFFF6 /* Interrupt Flag Register 1              */
#define        IRR1_BIT  (*(struct BIT *)0xFFF6)          /* Interrupt Flag Register 1               */
#define        IRRI3     IRR1_BIT.b3                      /* IRQ3 Interrupt Request Flag             */
#define        IRRI2     IRR1_BIT.b2                      /* IRQ2 Interrupt Request Flag             */
#define        IRRI1     IRR1_BIT.b1                      /* IRQ1 Interrupt Request Flag             */
#define        IRRI0     IRR1_BIT.b0                      /* IRQ0 Interrupt Request Flag             */
#define        IRR2      *(volatile unsigned char *)0xFFF7 /* Interrupt Flag Register 2              */
#define        IRR2_BIT  (*(struct BIT *)0xFFF7)          /* Interrupt Flag Register 2               */
#define        IRRTB1    IRR2_BIT.b5                      /* Timer B1 Interrupt Request Flag         */

#define        PMR1      *(volatile unsigned char *)0xFFE0 /* Port Mode Register 1                   */
#define        PMR1_BIT  (*(struct BIT *)0xFFE0)          /* Port Mode Register 1                    */
#define        IRQ1      PMR1_BIT.b5                      /* TMIB1 Input Pin                         */

#pragma        interrupt    (TB1INT)
#pragma        interrupt    (TVCMA)
```

```
/*********************************************************/
/* Function Definitions                                  */
/*********************************************************/
extern    void    INIT ( void );                          /* SP Set                              */
void      main      ( void );
void      TVCMA     ( void );
void      TB1INT    ( void );

/*********************************************************/
/*    RAM define                                         */
/*********************************************************/
unsigned char    USRF;                                    /* User Flag Area                      */
unsigned char    cnt;                                     /* 8 Bit Counter                       */
unsigned char    cnt_1;                                   /* TCB1 Value                          */
unsigned int     cnt_2;                                   /* 1 Sec Counter                       */

extern void _INITSCT();

/*********************************************************/
/*    Timer B1 Interrupt                                 */
/*********************************************************/
void TB1INT ( void )
{

     IRRTB1 = 0;                                          /* Clear IRRTB1                        */
     set_imask_ccr(0);                                    /* Interrupt Enable                    */

     if(cnt == 0xFF)
     {
         cnt = 0x00;                                      /* 8 Bit Counter Clear                 */
         cnt_1 = 0x00;                                    /* TCB1 Store Counter Initialize       */

         USRF = 0x01;
     }
     else
     {
         cnt = cnt+1;                                     /* 8 Bit Counter Increment             */
     }
}
```

```
/*********************************************************/
/*    Timer V Interrupt                                  */
/*********************************************************/
void TVCMA( void )
{
     CMFA = 0;                                    /* Clear IMIFA_0 to 0                        */

     if(cnt_2 == 0x1F4)                           /* 1 Sec Passed ?                            */
     {
        cnt_2 = 0x0000;                           /* 1 Sec Couter Clear                        */

        cnt_1 = TCB1;                             /* Store TCB1                                */
        USRF = 0x01;                              /* Program End                               */
        IENTB1 = 0;                               /* Timer B1 Interrupt Disable                */
        CMIEA = 0;                                /* Timer V Compaire Match A Interrupt Disable */
     }
     else
     {
        cnt_2 = cnt_2 + 1;                        /* 1 Sec Counter Count Up                    */
     }
}
```

Link Address Designation

Section Name	Address
CV1	H'0000
P	H'0100
V	H'FB80