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April 1st, 2010
Renesas Electronics Corporation

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H8/300L SLP Series

Pulse Counting by the 16-Bit Event Counter

Introduction

Rising edges of pulses input to Event Input Pin (TMIF) are counted. Counting 1024 rising edges, the operation is completed.

Target Device

H8/38024

Contents

1. Specifications

1. Rising edges of pulses input to Timer F Event Input Pin (TMIF) are counted using the Timer F 16-bit event counter function.
2. The Timer Counter F (TCF) is set to count the rising edges of external clock. Counting is continued until 1024 rising edges are counted.
3. Counting 1024 rising edges, input of external clock to the TCF is stopped and the operation is completed.

2. Description of Functions

1. In this task example, pulses input to the TMIF input pin are counted using Timer F 16-bit event counter function.
   A. Figure 2.1 shows the block diagram of the Timer F 16-bit event counter function which is described below.
   - The Timer Counter (TCF) is a 16-bit read/write up counter and is counted up by an internal or external clock which is input. The input clock can be selected from four clocks obtained by dividing the system clock by 4, 6 and 32, and subclock / 4, and an external clock. In this task example, an external clock is selected as the TCF input clock.
   - The Timer Control Register F (TCRF) is an 8-bit read/write register. It switches over 16 bit/8 bit modes, selects an input clock from among the four internal clocks and external events.
   - The Timer Control/Status Register F (TCSRF) is an 8-bit register. It selects the counter clearing, sets overflow flag and compare match flag, and enables/disables the overflow interrupt requests.
   - An external clock is input through Timer F Event Input Pin (TMIF).

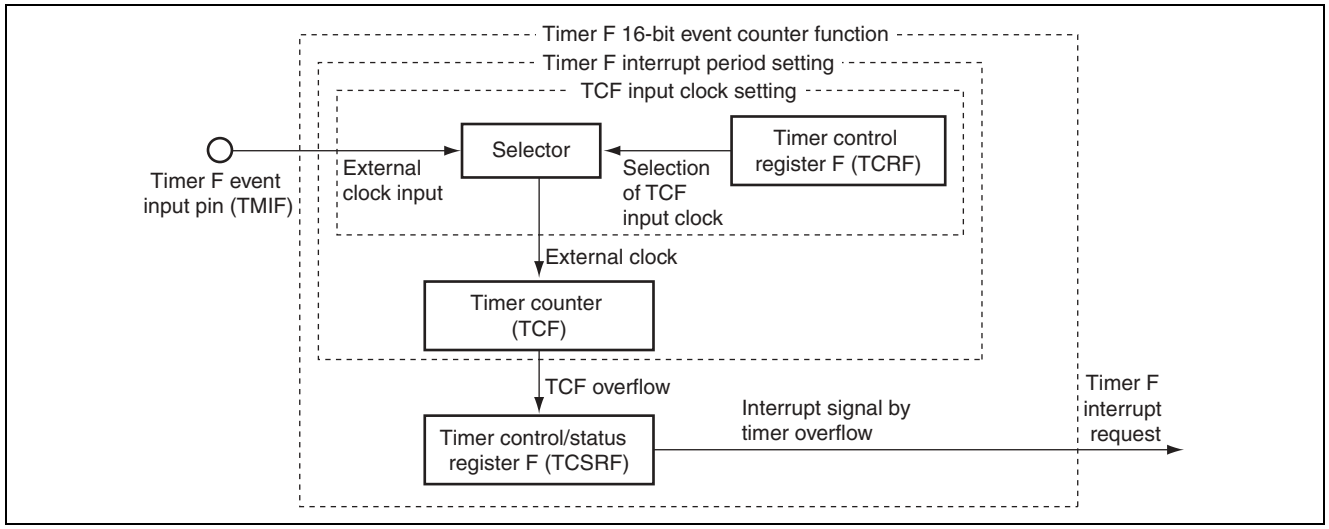


Figure 2.1 Block Diagram of Timer F 16-bit Event Counter Function

2. Table 2.1 shows function assignment in this task example. The functions are assigned as shown in table 2.1 and input pulses are counted by the Timer F 16-bit event counter function.

Table 2.1 Assignment of Functions

Function	Assignment
TCF	A 16-bit counter using external clock as input
TCRF	TCF input clock setting
TCSRF	Controls interrupt request signals by timer overflow
IENTFH	Enables Timer FH overflow interrupt requests.
IRRTFH	Timer FH overflow interrupt flag
TMIF	Pulse input pin

3. Principle of Operation

1. Figure 3.1 illustrates the principle of operation of this sample task. As shown in figure 3.1, input pulses are counted by the Timer F 16-bit event counter function by means of hardware processing and software processing.

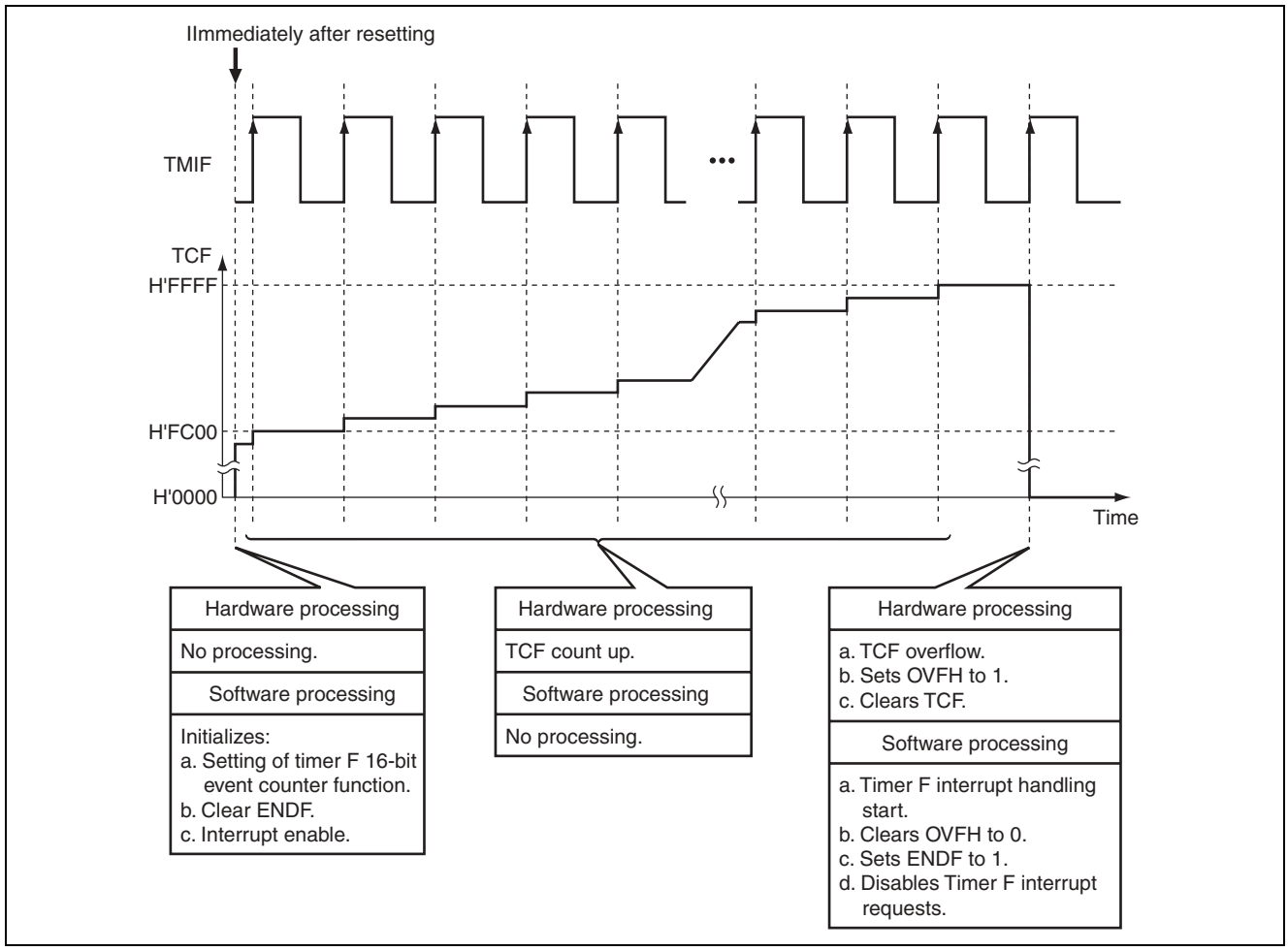


Figure 3.1 Operation Principle of Counting Input Pulses by Timer F 16-Bit Event Counter Function

4. Description of Software

4.1 Modules

Table 4.1 describes the modules in this task example.

Table 4.1 Description of Modules

Module	Label	Function
Main Routine	main	Sets the 16-bit event counter function, enables interrupts and stops operation when the 1024 times rising edge of the TCF input clock is counted.
Count Start	tfint	Sets ENDF to 1 and disables Timer F interrupts in Timer F interrupt handling.

4.2 Arguments

No arguments are used in this task example.

4.3 Internal registers

Table 4.2 describes the internal registers in this task example.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
TCRF	CKSH2 CKSH1 CKSH0	Timer Control Register F (Clock Select H) If (CKSH2 = 0, CKSH1 = 0 and CKSH0 = 0) or (CKSH2 = 0, CKSH1 = 0 and CKSH0 = 1) or (CKSH2 = 0, CKSH1 = 1 and CKSH0 = 0), TCF operates as a 16-bit counter.	H'FFB6 Bit 6 Bit 5 Bit 4	CKSH2 = 0 CKSH1 = 0 CKSH0 = 0
	CKSL2 CKSL1 CKSL0	Timer Control Register F (Clock Select L) If (CKSL2 = 0, CKSL1 = 0 and CKSL0 = 0) or (CKSL2 = 0, CKSL1 = 0 and CKSL0 = 1) or (CKSL2 = 0, CKSL1 = 1 and CKSL0 = 0), TCF counts at the rising/falling edge of external clock.	H'FFB6 Bit 2 Bit 1 Bit 0	CKSL2 = 0 CKSL1 = 0 CKSL0 = 0
TCSRF	OVFH	Timer Control/Status Register F (Timer Overflow Flag H) If OVFH = 0, TCF does not overflow. If OVFH = 1, TCF overflows.	H'FFB7 Bit 7	0
	CMFH	Timer Control/Status Register F (Compare Match Flag H) If CMFH = 0, compare match F is not generated. If CMFH = 1, compare match F is generated.	H'FFB7 Bit 6	0
	OVIEH	Timer Control/Status Register F (Timer Overflow Interrupt Enable H) If OVIEH = 0, TCF overflow interrupt requests are disabled. If OVIEH = 1, TCF overflow interrupt requests are enabled.	H'FFB7 Bit 5	1
	CCLRH	Timer Control/Status Register F (Counter Clear H) If CCLRH = 0, clearing TCF by compare match is disabled. If CCLRH = 1, clearing TCF by compare match is enabled.	H'FFB7 Bit 4	0

Register		Function	Address	Setting
TCF		Timer Counter F A 16-bit up counter using Timer F Event (TMIF) as input.	H'FFB8	H'F000
PMR1	IRQ3	Port Mode Register 1 (P17/$\overline{\text{IRQ3}}$/TMIF Pin Function Switch) If $\overline{\text{IRQ3}}$ = 0, set to P17 input/output pin. If $\overline{\text{IRQ3}}$ = 1, set to $\overline{\text{IRQ3}}$/TMIF input pin.	H'FFC8 Bit7	1
IEGR	IEG3	IRQ Edge Select Register (IRQ3 Edge Select) If IEG3 = 0, falling edge of IRQ3/TMIF pin input is detected. If IEG3 = 1, rising edge of IRQ3/TMIF pin input is detected.	H'FFF2 Bit 3	1
IENR2	IENTFH	Interrupt Enable Register 2 (Timer FH Interrupt Enable) Enables/disables timer FH interrupt requests. If IENTFH = 0, Timer FH interrupt requests are disabled. If IENTFH = 1, Timer FH interrupt requests are enabled.	H'FFF4 Bit 3	1
IRR2	IRRTFH	Interrupt Request Register 2 (Timer FH Interrupt Request Flag) Indicates whether or not a Timer FH interrupt is requested. If IRRTFH = 0, a Timer FH interrupt is not requested. If IENTFH = 1, a Timer FH interrupt is requested.	H'FFF7 Bit 3	0

4.4 Description of RAM

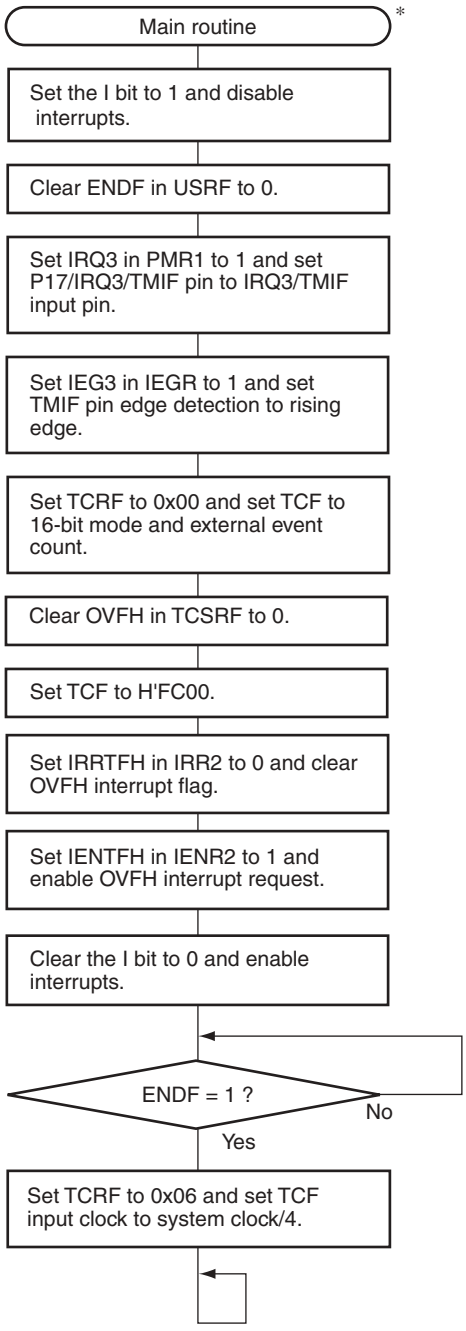
The RAMs used in this task example are described in table 4.3 below.

Table 4.3 Description of RAM

Label		Function	Address	Used in
USRF	ENDF	Flag to indicate that 1024 rising edges of input pulses have been detected.	H'FB80 Bit 0	Main Routine Count Start

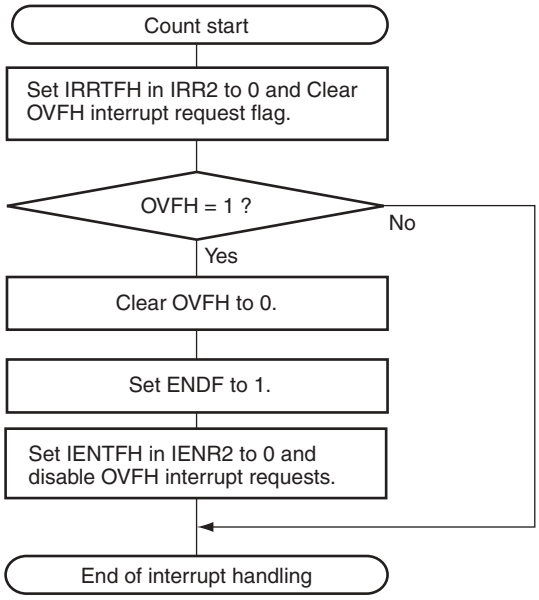
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer F Overflow Interrupt routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Measurement of Input Pulses by 16-bit                                                                              */
/*   Event Counter Function'                                                                                            */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Timer F 16bit Timer Counter                                                                                       */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TCRF        *(volatile unsigned char *)0xFFB6       /* Timer Control Register F                */
#define     TCRF_BIT    (*(struct BIT *)0xFFB6)                 /* Timer Control Register F                */
#define     TOLH        TCRF_BIT.b7                             /* Toggle Output Level F                   */
#define     CKSH2       TCRF_BIT.b6                             /* Clock Select H2                         */
#define     CKSH1       TCRF_BIT.b5                             /* Clock Select H1                         */
#define     CKSH0       TCRF_BIT.b4                             /* Clock Select H0                         */
#define     TCSRF       *(volatile unsigned char *)0xFFB7       /* Timer Control Status Register F         */
#define     TCSRF_BIT   (*(struct BIT *)0xFFB7)                 /* Timer Control Status Register F         */
#define     OVFH        TCSRF_BIT.b7                            /* Timer Overflow Flag H                   */
#define     CMFH        TCSRF_BIT.b6                            /* Compare Match Flag H                    */
```

```
#define     OVIEH       TCSRF_BIT.b5                        /* Timer Overflow Interrupt Enable          */
#define     CCLRH       TCSRF_BIT.b4                        /* Output Select 3                          */
#define     TCFH        *(volatile unsigned char *)0xFFB8   /* Timer Counter FL                         */
#define     TCFL        *(volatile unsigned char *)0xFFB9   /* Timer Counter FL                         */
#define     PMR1_BIT    (*(struct BIT *)0xFFC8)             /* Port Data Register 1                     */
#define     IRQ3        PMR1_BIT.b7                         /* P17/IRQ3 Select                          */
#define     IEGR_BIT    (*(struct BIT *)0xFFF2)             /* Interrupt Enable Register 2              */
#define     IEG3        IEGR_BIT.b3                         /* IEG0 Edge Select                         */
#define     IENR2       *(volatile unsigned char *)0xFFF4   /* Interrupt Enable Register 2              */
#define     IENR2_BIT   (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2              */
#define     IENTFH      IENR2_BIT.b3                        /* Timer FH Interrupt Enable                */
#define     IENTFL      IENR2_BIT.b2                        /* Timer FL Interrupt Enable                */
#define     IRR2_BIT    (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2             */
#define     IRRTFH      IRR2_BIT.b3                         /* Timer FH Interrupt Request Flag          */
#define     IRRTFL      IRR2_BIT.b2                         /* Timer FL Interrupt Request Flag          */

#pragma interrupt   (tfint)
/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                  /* SP Set                                   */
void        main ( void );
void        tfint ( void );

/************************************************************************************************************/
/*  RAM define                                                                                              */
/************************************************************************************************************/
unsigned char   USRF;                                       /* User Flag Area                           */

#define     USRF_BIT    (*(struct BIT *)&USRF)
#define     ENDF        USRF_BIT.b0                         /* End Flag                                 */

/************************************************************************************************************/
/*  Vector Address                                                                                          */
/************************************************************************************************************/
#pragma section     V1                                      /* Vector Section Set                       */
void (*const VEC_TBL1[])(void) = {                          /* 0x0000 - 0x000F                          */
    INIT                                                    /* 0x0000 Reset Vector                      */
};
#pragma section     V2                                      /* Vector Section Set                       */
void (*const VEC_TBL2[])(void) = {
    taint                                                   /* 0x001E Timer F Interrupt Vector          */
};

#pragma section                                             /* P                                        */
/************************************************************************************************************/
/*  Main Program                                                                                            */
/************************************************************************************************************/
void    main ( void )
{
    int tmp;

    set_imask_ccr(1);                                       /* Interrupt Disable                        */

    ENDF = 0;                                               /* Initialize ENDF                          */

    IRQ3 = 1;                                               /* Input Terminal Select TMIF               */
    IEG3 = 1;                                               /* Edge Select TMIF                         */
```

```
    TCRF = 0x00;                                    /* Initialize Clock Select              */
    tmp = TCSRF;                                    /* Dummy Read for Flag Clear            */
    TCSRF = 0x20;                                   /* Initialize Overflow Interrupt        */

    TCFH = 0xFC;                                    /* Clear Timer Counter F                */
    TCFL = 0x00;                                    /* Clear Timer Counter F                */

    IRRTFH = 0;                                     /* Clear IRRTFH                         */
    IENTFH = 1;                                     /* Timer FH Interrupt Enable            */

    set_imask_ccr(0);                               /* Interrupt Enable                     */

    while(ENDF ! = 1){                              /* ENDF = 1 ?                           */
        ;
    }

    TCRF = 0x06;                                    /* Initialize Clock Select              */

    while(1){
        ;
    }
}

/*****************************************************************************************************************/
/*  Timer F Interrupt                                                                                            */
/*****************************************************************************************************************/
void    tfint ( void )
{
    IRRTFH = 0;

    if ( OVFH == 1 ){
        OVFH = 0;                                   /* Clear OVFH                           */
        ENDF = 1;                                   /* Set ENDF                             */
        IENTFH = 0;                                 /* Timer FH Interrupt Disable           */
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'001E
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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