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M16C/64 Group

Procedure for Using the PLL Clock as the CPU Clock Source

1. Abstract

This application note describes the procedure for using the PLL clock as the CPU clock source. The PLL clock is produced by the PLL frequency synthesizer (one of the four clock generating circuits). Table 1 shows outline specifications of the main clock oscillator circuit and PLL frequency synthesizer.

Table 1. Outline Specifications of the Main Clock Oscillator Circuit and PLL Frequency Synthesizer

Item	Main clock oscillator circuit	PLL frequency synthesizer
Purposes of use	<ul style="list-style-type: none"> • Clock source for the CPU • Clock source for peripheral functions 	<ul style="list-style-type: none"> • Clock source for the CPU • Clock source for peripheral functions
Clock frequency	0–20 MHz	10–25 MHz
Connectable resonator	<ul style="list-style-type: none"> • Ceramic resonator • Crystal resonator 	— Note 1
Resonator connecting pin	XIN, XOUT	— Note 1
Oscillation stop, reoscillation	Available	Available
State after reset	Oscillating	Turned off
Other	Externally generated clock input usable	— Note 1

Note 1: The PLL frequency synthesizer uses the main clock oscillator circuit as its reference clock source. Therefore, these items of specifications depend on the main clock oscillator circuit.

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

- Microcomputers: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Description of the Application Example

The PLL clock is produced from the main clock by the PLL frequency synthesizer.

Figure 1 shows the relationship between the main clock and the PLL frequency synthesizer.

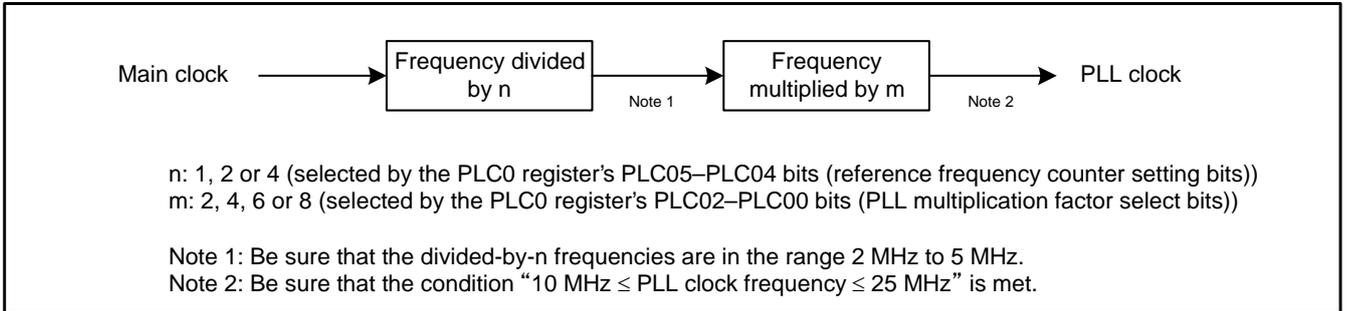


Figure 1. Relationship between the Main Clock and the PLL Frequency Synthesizer

Table 2 shows an example of PLL clock frequency settings.

Table 2. PLL Clock Frequency Setup Example

Main clock (Xin)	Set value		PLL clock
	PLC05–PLC04 bits	PLC02–PLC00 bits	
10MHz	01b (divided by 2)	010b (multiplied by 4)	20MHz
5MHz	00b (not divided)	010b (multiplied by 4)	
12MHz	10b (divided by 4)	100b (multiplied by 8)	24MHz
6MHz	01b (divided by 2)	100b (multiplied by 8)	

Figure 2 shows the procedure for using the PLL clock as the CPU clock source.

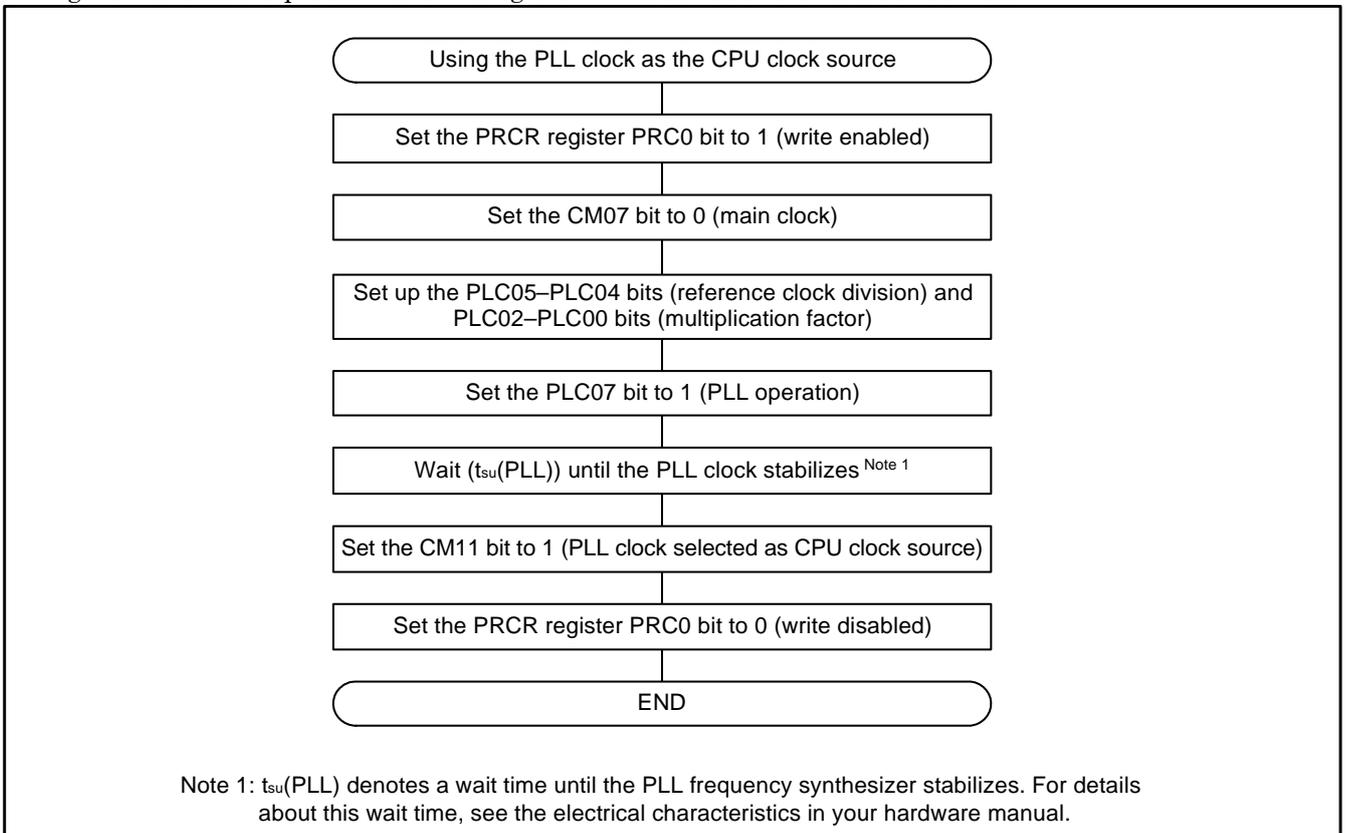


Figure 2. Procedure for Using the PLL Clock as the CPU Clock Source

4. How to Set Up

The following shows how to set up the registers in conformity with the procedure in Figure 2, "Procedure for Using the PLL Clock as the CPU Clock Source." For details about each register, see the hardware manual of the M16C/64 group.

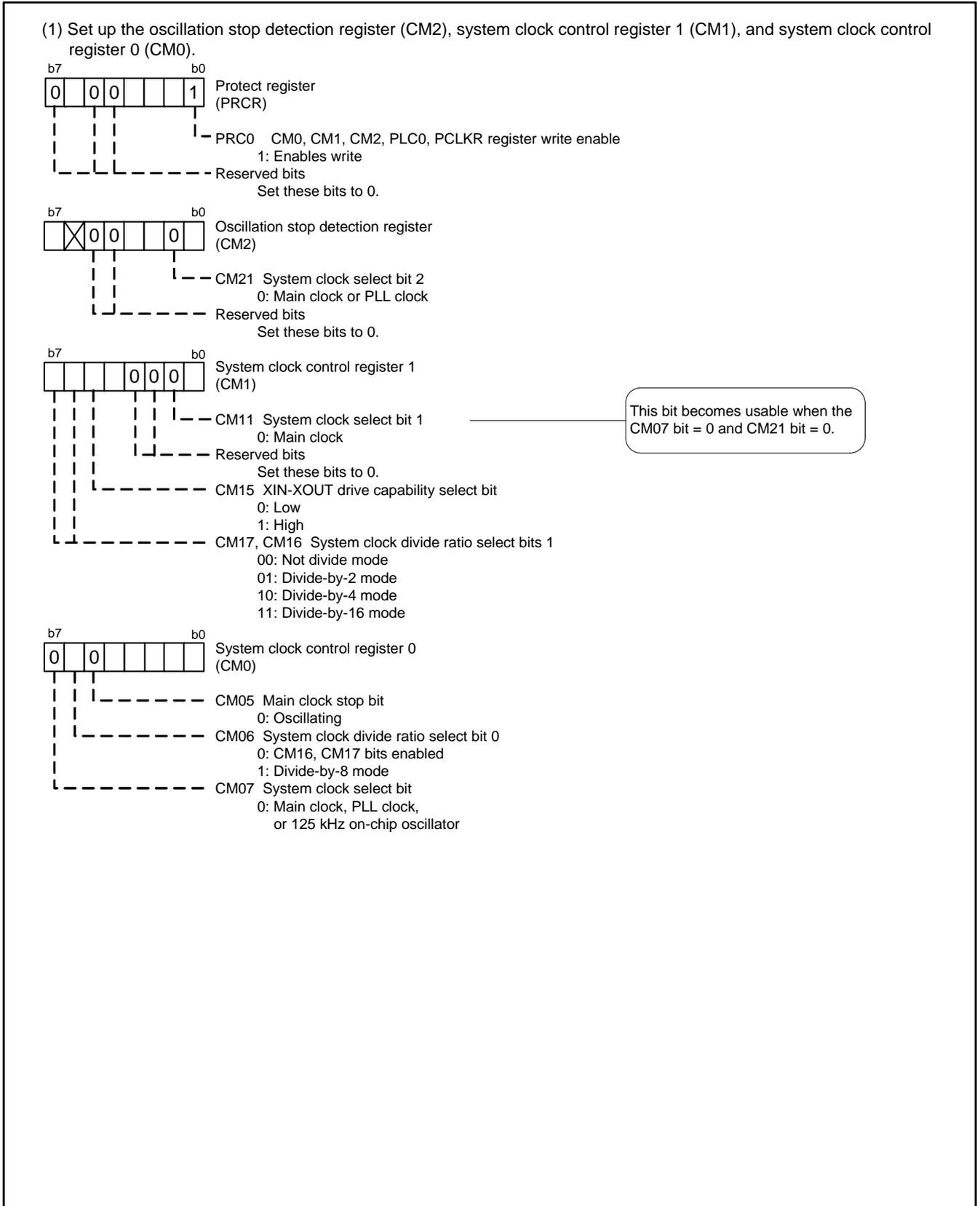
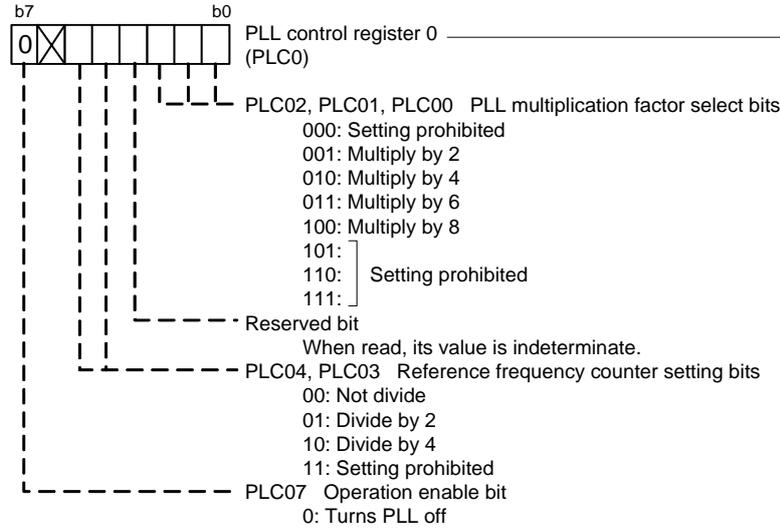


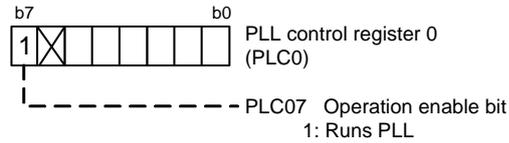
Figure 3. Procedure for Setting Up the Registers to Use the PLL Clock as the CPU Clock Source (1)

(3) Set PLC04 and PLC03 (reference frequency counter setting bits) and PLC02, PLC01 and PLC00 (PLL multiplication factor select bits).



To set up the PLL control register (PLC0), write to it when the PLC07 bit = 0 (PLL turned off).

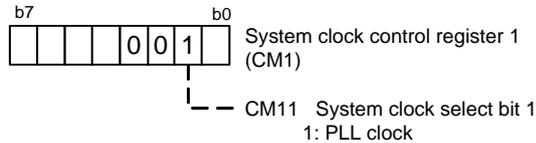
(4) Set the PLL operation (PLC07 bit).



Before setting the PLC07 bit to 1 (PLL operating), set the CM05 bit to 0 (main clock oscillating) first.

(5) Wait a while ($t_{su}(PLL)$) until the PLL oscillation stabilizes.

(6) Switch the system clock from the main clock to the PLL clock.



(7) Set up the protect register (PRCR).

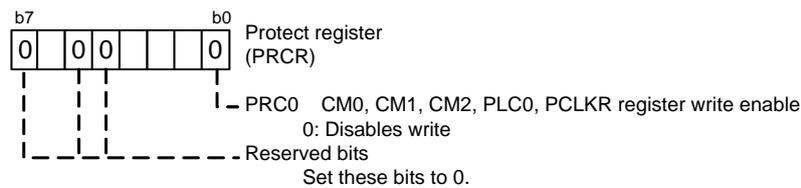


Figure 4. Procedure for Setting Up the Registers to Use the PLL Clock as the CPU Clock Source (2)

5. Sample Programs

Download a sample program from the Renesas Technology website. Click the screen menu “Application Note” on the left side of the M16C family’s top web page.

6. Reference Documents

Hardware manual

M16C/64 Group Hardware Manual

(Get the latest version from the Renesas Technology website.)

Technical updates and technical news

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