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RENESAS

M32C/85 Group

Procedure to Use the PLL Clock as the CPU Clock Source

1. Abstract

This application note describes a procedure to use the PLL clock as the CPU clock source.

2. Introduction

This application note is applied to the following condition:
Applicable MCU:M32C/85 Group

The program on this application note can also be used when operating other microcomputers within the M16C Family, provided they have the same SFR (Special Function Registers) as the M32C/85 Group. However, some functions may have been modified. Refer to each device's hardware manual for details. Use functions covered in this application note only after careful evaluation.

3. Detailed Description

The PLL-synthesized main clock becomes the PLL clock. To select the PLL clock as the CPU clock source, multiply and divide the main clock by given values.
Table 1 lists the PLL clock settings.

Table 1. PLL Clock Settings

m=f(XIN)

The PLC02 to PLC00 bits in the PLC0 register (to select the programmable counter)	The PLC12 bit in the PLC1 register (to select a PLL clock division)	Multiply	PLL clock
011 (multiply-by-6)	0 (divide-by-2)	Multiply-by-3	3 m
	1 (divide-by-3)	Multiply-by-2	2 m
100 (multiply-by-8)	0 (divide-by-2)	Multiply-by-4	4 m
	1 (divide-by-3)	Multiply-by-8/3	8/3 m

Figure 1 shows a flowchart to select the PLL clock as the CPU clock source.

```
┌─────────────────────────────────────────────────────────────────────────────┐
│                                                                               │
│              ╭──────────────────────────────────────────╮                     │
│              │  Select the PLL clock as the CPU clock    │                     │
│              ╰──────────────────────────────────────────╯                     │
│                                    │                                          │
│         ┌──────────────────────────────────────────┐                          │
│         │ Set the PRC1 and PRC0 bits in the PRCR    │                          │
│         │ register to "1" (write enabled)           │                          │
│         └──────────────────────────────────────────┘                          │
│                                    │                                          │
│         ┌──────────────────────────────────────────┐    ┌───────────────────┐ │
│         │ Set the PLC0 and PLC1 registers.         │    │ NOTE:             │ │
│         │ Set the PLC07 bit in the PLC0 register    │    │ The compiler must │ │
│         │ to "0" (PLL stopped).                     │    │ translate the     │ │
│         │ Change the PLC0 and PLC1 register         │    │ C code into the   │ │
│         │ settings in the 16-bit unit at the same   │    │ assembly code,    │ │
│         │ time.                                     │    │ and must not      │ │
│         └──────────────────────────────────────────┘    │ optimize the C-   │ │
│                                    │                     │ language          │ │
│         ┌──────────────────────────────────────────┐    │ instructions to   │ │
│         │ Set the PLC07 bit in the PLC0 register    │    │ the assembly      │ │
│         │ to "1" (PLL operated).                    │    │ instructions      │ │
│         │ Change the PLC0 and PLC1 register         │    │ except MOV.W.     │ │
│         │ settings in the 16-bit unit at the same   │    └───────────────────┘ │
│         │ time.                                     │                          │
│         └──────────────────────────────────────────┘                          │
│                                    │                                          │
│         ┌──────────────────────────────────────────┐                          │
│         │ Take tsu(PLL) until a PLL clock           │                          │
│         │ oscillation stabilizes                    │                          │
│         └──────────────────────────────────────────┘                          │
│                                    │                                          │
│         ┌──────────────────────────────────────────┐                          │
│         │ Set the CM17 bit in the CM1 register to   │                          │
│         │ "1" (PLL clock selected as the CPU clock  │                          │
│         │ source)                                   │                          │
│         └──────────────────────────────────────────┘                          │
│                                    │                                          │
│         ┌──────────────────────────────────────────┐                          │
│         │ Set the PRC1 and PRC0 bits to "0"         │                          │
│         │ (write disabled)                          │                          │
│         └──────────────────────────────────────────┘                          │
│                                    │                                          │
│              ╭──────────────────────────────────────────╮                     │
│              │                  END                      │                     │
│              ╰──────────────────────────────────────────╯                     │
│                                                                               │
└─────────────────────────────────────────────────────────────────────────────┘
```
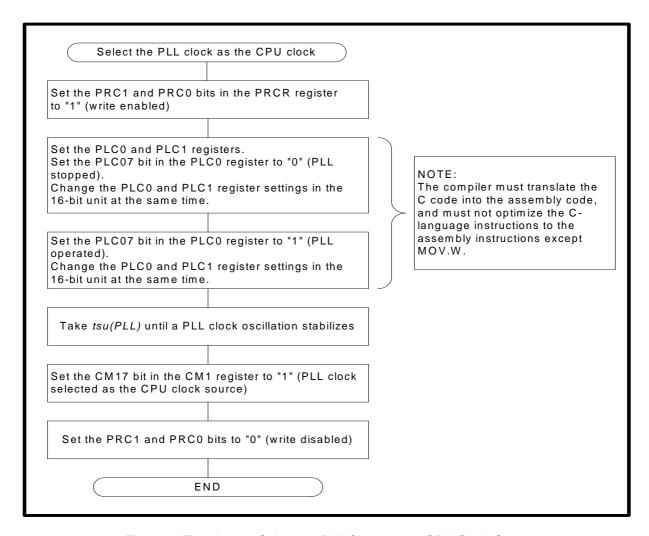
Figure 1. Flowchart to Select the PLL Clock as the CPU Clock Source

4. Sample Program

```
/*""FILE COMMENT""***********************************************
* System Name     : M32C/85 Program Collection
* File Name       : rjj05b0719_src.c
* Version         : 1.00
* Contents        : Procedure to use PLL clock as CPU clock source
* Customer        :
* Model           :
* Order           :
* CPU             : M32C/85 Group
* Compiler        : NC308WA (V.5.20 Release 1)
* OS              : Nothing
* Programmer      :
* Note            :
***********************************************************************
* Copyright,2005 RENESAS TECHNOLOGY CORPORATION
* AND RENESAS SOLUTIONS CORPORATION
***********************************************************************
* History     : 2005.2.28 Ver 1.00
*""FILE COMMENT END""*******************************************/

/*************************************/
/*    include file                  */
/*************************************/
#include "sfr32c85.h"

/*************************************/
/*    define                        */
/*************************************/
typedef unsigned short    USHORT16;

#define plc_reg           (volatile)plc     /* PLL control register 0,1  */
#define PLL_WAIT_1MS      800U              /* 1msec @8MHz   */
#define PLL_WAIT_CNT      5U                /* 5msec         */

/*************************************/
/*    Declaration of function prototype    */
/*************************************/
void main(void);

/*************************************/
/*    main                          */
/*************************************/
void main(void){

    USHORT16    i,j;
```

```
/*========================================*/
/*= Procedure to Use PLL Clock as CPU Clock Source =*/
/*========================================*/
    prcr = 0x03;                            /* Protect off                      */
    /* Protect register                                                         */
    /* 00000011B                                                                */
    /*        | |                                                               */
    /*        | +---- (PRC0):Protect bit 0                                      */
    /*        |       Enables writing to CM0,CM1,CM2,MCD,PLC0,PLC1             */
    /*        |         0:Write disable                                         */
    /*        |        *1:Write enable                                          */
    /*        +----- (PRC1):Protect bit 1                                       */
    /*                 Enables writing to PM0,PM1,PM2,INVC0,INVC1              */
    /*                  0:Write disable                                         */
    /*                 *1:Write enable                                          */

    plc_reg = 0x0254;
    plc_reg = 0x02d4;
    /* (note):Set the PLC0 and PLC1 registers                                   */
    /*         simultaneously in a 16-bit unit.                                 */
    /* (note):Set the PLC1 register when the PLC07 bit                          */
    /*         is set to "0"(PLL stop).                                         */
    /* PLL control register 0                                                   */
    /* X1010100B                                                                */
    /* | | | | | | | | |                                                        */
    /* | | | | | +++---- (PLC02-PLC00):Programmable counter select bit          */
    /* | | | | |        011:Multiply-by-6                                       */
    /* | | | | |       *100:Multiply-by-8                                       */
    /* | | | | +------- (b3):Reserved bit (Set to "0")                          */
    /* | | | +-------- (b4):Reserved bit (Set to "1")                           */
    /* | | +--------- (b5):Reserved bit (Set to "0")                            */
    /* | +---------- (b6):Reserved bit (Set to "1")                             */
    /* +----------- (PLC07):Operation enable bit                                */
    /*              0:PLL is off                                                */
    /*              1:PLL is on                                                 */
    /* PLL control register 1                                                   */
    /* 00000010B                                                                */
    /* | | | | | | | | |                                                        */
    /* | | | | | | | +---- (b0):Reserved bit (Set to "0")                       */
    /* | | | | | | +----- (b1):Reserved bit (Set to "1")                        */
    /* | | | | | +------ (PLC12):PLL clock division switch bit                  */
    /* | | | | |         *0:Divide-by-2                                         */
    /* | | | | |          1:Divide-by-3                                         */
    /* | | | | +------- (b3):Reserved bit (Set to "0")                          */
    /* | | | +-------- (b4):Reserved bit (Set to "0")                           */
    /* +++--------- (b7-b5):Reserved bit (Set to "0")                           */
```

```
    for (i = 0; i < PLL_WAIT_CNT; i++) {         /* about 5ms wait     */
        for (j = 0; j < PLL_WAIT_1MS; j++) {     /* Main clock 8MHz    */
        }
    }

    cm1 = 0xa0;
    /* System clock control register 1                                 */
    /* 10100000B                                                        */
    /* | | | | | | | |                                                  */
    /* | | | | | | | |+---- (CM10):All clock stop control bit           */
    /* | | | | | | | |          0:Clock oscillates                      */
    /* | | | |++++----- (b4-b1):Reserved bit (Set to "0")               */
    /* | |+--------- (b5):Reserved bit (Set to "1")                     */
    /* |+---------- (b6):Reserved bit (Set to "0")                      */
    /* +----------- (CM17):CPU clock select bit 1                       */
    /*                   1:PLL clock                                    */

    prcr = 0x00;                               /* Protect on          */

    while(1) {
    }
}
```

5.   Reference

Hardware Manual
   M32C/85 Group Hardware Manual Rev.1.03
   (Use the latest version on the home page: http://www.renesas.com/en/m16c)

TECHNICAL UPDATE/TECHNICAL NEWS
   (Use the latest information on the home page: http://www.renesas.com/en/m16c)

6.   Contact Information

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