

RZ/T2ME

Procedure for Converting from RZ/T2M to RZ/T2ME

Introduction

This document describes how to convert FSP configuration to run the RZ/T2M sample code as RZ/T2ME.

Target Device

RZ/T series: RZ/T2ME

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1. Introduction

1.1 Overview

This document describes how to convert FSP configuration to run the RZ/T2M sample code as RZ/T2ME .

1.2 Related Documentation Files

The related documentation files are shown in the following.

1.2.1 RZ/T2, RZ/N2 Getting Started with Flexible Software Package

This document can know how to operation FSP configurator and the easy usage of e² studio or EWARM.

Please access the following Renesas web site,

download “**RZ/T2,RZ/N2 Getting Started with Flexible Software Package**” from the Documentation area.

- <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzt2m-high-performance-multi-function-mpu-realizing-high-speed-processing-and-high-precision-control>

The screenshot shows the 'Documentation' page on the Renesas website. It features a search bar and a table of documents. The 'Quick Start Guide' document is highlighted with a red box. The table has columns for Type, Title, and Date.

Type	Title	Date
Release Note	RZ/T2M Group Encoder I/F EnDat Safety sample program PDF 583 KB 日本語 Related Files: • Sample Code	Jul 5, 2024
Quick Start Guide	RZ/T2,RZ/N2 Getting Started with Flexible Software Package PDF 11.97 MB	Jun 28, 2024

1.2.2 RZ/T2M Sample Code

Also, access the Renesas web site, select and download the **RZ/T2M sample code** you want to run as **RZ/T2ME** from the Sample Code area.

The screenshot shows the 'Sample Code' page on the Renesas website. It features a search bar and a table of sample code entries. The first entry is highlighted with a red box. The table has columns for Type, Title, and Date.

Type	Title	Date
Sample Code	RZ/T2M Group Encoder I/F EnDat Safety sample program [Software=RZ/T2M Encoder I/F EnDat Safety sample program v1.20],[Toolchains=GNU ARM Embedded v12.2.1.am-12-24;IAR Embedded Workbench for ARM v9.32.2] ZIP 4.95 MB 日本語 Compiler: GCC, ICCARM IDE: e2 studio, IAR EWARM	Jul 5, 2024
	RZ/T2M Group GPT Phase Count Sample Program (Z Phase support) [Software=FSP v1.3.0],[Toolchains=GNU ARM Embedded v12.2.1.am-12-24;IAR Embedded	

2. Set up Renesas Starter Kit+ for RZ/T2ME CPU Board

Setting up the configuration on the RSK+RZ/T2ME board is the same when using RSK+RZ/T2M.

For details on the settings for the RSK+RZ/T2M board, refer to README or the application note for the sample code you want to use.

3. Requirements for Software

The Requirements for software to use RZ/T2ME are shown below.

Item	Vendor	Description
IDE	IAR Systems	Embedded Workbench® for ARM Version 9.60.1
	Renesas Electronics	e ² studio 2024-04 Flexible Software Package (FSP) for Renesas RZ/T series v2.1.0 FSP Smart Configurator 2024-04 (FSP v2.1.0) Please download from the link below. https://github.com/renesas/rzt-fsp/releases
Emulator	IAR Systems	I-jet
	SEGGER	J-Link (Version : 7.96j)
GCC Compiler	Arm	12.2.Rel1

Download and install each software at the following GitHub.

➤ <https://github.com/renesas/rzt-fsp/releases/tag/v2.1.0>

- **Caution:**

please apply the following patch file to debug RZ/T2ME FSP project by using IAR EWARM 9.60.1.

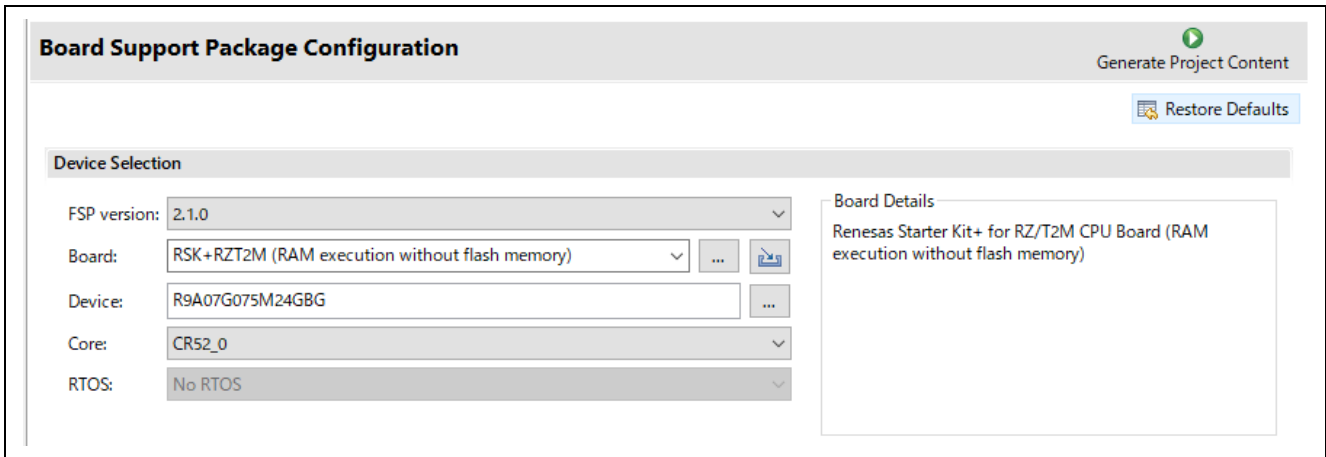
➤ **EWARM_Patch_for_RZT2ME_rev1.0.zip**

Regarding how to apply the patch, please read the readme file in patch file.

4. How to Convert FSP Configuration from RZ/T2M to RZ/T2ME

This section describes how to convert FSP configuration to run the RZ/T2M sample code as RZ/T2ME .

1. Refer to README or the application note of the sample code you want to use, open the **CPU0 project** in the IDE of your choice, either e² studio or EWARM.
2. Open the **FSP configuration file** of the CPU0 project.

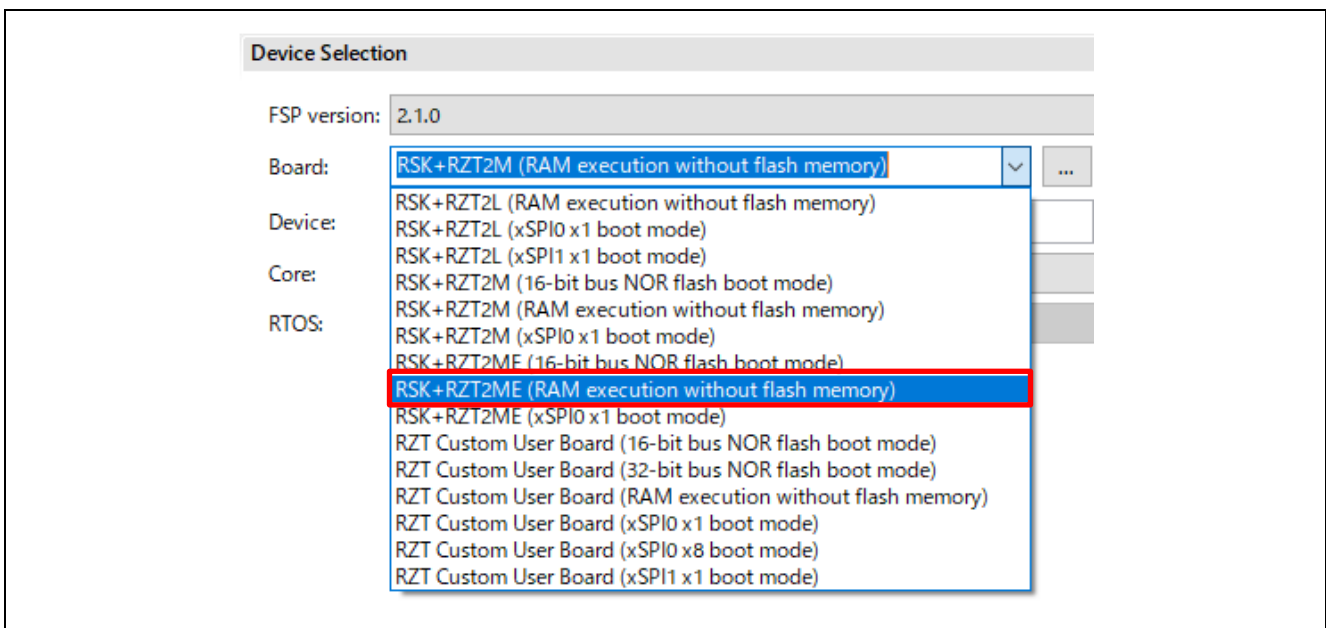


※ **Caution:**

The configurations of [**Properties**] in the [**BSP**] tab and the [**Clocks**] tab will become the **default** when the FSP configuration is changed from RZ/T2M to RZ/T2ME.

Therefore, **please record the current configurations.**

3. Open the [**BSP**] tab, change [**Board**] from [**RSK+RZT2M (RAM execution without flash memory)**] to [**RSK+RZT2ME (RAM execution without flash memory)**].



※ **Caution:**

In the case of xSPI0 boot mode, change [Board] from [RSK+RZT2M (xSPI0 x1 boot mode)] to [RSK+RZT2ME (xSPI0 x1 boot mode)].

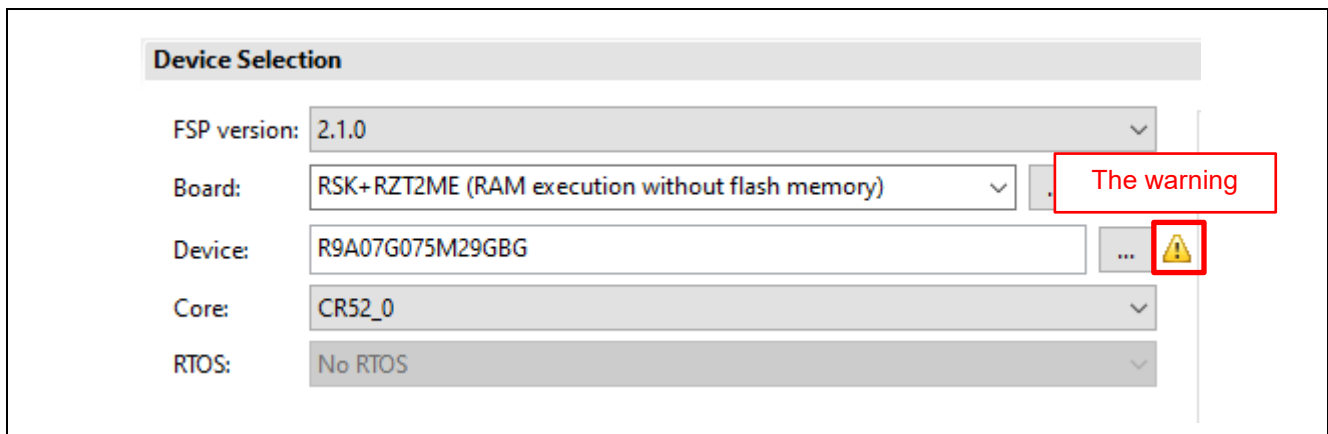
Also, In the case of NOR flash boot mode, change [Board] from [RSK+RZT2M (16-bit bus NOR flash boot mode)] to [RSK+RZT2ME (16-bit bus NOR flash boot mode)].

● **Note:**

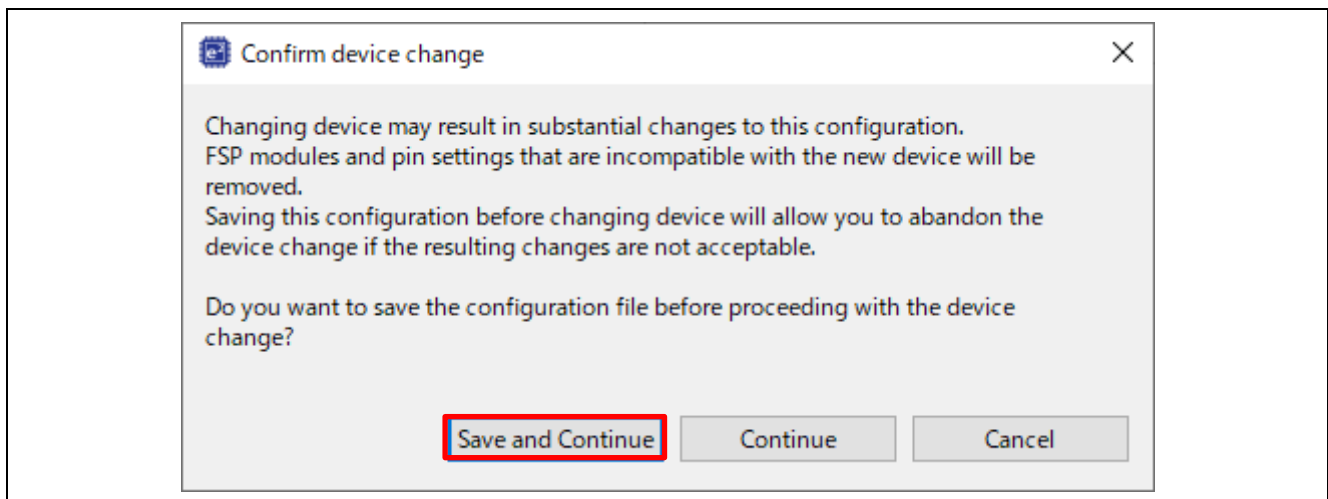
According to this procedure, the following **warning** may be displayed.

Temporarily **close the FSP configuration file** in the CPU0 project **after saving it** by pressing the [Shift] key and [S] key.

After reopening it, the warning will no longer be displayed.

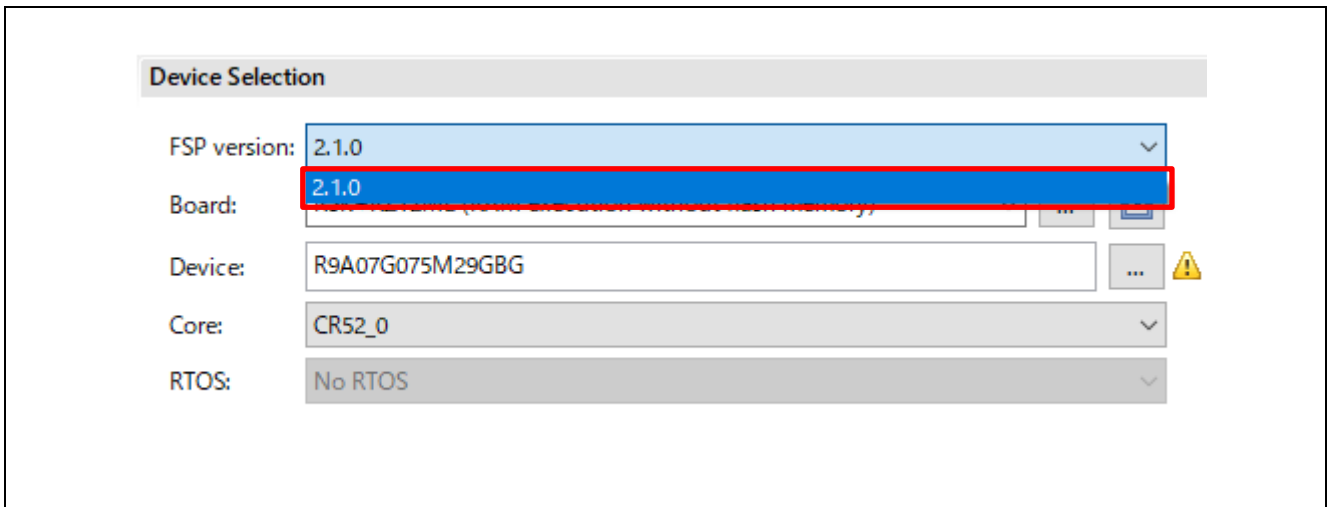


4. If the window [Confirm device change] is displayed, select [Save and Continue].

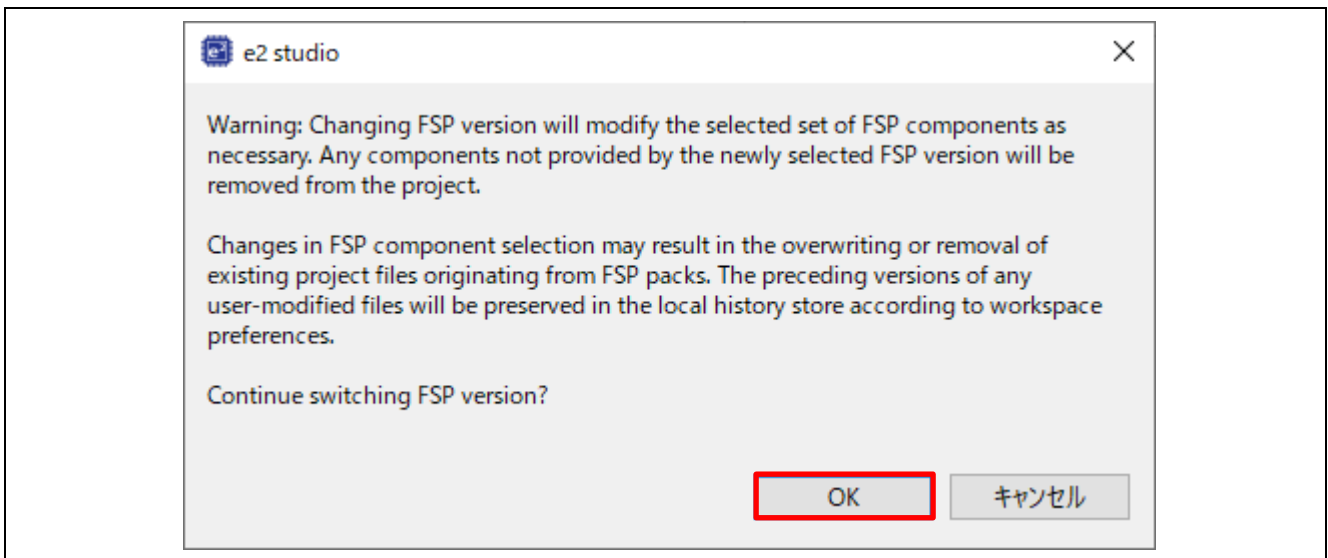


5. Reselect [FSP version:] from the drop-down list.

This operation is necessary **even if there is only one version in the lists**.



6. If the following window, select [OK].



7. While the [BSP] tab, open [Properties].

Since the settings of [Value] have become the default, **undo them to their original state.**

The screenshot shows the 'Device Selection' section with the following settings:

- FSP version: 2.1.0
- Board: RSK+RZT2ME (RAM execution without flash memory)
- Device: R9A07G075M29GBG
- Core: CR52_0
- RTOS: No RTOS

Below this, the 'Properties' tab is active for the 'RSK+RZT2ME (RAM execution without flash memory)' board. A table lists the properties and their values:

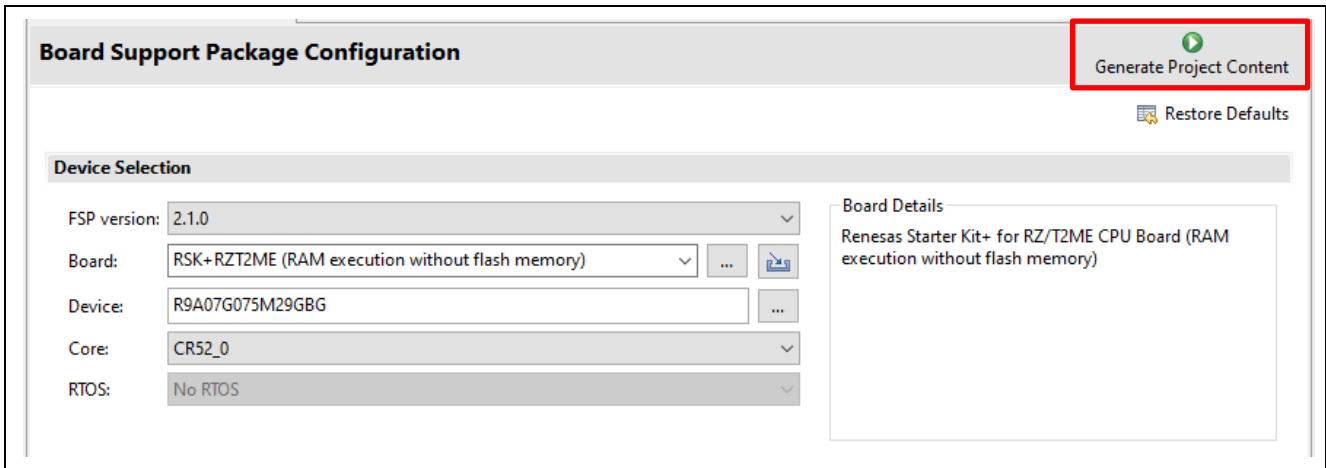
Property	Value
part_number	R9A07G075M29GBG
atcm_size_bytes	524288
btcm_size_bytes	65536
system_ram_size_bytes	2097152
package_style	BGA
package_pins	320
Cortex-R52 CPU core	CPU0
Semaphore	Enabled

Red boxes highlight the 'BSP' tab, the 'Properties' tab, and the 'Value' column of the table. A red text box states: "These settings of [Value] have become the default."

Also, open the [Clocks] tab, **undo the clock configurations to their original state.**

The screenshot shows the 'Clocks Configuration' diagram. A red box highlights the main clock configuration area, including PLL0 (2400MHz), PLL1 (1000MHz), and various peripheral clocks like CANFDCLK (40MHz), XSPI_CLK0 (12.5MHz), and CPU0CLK (200MHz). A red text box states: "These settings of the clock configurations have become the default."

8. Click the **[Generate Project Content]** button to generate the file for **RZ/T2ME** into the CPU0 project.



Board Support Package Configuration

Generate Project Content

Restore Defaults

Device Selection

FSP version: 2.1.0

Board: RSK+RZT2ME (RAM execution without flash memory)

Device: R9A07G075M29GBG

Core: CR52_0

RTOS: No RTOS

Board Details

Renesas Starter Kit+ for RZ/T2ME CPU Board (RAM execution without flash memory)

9. **All changes in the FSP configuration of the CPU0 project have been completed so far.**

Refer to README or the application note of the sample code you want to use.

If the additional build procedure is necessary, follow it.

Once the preparation for building is completed, **build the CPU0 project.**

※ **note:**

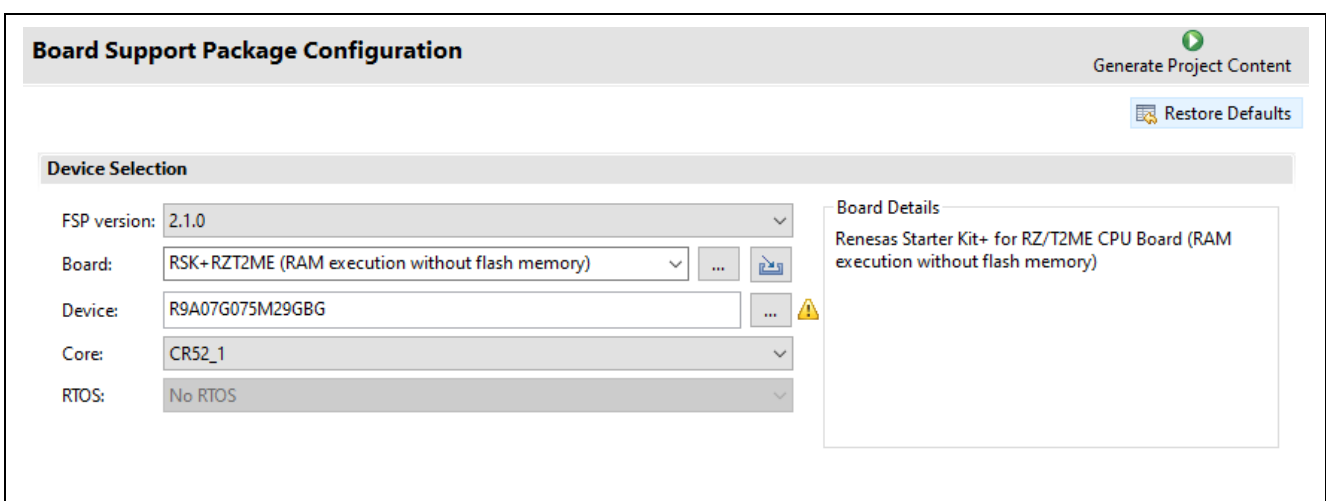
If the sample code you want to use is **only** the CPU0 project, you can **start debugging or downloading it immediately** after building the CPU0 project.

10. (Follow the procedures from here **only when the sample code supports multiprocessing.**)

Open the **CPU1 project** in e² studio or EWARM.

11. Open the **FSP configuration file** of the CPU1 project.

This FSP configuration has already been changed from RZ/T2M to RZ/T2ME.



Board Support Package Configuration

Generate Project Content

Restore Defaults

Device Selection

FSP version: 2.1.0

Board: RSK+RZT2ME (RAM execution without flash memory)

Device: R9A07G075M29GBG

Core: CR52_1

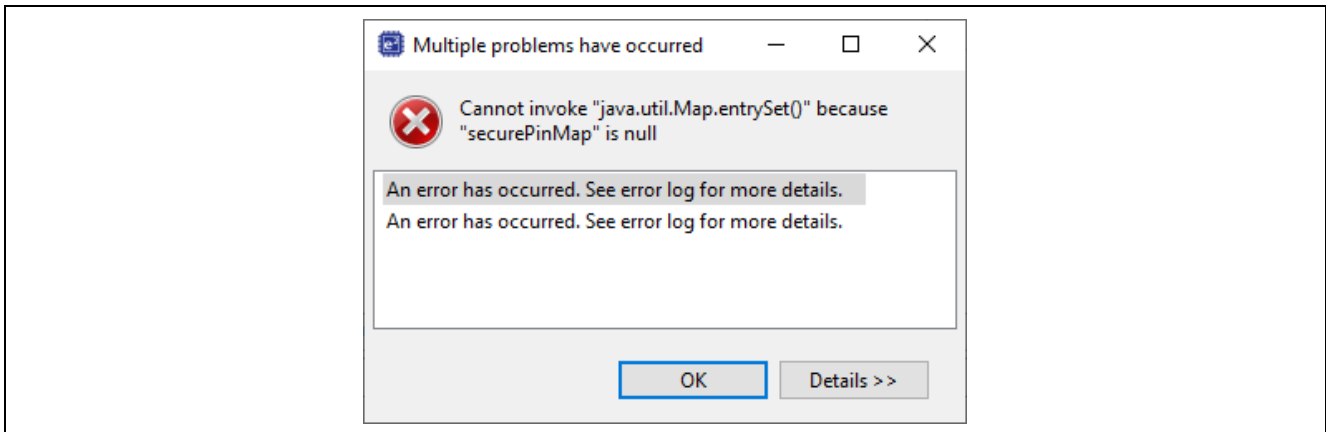
RTOS: No RTOS

Board Details

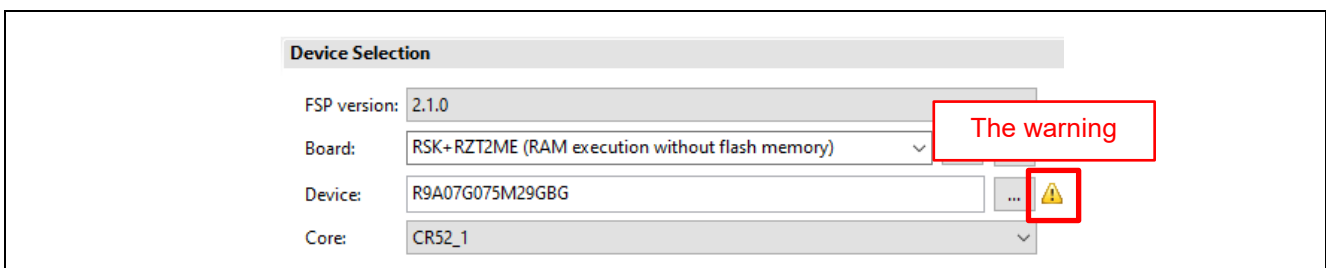
Renesas Starter Kit+ for RZ/T2ME CPU Board (RAM execution without flash memory)

※ **Caution:**

When using **e² studio**, the following error window might be displayed.



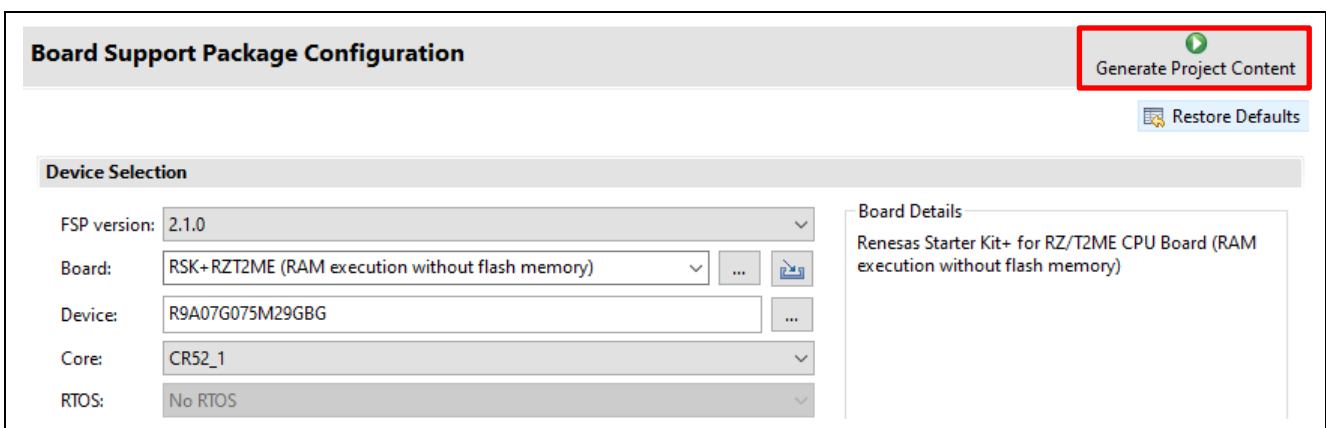
And the following **warning** may be displayed.



In that case, please click [OK], and then temporarily **close the FSP configuration file** of the CPU1 project **after saving it** by pressing the [Shift] key and [S] key.

After reopening it, this error window will no longer be displayed.

12. Click the [Generate Project Content] button to generate the file for **RZ/T2ME** into the CPU1 project.



13. All changes in the FSP configuration of the CPU1 project have been completed so far.

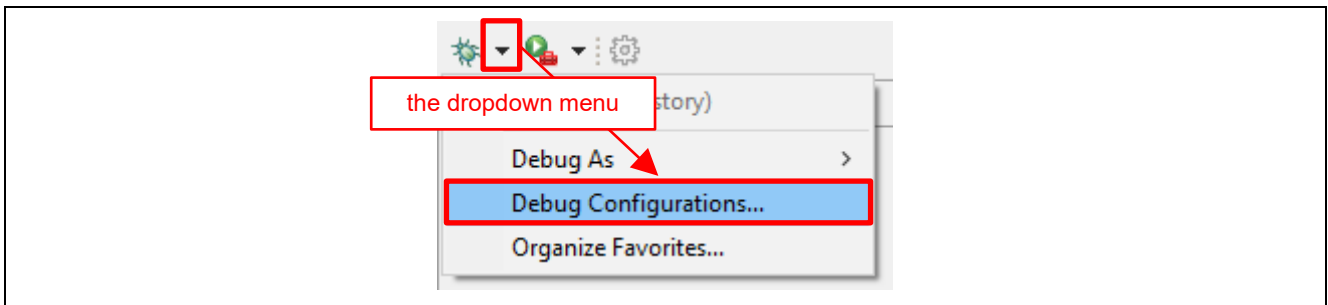
Refer to README or the application note of the sample code that you want to use.

If the additional build procedure of the CPU1 project is necessary, follow it.

Once the preparation for building is completed, **build the CPU1 project**.

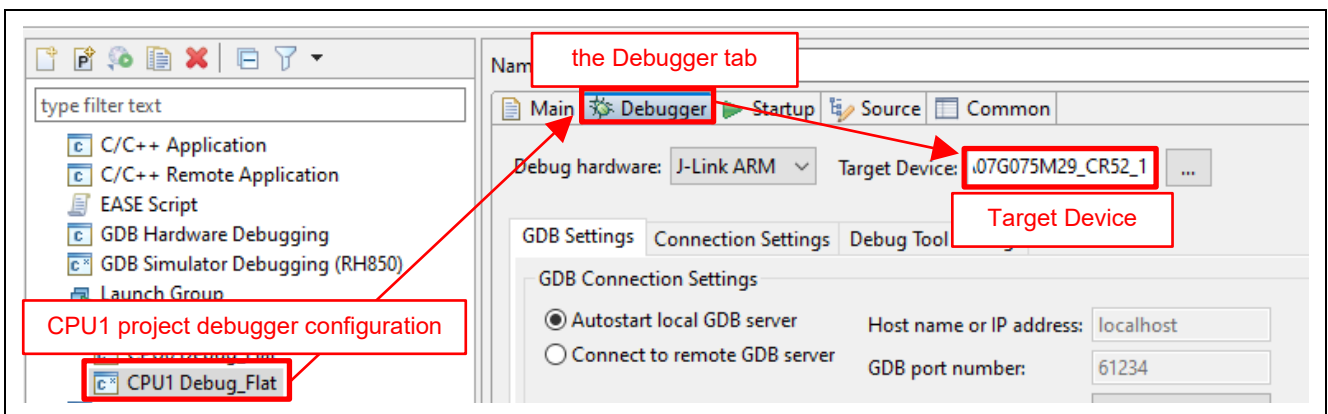
14. (Follow this procedure **only when the IDE is e² studio and boot mode is RAM execution.**)

Select the dropdown menu next to the Debug icon and select [Debugger Configurations...].



Select [CPU1 project debugger configuration], open the [Debugger] tab.

Please change [Target Device:] from R9A07G075M29_CR52_0 to R9A07G075M29_CR52_1.



After it is completed, press the [Apply] button on the lower right, and then press the [close] button.

15. **All procedures for changing the FSP configuration from RZ/T2M to RZ/T2ME are now complete!**

Follow README or the application note of the sample code that you want to use, **start debugging or downloading** the program for multiprocessing.

5. What to Modify for Running the RZ/T2M Source Code as RZ/T2ME?

When running the RZ/T2M sample code as RZ/T2ME, the source code, including the startup function and each driver, can be converted for RZ/T2ME by following the steps in Chapter 4.

However, the application source code is not automatically updated and must be manually modified for RZ/T2ME.

Therefore, this chapter describes what to modify for running the RZ/T2M application source code on RZ/T2ME.

The modification is only two points.

1. Change the byte size when using QSPI Write API

If QSPI Write API (**R_XSPI_QSPI_Write**) is used for writing to flash memory, the written size must be 1 or 2, or 4 bytes.

For example, if the original source code is the following something,

```
uint8_t p_src[64] = {0};
uint8_t *p_dest = 0x60000000;

R_XSPI_QSPI_Write(&g_qspi0_ctrl, p_src, p_dest, 64);
```

you must change the written size from 64 bytes to 4 bytes.

```
uint8_t p_src[64] = {0};
uint8_t *p_dest = 0x60000000;

for (uint32_t i=0; i<16; i++)
{
    R_XSPI_QSPI_Write(&g_qspi0_ctrl, p_src, p_dest, 4)
    p_src += 4;
    p_dest += 4;
}
```

2. Add RZ/T2ME Macro Definition

To support running on multiple devices (RZ/T2M, RZ/T2L, and RZ/N2L), the board macro definitions might be used in the application source code.

In that case, you must add the RZ/T2ME board macro definition to run on RZ/T2ME.

For example, you might need to add the following macro definitions.

```
BOARD_RZT2ME_RSK
BSP_MCU_GROUP_RZT2ME
```

In the case of RZ/T2M Group EtherCAT Sample program Package, the RZ/T2ME macro definitions are used for the following purposes.

- Selection of the I/O port pin number and the number of LEDs and DIP-SWs used in the application
- Selection of the written byte and the address when writing to flash memory
- Selection of whether the shared memory driver is used

Appendix. In the case of RZ/T2M EtherCAT Sample Code

This chapter describes the actual procedure for converting the FSP configuration in the case of operating **RZ/T2M Group EtherCAT Sample program Package** as RZ/T2ME.

Download RZ/T2M Group EtherCAT Sample program Package at the following Renesas web site on the Sample Code area.

➤ <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzt2m-high-performance-multi-function-mpu-realizing-high-speed-processing-and-high-precision-control>

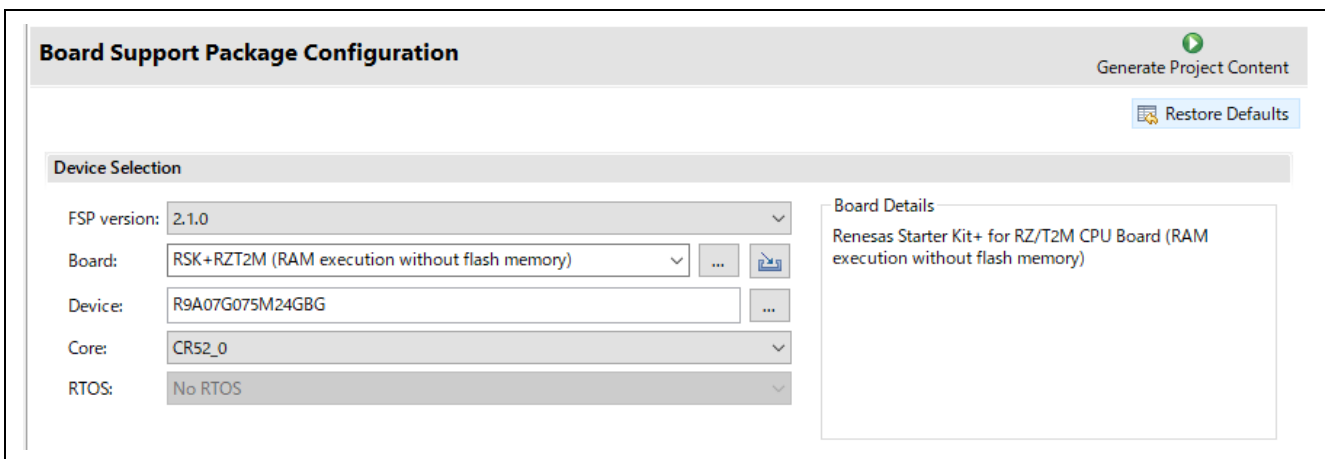
This sample code includes several application notes and projects.

Here, let's try to run the **EoE project using lwip with RAM boot mode**, as described in the application note "**r01an6635ejxxx-rzt2m-ecat-eoe.pdf**."

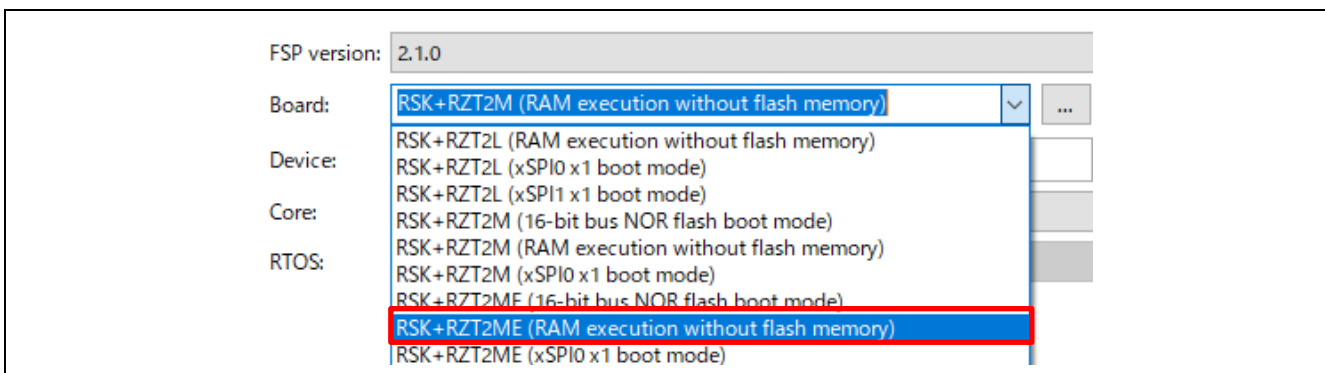
※ **note:**

The RZ/T2M Group EtherCAT Sample program Package already have been modified for Chapter 5. Therefore, you can run it as RZ/T2ME only by converting the FSP configuration.

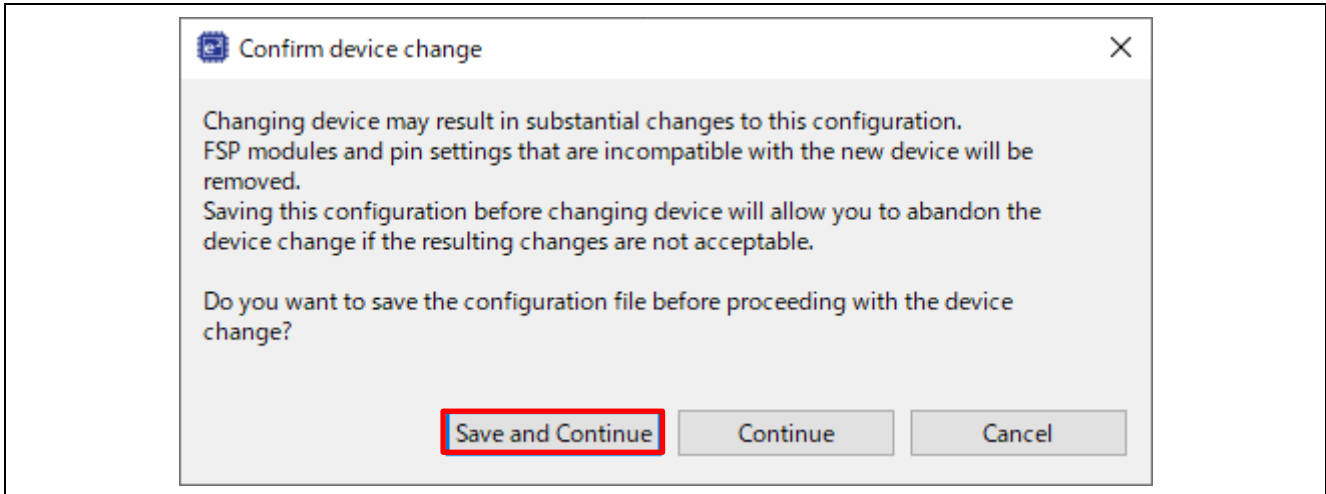
1. Refer to "**r01an6635ejxxx-rzt2m-ecat-eoe.pdf**" and follow the steps to open the **CPU0 project** in the IDE of your choice, either e² studio or EWARM.
2. Open the **FSP configuration file** of the CPU0 project.



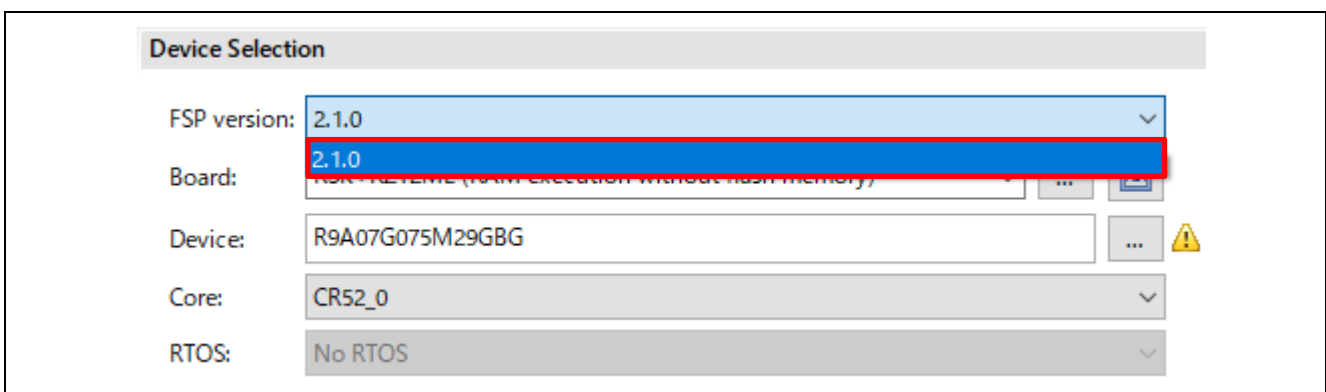
3. Open the [BSP] tab, change [Board] from [RSK+RZT2M (RAM execution without flash memory)] to [RSK+RZT2ME (RAM execution without flash memory)].



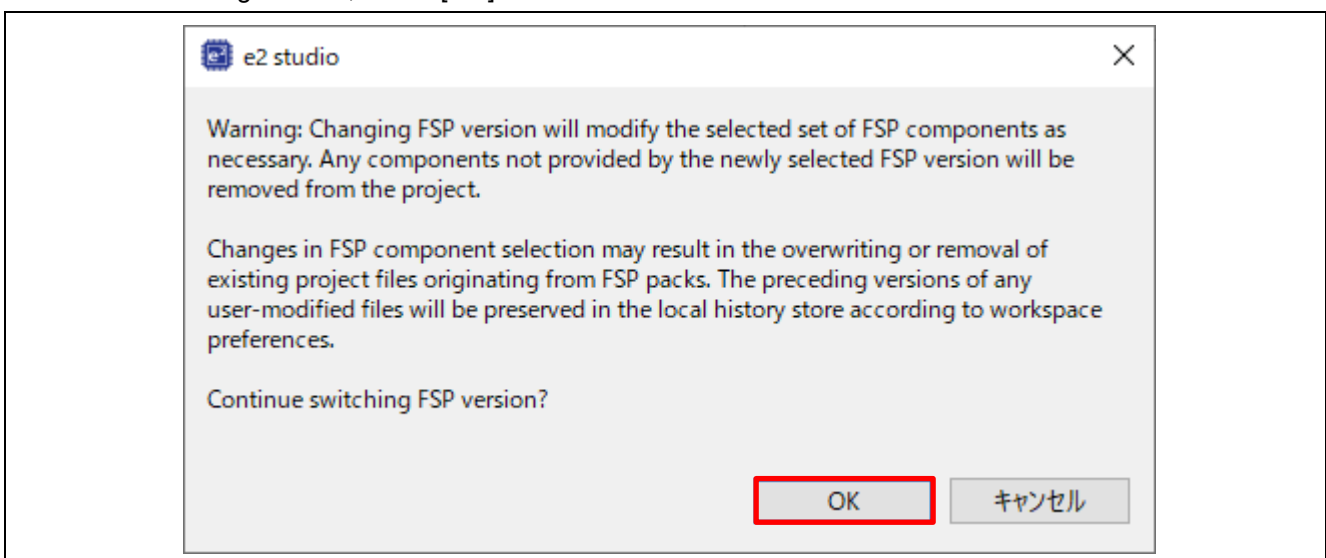
4. If the window [**Confirm device change**] is displayed, select [**Save and Continue**].



5. Reselect [**FSP version:**] from the drop-down list.



6. If the following window, select [**OK**].



7. In the case of this EoE project of the EtherCAT sample, the configurations of [Properties] in the [BSP] tab have been the default from the beginning.

Therefore, It is unnecessary to undo them again.

※ **Caution:**

In the case of the **IO_CiA402_FoE project** described in the application note “**r01an7378ejxxx-rzt2m-ecat-cia402-foe.pdf**,” It is necessary to undo them to the original settings again.

Next, open the [Clocks] tab, Undo **both CPU0CLK and CPU1CLK to 800MHz.**

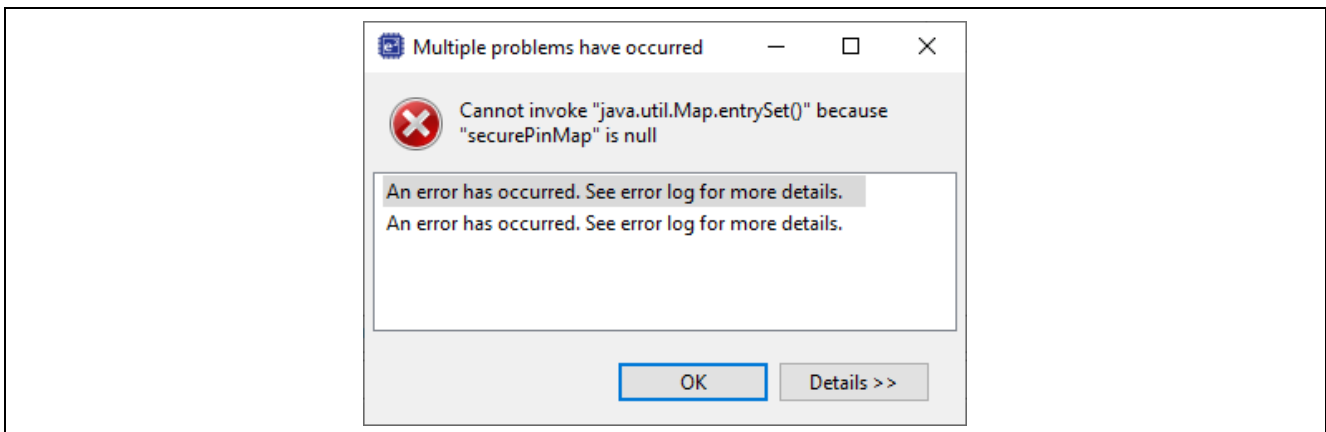
8. Click the [Generate Project Content] button to generate the file for RZ/T2ME into the CPU0 project.

9. All changes in the FSP configuration of the CPU0 project have been completed so far.
Refer to “[r01an6635ejxxx-rzt2m-ecat-oe.pdf](#)” and follow the steps to **build the CPU0 project**.
10. Refer to “[r01an6635ejxxx-rzt2m-ecat-oe.pdf](#)” and follow the steps to open the **CPU1 project** in the IDE of your choice, either e² studio or EWARM.
11. Open the **FSP configuration file** of the CPU1 project.
This FSP configuration has already been changed from RZ/T2M to RZ/T2ME.



※ **Caution:**

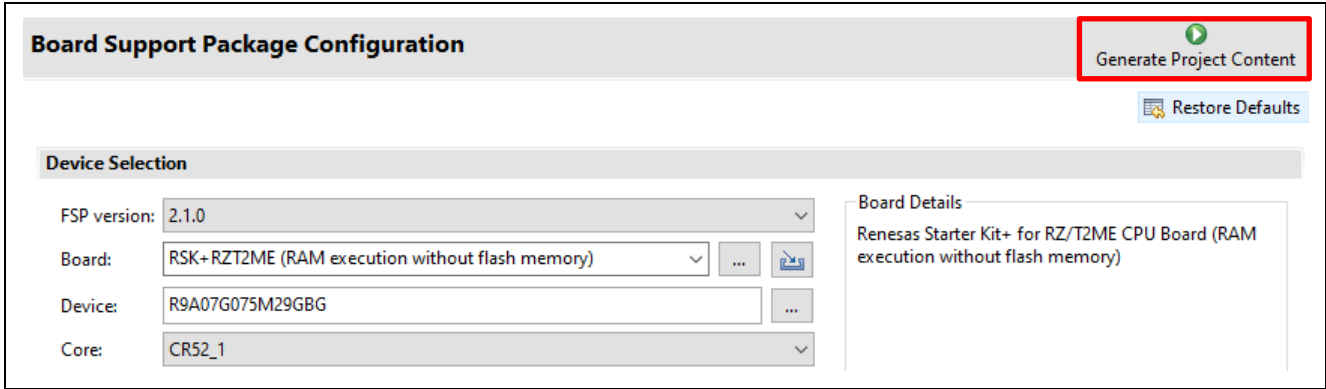
When using e² studio, the following error window might be displayed.



In that case, please click [OK], and then temporarily **close the FSP configuration file** of the CPU1 project **after saving it** by pressing the [Shift] key and [S] key.

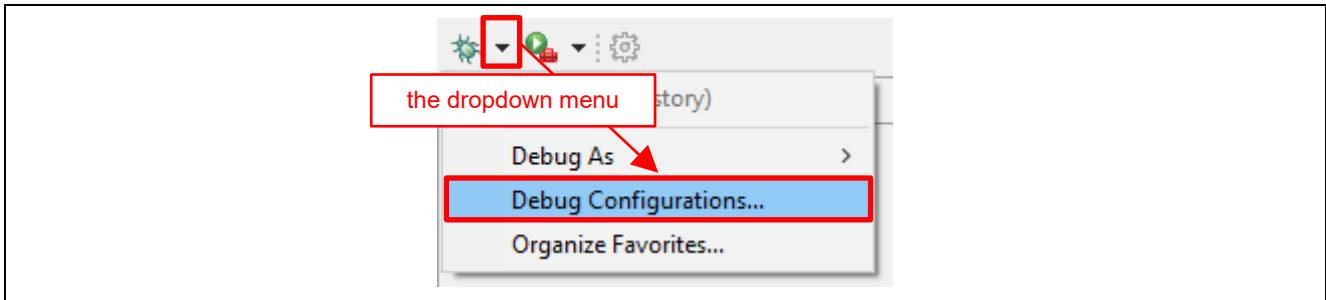
After reopening it, this error window will no longer be displayed.

12. Click the **[Generate Project Content]** button to generate the file for **RZ/T2ME** into the CPU1 project.

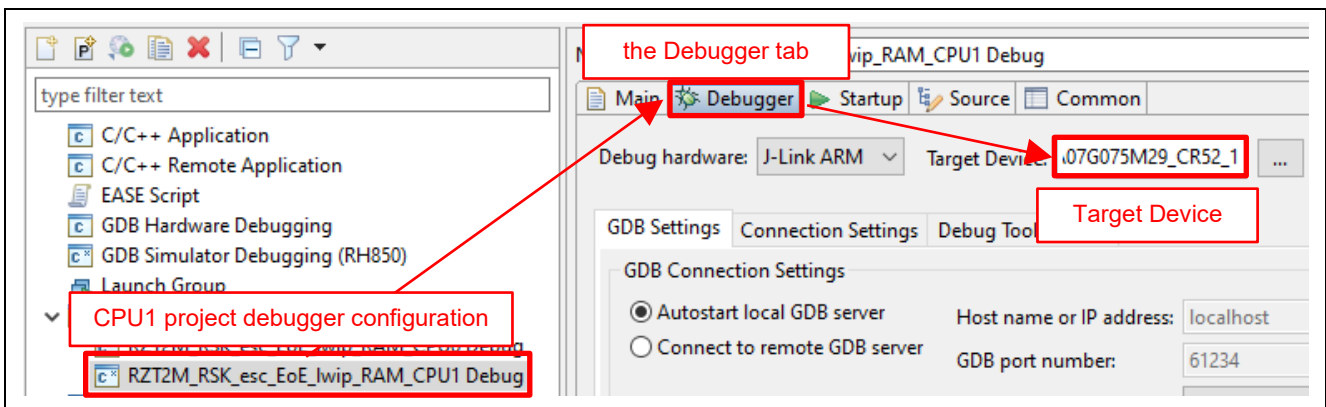


13. All changes in the FSP configuration of the CPU1 project have been completed so far.
Refer to “[r01an6635ejxxx-rzt2m-ecat-oe.pdf](#)” and follow the steps to **build the CPU1 project**.

14. (Follow this procedure **only when using the IDE as e² studio**.)
Select the dropdown menu next to the Debug icon and select **[Debugger Configurations...]**.



Select **[RZT2M_RSK_esc_EoE_lwip_RAM_CPU1 Debug]**, open the **[Debugger]** tab.
Please change **[Target Device:]** from **R9A07G075M29_CR52_0** to **R9A07G075M29_CR52_1**.



After it is completed, press the **[Apply]** button on the lower right, and then press the **[close]** button.

15. **All procedures for changing the FSP configuration from RZ/T2M to RZ/T2ME are now complete!**
Refer to “[r01an6635ejxxx-rzt2m-ecat-oe.pdf](#)” and follow the steps to **debug or download** the EoE program for multiprocessing.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug 21, 2024	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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- IEEE is a registered trademark of the Institute of Electrical and Electronics Engineers Inc
- EtherCAT® and TwinCAT® are registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.
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Notice

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