Printed Circuit Board Layout and Probing for GaN Power Switches

This document describes best practices for printed circuit board layout and probing of Renesas GaN Power Switches. Best practices for high switching speed design include low inductive board layout and proper referencing of signals to ground planes. Additionally, low inductive ground and signal connections are important for proper measurement results.

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1. INTRODUCTION

Renesas Gallium Nitride (GaN) Switches provide significant advantages over silicon (Si) Superjunction MOSFETs with lower gate charge, faster switching speeds and smaller reverse recovery charge. GaN Switches exhibit in-circuit switching speeds in excess of 150 V/ns and can be even pushed up to 500V/ns, compared to current silicon technology usually switching at rates less than 50V/ns.

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN Switches requires adherence to specific PCB layout guidelines and probing techniques.

Using a PFC demo board (Renesas reference design **TDPS300E1A8**) as an example, this application note introduces the general rules for PCB board layout and probing of fast switching GaN Switches.

2. LAYOUT CONSIDERATION IN A PFC BOARD

2.1 Power loop

Figure 1 shows the power semiconductor part/power loop of a typical boost converter based PFC circuit. It can be observed that there are multiple parasitic inductances and capacitances in the loop. Together, these parasitic elements form high frequency resonant tank circuits that can be excited by fast changing voltage and current transients when switching the transistor quickly. As GaN Switches operate with rise and fall times <10 ns, special care has to be taken when designing GaN power circuits to avoid excessive ringing in the circuit.

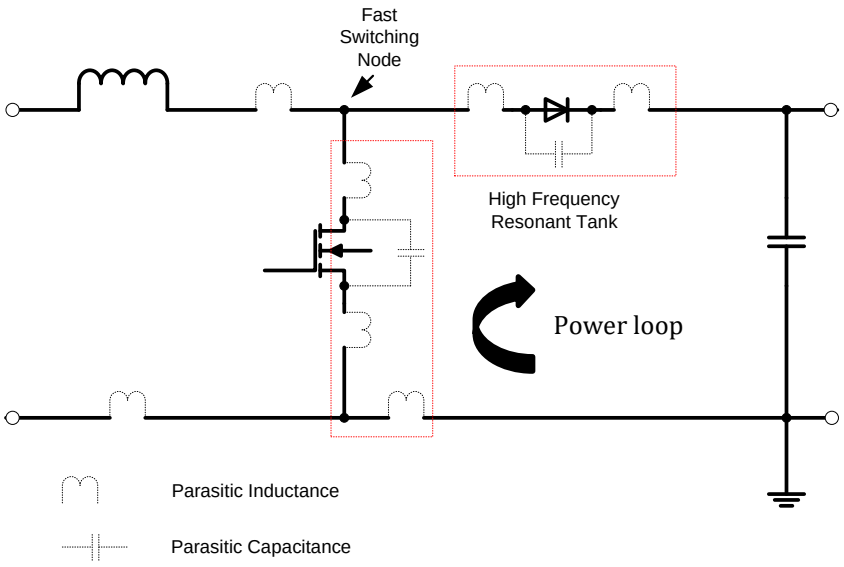

Fig.1. Typical Boost Converter Circuit with Parasitics

Renesas Inc. packages its transistors with a layout inside the package that keeps inductances and capacitances at a minimum. However, the designer is responsible for minimizing inductances and capacitances in the PCB layout.

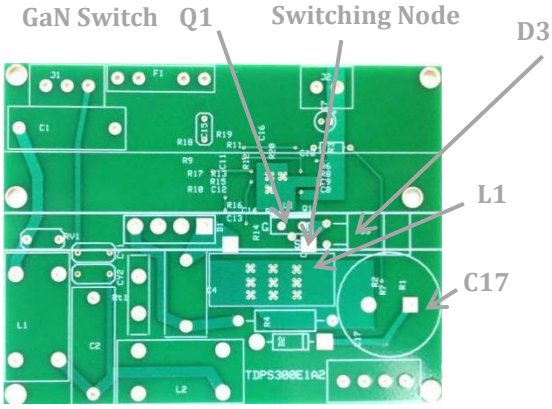

Fig.2 Top Side of the TDPS300E1A8

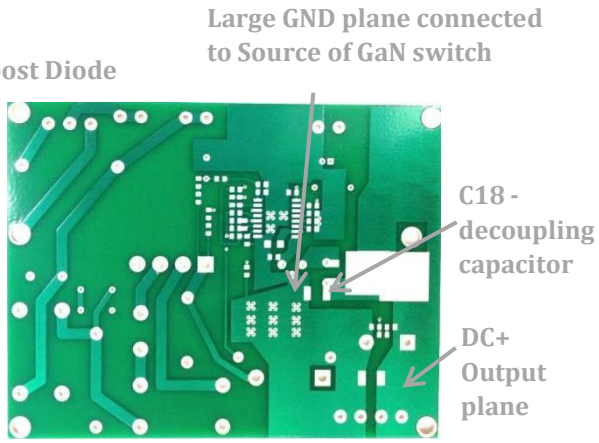

Fig.3 Bottom Side of TDPS300E1A8

Figure 2 and 3 show an example of proper layout of the power loop:

1. A large ground plane is used for low-inductance grounding of the GaN Switch (Q1).
2. The high voltage switching node has a small area to avoid extra capacitances on the switching node.
3. The power devices (GaN Switch (Q1) and diode (D3)), the inductor (L1), and the decoupling capacitor (C18) are placed as close as possible to each other to minimize inductances.
4. The DC+ output is a large plane for ease of decoupling, and it also acts as a heatsink for the boost diode (D3)
5. The decoupling output capacitor (C17) is connected between this plane and the ground plane with the shortest leads possible.
6. A fast film capacitor (C18) is placed right across the cathode of the boost diode and the Source of the GaN Switch, to absorb noise and to decouple the output trace inductances.

2.2 Gate Loop/ Gate Drive Circuit

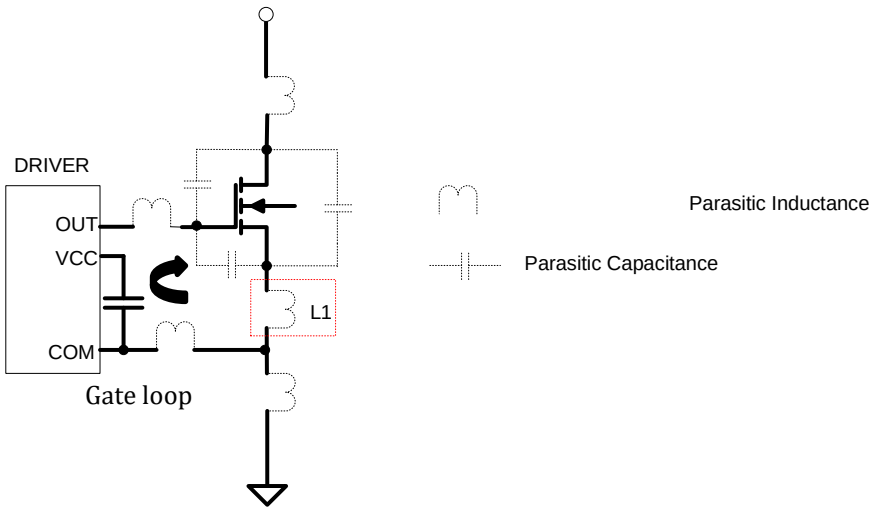

Fig.4. PFC Gate Drive Circuit with parasitic elements

Figure 4 shows the parasitic inductances and capacitances that can be found in the gate drive loop. Among all the parasitic inductances, L1 in Fig.4 is most critical as it is included in the gate drive loop as well as in the power loop. Current transients (di/dt) in the source of the transistor induce a voltage V_L across L1 (V_L=L1× di/dt), effectively changing the Gate-to-Source voltage V_{GS}. If L1 is too large, the induced voltage can turn on or off the transistor without intended change gate drive voltage. Therefore, it is important to keep L1 as low as possible, and directly connect the COM (ground) of the control IC to the Source pin of the HEMT, without including the power path into the drive loop.

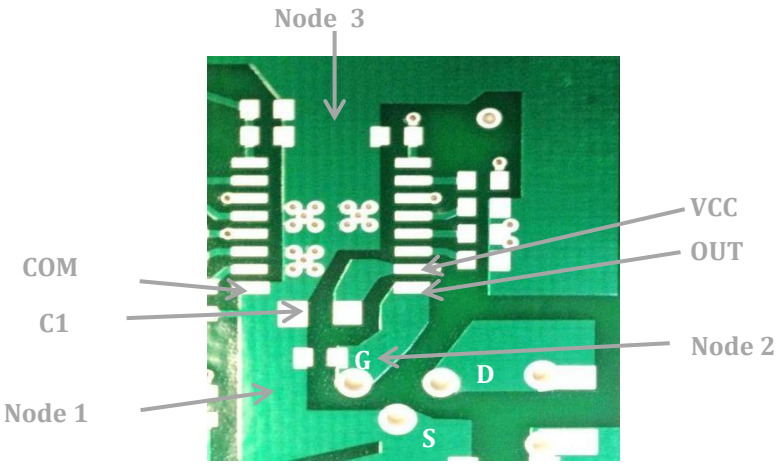

Fig.5. Close Look at the Gate Drive Layout

Figure 5 depicts the proper layout for the gate drive circuit:

1. The COM pin of the IC is directly connected to the Source pin of the GaN Switch with a wide trace (Node 1), which is separated from the power loop.
2. The OUT pin of the IC is directly connected to the Gate pin of the GaN Switch with a short wide trace (Node 2), no gate resistor is required.
3. A decoupling film capacitor (C1) is directly placed across the VCC and COM pins of the control IC.
4. A large GND plane is connected to the IC COM pin, providing the shortest routes for control circuits that must be connected to COM (Node 3).

A highly effective way to further reduce source inductance of the S-tab GaN Switches is the use of the metal tab of the GaN Switch as the current carrying Source terminal and the Source pin as a Kelvin connection to the current carrying Source for the drive circuit.

3. PROBING CONSIDERATIONS

3.1 Accurate Probing

To assess the proper layout of the PCB, it is important to accurately measure the voltages on the switching nodes. However, fast current transients on the switching nodes can induce voltage ringing in the measurement probe. Therefore, voltages seen on the oscilloscope during the measurement might be an artifact of the measurement and not actual voltages on the node.

The following best measurement practices can help to minimize the overall measurement error:

1. As the ground lead length of an oscilloscope probe is the most important item in properly capturing the transients of the switching node voltage, do not use the standard 3-inch long ground wire supplied with the oscilloscope probe. The long wire loop acts as an antenna that picks up radiated noise emitted by the board and will show a higher value of switching node voltage ringing than the one actually seen by the device (Fig. 6).
2. Instead, use a ground wire that is as short as possible and attaches to the outer ring of oscilloscope probe (Fig. 7). Placement of the oscilloscope tip and ground must be directly onto the device leads. Probe placement further away from the device increases measurement error.
3. Minimize the sensing loop area by adjusting the wire length and keeping it parallel with the tip.

Fig.6. Typical probe with 3-inch ground lead – should not be used

Fig.7 Probe with short ground lead – should be used

A combination of these measurement tips can yield proper measurement of the actual voltage transient seen by the GaN Switch.

3.2 Avoid Introducing Additional Parasitics

It is also important not to introduce additional parasitics into the circuit when probing.

For example:

1. Avoid adding additional wire to the parasitic resonant tanks of the power loop. Unfortunately, this eliminates the possibility of using a current probe to simultaneously measure the switching current.
2. Use truly floating oscilloscopes. If the oscilloscope's ground is not designed to be truly floating with minimum capacitance but simply disconnected from earth ground, a considerable parasitic capacitance will be present in the sensing loop as the sensing ground is connected to the oscilloscope’s chassis. Therefore, connecting such a scope ground to the switching node will introduce more ringing in the measured waveform.

4. CONCLUSION

Using fast switching GaN Switches requires special attention to layout, to placement of the components, and to probing in order to minimize ringing, to maximize performance, and to measure performance correctly. The key is to minimize parasitic inductances and capacitances in the circuit.