MOSFET

Precautions for parallel connection of power MOSFETs

Introduction

In this application note, we will explain the precautions for parallel connection of power MOSFETs.

Contents

1. Overview

In some cases, multiple devices may be connected in parallel to achieve higher power system or lower power MOSFET losses. In this case, it is important to balance the current flowing through each device, as if the current becomes unbalanced and concentrated on some devices, they may suffer excessive losses and be destroyed. Therefore, sufficient consideration is required for device characteristics variation, substrate layout symmetry, gate drive circuit, etc. Also, the problems that occur when using parallel connection can be classified into those that occur during the conduction period (steady state) of the power MOSFET and those that occur during the switching period (transient state) of the power MOSFET. These have different causes and require different countermeasures. The precautions for parallel connection are shown in Table 1-1.

Table 1-1. precautions for parallel connection of power MOSFETs

	During conduction (steady state)	During switching (transient state)
Circuit factors	▪ Symmetry of board layout (resistance component)	▪ Symmetry of board layout (resistance component) ▪ Avoid avalanche operation ▪ Gate oscillation
Power MOSFET factors	▪ Variation of $R_{DS(on)}$	▪ Variation of $V_{GS(th)}$

2. Precautions during conduction (steady state)

When power MOSFETs are turned on, the difference in $R_{DS(on)}$ of the parallel-connected devices and the resistance of the substrate and wiring cause an imbalance in the drain current. This current imbalance not only affects the loss of the devices during conduction, but also changes the current value during switching, affecting the transient loss. Therefore, it is necessary to take measures such as selecting devices from the same lot and minimizing the difference in $R_{DS(on)}$, and designing the parallel paths symmetrically. The $R_{DS(on)}$ of power MOSFETs has a positive temperature coefficient. Therefore, the current imbalance that occurs will self-balance to equalize, and the risk of failure due to heat generation during conduction is low.

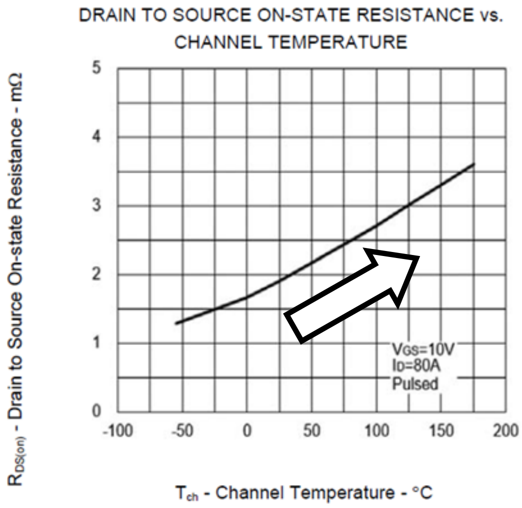

Fig. 2-1 $R_{DS(on)}$ Temperature characteristics

3. Precautions during switching (transient state)

When power MOSFETs are switching (transient state), the difference in $V_{GS(th)}$ of the parallel-connected devices and the difference in the inductance components of the substrate and wiring cause an imbalance in the drain current. Therefore, it is necessary to take measures such as selecting devices from the same lot and minimizing the difference in $V_{GS(th)}$, and designing the layout of the parallel paths symmetrically. When operating in avalanche mode in parallel connection, there is a possibility of destroying the device with low drain withstand voltage by concentrating all the current on it, so be careful.

3.1 Example of current imbalance during switching when samples with different $V_{GS(th)}$ are connected in parallel

The following figure shows the operation waveforms when samples with intentionally different $V_{GS(th)}$ are connected in parallel and switched. At turn-on, MOSFET2 with smaller $V_{GS(th)}$ turns on first, and at turn-off, MOSFET1 with larger $V_{GS(th)}$ turns off first, causing current imbalance. The current imbalance caused by the difference in $V_{GS(th)}$ can be prevented by using devices from the same lot and minimizing the difference in $V_{GS(th)}$ between MOSFETs.

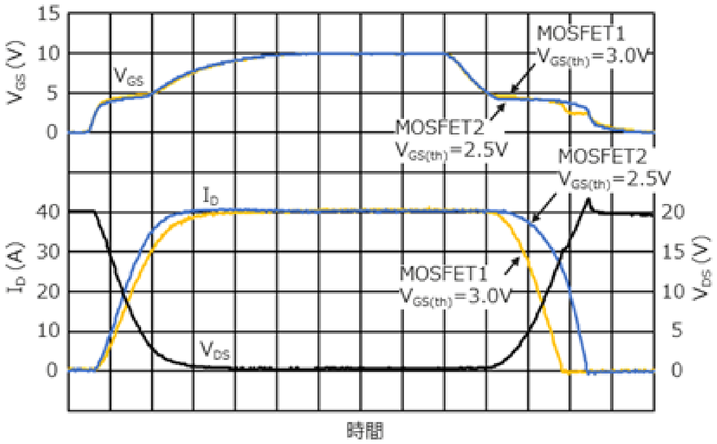

Fig. 3-1 Current imbalance waveforms during switching

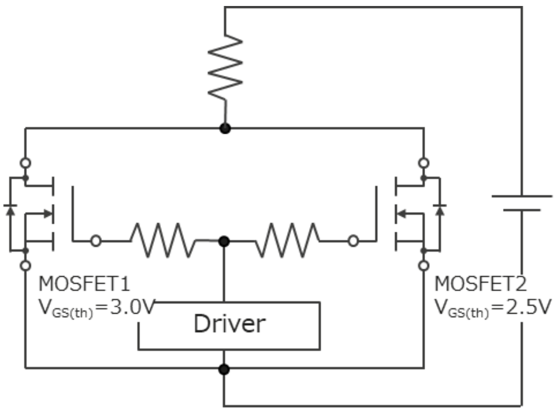

Fig. 3-2 Evaluation circuit

4. Regarding parasitic oscillation

When using power MOSFETs in parallel, parasitic oscillations are more likely to occur than when using a single power MOSFET. If the gates of the power MOSFETs are connected directly without resistance, oscillating waveforms may be seen on the gates because of parasitic parameters. These oscillating waveforms are caused by the voltage oscillation due to the drain wiring inductance (Ld) during switching (especially turn-off) and the resonant circuit composed of the gate-drain capacitance (Cgd) and the gate wiring inductance (Lg). Therefore, when there is no gate resistance, the Q factor (sharpness) of the resonant circuit becomes large, and when the resonance condition is met, a large oscillating voltage is generated between the gate-drain and the gate-source, causing parasitic oscillation. As a countermeasure, parasitic oscillation is suppressed by connecting a resistance (RG) to the gate of each device.

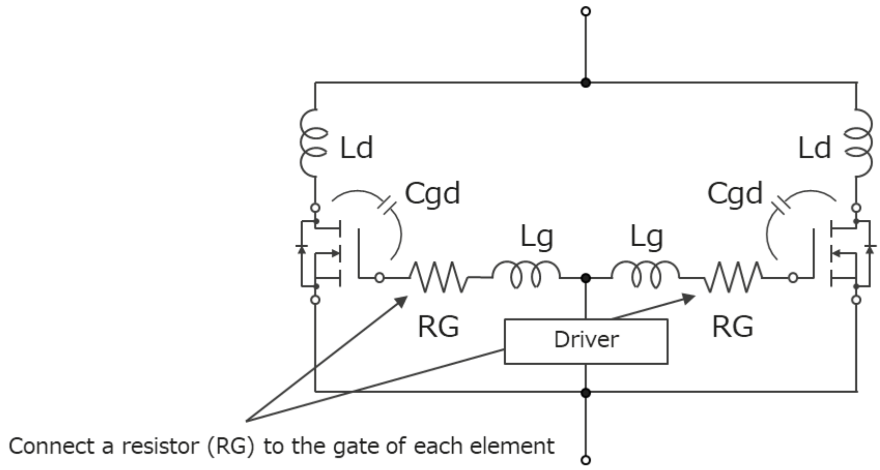

Fig. 4-1 Measures against gate oscillation

Revision History

Rev.	Date	Description	
		Page	Summary
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