Power MOSFETs

How does the frequency affect capacitance measurement?

About this document

This document will describe the accuracy of capacitance measurements for Power MOSFETs.

Target Device

Power MOSFETs

Contents

1. Introduction

This application note provides an overview of capacitance measurements in Power MOSFETs and examines how changes in measurement frequency affect the results. The influence of parasitic inductance in actual measurements is examined from various perspectives.

2. Capacitance Basics of Power MOSFETs

2.1 Definition of MOSFET Capacitance Values

The capacitance between each terminal of the Power MOSFET is shown in Figure 2-1. The relationships among input capacitance (Ciss), reverse transfer capacitance (Crss), and output capacitance (Coss) are as follows.

(a) Ciss = Cgd + Cgs --- Equation (1)

(b) Crss = Cgd --- Equation (2)

(c) Coss = Cgd + Cds --- Equation (3)

Cgs: Gate to source capacitance

Cds: Drain to source capacitance

Cgd: Gate to drain capacitance

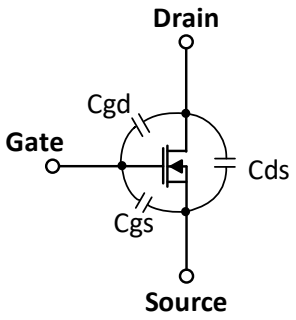


Figure 2-1 MOSFET Capacitance

2.2 Fundamentals of Measurement Methods for Each Capacity

The measurement conditions for capacitance are defined by the drain-to-source voltage (VDS), gate-to-source voltage (VGS), and a specified measurement frequency (f).

(a) Input Capacitance: Ciss

To measure input capacitance (Ciss), an AC voltage is applied to the gate while the source-side AC current is measured. During this process, the drain and source terminals are held at a fixed voltage. Although VDS is a DC bias, it is considered shorted for AC during measurement; as a result, Ciss equals the sum of Cgd and Cgs, as described in Equation (1).

(a) Ciss = Cgd + Cgs --- Equation (1)

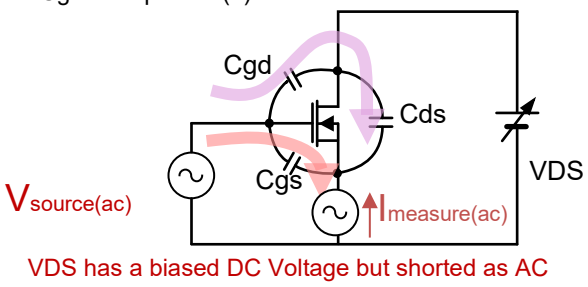


Figure 2-2 Ciss Measurement

(2) Reverse Transfer Capacitance ：Crss

To measure the reverse transfer capacitance (Crss), an AC voltage is applied to the gate while monitoring the AC current on the drain side. This process allows for the measurement of the capacitance (Cgd) between the gate and drain terminals, as described in Equation (2)

(b) Crss = Cgd --- Equation (2)

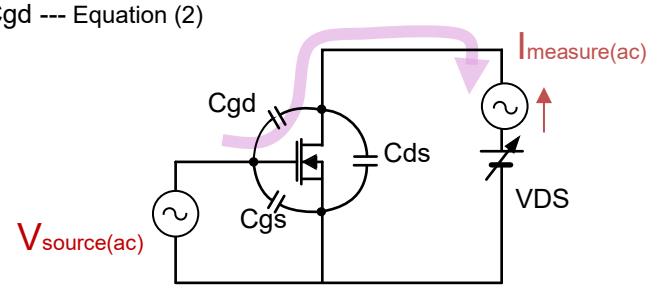


Figure 2-3 Crss Measurement

(3) Output capacitance Coss

To measure output capacitance (Coss), an AC voltage is applied to the drain while monitoring the AC current at the source; with Cgs terminals DC-shorted, Coss equals the sum of Cgd and Cds, as shown in Equation (3).

(c) Coss = Cgd + Cds --- Equation (3)

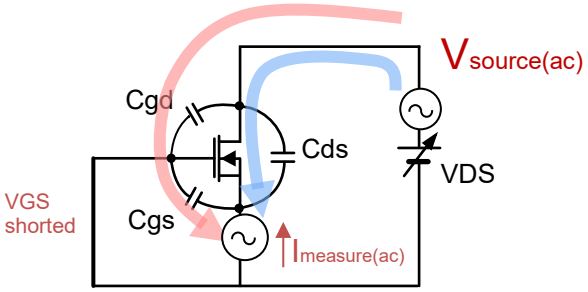


Figure 2-4 Coss Measurement

The impedance (Z) for AC current (I_{ac}) and voltage (V_{ac}) can be described as follows:

$$Z = \frac{V_{ac}}{I_{ac}} \quad \text{--- Equation (4)}$$

$$Z = R + jX \quad \text{--- Equation (5)}$$

Z is described in terms of its real (resistance, R) and imaginary (reactance, X) parts. In theoretical capacitance calculations, ignoring any parasitic inductance from the measurement, the capacitance appears as the imaginary portion of the impedance and can be found with Equation (6). This indicates that capacitance can be calculated once Vac, Iac, and f are known from the measurement setup.

$$C = \frac{1}{2\pi f X} = \frac{I_{ac}}{2\pi f V_{ac}} \quad \text{--- Equation (6)}$$

Please refer to Appendix Section 8 for impedance theory details.

Below are measurement examples illustrating the capacitance values for the RBA190N15YANS-3UA04, 150 V 3.9 mΩ MOSFET in TOLL package. The actual capacitance varies considerably with the VDS voltage, as shown in Figure 2-5. In particular, Crss exhibits significant changes in capacitance depending on the gate structure as described in the next section.

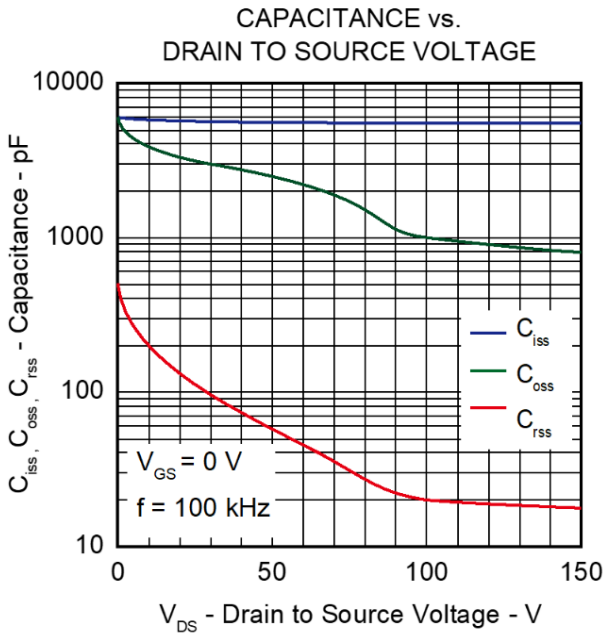
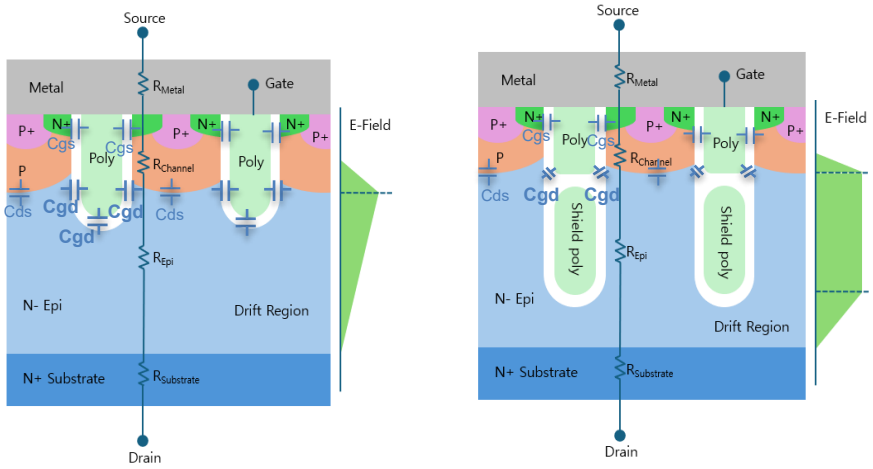


Figure 2-5 VDS vs Capacitance

3. Low Cgd by Split-Gate Structure

Figure 3-1 illustrates both MOSFET with the gate structure of Standard-Gate Trench and Split-Gate Trench design. In contrast to Standard-Gate structures, the Split-Gate configuration reduces Cgd by using a shield poly gate that separates the gate area from the drain plane. As a result, this advancement allows the latest MOSFETs to operate at higher speeds.[1]



Standard-Gate Trench Split-Gate Trench (=Shielded Gate)

Figure 3-1 Cross Section of MOSFET

Table 3-2 provides specific examples of Crss values for MOSFETs from both other vendors and Renesas that are currently available. Products featuring a Split-Gate design typically exhibit a reverse transfer capacitance (Crss) that is 1 % or less of their input capacitance (Ciss). In comparison, conventional trench structure MOSFETs generally have a Crss-to-Ciss ratio ranging from 2 % to 10 %.

As previously noted, the Split-Gate Trench structure possesses an inherently lower Cgd, resulting in a decreased Crss/Ciss ratio. This characteristic helps to prevent self-turn-on in DC/DC applications and is regarded as advantageous.[3]

Table 3-2 . Crss (=Cgd) Comparison between Conventional & Split-Gate Trench

MOSFET Structure	Process/Voltage	P/N	$R_{DS(on)\ max}$ (VGS=10V) (mΩ)	Crss (pF)	Ciss (pF)	**Crss/Ciss**
Conventional Standard-Gate Trench	Renesas (Trench) / 30 V	RJK03M5DPA	5.4	120	1350	***8.89 %***
	Renesas (ANM2) / 100 V	RBA250N10CHPF-4UA02	2.4	190	9500	***2.00 %***
	Renesas (ANL4) / 40 V	RBA100N04DANS-4UB02 / RBE020N04R0SZN6	2.0	335	4160	***8.05 %***
Split-Gate Trench	Renesas REXFET-1 / 150 V	RBA190N15YANS-3UA04 / RBE039N15R1SZQ4	3.9	33	5500	***0.60 %***
	Renesas REXFET-1 / 100 V	RBA300N10EANS-3UA02 / RBE015N10R1SZQ4	1.5	80	13000	***0.62 %***
	Renesas REXFET-1 / 80 V	RBA175N08EANS-4UA02 / RBE024N08R1SZN6	2.4	39	6900	***0.56 %***
	Company A / 80 V	MOSFET. A	2.6	38	5200	***0.73 %***
	Company B / 40 V	MOSFET. B	0.7	40	6500	***0.61 %***

4. Crss (Cgd) Measurements

When using standard measurement techniques, shorting G-S and D-S terminals respectably allows accurate capacitance measurement between Gate to Drain terminals in Figure 4-1(c). However, this approach does not allow for measurements with a VDS bias in place. Typical LCR meters are unable to measure capacitance effectively when a VDS bias is applied, so specialized equipment tools designed for MOSFET capacitance testing are required. For example, specialized power equipment such as power device analyzers/curve tracers can perform such measurements while maintaining the VDS bias.

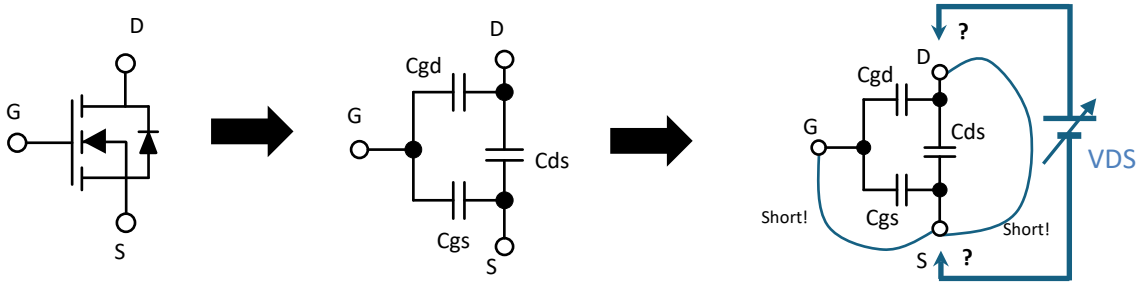


Figure 4-1 (a)
Impedance Z locus

Figure 4-1 (b)
AC Equivalent Symbol

Figure 4-1 (c)
How to measure Cgd while applying VDS bias?

The latest Power MOSFETs necessitate ultra-low resistance and rapid switching capabilities. As a result of advancements in MOSFET architecture, the feedback capacitance Cgd has been significantly reduced and now varies dynamically by more than an order of magnitude with changes in VDS bias. Consequently, accurate measurement of Cgd has become increasingly challenging.

When using equipment tools designed for MOSFETs with impedance analyzer, connecting the AC guard of the capacitance meter (see Figure 4-2) provides an alternative path for current. This ensures that the alternating current flowing through Cds does not return via Cgs to the CML node. The AC guard acts as the circuit common for the auto-balancing bridge and is connected to the shields of the four-terminal pair connectors. [4]

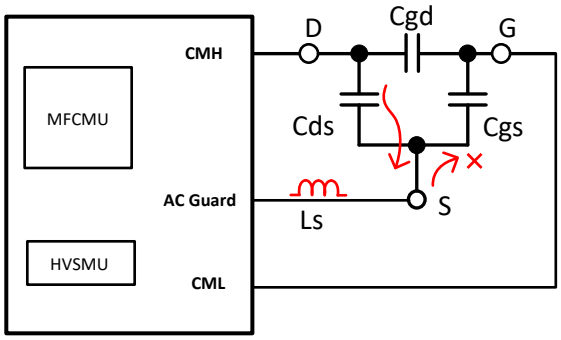


Figure 4-2 Crss Measurement using AC Guard Terminal

Connecting the AC guard to the third terminal ensures that current through the parasitic path (Cds) does not impact measurement accuracy of the target capacitance (Cgd), as measurements are taken via the CML node. This approach presumes that the impedance of the AC guard node is substantially lower than that of the parasitic path (Cgs).

In practice, however, the presence of parasitic inductance (Ls) on the AC Guard side can notably affect the measurement, thereby making accurate determination of Cgd challenging.

5. Capacitance calculation with TCAD Simulation.

In the field of power devices, TCAD is widely recognized as the industry standard device simulator tool for both process and structural development. For the constructed device elements, electrical characteristic simulations (DC/AC/Transient) can be performed by applying electrical signals to the electrodes. To calculate various junction capacitances within devices, it is incorporating a range of established computational methods and is routinely used to confirm AC characteristics.

Figure 5-1 shows TCAD simulation results that yield *completely identical* at both 100 kHz and 1 MHz—there is absolutely no difference between the outcomes at these two frequencies. In contrast, measurement results from the actual device taken at 100 kHz and 1 MHz show better agreement with the calculated values at 100 kHz. It should also be clearly stated here that the measurements were thoroughly open/short calibrated before measurement.

The fact that the simulations give the same results at both frequencies shows that capacitance should not change depending on the measurement frequency. So, if any differences are found in the experimental data, those differences are probably due to errors in how the measurements were taken.

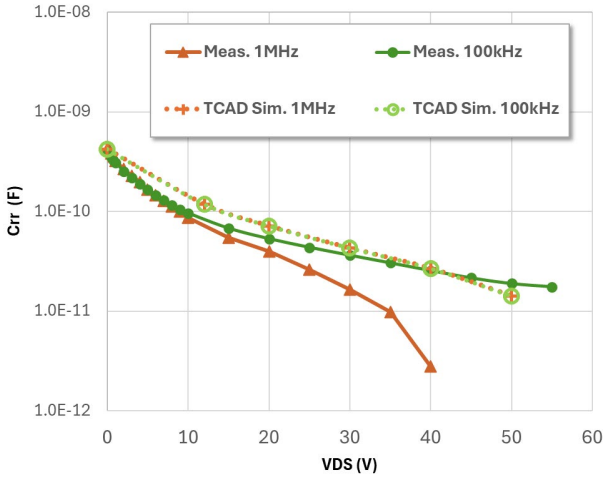
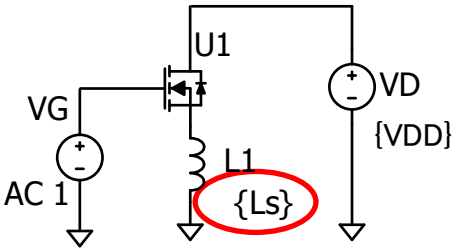


Figure 5-1 TCAD Results vs Measurement results by frequency calculation

6. Verification of the effects of inductance through simulation

SPICE models with Split-Gates can be downloaded from Renesas' website. These models are high-precision models and exhibit high reproducibility with actual measurements for DC characteristics [5]. Using this SPICE model, we compared simulations of conventional Standard-Gate Trench structures and Split-Gate structures for Crss.



.ac List {f}
.param f=1000k
.step dec param VDD 150m 150 10
.param Ls=100n

Figure 6-1 Simulation Circuit

Figure 6-2 shows SPICE simulation results using different Ls values from Figure 6-1. This Ls value indicates the parasitic inductance observed in actual measurements. Figure 6-2 (a) presents a Standard-Gate Trench structure, whereas Figure 6-2 (b) features a Split-Gate Trench design.

As you can see, in both graphs, when Ls = 0 nH, the values at 100 kHz and 1 MHz are identical. However, in the Split-Gate structure shown in Figure 6-2(b), even a slight increase in Ls causes the Crss value to change significantly. It is clear that the results diverge greatly from those at 100 kHz.

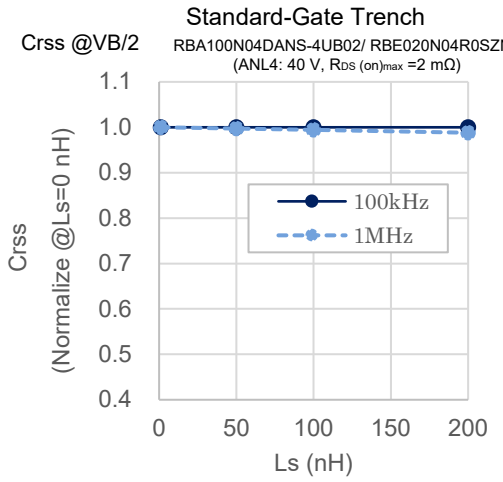


Figure 6-2 (a)

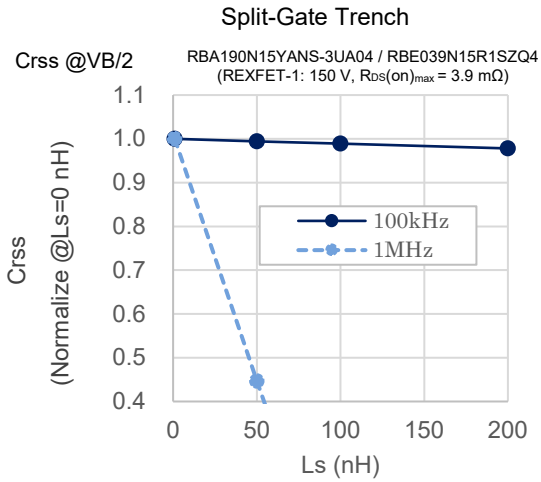


Figure 6-2 (b)

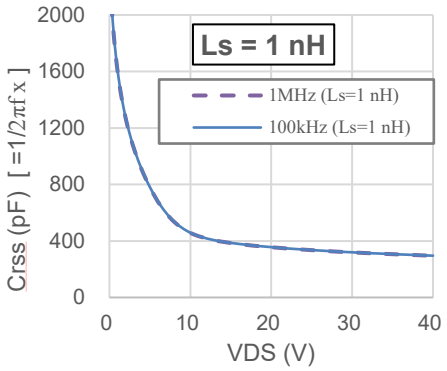
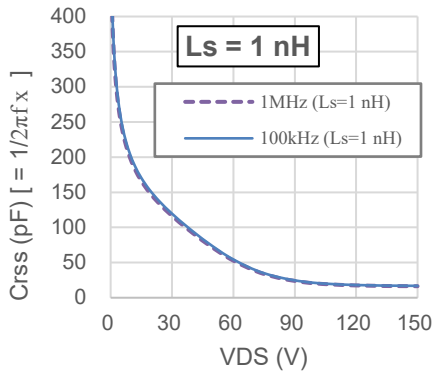
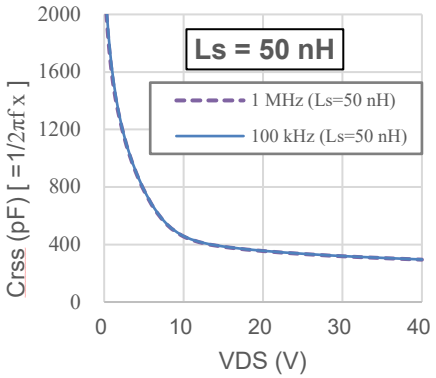
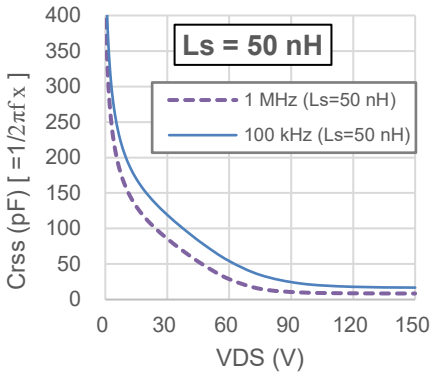
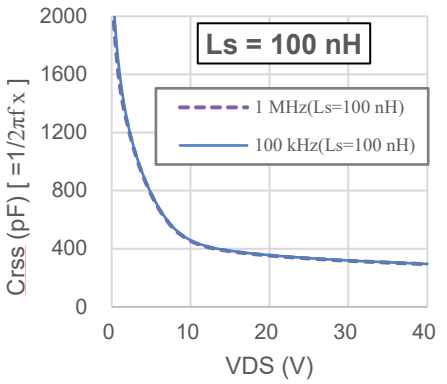
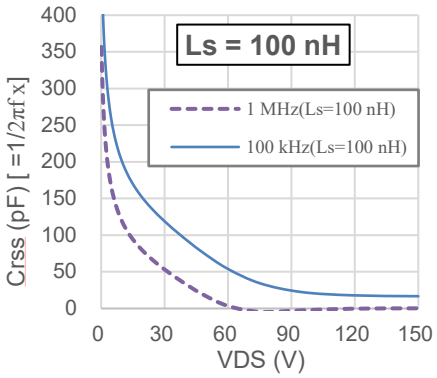
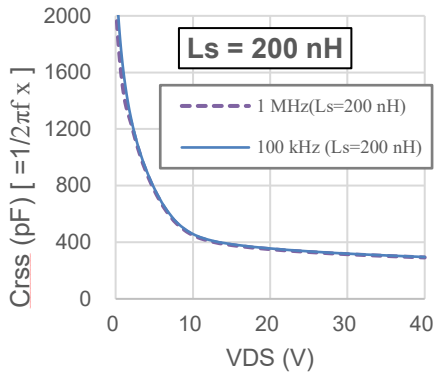
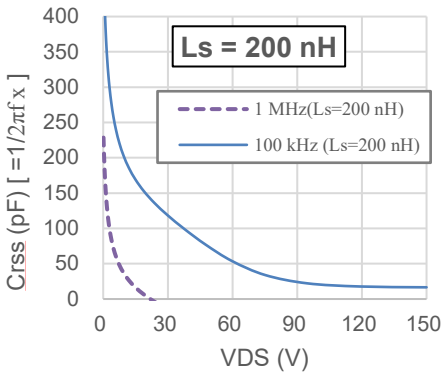
Crss value by parasitic inductance Ls

(Normalize Value as of Ls=0nH)

Next, let's examine the voltage dependence of Crss with respect to VDS. Figure 6-3 shows for the Crss graph dependent on VDS. Looking at the results for the Split-Gate Trench on the right side of Figure 6-3, In case of frequency of 1 MHz with L ≥ 50 nH, the values are significantly different from those at 100 kHz. On the other hand, in conventional Standard-Gate Trench structures, even when Ls reaches 200 nH, no frequency-dependent differences are observed.

Given the commonly accepted physical constant that 1 nH is approximately equivalent to 1 mm in length, a value of 50 nH corresponds to roughly 50 mm of wiring. Since such measurements require strict tolerance, most devices are insufficient for accurate evaluation.

Figure 6-3 Crss Calculation by Ls

	Standard-Gate Trench RBA100N04DANS-4UB02/ RBE020N04R0SZN6 (ANL4: 40 V, RDS(on)max = 2 mΩ)	Split-Gate Trench RBA190N15YANS-3UA04 / RBE039N15R1SZQ4 (REXFET-1: 150 V, RDS(on)max = 3.9 mΩ)
Ls 1.0nH		
Ls 50nH		
Ls 100nH		
Ls 200nH		

7. Summary and Conclusion

The latest technology with split-gate structures exhibits exceptionally low Crss values, with relatively large Ciss which poses significant challenges for accurate measurement due to the impact of the structural input capacitance ratio and parasitic inductance components.

In theory, if parasitic inductance components are ignored, TCAD and SPICE simulations produce results that do not depend on measurement frequency. However, in actual measurements, measurement errors due to parasitic components (inductive reactance) have a large impact, making it important to measure at an appropriate frequency.

For such Split-Gate structure of Power MOSFETs, it has been demonstrated that even with proper calibration applied, actual measurements become very difficult in high-frequency regions such as 1 MHz due to the influence of parasitic inductance. On the other hand, conventional Standard-Gate Trench structures allow relatively accurate measurements even at 1 MHz.

Renesas REXFET datasheets do not specify the 1 MHz data because it is extremely challenging to conduct an actual measurement, not only for vendors but also for the users who use these products. Instead, Renesas datasheet provides results at *100 kHz*, enabling users to subsequently obtain measurements using an impedance meter/power analyzer, which can measure accurately for the sake of users.

Table 7-1 example of datasheet capacitance.（RBA190N15YANS-3UA04 / RBE039N15R1SZQ4)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{iss}	—	5500	—	pF	V_{DS} = 75 V, V_{GS} = 0 V *f = 100 kHz*
Output Capacitance	C_{oss}	—	1800	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	33	—	pF	

8. [Appendix] Capacitive Reactance and Inductive Reactance

A basic understanding of electrical circuits is provided to explain impedance components and assess measured values.

Let's review capacitive and inductive reactance using a simple series RLC circuit (see Figure 8-1). The impedance Z at angular frequency ω can be separated into real and imaginary components as shown in equation (7). In Figure 8-2, when $\omega < 1/\sqrt{LC}$ (or when $\varphi < 0$), the reactance X is capacitive. Thus, for the RLC circuit to display capacitive behavior, the frequency f must be at or below $1/(2\pi\sqrt{LC})$.

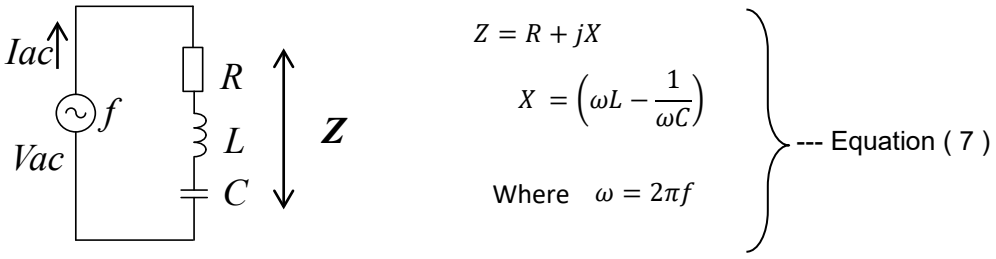


Figure 8-1 Series RLC Circuit

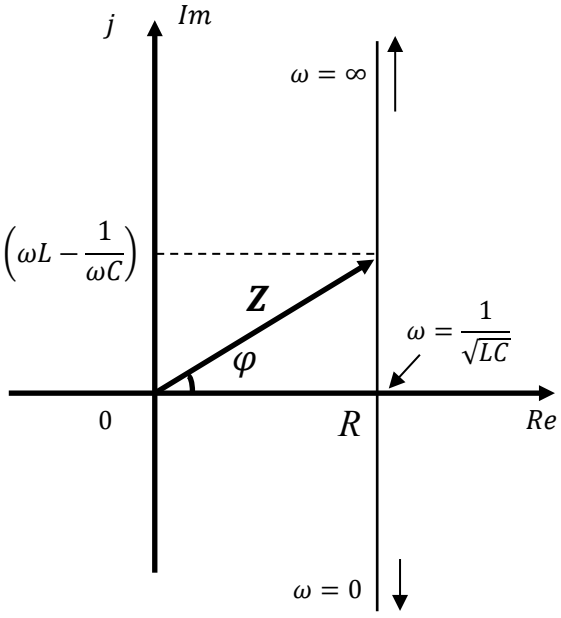


Figure 8-2 Impedance Z locus

During capacitance measurements with an impedance analyzer, the inductive component is accurately eliminated through calibration. However, MOSFET capacitance does not correspond to a straightforward series RLC circuit; it varies according to the VDS bias and includes intricate pathways for parasitic RLC elements, thereby requiring highly precise measurement techniques.

Consequently, it is essential to consider these complexities when performing measurements in actual circuits.

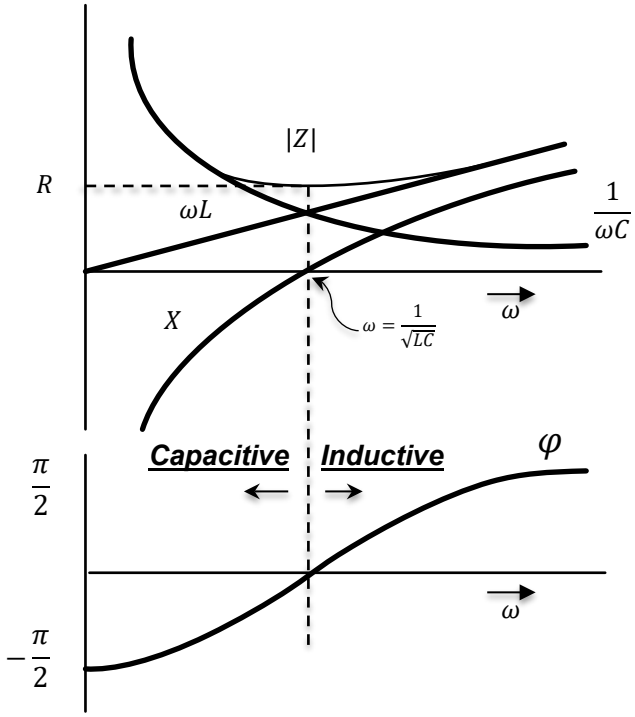


Figure 8-3 Frequency Response

9. Reference

1. Renesas Electronics Corporation. (2025, November). *MOSFET REXFET-1 Middle Voltage Product Technology Development: Application Note (R07AN0040EJ0100)*. Renesas Electronics Corporation.
2. Renesas Electronics Corporation. (2025, October). *Leveraging Split-Gate Trench Process to Advance MOSFET Performance: White Paper*. Renesas Electronics Corporation:
3. Renesas Electronics Corporation. (2022, December). *Power MOSFETs Application Note: Application Note (R07AN0007EJ0110)*. Renesas Electronics Corporation.
4. Keysight Technologies. (2015). *Direct Power MOSFET Capacitance Measurement at 3000V: Application Note (No. 5990-7145EN)*. Keysight Technologies.
5. Renesas Electronics Corporation. (2025, May). *Renesas Power MOS SPICE Model: Application Note (R07AN0048EJ0100)*. Renesas Electronics Corporation.

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