MOSFET

Power Discrete Bare Die Products Reliability

Introduction

This document explains the reliability of Renesas power discrete products shipped as bare die.

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1. Bare Die Product Reliability

1.1 Approach to Quality

In accordance with the quality policy stated in Figure 1-1, Renesas Electronics has established a quality assurance system based on the ISO 9001 and ISO/TS 16949 standards. Renesas is developing consistent quality assurance and quality control across all stages from product planning to after-sales services, based on “built-in quality” that is backed up with reliability technologies. Renesas has always placed great emphasis on maintaining and improving levels of quality and reliability. From the development to the delivery of a products, Renesas implements quality control and reliability verification from the three standpoints of “quality control and reliability verification in design”, “quality control in production”, and “quality assurance of product”. All Renesas parties uphold the basic principle that quality comes first. To this end, they are concerned with the achievement of quality levels that satisfy customer expectations.

Figure 1-1 Renesas Electronics Quality Policy

1.2 Bare Die Product Quality Assurance

Guaranteeing the quality of bare die presumes equivalency with packaged products; such equivalency across all semiconductor devices is difficult given current technological and cost considerations.

Therefore, the quality level of bare die is classified into three levels in accordance with JEITA EDR-4703A and is based on four criteria: visual, electrical characteristics, early failures, and long-term reliability. The three levels, Level 1: Known Good Die (KGD), Level 2: Known Tested Die (KTD), and Level 3: Probed Die (PD). Are described in detail below. Table 1-1 shows an overview of the quality assurance scope at each level, including customers and end users.

Renesas power discrete products are classified as Level 3/Probed Die, unless special delivery specifications have been agreed upon.

1.2.1 Level: KGD (Known Good Die)

(1) Visual

A full visual inspection is conducted. Definitions of defects and defective products, inspection items, inspection methods, etc. are stipulated in an individual specification, with user agreement as stipulated in the delivery specifications.

(2) Electrical characteristics

Probing tests are conducted with the aim of meeting the characteristics equivalent to those of packaged products that have passed the final special characteristics inspection. Specific measurement items and standards must be stipulated in an individual specification, with user agreement as stipulated in the delivery specifications.

(3) Characteristics results after semiconductor user implementation

Early defects (including defects resulting from the wafer process that become apparent after user mounting, such as aging on boards and equipment) equivalent to the quality rate of packaged products are guaranteed.

Electrical characteristic defects cannot be guaranteed after mounting because AC characteristics are affected by the mounting configuration itself.

(4) Early failures

The early failure rate of the bare die resulting from the wafer process should be equivalent to that of the packaged products. This excludes any failure modes caused by package assembly or mounting carried out by the user. If the specified level is not met, additional screening processes, including burn-in, will be applied in the same way they are for normal packaged products to ensure the required quality level is achieved.

(5) Long-term reliability

The failure rate of the bare die resulting from the wafer process should be equivalent to that of packaged products. (Failure modes caused by package assembly or mounting carried out by the user are excluded.)

1.2.2 Level 2: KTD (Known Tested Die)

(1) Visual

The same inspection as for Level 1/KGD is conducted.

(2) Electrical characteristics

The same tests as for Level 1/KGD are conducted.

(3) Characteristics results after semiconductor user implementation

- Early defects:
  Early defects resulting from the wafer process are guaranteed to be equivalent to those of packaged products. However, defects that become apparent after user mounting, such as aging on boards and equipment, are not covered by the guarantee.
- Electrical characteristic defects:
  Electrical characteristics cannot be guaranteed after mounting because AC characteristics are affected by the mounting configuration itself.

(4) Early failures

Not covered by the guarantee.

(5) Long-term reliability

Not covered by the guarantee.

1.2.3 Level 3: PD (Probed Die)

(1) Visual

Sampling inspection is conducted.

(2) Electrical characteristics

Probing tests are conducted with the aim of meeting the characteristics equivalent to packaged products that have passed the final special characteristics inspection. The specific measurement items and standards are stipulated in an individual specification, with user agreement as stipulated in the delivery specifications.

(3) Characteristics results after semiconductor user implementation

Not covered by the guarantee.

(4) Early failures

Not covered by the guarantee.

(5) Long-term reliability

Not covered by the guarantee.

Table 1-1 Quality Assurance Application Overview

Process		Level 1/KGD	Level 2/KTD	Level 3/PD
Semiconductor Manufacturers	Wafer	Products that have completed the wafer process before characteristics inspection.	Same as Level 1	Same as Level 1
	Probing characteristics inspection	Non-defective products selected based on the same criteria as final inspection of packaged products. Details are stipulated in individual specifications.	Same as Level 1	Non-defective products selected based on some of the final inspection criteria for packaged products. Details are stipulated in individual specifications.
	Visual inspection	A full visual inspection is conducted. Details are stipulated in individual specifications.	Same as Level 1	Sampling inspection is conducted. Details are stipulated in individual specifications.
	Shipment	Shipping format is stipulated in individual specifications.	Same as Level 1	Same as Level 1
Semiconductor Users	Acceptance inspection process	Defined in individual specifications. Visual and electrical characteristics are covered by guarantee.	Same as Level 1	Same as Level 1
	Mounting process	Defects caused by mounting are not covered by guarantee.	Same as Level 1	Same as Level 1
	Characteristics inspection process	・Early defects resulting from the wafer process (including defects that become apparent, such as in-process aging) should be equivalent to those of packaged products. However, failures due to mounting are excluded. ・Electrical characteristics are not covered by guarantee.	・Early defects resulting from the wafer process should be equivalent to those of packaged products. However, defects that become apparent due to in-process aging or mounting are excluded. ・Electrical characteristics are not covered by guarantee.	Not covered by guarantee.
Market	Early failures	Failures resulting from the wafer process should be equivalent to those of packaged products.	Not covered by guarantee.	Same as Level 2
	Long-term reliability	Failures resulting from the wafer process should be equivalent to those of packaged products.	Not covered by guarantee.	Same as Level 2

1.3 Power Discrete Bare Die Product Reliability

The reliability of Renesas power discrete bare die products is tested under the conditions stipulated in the reliability documentation. However, the reliability of a bare die product in its fully assembled state depends not only on chip-specific factors, but also on storage conditions, assembly conditions, sealing conditions, etc., so it is difficult to guarantee the reliability of the chip alone. We highly recommend that customers conduct sufficient verification in conditions reflecting the actual application.

1.4 Reliability Testing

Reliability testing is a series of laboratory tests carried out under known stress conditions to evaluate the lifetime of a device or system. Reliability tests are performed to ensure that semiconductor devices maintain the performance and functions throughout their life.

These reliability tests aim to simulate or accelerate by the stresses that the semiconductor device may encounter during all phases of its life, including mounting, aging, field installation and operation.

Reliability tests are defined individually in the specifications for each product. Table 1-2 shows an example of a reliability test for automotive quality bare die product.

Table 1-2 Automotive Quality Bare Die Product Reliability Testing Example

Reliability Testing Example (MOSFET)				
No.	Test Item	Symbol	Test Conditions	Test Qty.
1	High Temperature Reverse Bias	HTRB	T_j=175°C, V_{DSS}=Maximum rating, 1000h	3 Lots 231 pcs
2	High Temperature Gate Bias	HTGB	T_j=175°C, V_{GSS}=20V, 1000h	3 Lots 231 pcs
3	Electrostatic Discharge Human Body Model	ESDH	C=100pF, R=1.5kΩ	1 Lot 30 pcs

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.11.2025	-	First edition

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