RZ/G2L
Power Consumption Measurement

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Information

This application note provides measurement results of power consumption of RZ/G2L in some use cases.

Target Device

RZ/G2L

Table of Contents

1. Power Rail Overview

The RZ/G2L has several power supply domains; 1.1V, 1.8V, 1.2V and 3.3V. A power system example with a power management IC, PMIC, is depicted in the following figure. The 1.1V power supply to the core logic of this SoC is aggregated to the VDD. Thus, Current flow on the VDD changes along with computationally demands. Current flows on other power rails also change along with each function demands.

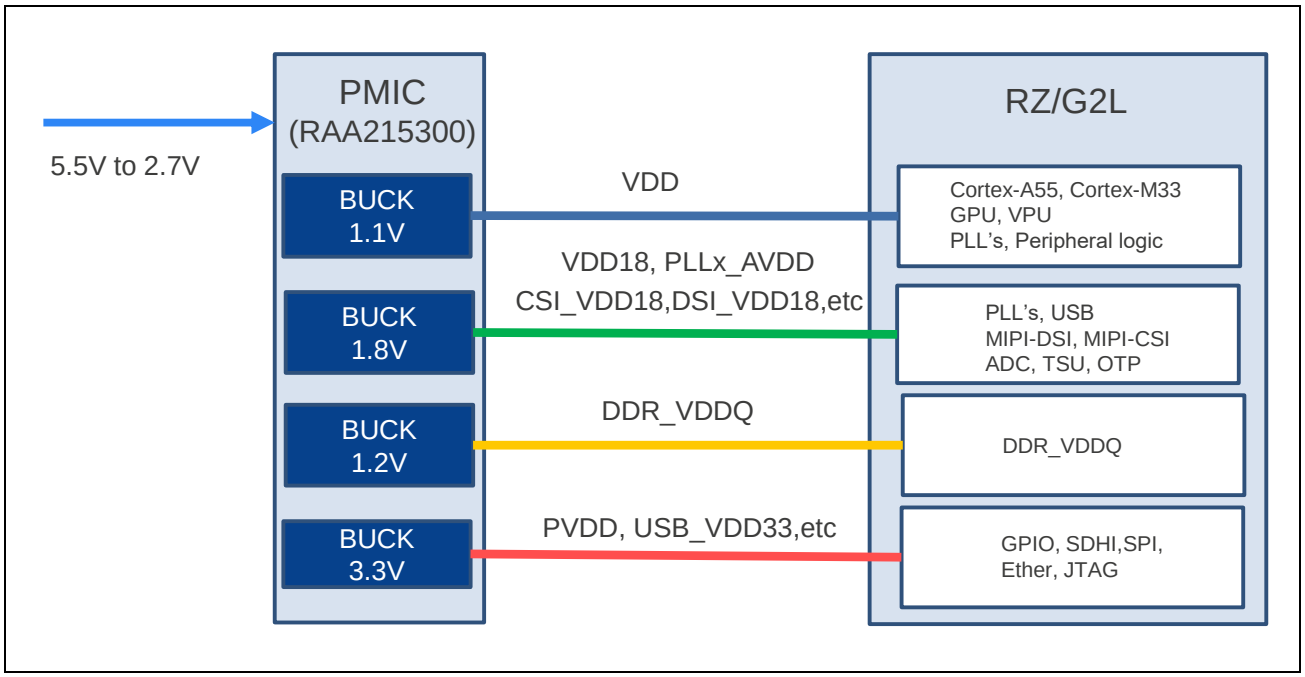

Figure 1.1 A power system example

2. Measurement Condition

- Device condition
  - Process TYP
  - VDD TYP
  - Temperature Room (Ta ≈ 25°C)
- DRAM configuration
  Two packages
- Target power rails
  Power rails for only core supplies, 1.1V for VDD and 1.2V for VDDQ of a DRAM.
  Power rails for 1.8V and 3.3V supply for not only the SoC core logic but other devices. Thus, these two supplies are not suitable for evaluation of SoC's internal power.
- Use cases
  - Suspend to Console (Idle State)
  - 1-Core Dhrystone
  - 2-Core Dhrystone
  - Qt (Cinematic Experience) Demo
  - 2-Core Dhrystone + GPU

3. Measurement Results

This chapter provides measurement results of power consumption in five use cases;

- Suspend to Console (Idle State)
- 1-Core Dhrystone
- 2-Core Dhrystone
- Qt (Cinematic Experience) Demo
- 2-Core Dhrystone + GPU

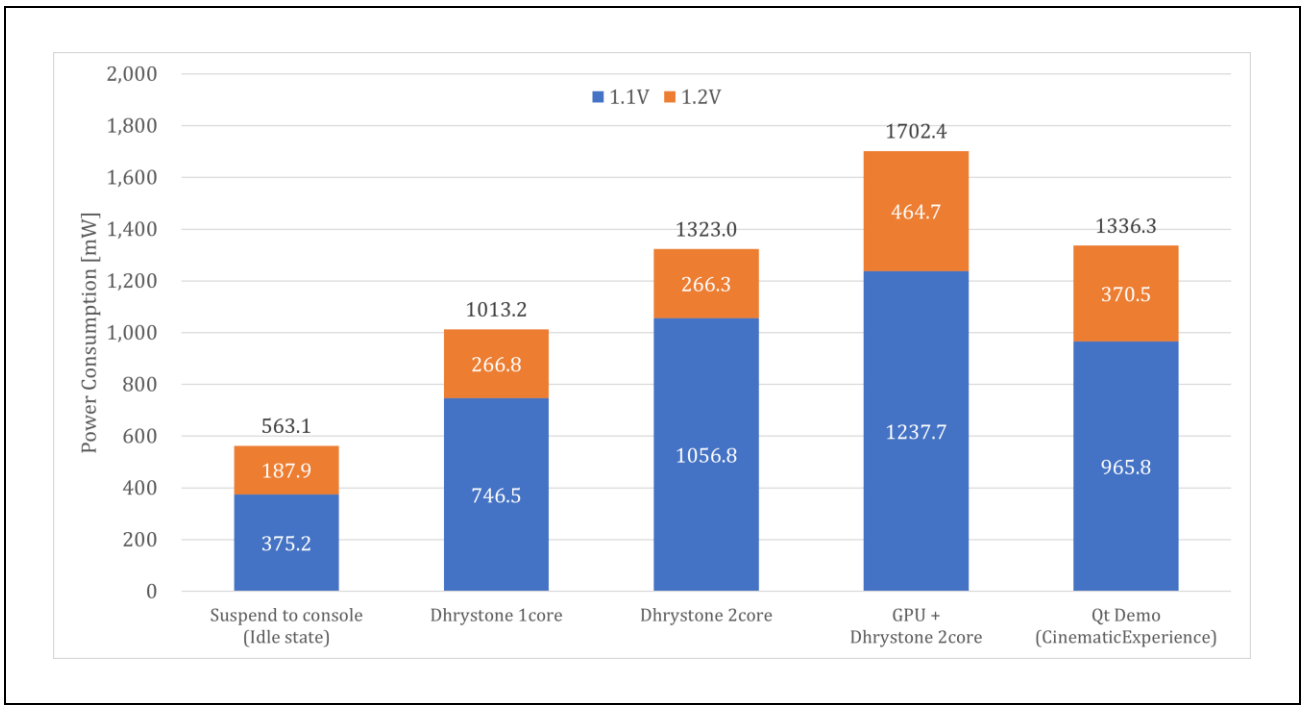

Figure 3.1 Power Consumption in Each Use Case

3.1 Suspend to Console (Idle State)

In this use case, the CPU clocks down to 150MHz, and other clocks are gated except for ones needed for wake-up from the serial console interruption.

During this use case, both Arm Cortex-A55 and M33 cores are powered on because the power-gating is NOT available.

Table 3.1 Measurement result in suspend to console

Power Rail	Voltage*1 [V]	Current [mA]	Power [mW]
VDD	1.1	308.1	375.2
VDDQ for DDR	1.2	155.5	187.9
Total Power	—	—	563.1

Note 1. Design values.

3.2 1-Core Dhrystone

In this use case, “Dhrystone”, well-known CPU benchmark program, is executed on one CPU core with 1.2GHz clock.

Table 3.2 Measurement result in 1-core Dhrystone

Power Rail	Voltage*1 [V]	Current [mA]	Power [mW]
VDD	1.1	678.6	746.5
VDDQ for DDR	1.2	221.8	266.8
Total Power	—	—	1013.2

Note 1. Design values.

3.3 2-Core Dhrystone

In this use case, “Dhrystone” is executed on both two CPU cores with 1.2GHz clock.

Table 3.3 Measurement result in 2-core Dhrystone

Power Rail	Voltage*1 [V]	Current [mA]	Power [mW]
VDD	1.1	960.7	1056.8
VDDQ for DDR	1.2	221.4	266.3
Total Power	—	—	1323.0

Note 1. Design values.

3.4 Qt (Cinematic Experience) Demo

In this use case, “Qt (Cinematic Experience) Demo” is executed on both two CPU cores with 1.2GHz clock, and “GUI of Qt” is also executed with the GPU.

Table 3.4 Measurement result in Qt (Cinematic Experience) Demo

Power Rail	Voltage*1 [V]	Current [mA]	Power [mW]
VDD	1.1	878.0	965.8
VDDQ for DDR	1.2	308.1	370.5
Total Power	—	—	1336.3

Note 1. Design values.

3.5 2-Core Dhrystone + GPU

In this use case, “Dhrystone” is executed on both two CPU cores with 1.2GHz clock, and “glmark2” is also executed with the GPU.

Table 3.5 Measurement result in 2-core Dhrystone + GPU (glmark2)

Power Rail	Voltage*1 [V]	Current [mA]	Power [mW]
VDD	1.1	1125.2	1237.7
VDDQ for DDR	1.2	386.4	464.7
Total Power	—	—	1702.4

Note 1. Design values.

REVISION HISTORY	RZ/G2L Power Consumption Measurement

Rev.	Date	Description	
		Page	Summary
1.00	Aug 10, 2022	—	First edition issued
1.10	Jan 24, 2023	4, 5	Qt (Cinematic Experience) Demo, added to the description of the use cases
		5	Figure 3.1, added
		6	The power value in Table 3.1, modified
		9	Section 3.4, added

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   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
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