RL78/F22

Porting Guide from RL78/F12, F13 to RL78/F22 Products

R01AN7698EJ0100
Rev.1.00
2025. 7.30

Introduction

RL78/F22 product is successors of RL78/F12, F13 (LIN) products and support security, 12-bit A/D converter and other enhanced peripheral functions.

RL78/F22 product has the same functions of general-timers and serial interfaces as RL78/F13 (LIN) product. Pin assignments and software of RL78/F22 products are compatible with current products.

The peripheral functions installed in RL78/F22 product are partially different from those of RL78/F12 product. The pin assignments are also partially different.

This application note provides comparisons between RL78/F12, F13 (LIN) products and RL78/F22 products, and can be used as a general guide during the migration from RL78/F12, F13 (LIN) products to RL78/F22 products.

Target Devices

Source Devices	Destination Devices
RL78/F13 (LIN) (48/32/30/20-pin)	**RL78/F22 (48/32/24-pin)**
RL78/F12 (48/32/30/20-pin)	**RL78/F22 (48/32/24-pin)**

Contents

1. Overview

This document describes differences between RL78/F22 products and RL78/F12, F13 (LIN) products, and provides notes when replacing RL78/F12, F13 (LIN) products with RL78/F22 products.

A thorough evaluation needs to be performed when replacing RL78/F12, F13 (LIN) products with RL78/F22 products. For details of each product, refer to the hardware user's manuals.

1.1 Product Lineup

Tables below show the lineup of RL78/F22 products together with corresponding RL78/F12 and RL78/F13 (LIN) products.

Table 1-1. RL78/F22 Products Lineup, Compared with RL78/F13 (LIN) products

Source Devices: RL78/F13 (LIN) Products						Destination Devices: RL78/F22 Products					
Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature Ta (°C)	Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature Ta (°C)
80QFP	128/96/64	4	8/6/4	32	-40 to 105	48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						–
64QFP	128/96/64/ 48/32	4	8/6/4/ 3/2	32	-40 to 105	48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						–
48QFP 48QFN	128/96/64/ 48/32/16	4	8/6/4/ 3/2/1	32	-40 to 105	48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						–
32QFN	64/48/32/16	4	4/3/2/1	32	-40 to 105	32QFN	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						–
30SSOP	64/48/32/16	4	4/3/2/1	32	-40 to 105	32QFN	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						–
20SSOP	64/48/32/16	4	4/3/2/1	32	-40 to 105	24QFN	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						–

Caution RL78/F22 product does not have packages 80-QFP and 64-QFP. If many I/O pins are used, RL78/F22 product is not a candidate for replacement. Please consider replacing it with RL78/F23, F24 and RL78/F25 products.
RL78/F22 product is available in temperature grades 3 and 4 (grade-3: -40 to 105 °C, grade-4: -40 to 125 °C). In that case, consider RL78/F23, F24 (grade-5) product, which offers improved performance and functionality over RL78/F13 (LIN) (Y-grade) product.

Table 1-2. RL78/F22 Products Lineup, Compared with RL78/F12 products

Source Devices: RL78/F12 Products						Destination Devices: RL78/F22 Products					
Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature Ta (°C)	Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature Ta (°C)
64QFP	64/48/32/ 24/16	4	4/3/2/ 1.5/1	32	-40 to 85	48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
48QFP 48QFN	64/48/32/ 24/16	4	4/3/2/ 1.5/1	32	-40 to 85	48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
32QFN	64/48/32/ 24/16	4	4/3/2/ 1.5/1	32	-40 to 85	32QFN	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
30SSOP	64/48/32/ 24/16	4	4/3/2/ 1.5/1	32	-40 to 85	32QFN	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
20SSOP	64/48/32/ 24/16/8	4	4/3/2/ 1.5/1/0.5	32	-40 to 85	24QFN	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125

Caution RL78/F22 product does not have package 64-QFP. If many I/O pins are used, RL78/F22 product is not a candidate for replacement. Please consider replacing it with RL78/F23, F24 and RL78/F25 products.

1.2 Product Feature Comparison

Tables below show the feature comparisons between RL78/F22 products and RL78/F12, F13 (LIN) products. Each function of RL78/F13 (LIN) product and RL78/F12 product shown in the table below is an example of the maximum memory product.

Table 1-3. Main Features of RL78/F22, Compared with RL78/F13 (LIN)

Features		RL78/F22			RL78/F13 (LIN)				Reference pages Note
		48 QFP	32 QFP	24 QFP	48 QFP	32 QFN	30 SSOP	20 SSOP	
CPU		RL78 CPU Core			RL78 CPU Core				P.10
Memory	Code Flash	128KB			128KB	64KB			P.11
	Data Flash	8KB			4KB				
	RAM	12KB			8KB	4KB			
Supply Voltage		**1.8V** to 5.5V			2.7V to 5.5V				–
Operation Frequency		(max) **40MHz**			(max) 32MHz, 24MHz@K,Y-grade				P.16
System Clock	f_X	2MHz to 20MHz			1MHz to 20MHz				
	f_{IH}	**40MHz**			32MHz, 24MHz@K, Y-grade				
	f_{IL}	15kHz			15kHz				
	f_{SUB}	32.7kHz	–		32.7kHz	–			
	f_{PLL}	**40MHz**			32MHz, 24MHz@K, Y-grade				
Clock for Peripherals	f_{WDT}	15kHz			15kHz				
	f_{PLL}	**80MHz**			64MHz, 48MHz@K, Y-grade				
	f_{IH}	**80MHz**			64MHz, 48MHz@K, Y-grade				
POR		Yes			Yes				–
LVD		Yes			Yes				P.18
Window Watchdog Timer		Yes			Yes				–
Illegal Instruction Execution Detection Function		Yes			Yes				P.25
Flash Memory CRC Operation Function		Yes			Yes				
RAM ECC Detection Function		Yes			Yes				
Code Flash Memory ECC Function		**Yes**			–				
CAN-FD RAM ECC Detection Function		–			–				
Invalid Memory Access Detection Function		Yes			Yes				
Frequency Detection Function		Yes			Yes				
Clock Monitor Function		Yes			Yes				
Stack Pointer Monitor Function		Yes			Yes				
I/O Port Output Level Detection Function		Yes			Yes				
A/D Test Function		Yes			Yes				
I/O Port		36	23	15	38	25	23	13	P.15
	Output Only	1	0	0	1	0	0	0	
	Input Only	5	3	3	5	3	3	3	
Power Supply Pin	Internal Circuit	V_{DD}, V_{SS}, REGC			V_{DD}, V_{SS}, REGC				
	I/O Port	–			–				
	Analog	V_{DD}, V_{SS}, **AV_{DD}, AV_{SS}**, AV_{REFP}, AV_{REFM}			V_{DD}, V_{SS}, AV_{REFP}, AV_{REFM}				
Interrupt	External	12	8	7	12	8	8	7	P.28
	Internal	39	39	39	35	26	26	26	
DTC		37	36	35	36	29	29	28	–
Timer	TAU (16-bit)	12			12	8			P.20
	Timer RD	16-bit×2 (**w/ PWMOPA and Dithering/Gate**)			16-bit×2				
	Timer RJ	16-bit×1			16-bit×1				
	RTC	1			1				
Serial I/F	SAU CSI/simplified I^2C/UART/ **Simplified-I^2S**	4/4/2/**1**	3/3/2/**1**	2/2/2/**1**	4/4/2/0	2/2/1/0			P.22
	SPI	Yes (CSI mode)			Yes (CSI mode)				
	Multimaster I^2C	1			1	0			
	LIN/UART module	RLIN3: 1			RLIN3: 1				
	CAN interface	–			–				
A/D Converter	Resolution	**12-bit**			10-bit				P.23
	Number of ch	17	8	4	15	8	10	4	
8-bit D/A Converter		–			–				–
Comparator		–			–				–
Application Accelerator Unit (AAU)		**Yes**			–				P.26
Secure Module (AESEA)		**Yes**			–				P.27
Capacitive Sensing Unit (CTSU2SLa)		**12**	**10**	**7**	–				P.27
ELC		–			–				–

Note Refers to the detail page of each function.

Table 1-4. Main Features of RL78/F22, Compared with RL78/F12

Features		RL78/F22			RL78/F12				Reference pages Note
		48 QFP	32 QFP	24 QFP	48 QFP	32 QFN	30 SSOP	20 SSOP	
CPU		RL78 CPU Core (S3)			RL78 CPU Core (S2)				P.10
Memory	Code Flash	128KB			64KB				P.11
	Data Flash	8KB			4KB				
	RAM	12KB			4KB				
Supply Voltage		1.8V to 5.5V			1.8V to 5.5V				–
Operation Frequency		(max) **40MHz**			(max) 32MHz, 24MHz@K-grade				P.16
System Clock	f_X	2MHz to 20MHz			1MHz to 20MHz				
	f_{IH}	**40MHz**			32MHz, 24MHz@K-grade				
	f_{IL}	15kHz			15kHz				
	f_{SUB}	32.7kHz	–		32.7kHz	–			
	f_{PLL}	**40MHz**			–				
Clock for Peripherals	**f_{WDT}**	15kHz			15kHz (f_{IL})				
	f_{PLL}	**80MHz**			–				
	f_{IH}	**80MHz**			32MHz, 24MHz@K-grade				
POR		Yes			Yes				–
LVD		Yes			Yes				P.18
Window Watchdog Timer		Yes			Yes				–
Illegal Instruction Execution Detection Function		Yes			Yes				P.25
Flash Memory CRC Operation Function		Yes			Yes				
RAM ECC Detection Function		Yes			Yes (Only RAM parity error detection)				
Code Flash Memory ECC Function		**Yes**			–				
CAN-FD RAM ECC Detection Function		–			–				
Invalid Memory Access Detection Function		Yes			Yes				
Frequency Detection Function		Yes			Yes				
Clock Monitor Function		Yes			–				
Stack Pointer Monitor Function		Yes			–				
I/O Port Output Level Detection Function		Yes			–				
A/D Test Function		Yes			Yes				
I/O Port		36	23	15	38	25	23	13	P.15
	Output Only	1	0	0	1	0	0	0	
	Input Only	5	3	3	5	3	3	3	
Power Supply Pin	Internal Circuit	V_{DD}, V_{SS}, REGC			V_{DD}, V_{SS}, REGC				
	I/O Port	–			–				
	Analog	V_{DD}, V_{SS}, **AV_{DD}, AV_{SS}**, AV_{REFP}, AV_{REFM}			V_{DD}, V_{SS}, AV_{REFP}, AV_{REFM}				
Interrupt	External	12	8	7	10	6	6	5	P.28
	Internal	39	39	39	34	34	34	28	
DTC		37	36	35	DMA: 2				–
Timer	TAU (16-bit)	12			8				P.20
	Timer RD	16-bit×2 (**w/ PWMOPA and Dithering/Gate**)			–				
	Timer RJ	16-bit×1			Interval timer: 12-bit×1 Wakeup timer: 16-bit×1				
	RTC	1			1	–			
Serial I/F	SAU CSI/simplified I^2C/UART/ **Simplified-I^2S**	4/4/2/**1**	3/3/2/**1**	2/2/2/**1**	6/5/2/0	4/3/4/0		2/1/2/0	P.22
	SPI	Yes (CSI mode)			Yes (CSI mode)				
	Multimaster I^2C	1			1			0	
	LIN/UART module	RLIN3: 1			LIN-UART (UARTF): 1				
	CAN interface	–			–				
A/D Converter	Resolution	**12-bit**			10-bit				P.23
	Number of ch	17	8	4	10	8	8	4	
8-bit D/A Converter		–			–				–
Comparator		–			–				–
Application Accelerator Unit (AAU)		**Yes**			–				P.26
Secure Module (AESEA)		**Yes**			–				P.27
Capacitive Sensing Unit (CTSU2SLa)		**12**	**10**	**7**	–				P.27
ELC		–			–				–

Note Refers to the detail page of each function.

2. Pin Assignment

2.1 Pin Assignment Comparison

Tables below show the pin functional comparisons and differences between RL78/F22 product and RL78/F12, F13 (LIN) product. Each function of RL78/F22, RL78/F13 (LIN) and RL78/F12 product shown in the tables below is an example of the 48-QFP product.

Table 2-1. Port Functions of RL78/F22, Compared with RL78/F13 (LIN)

RL78/F22			RL78/F13				RL78/F22 Pin Function	RL78/F13 (LIN) Pin Function
48QFP	32QFN	24QFN	48QFP	32QFN	30SSOP	20SSOP		
1	1	24	1	1	6	2	P120/ANI23/TI07/TO07/(TO13)/TRDIOD0/SO01/(SCK10)/INTP4	P120/ANI25/TI07/TO07/TRDIOD0/SO01/(SCK10)/INTP4
2	2	-	2	2	7	-	P41/TI10/TO10/TRJIO0/TRD0RES/(SI10)/(RXD1)/SNZOUT2	P41/TI10/TO10/TRJIO0/SNZOUT2
3	3	1	3	3	8	3	P40/TOOL0	P40/TOOL0
4	4	2	4	4	9	4	RESET	RESET
5	-	-	5	-	-	-	P124/XT2/EXCLKS	P124/XT2/EXCLKS
6	-	-	6	-	-	-	P123/XT1	P123/XT1
7	5	3	7	5	10	5	P137/INTP0	P137/INTP0
8	6	4	8	6	11	6	P122/X2/EXCLK	P122/X2/EXCLK
9	7	5	9	7	12	7	P121/X1	P121/X1
10	8	6	10	8	13	8	REGC	REGC
11	9	7	11	9	14	9	V_{SS}	V_{SS}
12	10	8	12	10	15	10	V_{DD}	V_{DD}
13	11	-	13	11	-	-	P60/(TO01)/(SCK00)/(SCL00)/TS0	P60/(SCK00)/(SCL00)
14	12	-	14	12	-	-	P61/(TO02)/(SI00)/(SDA00)/(RXD0)/TS1	P61/(SI00)/(SDA00)/(RXD0)
15	13	9	15	13	-	-	P62/(TO03)/(SO00)/(TXD0)/SCLA0/TS2	P62/(SO00)/(TXD0)/SCLA0
16	14	10	16	14	-	-	P63/(TO07)/(SSI00)/SDAA0/TS3	P63/(SSI00)/SDAA0
17	-	-	17	-	-	-	P00/(TI05)/(TO05)/INTP9	P00/(TI05)/(TO05)/INTP9
18	-	-	18	-	-	-	P140/TRD1RES/PCLBUZ0	P140/PCLBUZ0
19	-	-	19	-	-	-	P130/RESOUT	P130/RESOUT
20	-	-	20	-	-	-	P73/ANI27/SSI11/SNZOUT7/TS4	P73/SSI11/SNZOUT7
21	-	-	21	-	-	-	P72/ANI26/SO11/SNZOUT6/TS5	P72/SO11/SNZOUT6
22	-	-	22	-	-	-	P71/ANI25/SCK11/SCL11/INTP6/SNZOUT5	P71/SCK11/SCL11/INTP6/SNZOUT5
23	-	-	23	-	-	-	P70/ANI24/SI11/SDA11/INTP8/SNZOUT4	P70/SI11/SDA11/INTP8/SNZOUT4
24	-	-	24	-	-	-	P32/(SO11)/INTP7	P32/INTP7
25	15	11	25	15	16	11	P30/TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0	P30/TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0
26	16	12	26	16	17	12	P17/TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3/TS6	P17/TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3
27	17	13	27	17	18	13	P16/TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD/TS7	P16/TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
28	18	14	28	18	19	14	P15/TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/RTC1HZ/TOOLTXD/TS8	P15/TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/RTC1HZ/TOOLTXD
29	-	-	29	-	-	-	P31/(INTP2)/STOPST	P31/(INTP2)/STOPST
30	19	15	30	19	20	15	P14/TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0/TS9	P14/TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0
31	20	16	31	20	21	16	P13/TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0/TS10	P13/TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
32	21	17	32	21	22	-	P12/TI11/TO11/(TRDIOD0)/SO10/TXD1/INTP5/SNZOUT3/TSCAP	P12/TI11/TO11/(TRDIOD0)/SO10/TXD1/INTP5/SNZOUT3
33	22	23	33	22	23	-	P11/TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1	P11/TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1
34	23	-	34	23	24	-	P10/TI13/TO13/TRJO0/SCK10/SCL10/TS11	P10/TI13/TO13/TRJO0/SCK10/SCL10
35	24	18	35	24	25	17	AV_{DD}/AV_{REFP}	P33/AV_{REFP}/ANI0
36	25	19	36	25	26	18	AV_{SS}/AV_{REFM}	P34/AV_{REFM}/ANI1
37	26	20	37	26	27	19	P80/ANI0	P80/ANI2
38	27	21	38	27	28	20	P81/ANI1	P81/ANI3
39	28	22	39	28	29	-	P82/ANI2	P82/ANI4
40	29	-	40	29	30	-	P83/ANI3	P83/ANI5
41	30	-	41	30	1	-	P84/ANI4	P84/ANI6
42	31	-	42	31	2	-	P85/ANI5	P85/ANI7
43	-	-	43	-	3	-	P86/ANI6	P86/ANI8
44	-	-	44	-	4	-	P87/ANI7	P87/ANI9
45	-	-	45	-	-	-	P90/ANI8	P90/ANI10
46	-	-	46	-	-	-	P91/ANI9	P91/ANI11
47	-	-	47	-	-	-	P92/ANI10	P92/ANI12
48	32	-	48	32	5	1	P125/ANI22/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1	P125/ANI24/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1

Remark: KRx (Key Return) function depends on the product. For details, see “Table 2-3. Pin Assignment for KRx Function”.

Table 2-2. Port Functions of RL78/F22, Compared with RL78/F12

RL78/F22			RL78/F12				RL78/F22 Pin Function	RL78/F12 Pin Function
48QFP	32QFN	24QFN	48QFP	32QFN	30SSOP	20SSOP		
1	1	24	37	32	4	-	P120/ANI23/TI07/TO07/(TO13)/TRDIOD0/SO01/(SCK10)/INTP4	P120/ANI19
2	2	-	38	-	-	-	P41/TI10/TO10/TRJIO0/TRD0RES/(SI10)/(RXD1)/SNZOUT2	P41/TI07/TO07
3	3	1	39	1	5	3	P40/TOOL0	P40/TOOL0
4	4	2	40	2	6	4	RESET	RESET
5	-	-	41	-	-	-	P124/XT2/EXCLKS	P124/XT2/EXCLKS
6	-	-	42	-	-	-	P123/XT1	P123/XT1
7	5	3	43	3	7	5	P137/INTP0	P137/INTP0
8	6	4	44	4	8	6	P122/X2/EXCLK	P122/X2/EXCLK
9	7	5	45	5	9	7	P121/X1	P121/X1
10	8	6	46	6	10	8	REGC	REGC
11	9	7	47	7	11	9	V_{SS}	V_{SS}
12	10	8	48	8	12	10	V_{DD}	V_{DD}
13	11	-	1	9	13	-	P60/(TO01)/(SCK00)/(SCL00)/**TS0**	P60/SCLA0
14	12	-	2	10	14	-	P61/(TO02)/(SI00)/(SDA00)/(RXD0)/**TS1**	P61/SDAA0
15	13	9	3	11	-	-	P62/(TO03)/(SO00)/(TXD0)/SCLA0/**TS2**	P62
16	14	10	4	-	-	-	P63/(TO07)/(SSI00)/SDAA0/**TS3**	P63
17	-	-	5	12	15	11	P00/(TI05)/(TO05)/INTP9	P31/TI03/TO03/INTP4/(PCLBUZ0)
18	-	-	6	-	-	-	P140/TRD1RES/PCLBUZ0	P75/SCK01/SCL01/INTP9
19	-	-	7	-	-	-	P130/RESOUT	P74/SI01/SDA01/INTP8/KR4
20	-	-	8	-	-	-	P73/ANI27/SSI11/SNZOUT7/**TS4**	P73/SO01/KR3
21	-	-	9	-	-	-	P72/ANI26/SO11/SNZOUT6/**TS5**	P72/SO21/KR2
22	-	-	10	-	-	-	P71/ANI25/SCK11/SCL11/INTP6/SNZOUT5	P71/SI21/SDA21/KR1
23	-	-	11	13	-	-	P70/ANI24/SI11/SDA11/INTP8/SNZOUT4	P70/SCK21/SCL21/KR0
24	-	-	12	14	16	-	P32/(SO11)/INTP7	P30/SCK11/SCL11/RTC1HZ/INTP3
25	15	11	13	15	17	12	P30/TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0	P50/SI11/SDA11/LRXD0/INTP1
26	16	12	14	16	18	13	P17/TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3/**TS6**	P51/SO11/LTXD0/INTP2
27	17	13	15	17	19	14	P16/TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD/**TS7**	P17/TI02/TO02/(TXD0)
28	18	14	16	18	20	15	P15/TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/RTC1HZ/TOOLTXD/**TS8**	P16/TI01/TO01/(RXD0)/INTP5
29	-	-	17	19	21	-	P31/(INTP2)/STOPST	P15/(TI02)/(TO02)/SCK20/SCL20/PCLBUZ1
30	19	15	18	20	22	-	P14/TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0/**TS9**	P14/(TI03)/(TO03)/SI20/SDA20/RXD2/(SCLA0)
31	20	16	19	21	23	-	P13/TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0/**TS10**	P13/(TI04)/(TO04)/SO20/TXD2/(SDAA0)
32	21	17	20	22	24	16	P12/TI11/TO11/(TRDIOD0)/SO10/TXD1/INTP5/SNZOUT3/**TSCAP**	P12/(TI05)/(TO05)/SO00/TXD0/SOS0/TOOLTXD
33	22	23	21	23	25	17	P11/TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1	P11/(TI06)/(TO06)/SI00/SDA00/RXD0/SIS0/RXDS0/TOOLRXD
34	23	-	22	24	26	18	P10/TI13/TO13/TRJO0/SCK10/SCL10/**TS11**	P10/(TI07)/(TO07)/SCK00/SCL00/SCKS0
35	24	18	23	-	-	-	**AV_{DD}**/AV_{REFP}	P146
36	25	19	24	25	27	-	**AV_{SS}**/AV_{REFM}	P147/ANI18
37	26	20	25	-	-	-	P80/ANI0	P27/ANI7
38	27	21	26	-	-	-	P81/ANI1	P26/ANI6
39	28	22	27	-	-	-	P82/ANI2	P25/ANI5
40	29	-	28	-	-	-	P83/ANI3	P24/ANI4
41	30	-	29	26	28	-	P84/ANI4	P23/ANI3
42	31	-	30	27	29	19	P85/ANI5	P22/ANI2
43	-	-	31	28	30	20	P86/ANI6	P21/ANI1/AV_{REFM}
44	-	-	32	29	1	1	P87/ANI7	P20/ANI0/AV_{REFP}
45	-	-	33	-	-	-	P90/ANI8	P130
46	-	-	34	30	2	2	P91/ANI9	P01/TO00/RXD1
47	-	-	35	31	3	-	P92/ANI10	P00/TI00/TXD1
48	32	-	36	-	-	-	P125/ANI22/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1	P140/INTP6/PCLBUZ0

Remark: KRx (Key Return) function of RL78/F22 product varies depending on the product. For details, see “Table 2-3. Pin Assignment for KRx Function”.

Caution: Pins P60 to P63 of RL78/F12 have an N-channel open-drain port.

Table 2-3. Pin Assignment for KRx Function

Pin Function (Key return)	KRx Assigned Pin (No difference between RL78/F22 and RL78/F13 (LIN) products)									
	48QFP		32QFN		30SSOP		24QFN		20SSOP	
	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1
KR7	-	P92	-	-	-	P87	-	-	-	-
KR6	-	P91	-	-	-	P86	-	-	-	-
KR5	-	P90	-	P85	-	P85	-	-	-	-
KR4	-	P87	-	P84	-	P84	-	-	-	-
KR3	P73	P86	-	P83	-	P83	-	-	-	-
KR2	P72	P85	-	P82	-	P82	-	P82	-	-
KR1	P71	P84	-	P81	-	P81	-	P81	-	P81
KR0	P70	P83	-	P80	-	P80	-	P80	-	P80

The table below shows extended functions on RL78/F22 products.

Table 2-4. Pin Function Added to RL78/F22 Product

Pin Function	Description
AV_{DD}, AV_{SS}	It is equipped with a dedicated analog power supply pin.
TSCAP	It is the reference power supply pin for the CTSU2SLa.
TS0 to TS11	These are measurement pins for the CTSU2SLa.
TRD0RES, TRD1RES	It is the counter reset signal input pin for TRD0 and TRD1 of the Timer RDe.

Table 2-5. RL78/F22 Pin Function Added from RL78/F13 (LIN) Product

Added Pin Function	Added Purpose	Setting to Use
P32/**(SO11)**	**Expanded pin allocation**	PIOR43 = 0, PIOR92 = 1
P41/**TRD0RES**	**Expanded the Timer RDe function**	– (TRD0 for Timer RDe counter reset signal input)
P41/**(SI10)/(RXD1)**	**Expanded pin allocation**	PIOR42 = 0, PIOR91 = 1
P60/**(TO01)**	**Expanded pin allocation**	PIOR11 = 1, PIOR90 = 1
P61/**(TO02)**	**Expanded pin allocation**	PIOR12 = 1, PIOR90 = 1
P62/**(TO03)**	**Expanded pin allocation**	PIOR13 = 1, PIOR90 = 1
P63/**(TO07)**	**Expanded pin allocation**	PIOR17 = 1, PIOR90 = 1
P120/**(TO13)**	**Expanded pin allocation**	PIOR33 = 1, PIOR95 = 1
P120/**(SCK10)**	**Expanded pin allocation**	PIOR42 = 0, PIOR91 = 1
P140/**TRD1RES**	**Expanded the Timer RDe function**	– (TRD1 for Timer RDe counter reset signal input)
TS0 to TS11, TSCAP	**Added CTSU2SLa function pin**	TSPMCxx = 1

Remarks: PIOR11, PIOR12, PIOR13, PIOR17: Bit of the PIOR1 register
PIOR33: Bit of the PIOR3 register
PIOR42, PIOR43: Bit of the PIOR4 register
PIOR90, PIOR91, PIOR92, PIOR95: Bit of the PIOR9 register (This register has been added to the RL78/F22 product.)

The table below shows functions changed on RL78/F22 products.

Table 2-6. RL78/F22 Pin Function Changed from RL78/F13 (LIN) Product

Pin Function	RL78/F13 (LIN)	RL78/F22	Purpose of Change
AV_{DD}/AV_{REFP}	P33/AV_{REFP}/ANI0	AV_{DD}/AV_{REFP}	It is equipped with a dedicated analog power supply pin.
AV_{SS}/AV_{REFM}	P34/AV_{REFM}/ANI1	AV_{SS}/AV_{REFM}	
ANI1, ANI2	P34, P80	P81, P82	ANI1, 2 have dedicated-channel S&H circuit.
ANI0 to ANI10, ANI22 to ANI27	P33, P34, P80 to P87, P90 to P92, P125, P120	P80 to P87, P90 to P92, P125, P120, P70 to P73	Changed ANI0 and ANI1 pin assignment.

For details, refer to chapters on functions A/D converter in this document.

Key Points for Porting:

- **Porting from RL78/F12 product to RL78/F22 product**

  The pin assignments differ between products RL78/F22 and RL78/F12 due to differences in the installed peripheral functions. For details, please refer to RL78/F22 User's Manual.

3. CPU Architecture

The CPU architectures of RL78/F22 product and RL78/F12, F13 products are shown in the table.

Table 3-1. CPU Architecture of RL78/F22, Compared with RL78/F12, F13

	RL78/F12	RL78/F13	RL78/F22
CPU Architecture	RL78-S2 Core	RL78-S3 Core	RL78-S3 Core
Number of Instructions	75	81	81
Multiply Instruction	Yes (MULU)	Yes (MULU/MULHU/ MULH)	Yes (MULU/MULHU/ MULH)
Division Instruction	No	Yes (DIVHU/DIVWU)	Yes (DIVHU/DIVWU)
Multiply-Accumulate Instruction	No	Yes (MACHU/MACH)	Yes (MACHU/MACH)

Remark RL78/F12 product does not have a division instruction but can use a division circuit to perform the operation.

4. Memory Map

4.1 Memory Size by Products

RL78/F22 memory sizes are Code Flash: 128 KB, Data Flash: 8 KB, and RAM: 12 KB. The memory size of Data Flash and RAM are expanded from RL78/F12, F13 (LIN) products.

Key Points for Porting:

- **Difference in memory size**
  The memory sizes have been expanded from RL78/F12, F13 (LIN) product to RL78/F22 product.
- **Difference in package**
  RL78/F22 product does not have an 80-QFP, 64-QFP, 48-QFN, 30-SSOP, or a 20-SSOP package. Consider 48-QFP, 32-QFN or 24-QFN products when migrating from those products.

4.2 Memory Map

The figures below show the comparison of memory maps for products of RL78/F22 and RL78/F13 (LIN) and products of RL78/F22 and RL78/F12.

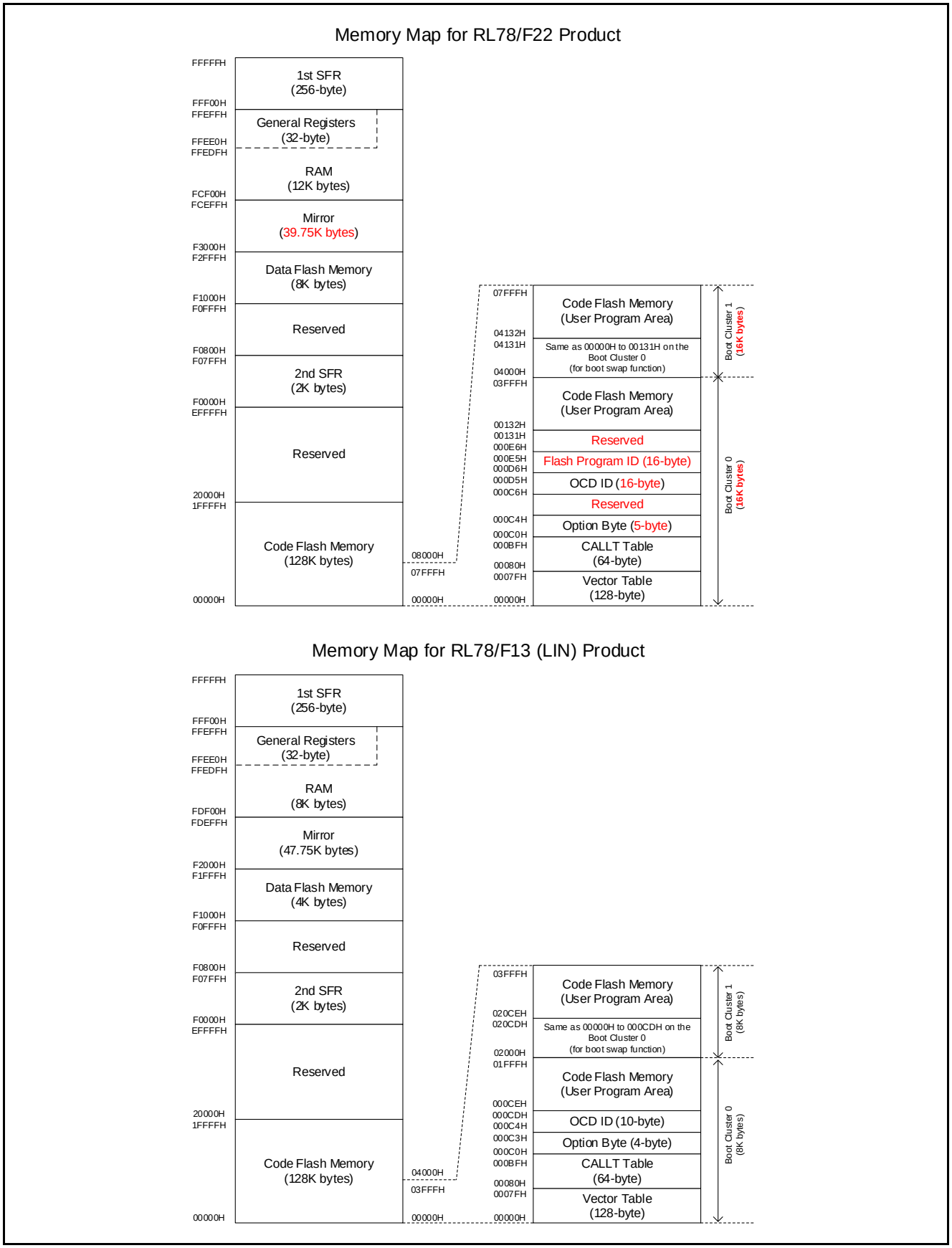


Figure 4-1. Memory Map of RL78/F22, Compared with RL78/F13 (LIN)

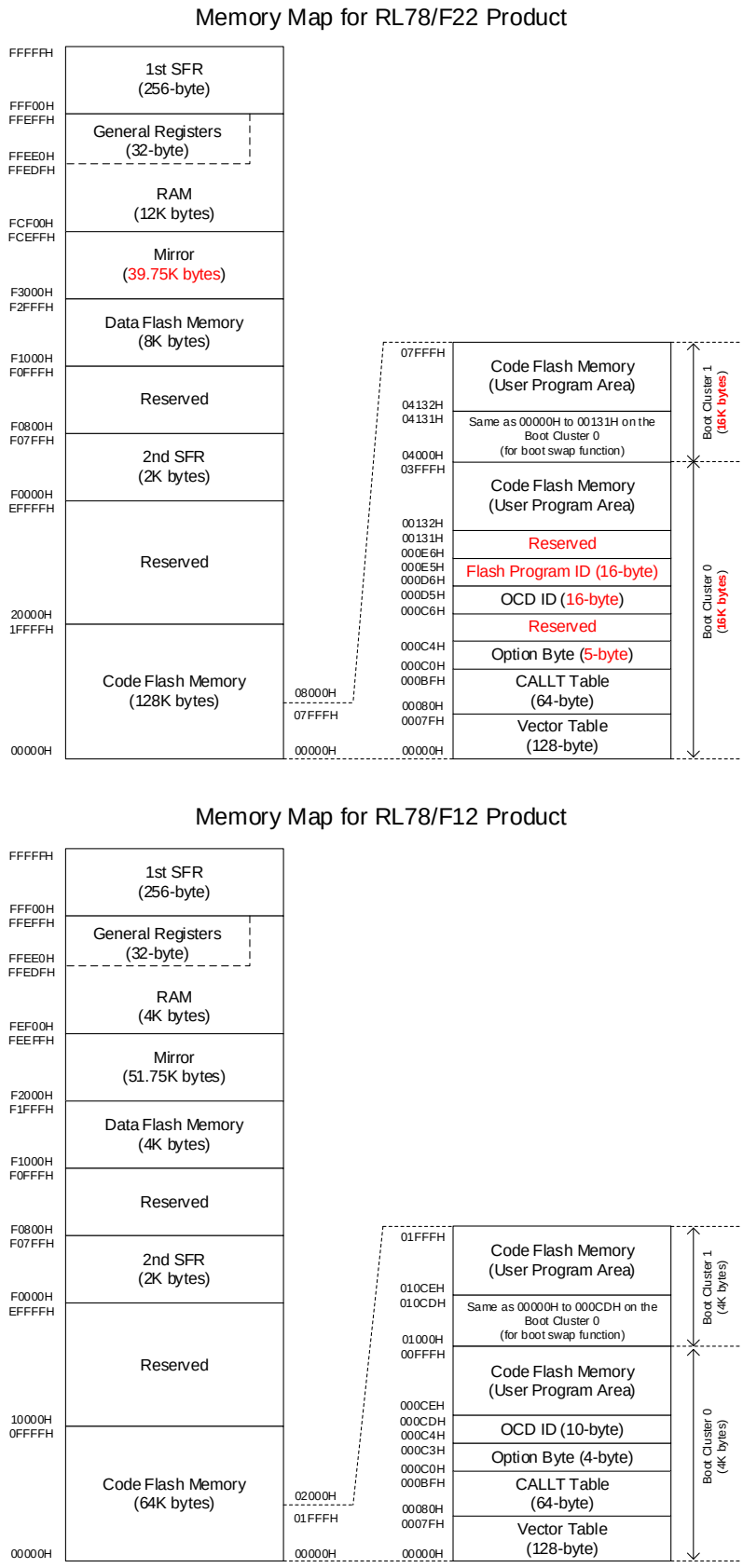


Figure 4-2. Memory Map of RL78/F22, Compared with RL78/F12

The differences in memory map between RL78/F22 product and RL78/F12, F13 (LIN) products are shown below.

- Added Security Option Byte (000C4H)
- Expanded On-chip Debug Security ID area (000C6H – 000D5H) from 80-bit to 128-bit
- Added Flash Programmer Security ID area (000D6H – 000E5H)
- Expanded Boot Cluster 0/1 memory sizes from 4 KB or 8 KB to 16 KB

The table below shows the difference between option bytes for RL78/F22 product and RL78/F12, F13 (LIN) products.

Table 4-1. Option Bytes Area of RL78/F22, Compared with RL78/F12, F13

Item	RL78/F22	RL78/F12	RL78/F13
User Option Byte 0	WDT control (000C0H/040C0H)	WDT control (000C0H/010C0H)	WDT control (000C0H/020C0H)
User Option Byte 1	LVD0, Clock monitoring function control (000C1H/040C1H)	LVD control (000C1H/010C1H)	LVD, Clock monitoring function control (000C1H/020C1H)
User Option Byte 2	High-speed OCO, RESOUTB control (000C2H/040C2H)	High-speed OCO, **Threshold**, **Flash memory operation mode control** (000C2H/010C2H)	High-speed OCO, RESOUTB control (000C2H/020C2H)
On-chip Debug Option Byte	OCD, Hot-plug-in function, Flash serial programing control (000C3H/040C3H)	OCD control (000C3H/010C3H)	OCD, Hot-plug-in function control (000C3H/020C3H)
Security Option Byte	OCD, Flash serial programing ID read control (000C4H/040C4H)	–	–

Key Points for Porting:

- **Difference in memory map**

  Security option byte, on-chip debug security ID area, and flash programmer security ID area have been expanded with the addition of security features on RL78/F22 product. Set the data according to this specification for security option byte (000C4H) added in RL78/F22 product.

- **Mirror area**

  Mirror area (mirroring the code flash memory “F0000H to FFFFFH” to “00000H to 0FFFFH or 10000H to 1FFFFH”) differs depending on the product. When using a mirror area, place the data table to be used in the mirror area in the corresponding area of the code flash memory area.
  RL78/F22 product increases RAM and Data Flash memory from RL78/F12, F13 (LIN) products. As these areas increase, the available space in mirror area decreases. If the mirror area is insufficient, access code flash memory area directly. Alternatively, copy the data from code flash memory to RAM and then access the RAM area.

- **RAMSAR register**

  RL78/F22 product sets the start address of the RAM area using RAMSAR register. The initial value of RAMSAR register is “**EFH**” (Effective area: F**EF**00H to FFEFFH (4 KB)). Be sure to set the RAM area to be used by the software.

- **Invalid memory access detection**

  RL78/F22 product extends RAM area (specified by RAMSAR register) into the area of invalid memory access detection area.

- **Port threshold selection**

  RL78/F22 and RL78/F13 products use PITHLx register to set the pin threshold selection.

- **Flash memory operation mode selection**

  In RL78/F22 and RL78/F13 products, flash memory operates only in high-speed mode (HS mode). There is no low-speed mode (LS mode).

5. Port Function

The registers that control port function of RL78/F22 product and RL78/F12, F13 products have been added due to changes in peripheral functions.

5.1 Port Function Comparison

The table below shows the differences between RL78/F22 product and RL78/F12, F13 products port function.

Table 5-1. I/O Port Register Differences of RL78/F22, Compared with RL78/F12, F13

Register	Register Description	RL78/F22
PMx	Port mode register (Input or output mode setting)	Same as RL78/F12, F13
Px	Port register (Input or output level)	Same as RL78/F12, F13
PUx	Pull-up resistor option register (Internal pull-up setting)	Same as RL78/F13, F14
PIMx	Port input mode register (C-MOS or TTL level)	Same as RL78/F12, F13
POMx	Port output mode register (C-MOS or N-ch open drain)	Added POM32 bit from RL78/F13
PMCx	Port mode control register (Digital I/O or analog I/O)	Added PMC8, 9 registers from RL78/F13
ADPC	A/D port configuration register (Digital I/O or analog I/O)	Deleted from RL78/F13 (correspond with PMCx)
PITHLx	Port input threshold control register (Schmitt 1, 3, or TTL level)	Added PITHL41, PITHL120 bits from RL78/F13
PIORx	Peripheral I/O redirection register	Added PIOR9 register from RL78/F13
PMXx	Port mode register X (Switches the pin assignment for the serial function)	Only RL78/F12 product
PSRSEL	Port output slew rate register (Normal or slow)	Same as RL78/F13
PSNZCNTx	SNOOZE status output control register (Output pun setting)	Same as RL78/F13
PMS	Port mode select register (Read from output pin level)	Same as RL78/F13
PIEN	Port input enable register (Enables pin input for serial function)	Only RL78/F12 product
TSPMCx	Touch sensor port mode control register (set the pin to be used for capacitive sensing unit)	Added in RL78/F22 product

Caution Port-related registers vary depending on the product. For details, see the user's manual.

Key Points for Porting:

- **Analog port selection**

  In RL78/F22 product, select analog input/output port with PMCx register for each pin. If the system is concerned about a short circuit between analog input adjacent pins, an open pin which output low level can be assigned between analog input pin (A) and analog input pin (B).

- **Capacitive sensing unit port selection**

  In RL78/F22 product, select capacitive sensing unit (CTSU2SLa) port with TSPMCx register for each pin.

- **Added PIOR9 register**

  In RL78/F22 product, output pin is extended so that PWM output and serial I/F can be used independently. For details, see Table 2-5.

6. Clock Generator

The table below shows the differences between RL78/F22 product and RL78/F12, F13 (LIN) products clock generator circuit.

Table 6-1. Clock Generator of RL78/F22, Compared with RL78/F12, F13

Clock Generator	RL78/F22	RL78/F12	RL78/F13
X1 clock	2MHz to 20MHz	1MHz to 20MHz	1MHz to 20MHz
XT1 clock	32.768kHz	32.768kHz	32.768kHz
PLL circuit	Max. 80MHz	No	Max. 64MHz
High-speed OCO	2MHz to 80MHz	1MHz to 32MHz	1MHz to 64MHz
Low-speed OCO	15kHz	15kHz	15kHz
Low-speed OCO for WDT	15kHz	No	15kHz
CPU operating clock	2.7V to 5.5V: MAX. 40MHz 1.8V to 2.7V: MAX. 16MHz	2.7V to 5.5V: MAX. 32MHz 1.8V to 2.7V: MAX. 8MHz	2.7V to 5.5V: MAX. 32MHz

6.1 PLL Clock Circuit

PLL clock circuit of RL78/F22 product is expanded PLL clock frequency to 80 MHz. RL78/F22 product can use up to 80 MHz PLL clock frequency or high-speed on-chip oscillator clock frequency when using Timer RDe module (count clock).

The table below shows the PLL clock circuit specifications in RL78/F22 product.

Table 6-2. PLL Clock Settings of RL78/F22

X1 Clock	X1 Clock Divider (FMAINDIV)	PLL Multiplier (PLLMULA, PLLMUL)	PLL Divider (PLLDIV0, FPLLDIV)	PLL Frequency
4MHz	00B (×1/1)	11B (×20)	01B (×1/1)	80MHz
	00B (×1/1)	11B (×20)	00B (×1/2)	40MHz
8MHz	00B (×1/1)	10B (×10)	01B (×1/1)	80MHz
	00B (×1/1)	01B (×16)	00B (×1/2)	64MHz
	00B (×1/1)	00B (×12)	00B (×1/2)	48MHz
	00B (×1/1)	10B (×10)	00B (×1/2)	40MHz
	00B (×1/1)	01B (×16)	10B (×1/4)	32MHz
	00B (×1/1)	00B (×12)	10B (×1/4)	24MHz
16MHz	10B (×1/2)	10B (×10)	01B (×1/1)	80MHz
	10B (×1/2)	01B (×16)	00B (×1/2)	64MHz
	10B (×1/2)	00B (×12)	00B (×1/2)	48MHz
	10B (×1/2)	10B (×10)	00B (×1/2)	40MHz
	10B (×1/2)	01B (×16)	10B (×1/4)	32MHz
	10B (×1/2)	00B (×12)	10B (×1/4)	24MHz
20MHz	11B (×1/4)	01B (×16)	01B (×1/1)	80MHz
	11B (×1/4)	01B (×16)	00B (×1/2)	40MHz

Caution: Bit values other than above are prohibited.

Remarks: FMAINDIV, FPLLDIV: Bits of the CKSEL register
PLLMULA, PLLMUL, PLLDIV0: Bits of the PLLCTL register

Key Points for Porting:

- **Using PLL clock circuit**

  When using PLL clock circuit, be sure to select settings shown in the table. When using a power supply voltage between 1.8 V and 2.7 V, PLL function cannot be used.

6.2 High-speed On-chip Oscillator Frequency Selection

High-speed on-chip oscillator frequency is selected by user option byte (000C2H) and HOCODIV register. In RL78/F22 product, the frequency of HOCO frequency is also expanded to 80 MHz as the maximum operating frequency is expanded. The table below shows the differences between RL78/F22 and RL78/F12, F13 products HOCO specifications.

Table 6-3. High-Speed OCO of RL78/F22, Compared with RL78/F13

HOCO DIV2	HOCO DIV1	HOCO DIV0	RL78/F22				RL78/F13			
			High-speed on-chip oscillator frequency (f_{IH})				High-speed on-chip oscillator frequency (f_{IH})			
			32 MHz base	40 MHz base	64 MHz base	80 MHz base	24 MHz base	32 MHz base	48 MHz base	64 MHz base
			FRQSEL4 = 0		FRQSEL4 = 1		FRQSEL4 = 0		FRQSEL4 = 1	
			FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1
0	0	0	32 MHz	40 MHz	64 MHz	80 MHz	24 MHz	32 MHz	48 MHz	64 MHz
0	0	1	16 MHz	20 MHz	32 MHz	40 MHz	12 MHz	16 MHz	24 MHz	32 MHz
0	1	0	8 MHz	10 MHz	16 MHz	20 MHz	6 MHz	8 MHz	12 MHz	16 MHz
0	1	1	4 MHz	5 MHz	8 MHz	10 MHz	3 MHz	4 MHz	6 MHz	8 MHz
1	0	0	2 MHz	prohibited	4 MHz	5 MHz	prohibited	2 MHz	prohibited	4 MHz
1	0	1	prohibited	prohibited	prohibited	prohibited	prohibited	1 MHz	prohibited	2 MHz
Settings other than the above are prohibited.										

Remarks: HOCODIV[2:0]: Bits of the HOCODIV register
FRQSEL4, 3: Bits of the User Option Byte (000C2H/040C2H)

Table 6-4. High-Speed OCO of RL78/F22, Compared with RL78/F12

HOCO DIV2	HOCO DIV1	HOCO DIV0	RL78/F22				RL78/F12	
			High-speed on-chip oscillator frequency (f_{IH})				High-speed on-chip oscillator frequency (f_{IH})	
			32 MHz base	40 MHz base	64 MHz base	80 MHz base	24 MHz base	32 MHz base
			FRQSEL4 = 0		FRQSEL4 = 1		–	–
			FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1
0	0	0	32 MHz	40 MHz	64 MHz	80 MHz	24 MHz	32 MHz
0	0	1	16 MHz	20 MHz	32 MHz	40 MHz	12 MHz	16 MHz
0	1	0	8 MHz	10 MHz	16 MHz	20 MHz	6 MHz	8 MHz
0	1	1	4 MHz	5 MHz	8 MHz	10 MHz	3 MHz	4 MHz
1	0	0	2 MHz	prohibited	4 MHz	5 MHz	prohibited	2 MHz
1	0	1	prohibited	prohibited	prohibited	prohibited	prohibited	1 MHz
Settings other than the above are prohibited.								

Remarks: HOCODIV[2:0]: Bits of the HOCODIV register
FRQSEL4, 3: Bits of the User Option Byte (000C2H/040C2H)

Key Points for Porting:

- **HOCO frequency setting**

  In RL78/F22 product, high-speed on-chip oscillator frequency is selected by FRQSEL[4:0] bits of the user option byte (000C2H/040C2H) and HOCODIV register. Set user option byte (000C2H/040C2H) according to the frequency used by the system.

- **PLL clock setting when FRQSEL3 bit is 0**

  In RL78/F22 product, if the FRQSEL3 bit in the user option byte 2 is set to 0 (HOCO frequency = 64/ 32/ 16/ 8/ 4/ 2 MHz), and moreover the CPU/peripheral hardware clock (f_{CLK}) is selected as the PLL clock, the f_{CLK} must not be set to 40 MHz.

7. Low Voltage Detector (LVD)

A comparison of the LVD circuit of RL78/F22 and RL78/F12, F13 products is shown in the table below.

Table 7-1. LVD Circuit of RL78/F22, Compared with RL78/F12, F13

LVD Function	RL78/F25	RL78/F12, F13
Specification	• Compare power supply voltage (V_{DD}) and LVD detection voltage (V_{LVD0}, V_{LVD1}) to generate internal reset or interrupt request. • LVD0 circuit The detection level of internal reset can be selected from 3 levels by setting user option byte. • LVD1 circuit The detection level of an interrupt request can be selected from 11 levels by setting the register.	• Compare power supply voltage (V_{DD}) and LVD detection voltage (V_{LVDH}, V_{LVDL}) to generate internal reset or interrupt request. RL78/F12: The detection level can be selected from 12 levels by setting user option byte. RL78/F13: The detection level can be selected from 6 levels by setting user option byte.
Operating mode	• Reset mode (LVD0) • Interrupt mode (LVD1)	• Interrupt & Reset mode • Reset mode • Interrupt mode
Detection voltage	• Reset mode (LVD0) - 3.96V (Rise), 3.88V (Fall) - 2.97V (Rise), 2.91V (Fall) - 1.90V (Rise), 1.86V (Fall) (*) • Interrupt mode (LVD1) - 4.16V (Rise), 4.08V (Fall) - 3.96V (Rise), 3.88V (Fall) - 3.75V (Rise), 3.67V (Fall) - 3.55V (Rise), 3.47V (Fall) - 3.35V (Rise), 3.47V (Fall) - 3.13V (Rise), 3.06V (Fall) - 2.97V (Rise), 2.91V (Fall) - 2.82V (Rise), 2.76V (Fall) - 2.09V (Rise), 2.04V (Fall) (*) - 1.98V (Rise), 1.94V (Fall) (*) - 1.88V (Rise), 1.84V (Fall) (*) (*) Only when used in the voltage range of 1.8 V.	RL78/F12: • Interrupt & Reset mode - RESET: 2.75V, 4.06V (Rise), 3.98V (Fall) - RESET: 2.75V, 3.02V (Rise), 2.96V (Fall) - RESET: 2.75V, 2.92V (Rise), 2.86V (Fall) - RESET: 2.45V, 3.75V (Rise), 3.67V (Fall) (*) - RESET: 2.45V, 2.71V (Rise), 2.65V (Fall) (*) - RESET: 2.45V, 2.61V (Rise), 2.55V (Fall) (*) - RESET: 1.84V, 3.13V (Rise), 3.06V (Fall) (*) - RESET: 1.84V, 2.09V (Rise), 2.04V (Fall) (*) - RESET: 1.84V, 1.98V (Rise), 1.94V (Fall) (*) • Reset mode, Interrupt mode - 4.06V (Rise), 3.98V (Fall) - 3.75V (Rise), 3.67V (Fall) - 3.13V (Rise), 3.06V (Fall) - 3.02V (Rise), 2.96V (Fall) - 2.92V (Rise), 2.86V (Fall) - 2.81V (Rise), 2.75V (Fall) - 2.71V (Rise), 2.65V (Fall) (*) - 2.61V (Rise), 2.55V (Fall) (*) - 2.50V (Rise), 2.45V (Fall) (*) - 2.09V (Rise), 2.04V (Fall) (*) - 1.98V (Rise), 1.94V (Fall) (*) - 1.88V (Rise), 1.84V (Fall) (*) (*) Only when used in the voltage range of 1.8 V. RL78/F13: • Interrupt & Reset mode - RESET: 2.75V, 4.74V (Rise), 4.64V (Fall) - RESET: 2.75V, 4.62V (Rise), 4.52V (Fall) - RESET: 2.75V, 4.42V (Rise), 4.32V (Fall) - RESET: 2.75V, 3.32V (Rise), 3.15V (Fall) • Reset mode, Interrupt mode - 4.74V (Rise), 4.64V (Fall) - 4.62V (Rise), 4.52V (Fall) - 4.42V (Rise), 4.32V (Fall) - 3.22V (Rise), 3.15V (Fall) - 3.02V (Rise), 2.96V (Fall) - 2.81V (Rise), 2.75V (Fall)
Interrupt	INTLVI	INTLVI

Key Points for Porting:

- **LVD reset**

  RL78/F22 product uses LVD0 circuit for LVD reset voltage detection. The reset voltage setting is selected by LVD0V[2:0] bit of user option byte (000C1H/040C1H), and operation is enabled by LVD0ENB bit. If the board using RL78/F22 product does not have a reset circuit (power on reset (POR) function is used), be sure to set the reset release voltage in LVD0V[2:0] bit and write a value that enables the operation of LVD0 circuit in LVD0ENB bit.

- **LVD interrupt**

  RL78/F22 product uses LVD1 circuit for LVD interrupt voltage detection. Before setting LVD1EN bit of LVIS register to 1 (LVD1 circuit operation enabled), set the voltage to be detected in LVD1V[4:0] bit of LVIS register.

8. Timer Functions

The timer functions of RL78/F22 product is extended for the maximum operating frequency. In addition, the Timer RDe extends the PWM output control function in addition to the conventional functions. The tables below show the differences between RL78/F22 product and RL78/F12, F13 (LIN) products timer functions. RL78/F22 and RL78/F12, F13 products in the table below indicate the maximum number of channels available for the product.

Table 8-1. Timer Functions of RL78/F22, Compared with RL78/F13

Timer Function	RL78/F22	RL78/F13 (LIN)
Timer Array Unit (TAU)	16-bit × 12ch Operating frequency: 40MHz	16-bit × 12ch Operating frequency: 32MHz
Timer RD	16-bit × 2ch (Timer RDe) Operating frequency: 80MHz with PWMOPA, Dithering/Gate control	16-bit × 2ch Operating frequency: 64MHz
Timer RJ	16-bit × 1ch Operating frequency: 40MHz	16-bit × 1ch Operating frequency: 32MHz
Real-time Clock	1ch	1ch

Table 8-2. Timer Functions of RL78/F22, Compared with RL78/F12

Timer Function	RL78/F22	RL78/F12
Timer Array Unit (TAU)	16-bit × 12ch Operating frequency: 40MHz	16-bit × 8ch Operating frequency: 32MHz
Timer RD	16-bit × 2ch (Timer RDe) Operating frequency: 80MHz with PWMOPA, Dithering/Gate control	No
Interval Timer	No	12-bit × 1ch
Timer RJ	16-bit × 1ch Operating frequency: 40MHz	No
Wakeup Timer	No	16-bit × 1ch
Real-time Clock	1ch	1ch

Table 8-3. Timer RDe Functions of RL78/F22

Timer RDe Features		RL78/F22 Timer RDe
Input capture function		MAX. 8ch (Same as RL78/F13.)
Output compare function		MAX. 8ch (Same as RL78/F13.)
PWM function	Reset synchronous PWM mode	MAX. 6ch [Positive-phase: 3, Negative-phase: 3] (Same as RL78/F13.)
	Complementary PWM mode	MAX. 6ch [Positive-phase: 3, Negative-phase: 3] (Same as RL78/F13.)
	PWM3 mode	MAX. 2ch (Same as RL78/F13.)
	Extended PWM mode	**MAX. 4ch [Dithering function, Gate function]**
	Extended complementary PWM mode	**MAX. 6ch [Positive-phase: 3, Negative-phase: 3, Asymmetric PWM pulse control, Interrupt and A/D trigger signal decimation function]**
PWM output forced cutoff function		**PWMOPA**
Interrupt, A/D trigger		Interrupt: INTTRD0, INTTRD1 **A/D trigger: INTTRD0_IFA, INTTRD1_IFA, INTTRD0_IFB, INTTRD1_IFB, INTTRD1_UDF, INTTRD_ADTRG** **Supports interrupt request and A/D trigger decimation function.**

Key Points for Porting:

- **Timer operating frequency**

  Set the count source and counter value for each timer function according to the maximum operating frequency extension of RL78/F22 product.

- **Timer RDe extended functionality**

  Timer RDe of RL78/F22 product extends the function from Timer RD of RL78/F13 product. Extended complementary PWM mode (synchronous/asynchronous three-phase PWM output), extended PWM mode (with dithering/gate, and counter reset input function), and PWM forced cutoff circuit (PWMOPA) have been added while maintaining the conventional specifications. Moreover, the resolution of a timer is improved by expanding the maximum operating frequency.

9. Serial Interfaces

Tables below show the differences between RL78/F22 product and RL78/F12, F13 products serial I/F. RL78/F22 and RL78/F12, F13 products in the table below indicate the maximum number of channels available for the product.

Table 9-1. Serial I/F of RL78/F22, Compared with RL78/F13

Serial I/F	RL78/F22	RL78/F13 (LIN)
Serial Array Unit (SAU)	2 units (SAU0, 1)	2 units (SAU0, 1)
CSI (SPI) mode	4 channels	4 channels
UART mode	2 channels	2 channels
Simplified-I²C mode	4 channels	4 channels
Simplified-I²S mode	**1 channel**	–
Multimaster I²C (IICA)	1 channel	1 channel
LIN/UART module (RLIN3)	1 channel	1 channel

Table 9-2. Serial I/F of RL78/F22, Compared with RL78/F12

Serial I/F	RL78/F22	RL78/F12
Serial Array Unit (SAU)	2 units (SAU0, 1)	3 units (SAU0, 1, S)
CSI (SPI) mode	4 channels	8 channels
UART mode	2 channels	4 channels
Simplified-I²C mode	4 channels	6 channels
Simplified-I²S mode	**1 channel**	–
Multimaster I²C (IICA)	1 channel	1 channel
LIN/UART module	1 channel (RLIN3)	1 channel (UARTF)

Key Points for Porting:

- **Serial I/F operating frequency**

  Set the count source and baud rate generator for each serial I/F function according to the maximum operating frequency extension of RL78/F22 product.

- **Simplified-I²S function**

  In RL78/F22 product, simplified-I²S (master only) communication is possible using serial array unit (CSI10) and timer array unit (TAU12, TAU13).

10. A/D Converter

The table below shows differences between RL78/F22 product and RL78/F12, F13 products A/D converter.

Table 10-1. A/D Converter of RL78/F22, Compared with RL78/F13

A/D Converter Features	RL78/F22	RL78/F13 (LIN)
Resolution	**12 bits**	10 bits
Analog input channels	48-QFP: 17ch [ANI0 to ANI10, ANI22 to ANI27] 32-QFN: 8ch [ANI0 to ANI5, ANI22, ANI23] 24-QFN: 4ch [ANI0 to ANI2, ANI23] High-speed channels: ANI0 to ANI10 Normal-speed channels: ANI22 to ANI27	80-QFP: 20ch [ANI0 to ANI15, ANI24 to ANI27] 64-QFP: 12ch [ANI0 to ANI11] 48-QFP: 12ch [ANI0 to ANI11] 32-QFN: 8ch [ANI0 to ANI7] 30-SSOP: 10ch [ANI0 to ANI9] 20-SSOP: 4ch [ANI0 to ANI3] Normal channels: ANI0 to ANI15 Extended channels: ANI24 to ANI27
Expansion input channels	• Internal reference voltage (V_{BGR})	• Internal reference voltage (V_{BGR}) • **Internal temperature sensor**
Operating modes	• Single scan mode • Continuous scan mode • Group scan mode (group A and B)	• One-shot conversion mode • Sequential conversion mode
A/D trigger	• Software trigger • Synchronous trigger	• Software trigger • Hardware trigger (no-wait or wait mode)
Interrupt	• INTAD (A/D conversion end) • INTADGB (group B A/D conversion end)	• INTAD (A/D conversion end)
Others	**Channel-dedicated S&H circuit (ANI1, ANI2)**	–
	Sampling state cycle setting for each channel	–
	Self-diagnosis mode (ANin=Vref, Vref/2, 0)	Self-diagnosis mode (ANin=Vref, 0)
	Addition/Average operation mode	–
	Disconnection detection assist function	Self-diagnosis mode

Table 10-2. A/D Converter of RL78/F22, Compared with RL78/F12

A/D Converter Features	RL78/F22	RL78/F12
Resolution	**12 bits**	10 bits
Analog input channels	48-QFP: 17ch [ANI0 to ANI10, ANI22 to ANI27] 32-QFN: 8ch [ANI0 to ANI5, ANI22, ANI23] 24-QFN: 4ch [ANI0 to ANI2, ANI23] High-speed channels: ANI0 to ANI10 Normal-speed channels: ANI22 to ANI27	64-QFP: 12ch [ANI0 to ANI7, ANI16 to ANI19] 48-QFP: 10ch [ANI0 to ANI7, ANI18, ANI19] 32-QFN: 8ch [ANI0 to ANI3, ANI16 to ANI19] 30-SSOP: 8ch [ANI0 to ANI3, ANI16 to ANI19] 20-SSOP: 4ch [ANI0 to ANI2, ANI16] Normal channels: ANI0 to ANI7 Extended channels: ANI16 to ANI19
Expansion input channels	• Internal reference voltage (V_{BGR})	• Internal reference voltage (V_{BGR}) • **Internal temperature sensor**
Operating modes	• Single scan mode • Continuous scan mode • Group scan mode (group A and B)	• One-shot conversion mode • Sequential conversion mode
A/D trigger	• Software trigger • Synchronous trigger	• Software trigger • Hardware trigger (no-wait or wait mode)
Interrupt	• INTAD (A/D conversion end) • INTADGB (group B A/D conversion end)	• INTAD (A/D conversion end)
Others	**Channel-dedicated S&H circuit (ANI1, ANI2)**	–
	Sampling state cycle setting for each channel	–
	Self-diagnosis mode (ANin=Vref, Vref/2, 0)	Self-diagnosis mode (ANin=Vref, 0)
	Addition/Average operation mode	–
	Disconnection detection assist function	Use self-diagnosis mode

Key Points for Porting:

- **Analog input channels**

  In RL78/F22 product, ANI1 and ANI2 implement channel dedicated sample & hold circuit and can be sampled at the same time by hardware trigger input. Use ANI0 to ANI10 analog input channels when fast A/D conversion time is required.

- **A/D data register**

  RL78/F22 product A/D data registers (stores A/D conversion result) are implemented for each channel. In addition, the A/D data register can be right-aligned (store in bits 0 to 11) or left-aligned (store in bits 4 to 15) when storing the A / D conversion result.

- **A/D converter related register**

  In RL78/F22 A/D module, the register is window type. Select a window to access the corresponding register. A/D data register from ANI0 to ANI7 can be accessed as mirror register without setting the window. Software processing can be reduced by preferentially using the ANI0 to ANI7 inputs.

11. Safety Functions

The table below shows the differences between RL78/F22 and RL78/F12, F13 products safety functions.

Table 11-1. Safety Function Differences of RL78/F22, Compared with RL78/F12, F13

Safety Features	RL78/F22	RL78/F13 (LIN)	RL78/F12
Window watchdog timer	Yes	Yes	Yes
Illegal instruction execution detection function	Yes	Yes	Yes
Flash memory CRC operation function	Yes	Yes	Yes
General-purpose CRC function	Yes	Yes	Yes
RAM ECC (1-bit correction/ 2-bit detection)	Yes	Yes	No (RAM parity error detection)
Invalid memory access detection function	Yes (The range set in RAMSAR register is also included.)	Yes	Yes
Frequency detection function	Yes	Yes	Yes
Clock monitor function	Yes (Supports self-diag function)	Yes	Yes
Stack pointer monitor function	Yes	Yes	No
I/O port output level detection function	Yes	Yes	Yes
A/D test function	Yes (Disconnection detection assist function, Self-diag function)	Yes (Disconnection detection assist function, Self-diag function)	Yes (Disconnection detection assist function, Self-diag function)
SFR, RAM guard function	Yes	Yes	Yes (Only RAM guard function)
Code Flash memory ECC function (SEC/DED)	Yes	No	No

11.1 Memory Guard Function

The table below shows the differences between RL78/F22 and RL78/F13 products memory guard function.

Table 11-2. SFR Guard Function of RL78/F22, Compared with RL78/F13

SFR Guard Function	RL78/F22	RL78/F13 (LIN)
	Guarded SFRs	Guarded SFRs
Port function SFR guard controlled by IAWCTL.GPORT bit	PMxx, PUxx, PIMxx, POMxx, PMCxx, TSPMCx, PITHLxx, PIORx	PMxx, PUxx, PIMxx, POMxx, PMCxx, PITHLxx, PIORx
		ADPC
Interrupt function SFR guard controlled by IAWCTL.GINT bit	IFxx, MKxx, PRxx, EGPx, EGNx	IFxx, MKxx, PRxx, EGPx, EGNx
Clock control function SFR guard controlled by IAWCTL.GCSC bit	CMC, CSC, OSTS, CKC, PERx, OSMC, LVIM, LVIS, LINCKSEL, CKSEL, PLLCTL, MDIV, RTCCL, POCRES, STPSTC	CMC, CSC, OSTS, CKC, PERx, OSMC, LVIM, LVIS, LINCKSEL, CKSEL, PLLCTL, MDIV, RTCCL, POCRES, STPSTC
	CLMTES, ADCKS, PSMCR	

Key Points for Porting:

- **Difference in SFR guard function**

  As shown in the table above, some registers have been added and some have been deleted.

12. Other Features

12.1 AAU (Application Accelerator Unit)

The table below describes the AAU function added in RL78/F22 product.

Table 12-1. AAU Functions of RL78/F22

No.	AAU Algorithm Mode	Data Type	Execution Time Note 1
1	Sine operation	Input, Output: 16-bit (integer)	1 clock
2	Cosine operation	Input, Output: 16-bit (integer)	1 clock
3	Clarke and Park transformation (for FOC controls) Note 2	Input, Output: 16-bit (integer)	7 clocks
4	Inverse Park (I-Park) transformation (for FOC controls)	Input, Output: 16-bit (integer)	6 clocks
5	Inverse Clarke (I-Clarke) transformation (for FOC controls) Note 2	Input, Output: 16-bit (integer)	5 clocks
6	PI control for motor (for FOC controls)	Input, Output: 16-bit (integer)	15 clocks
7	Clarke & Park transformation and PI control for motor (for FOC controls) Note 2	Input, Output: 16-bit (integer)	22 clocks
8	I-Park & I-Clarke transformation (for FOC controls) Note 2	Input, Output: 16-bit (integer)	11 clocks
9	PI control for DC/DC control	Input, Output: 16-bit (integer)	6 clocks / ch
10	Multiply: 32-bit × 32-bit = 64-bit	Input: 32-bit (integer), Output: 64-bit (integer)	5 clocks

Notes 1. If STM=1 (Software trigger), the execution time is added by 1 cycle.
2. The AAU supports both algorithms, power invariant transformation and amplitude invariant transformation.

Key Points for Porting:

- **AAU function**

  AAU is a new function added in RL78/F22 product. By using this function, it is possible to speed up software processing such as motor vector control processing and 32-bit multiplication.

12.2 Capacitive Sensor Unit (CTSU2SLa)

The table below describes the capacitive sensing unit (CTSU2SLa) function added in RL78/F22 product.

Table 12-2. Capacitive Sensing Unit (CTSU2SLa) of RL78/F22

Item	Specification
Number of channels	• 48-QFP: 12 channels (TS0 to TS11) • 32-QFN: 10 channels (TS0 to TS3, TS6 to TS11) • 24-QFN: 7 channels (TS2, TS3, TS6 to TS10)
Pin for connecting a power supply stabilization capacitor for the touch sensor interface	TSCAP (Connect to Vss via a 10nF capacitor)
Measurement mode	• Self-capacitance measurement mode • Mutual capacitance measurement mode • Current measurement mode
Calibration mode	Characteristics correction of the current control oscillator for measurement
Adjustment for each pin	• Offset current adjustment function • Sensor drive pulse frequency specification • Measurement time specification
Noise prevention	• Synchronous noise prevention • High-pass noise prevention • Majority decision by multi-frequency measurement
Start condition	• Software trigger • External trigger
Low-power function	SNOOZE function supported
Interrupts	• INTCTSUWR (Request to write to a configuration register of an individual channel) • INTCTSURD (Request to transfer data measured by the CTSU) • INTCTSUFN (Measurement end interrupt)

Key Points for Porting:

- **Capacitive Sensing Unit (CTSU2SLa)**

  The CTSU2SLa measures the electrostatic capacitance of the capacitive sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the capacitive sensor. The CTSU2SLa function can operate in SNOOZE mode.

12.3 Security Function

The table below describes the security function added in RL78/F22 product.

Table 12-3. Security Function of RL78/F22

Item	Specification
AESEA	• Key length: 128/192/256 bits • Operating mode: ECB/CBC mode, CMAC
Random number generator	Supports

Key Points for Porting:

- **Security function**

  The security function can be used for data encryption/decryption and message authentication.

13. Interrupt

RL78/F22 product adds some interrupt sources compared to RL78/F12, F13 (LIN) products. The tables below show the differences between RL78/F22 and RL78/F12, F13 (LIN) products interrupt source.

Table 13-1. Interrupt Functions of RL78/F22, Compared with RL78/F13 (LIN) (1/2)

Vector Address	Interrupt Factor	RL78/F22			RL78/F13 (LIN)					
		48 QFP	32 QFN	24 QFN	80 QFP	64 QFP	48 QFP	32 QFN	30 SSOP	20 SSOP
0000H	RESET/POR/LVD/WDT/TRAP/IAW/CLM	○	○	○	○	○	○	○	○	○
0002H	Reserved	–	–	–	–	–	–	–	–	–
0004H	INTWDTI (Watchdog timer interval)	○	○	○	○	○	○	○	○	○
0006H	INTLVI (Voltage detection)	○	○	○	○	○	○	○	○	○
0008H	INTP0 (Pin edge detection)	○	○	○	○	○	○	○	○	○
000AH	INTP1 (Pin edge detection)	○	○	–	○	○	○	○	○	○
000CH	INTP2 (Pin edge detection)	○	○	○	○	○	○	○	○	○
000EH	INTP3 (Pin edge detection)	○	○	○	○	○	○	○	○	○
0010H	INTP4 (Pin edge detection)	○	○	○	○	○	○	○	○	○
	INTSPM (Stack pointer overflow / underflow)	○	○	○	○	○	○	○	○	○
0012H	INTP5 (Pin edge detection)	○	○	○	○	○	○	○	○	–
0014H	INTCLM (PLL clock stop detection)	○	○	○	○	○	○	○	○	○
0016H	INTST0/INTCSI00/INTIIC00 (SAU0 ch0)	○	○	○	○	○	○	○	○	○
0018H	INTSR0/INTCSI01/INTIIC01 (SAU0 ch1)	○	○	○	○	○	○	○	○	○
001AH	INTTRD0 (Timer RD0 interrupt)	○	○	○	○	○	○	○	○	○
001CH	INTTRD1 (Timer RD1 interrupt)	○	○	○	○	○	○	○	○	○
001EH	INTTRJ0 (Timer RJ0 interrupt)	○	○	○	○	○	○	○	○	○
0020H	INTRAM (RAM ECC detection)	○	○	○	○	○	○	○	○	○
0022H	INTCTSUWR (CTSU register write request)	○	○	○	–	–	–	–	–	–
	INTLIN0TRM (LIN0 transmission)	–	–	–	○	○	○	○	○	○
0024H	INTCTSURD (CTSU register read request)	○	○	○	–	–	–	–	–	–
	INTLIN0RVC (LIN0 reception)	–	–	–	○	○	○	○	○	○
0026H	INTCTSUFN (CTSU measurement end)	○	○	○	–	–	–	–	–	–
	INTLIN0STA/INTLIN0 (LIN0 interrupt)	–	–	–	○	○	○	○	○	○
0028H	INTIICA0 (Multimaster I2C interrupt)	○	○	○	○	○	○	○	–	–
002AH	INTP8 (Pin edge detection)	○	–	–	○	○	○	–	–	–
	INTRTC (RTC interrupt)	○	○	○	○	○	○	○	○	○
002CH	INTTM00 (TAU0 ch0 interrupt)	○	○	○	○	○	○	○	○	○
002EH	INTTM01 (TAU0 ch1 interrupt)	○	○	○	○	○	○	○	○	○
0030H	INTTM02 (TAU0 ch2 interrupt)	○	○	○	○	○	○	○	○	○
0032H	INTTM03 (TAU0 ch3 interrupt)	○	○	○	○	○	○	○	○	○
0034H	INTAD (A/D interrupt)	○	○	○	○	○	○	○	○	○
0036H	INTP6 (Pin edge detection)	○	–	–	○	○	○	–	–	–
	INTTM11H (TAU1 ch1 8-bit timer interrupt)	○	○	○	○	○	○	○	○	–
0038H	INTP7 (Pin edge detection)	○	–	–	○	○	○	–	–	–
	INTTM13H (TAU1 ch3 8-bit timer interrupt)	○	○	○	○	○	○	○	○	–
003AH	INTP9 (Pin edge detection)	○	–	–	○	○	○	–	–	–
	INTTM01H (TAU0 ch1 8-bit timer interrupt)	○	○	○	○	○	○	○	○	○
003CH	INTP10 (Pin edge detection)	–	–	–	○	○	–	–	–	–
	INTTM03H (TAU0 ch3 8-bit timer interrupt)	○	○	○	○	○	○	○	○	○
003EH	INTST1/INTCSI10/INTIIC10 (SAU1 ch0)	○	○	○	○	○	○	○	○	–
0040H	INTSR1/INTCSI11/INTIIC11 (SAU1 ch1)	○	○	○	○	○	○	○	○	–
0042H	INTTM04 (TAU0 ch4 interrupt)	○	○	○	○	○	○	○	○	○
0044H	INTTM05 (TAU0 ch5 interrupt)	○	○	○	○	○	○	○	○	○
	INTLIN0TRM (LIN0 transmission)	○	○	○	–	–	–	–	–	–
0046H	INTTM06 (TAU0 ch6 interrupt)	○	○	○	○	○	○	○	○	○
	INTLIN0RVC (LIN0 reception)	○	○	○	–	–	–	–	–	–
0048H	INTTM07 (TAU0 ch7 interrupt)	○	○	○	○	○	○	○	○	○
	INTLIN0STA/INTLIN0 (LIN0 interrupt)	○	○	○	–	–	–	–	–	–
004AH	INTP11 (Pin edge detection)	–	–	–	○	○	–	–	–	–
	INTLIN0WUP (LIN0 wakeup detection)	○	○	○	○	○	○	○	○	○

Table 13-1. Interrupt Functions of RL78/F22, Compared with RL78/F13 (LIN) (2/2)

Vector Address	Interrupt Factor	RL78/F22			RL78/F13 (LIN)					
		48 QFP	32 QFN	24 QFN	80 QFP	64 QFP	48 QFP	32 QFN	30 SSOP	20 SSOP
004CH	INTTM10 (TAU1 ch0 interrupt)	○	○	○	–	–	–	–	–	–
	INTKR (Key return edge detection)	–	–	–	○	○	○	○	○	○
004EH	INTTM11 (TAU1 ch1 interrupt)	○	○	○	–	–	–	–	–	–
0050H	INTTM12 (TAU1 ch2 interrupt)	○	○	○	–	–	–	–	–	–
0052H	INTTM13 (TAU1 ch3 interrupt)	○	○	○	–	–	–	–	–	–
0054H	Reserved	–	–	–	–	–	–	–	–	–
0056H	Reserved	–	–	–	–	–	–	–	–	–
0058H	INTADGB (A/D (group-B) interrupt)	○	○	○	–	–	–	–	–	–
005AH	INTROM (Code Flash ECC error detection)	○	○	○	–	–	–	–	–	–
	INTTM10 (TAU1 ch0 interrupt)	–	–	–	○	○	○	○	○	–
005CH	INTKR (Key return edge detection)	○	○	○	–	–	–	–	–	–
	INTTM11 (TAU1 ch1 interrupt)	–	–	–	○	○	○	○	○	–
005EH	INTTM12 (TAU1 ch2 interrupt)	–	–	–	○	○	○	○	○	–
0060H	INTTM13 (TAU1 ch3 interrupt)	–	–	–	○	○	○	○	○	–
0062H	Reserved	–	–	–	–	–	–	–	–	–
0064H	Reserved	–	–	–	–	–	–	–	–	–
0066H	Reserved	–	–	–	–	–	–	–	–	–
0068H	Reserved	–	–	–	–	–	–	–	–	–
006AH	Reserved	–	–	–	–	–	–	–	–	–
006CH	Reserved	–	–	–	–	–	–	–	–	–
006EH	Reserved	–	–	–	–	–	–	–	–	–
0070H	Reserved	–	–	–	–	–	–	–	–	–
0072H	Reserved	–	–	–	–	–	–	–	–	–
0074H	Reserved	–	–	–	–	–	–	–	–	–
0076H	Reserved	–	–	–	–	–	–	–	–	–
0078H	Reserved	–	–	–	–	–	–	–	–	–
007AH	Reserved	–	–	–	–	–	–	–	–	–
007CH	Reserved	–	–	–	–	–	–	–	–	–
007EH	BRK (BRK instruction interrupt)	○	○	○	○	○	○	○	○	○

Table 13-2. Interrupt Functions of RL78/F22, Compared with RL78/F12 (1/2)

Vector Address	Interrupt Factor	RL78/F22			RL78/F12				
		48 QFP	32 QFN	24 QFN	64 QFP	48 QFP	32 QFN	30 SSOP	20 SSOP
0000H	RESET/POR/LVD/WDT/TRAP/IAW/CLM	○	○	○	○	○	○	○	○
0002H	Reserved	–	–	–	–	–	–	–	–
0004H	INTWDTI (Watchdog timer interval)	○	○	○	○	○	○	○	○
0006H	INTLVI (Voltage detection)	○	○	○	○	○	○	○	○
0008H	INTP0 (Pin edge detection)	○	○	○	○	○	○	○	○
000AH	INTP1 (Pin edge detection)	○	○	–	○	○	○	○	○
000CH	INTP2 (Pin edge detection)	○	○	○	○	○	○	○	○
000EH	INTP3 (Pin edge detection)	○	○	○	○	○	○	○	–
0010H	INTP4 (Pin edge detection)	○	○	○	○	○	○	○	○
	INTSPM (Stack pointer overflow / underflow)	○	○	○	–	–	–	–	–
0012H	INTP5 (Pin edge detection)	○	○	○	○	○	○	○	○
0014H	INTCLM (PLL clock stop detection)	○	○	○	–	–	–	–	–
	INTST2/INTCSI20/INTIIC20 (SAU2 ch0)	–	–	–	○	○	○	○	–
0016H	INTST0/INTCSI00/INTIIC00 (SAU0 ch0)	○	○	○	–	–	–	–	–
	INTSR2/INTCSI21/INTIIC21 (SAU2 ch1)	–	–	–	○	○	○	○	–
0018H	INTSR0/INTCSI01/INTIIC01 (SAU0 ch1)	○	○	○	–	–	–	–	–
	INTSRE2 (UART2 receive error detection)	–	–	–	○	○	○	○	–
001AH	INTTRD0 (Timer RD0 interrupt)	○	○	○	–	–	–	–	–
	INTDMA0 (DMA0 transfer end)	–	–	–	○	○	○	○	○
001CH	INTTRD1 (Timer RD1 interrupt)	○	○	○	–	–	–	–	–
	INTDMA1 (DMA1 transfer end)	–	–	–	○	○	○	○	○
001EH	INTTRJ0 (Timer RJ0 interrupt)	○	○	○	–	–	–	–	–
	INTST0/INTCSI00/INTIIC00 (SAU0 ch0)	–	–	–	○	○	○	○	○
0020H	INTRAM (RAM ECC detection)	○	○	○	–	–	–	–	–
	INTSR0/INTCSI01/INTIIC01 (SAU0 ch1)	–	–	–	○	○	○	○	○
0022H	INTCTSUWR (CTSU register write request)	○	○	○	–	–	–	–	–
	INTSRE0 (UART0 receive error detection)	–	–	–	○	○	○	○	○
	INTTM01H (TAU0 ch1 8-bit timer interrupt)	–	–	–	○	○	○	○	○
0024H	INTCTSURD (CTSU register read request)	○	○	○	–	–	–	–	–
	INTST1/INTCSI10/INTIIC10 (SAU1 ch0)	–	–	–	○	○	○	○	–
0026H	INTCTSUFN (CTSU measurement end)	○	○	○	–	–	–	–	–
	INTSR1/INTCSI11/INTIIC11 (SAU1 ch1)	–	–	–	○	○	○	○	–
0028H	INTIICA0 (Multimaster I2C interrupt)	○	○	○	–	–	–	–	–
	INTSRE1 (UART1 receive error detection)	–	–	–	○	○	○	○	–
	INTTM03H (TAU0 ch3 8-bit timer interrupt)	–	–	–	○	○	○	○	○
002AH	INTP8 (Pin edge detection)	○	–	–	–	–	–	–	–
	INTRTC (RTC interrupt)	○	○	○	–	–	–	–	–
	INTIICA0 (Multimaster I2C interrupt)	–	–	–	○	○	○	○	–
002CH	INTTM00 (TAU0 ch0 interrupt)	○	○	○	○	○	○	○	○
002EH	INTTM01 (TAU0 ch1 interrupt)	○	○	○	○	○	○	○	○
0030H	INTTM02 (TAU0 ch2 interrupt)	○	○	○	○	○	○	○	○
0032H	INTTM03 (TAU0 ch3 interrupt)	○	○	○	○	○	○	○	○
0034H	INTAD (A/D interrupt)	○	○	○	○	○	○	○	○
0036H	INTP6 (Pin edge detection)	○	–	–	–	–	–	–	–
	INTTM11H (TAU1 ch1 8-bit timer interrupt)	○	○	○	–	–	–	–	–
	INTRTC (RTC interrupt)	–	–	–	○	○	○	○	○
0038H	INTP7 (Pin edge detection)	○	–	–	–	–	–	–	–
	INTTM13H (TAU1 ch3 8-bit timer interrupt)	○	○	○	–	–	–	–	–
	INTIT (Interval timer interrupt)	–	–	–	○	○	○	○	○
003AH	INTP9 (Pin edge detection)	○	–	–	–	–	–	–	–
	INTTM01H (TAU0 ch1 8-bit timer interrupt)	○	○	○	–	–	–	–	–
	INTKR (Key return function interrupt)	–	–	–	○	○	–	–	–
003CH	INTTM03H (TAU0 ch3 8-bit timer interrupt)	○	○	○	–	–	–	–	–
	INTCSIS0/INTSTS0 (SAUS ch0)	–	–	–	○	○	○	○	○
003EH	INTST1/INTCSI10/INTIIC10 (SAU1 ch0)	○	○	○	–	–	–	–	–
	INTCSIS1/INTSRS0 (SAUS ch1)	–	–	–	○	○	○	○	○
0040H	INTSR1/INTCSI11/INTIIC11 (SAU1 ch1)	○	○	○	–	–	–	–	–
	INTWUTM (Wakeup timer interrupt)	–	–	–	○	○	○	○	○

Table 13-2. Interrupt Functions of RL78/F22, Compared with RL78/F12 (2/2)

Vector Address	Interrupt Factor	RL78/F22			RL78/F13 (LIN)				
		48 QFP	32 QFN	24 QFN	64 QFP	48 QFP	32 QFN	30 SSOP	20 SSOP
0042H	INTTM04 (TAU0 ch4 interrupt)	○	○	○	○	○	○	○	○
0044H	INTTM05 (TAU0 ch5 interrupt)	○	○	○	○	○	○	○	○
	INTLIN0TRM (LIN0 transmission)	○	○	○	–	–	–	–	–
0046H	INTTM06 (TAU0 ch6 interrupt)	○	○	○	○	○	○	○	○
	INTLIN0RVC (LIN0 reception)	○	○	○	–	–	–	–	–
0048H	INTTM07 (TAU0 ch7 interrupt)	○	○	○	○	○	○	○	○
	INTLIN0STA/INTLIN0 (LIN0 interrupt)	○	○	○	–	–	–	–	–
004AH	INTLIN0WUP (LIN0 wakeup detection)	○	○	○	–	–	–	–	–
	INTP6 (Pin edge detection)	–	–	–	○	○	–	–	–
004CH	INTTM10 (TAU1 ch0 interrupt)	○	○	○	–	–	–	–	–
	INTP7 (Pin edge detection)	–	–	–	○	–	–	–	–
	INTLT (LIN-UART transmission)	–	–	–	○	○	○	○	○
004EH	INTTM11 (TAU1 ch1 interrupt)	○	○	○	–	–	–	–	–
	INTP8 (Pin edge detection)	–	–	–	○	○	–	–	–
	INTLR (LIN-UART reception)	–	–	–	○	○	○	○	○
0050H	INTTM12 (TAU1 ch2 interrupt)	○	○	○	–	–	–	–	–
	INTP9 (Pin edge detection)	–	–	–	○	○	–	–	–
	INTLS (LIN-UART status interrupt)	–	–	–	○	○	○	○	○
0052H	INTTM13 (TAU1 ch3 interrupt)	○	○	○	–	–	–	–	–
	INTP10 (Pin edge detection)	–	–	–	○	–	–	–	–
	INTSRES0 (UARTS0 error detection)	–	–	–	○	○	○	○	○
0054H	INTP11 (Pin edge detection)	–	–	–	○	–	–	–	–
0056H	Reserved	–	–	–	–	–	–	–	–
0058H	INTADGB (A/D (group-B) interrupt)	○	○	○	–	–	–	–	–
005AH	INTROM (Code Flash ECC error detection)	○	○	○	–	–	–	–	–
005CH	INTKR (Key return edge detection)	○	○	○	–	–	–	–	–
005EH	INTMD (Division operation end)	–	–	–	○	○	○	○	○
0060H	Reserved	–	–	–	–	–	–	–	–
0062H	INTFL (Flash sequencer operation end)	–	–	–	○	○	○	○	○
0064H	Reserved	–	–	–	–	–	–	–	–
0066H	Reserved	–	–	–	–	–	–	–	–
0068H	Reserved	–	–	–	–	–	–	–	–
006AH	Reserved	–	–	–	–	–	–	–	–
006CH	Reserved	–	–	–	–	–	–	–	–
006EH	Reserved	–	–	–	–	–	–	–	–
0070H	Reserved	–	–	–	–	–	–	–	–
0072H	Reserved	–	–	–	–	–	–	–	–
0074H	Reserved	–	–	–	–	–	–	–	–
0076H	Reserved	–	–	–	–	–	–	–	–
0078H	Reserved	–	–	–	–	–	–	–	–
007AH	Reserved	–	–	–	–	–	–	–	–
007CH	Reserved	–	–	–	–	–	–	–	–
007EH	BRK (BRK instruction interrupt)	○	○	○	○	○	○	○	○

In RL78/F22 product, multiple interrupt factors are assigned to one vector table. The following table shows the methods for determining the interrupt factors.

Table 13-3. Interrupt Determination Method for RL78/F22 Product

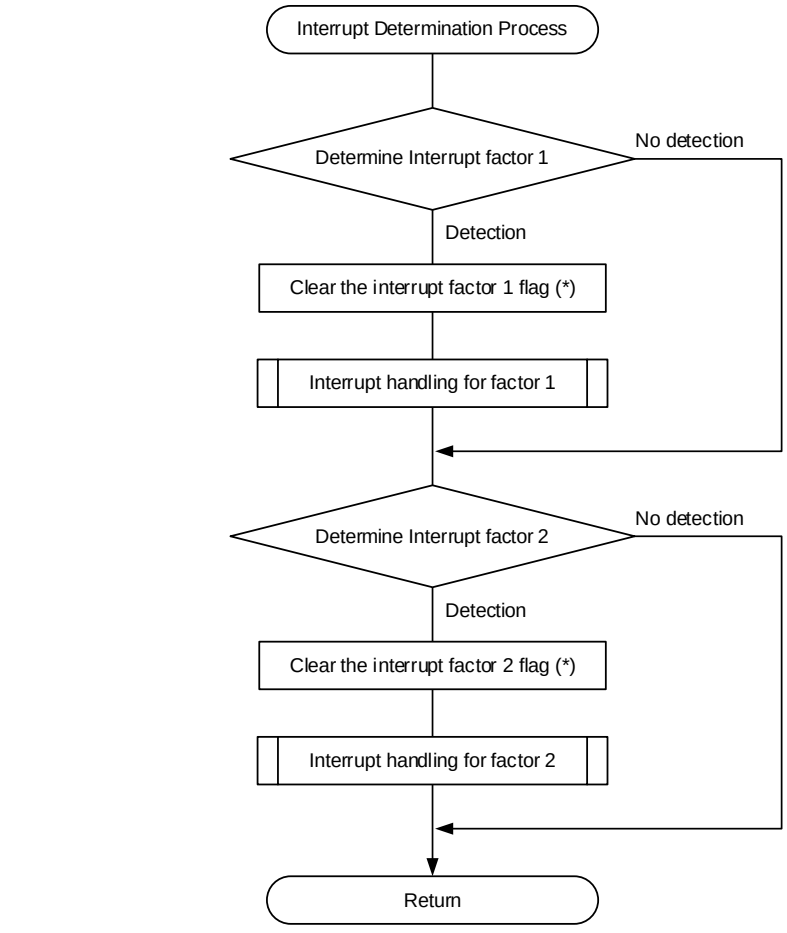
Vector Address	Interrupt Factor	Interrupt Determination Method
0010H	INTP4 (Pin edge detection)	INTFLG0.INTFLG00 bit
	INTSPM (Stack pointer monitor overflow/ underflow detection)	The SP is read by software and judged.
002AH	INTP8 (Pin edge detection)	INTFLG0.INTFLG2 bit
	INTRTC (Real-time clock interrupt)	RTCC1.[WAFG, RIFG] bit
0036H	INTP6 (Pin edge detection)	If used simultaneously, it is impossible to judge.
	INTTM11H (TAU1 CH1 8-bit timer interrupt)	
0038H	INTP7 (Pin edge detection)	If used simultaneously, it is impossible to judge.
	INTTM13H (TAU1 CH3 8-bit timer interrupt)	
003AH	INTP9 (Pin edge detection)	If used simultaneously, it is impossible to judge.
	INTTM01H (TAU0 CH1 8-bit timer interrupt)	
0044H	INTTM05 (TAU0 CH5 interrupt)	INTFLG1.INTFLG15 bit
	INTLIN0TRM (LIN0 transmission)	(Note 1)
0046H	INTTM06 (TAU0 CH6 interrupt)	INTFLG1.INTFLG16 bit
	INTLIN0RVC (LIN0 reception)	(Note 2)
0048H	INTTM07 (TAU0 CH7 interrupt)	INTFLG1.INTFLG17 bit
	INTLIN0STA/INTLIN0 (LIN0 interrupt)	(Note 3)
004AH	INTP11 (Pin edge detection)	Select INTP11 or INTLIN0WUP in ISC.ISC2 bit.
	INTLIN0WUP (LIN0 wakeup detection)	

Notes 1, 2, 3 Varies depending on the operation mode of RLIN3 module. See Table 13-4 for details.

Table 13-4. Interrupt Determination Method of RL78/F22 RLIN3 Module

	LIN Master mode	LIN Slave mode	UART mode
(Note 1) INTLIN0TRM	Header transmission (LST0.HTRC) Frame transmission (LST0.FTC) Wakeup signal transmission (LST0.FTC)	Header transmission (LST0.HTRC) Wakeup signal transmission (LST0.FTC)	Transmission start (LST0.UTS) Transmission end (LST0.FTC)
(Note 2) INTLIN0RVC	Frame reception (LST0.FRC) Wakeup signal reception (LST0.FRC)	Header reception (LST0.HTRC) Response reception (LST0.FRC) Wakeup signal reception (LST0.FRC)	Reception end (LST0.URS) Expansion bit mismatch (LEST0.EXBT)
(Note 3) INTLIN0STA	Error detection (LST0.ERR)	Error detection (LST0.ERR)	Error detection (LST0.FTC)
(Note 3) INTLIN0	Header transmission (LST0.HTRC) Frame transmission (LST0.FTC) Frame reception (LST0.FRC) Wakeup signal transmission (LST0.FTC) Wakeup signal reception (LST0.FRC) Error detection (LST0.ERR)	Header reception (LST0.HTRC) Header transmission (LST0.HTRC) Response reception (LST0.FRC) Wakeup signal transmission (LST0.FTC) Wakeup signal reception (LST0.FRC) Error detection (LST0.ERR)	Not available

The figure below shows the process when using interrupts with multiple interrupt sources assigned to a single interrupt vector table.



(*) Clear the target interrupt factor flag. When processing an RLIN3 error status interrupt, be sure to also clear the flags (flag in the LEST0 register) that are subject to error detection.

Figure 13-1. Interrupt Determination Process for RL78/F22 product

Key Points for Porting:

- **Difference in interrupt functions**

  RL78/F22 product add some sources from RL78/F12, F13 (LIN) products. With the addition of these functions, the related registers (IFxx, MKxx, and PRxx) have also been expanded. When using the additional interrupt, set the interrupt vector and the register related to that interrupt. In addition, when using multiple interrupt functions that share an interrupt vector at the same time, it is necessary to identify the cause of the interrupt that occurred.

14. Standby Control

The table below shows the differences between RL78/F22 and RL78/F12, F13 (LIN) products standby control.

Table 14-1. Stand-by Functions of RL78/F22, Compared with RL78/F12, F13

Item	RL78/F22	RL78/F13 (LIN)	RL78/F12
HALT mode	Yes	Yes	Yes
STOP mode	Yes	Yes	Yes
SNOOZE mode	Yes	Yes	Yes
LIN/UART module (RLIN3)	Yes	Yes	No
CSI00/UART0 (SAU0)	**No**	No	Yes
A/D converter	**No**	Yes	Yes
DTC	Yes	Yes	Yes
CTSU2SLa (Touch detection)	**Yes**	No	No

RL78/F22 product does not support A/D converter in SNOOZE mode. However, the same measures are possible as shown in the figure below.

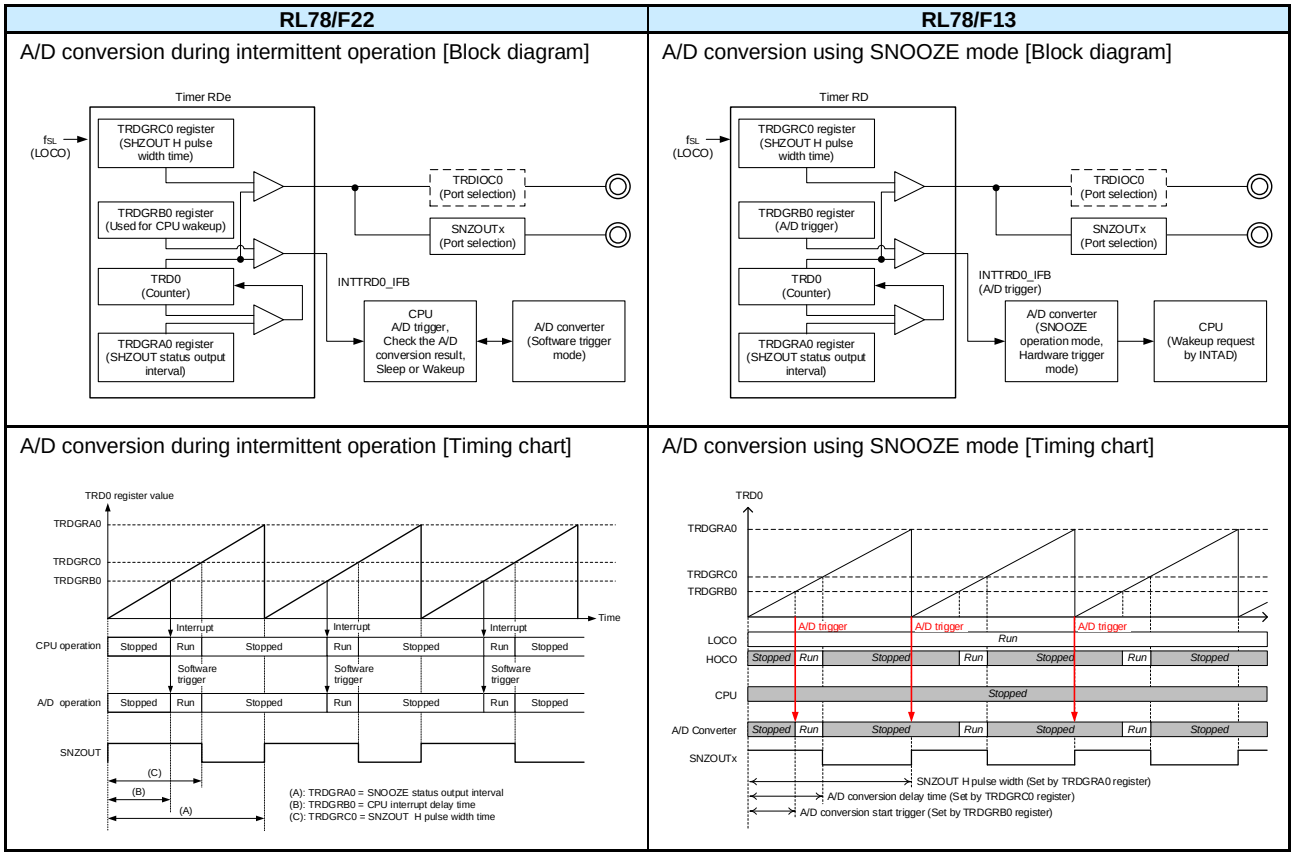


Figure 14-1. A/D Conversion Using SNOOZE Mode for RL78/F22 Product

Key Points for Porting:

- **A/D conversion in SNOOZE mode**

  RL78/F22 product does not support A/D conversion in the SNOOZE mode. Refer to the figure shown above when performing the same process as A/D conversion in SNOOZE mode on RL78/F13 product.

15. Flash Memory

RL78/F22 product has Code Flash Memory ECC Function (1-bit correction/2-bit error detection).
RL78/F12, F13 products used FSL (Flash Self Library) and FDL, EEL (Data Flash Library) to rewrite Flash Memory (Code/ Data Flash), but RL78/F22 product uses user software. The flash memory control software (RFD: Renesas Flash Drivers) will be provided in the same way as conventional products.

Key Points for Porting:

- **Code flash memory ECC function**

  With this function, if CPU reads the erased area after erasing the code flash memory, it will not become FFH. We recommend writing the free area with "FFH" to prevent abnormal operations such as CPU runaway. If the CPU fetches FFH, it will cause an internal reset due to illegal instruction execution.

- **Flash memory rewriting**

  The flash memory control software (RFD: Renesas Flash Drivers) is provided as source code. It is the customer's responsibility to ensure functional safety of flash memory rewriting software.

- **Security ID area**

  In “On-chip debug security ID area (000C6H to 000D5H)” and “Flash serial programing security ID area (000D6H to 000E5H)”, if IDRDEN bit in Security option byte is 0, all bits will be read as 0 when read by the CPU. Be careful when performing checksum calculation on the CPU.

16. Development Environment

The table below shows the differences between RL78/F22 and RL78/F12, F13 products software development environment.

Table 16-1. Software Development Environment of RL78/F22, Compared with RL78/F12, F13

Item	RL78/F22	RL78/F12, F13
Integrated Development Environment / Compiler	CS+, e^2 studio / CC-RL	CS+, e^2 studio / CC-RL, CA78K0R
	Embedded Workbench / IAR Compiler	Embedded Workbench / IAR Compiler
Emulator	E2, E2 Lite	IECUBE E1, E2, E2 Lite

17. Electrical Specifications

Comparisons of the electrical characteristics of RL78/F22 and RL78/F12, F13 are shown below. For details, refer to the user's manual for the target product.

17.1 Supply Current Characteristics

Shown below is a comparison of supply current consumptions in each operation mode between RL78/F22 and RL78/F12, F13 products. RL78/F22 and RL78/F12, F13 products in the table below indicate the maximum number of channels available for the product.

Table 17-1. Supply Current Characteristics of RL78/F22, Compared with RL78/F13

Mode	RL78/F22		RL78/F13 (LIN)	
	Conditions	Supply Current Specifications	Conditions	Supply Current Specifications
Operation Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 5.6 mA, (MAX.) 11.0 mA Grade-4: (TYP.) 5.6 mA, (MAX.) 11.0 mA	f_{CLK} = 32 MHz, f_{PLL} = 64 MHz, f_{MX} = 8 MHz	L-grade: (TYP.) 6.4 mA, (MAX.) 14.0 mA
			f_{CLK} = 24 MHz, f_{PLL} = 48 MHz, f_{MX} = 8 MHz	K-grade: (TYP.) 5.0 mA, (MAX.) 12.0 mA Y-grade: (TYP.) 5.0 mA, (MAX.) 12.5 mA
HALT Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 1.8 mA, (MAX.) 6.5 mA Grade-4: (TYP.) 1.8 mA, (MAX.) 6.5 mA	f_{CLK} = 32 MHz, f_{PLL} = 64 MHz, f_{MX} = 8 MHz	L-grade: (TYP.) 1.1 mA, (MAX.) 10.0 mA
			f_{CLK} = 24 MHz, f_{PLL} = 48 MHz, f_{MX} = 8 MHz	K-grade: (TYP.) 0.9 mA, (MAX.) 8.0 mA Y-grade: (TYP.) 0.9 mA, (MAX.) 8.5 mA
STOP Mode	–	Grade-3: (TYP.) 0.5 µA, (MAX.) 75.0 µA Grade-4: (TYP.) 0.5 µA, (MAX.) 175.0 µA	–	L-grade: (TYP.) 0.5 µA, (MAX.) 30.0 µA K-grade: (TYP.) 0.5 µA, (MAX.) 60.0 µA Y-grade: (TYP.) 0.5 µA, (MAX.) 150.0 µA

Table 17-2. Supply Current Characteristics of RL78/F22, Compared with RL78/F12

Mode	RL78/F22		RL78/F12	
	Conditions	Supply Current Specifications	Conditions	Supply Current Specifications
Operation Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 5.6 mA, (MAX.) 11.0 mA Grade-4: (TYP.) 5.6 mA, (MAX.) 11.0 mA	f_{CLK} = 32 MHz, f_{IH} = 32 MHz	J-grade: (TYP.) 5.6 mA, (MAX.) 8.2 mA
			f_{CLK} = 24 MHz, f_{IH} = 24 MHz	K-grade: (TYP.) 4.5 mA, (MAX.) 6.9 mA
HALT Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 1.8 mA, (MAX.) 6.5 mA Grade-4: (TYP.) 1.8 mA, (MAX.) 6.5 mA	f_{CLK} = 32 MHz, f_{IH} = 32 MHz	J-grade: (TYP.) 0.55 mA, (MAX.) 3.2 mA
			f_{CLK} = 24 MHz, f_{IH} = 24 MHz	K-grade: (TYP.) 0.48 mA, (MAX.) 5.58 mA
STOP Mode	–	Grade-3: (TYP.) 0.5 µA, (MAX.) 75.0 µA Grade-4: (TYP.) 0.5 µA, (MAX.) 175.0 µA	–	J-grade: (TYP.) 0.22 µA, (MAX.) 4.16 µA K-grade: (TYP.) 0.22 µA, (MAX.) 35.0 µA

Table 17-3. Operation Current Characteristics of RL78/F22, Compared with RL78/F12, F13

Mode	RL78/F22		RL78/F12, F13	
	Conditions	Supply Current Specifications	Conditions	Supply Current Specifications
Watchdog timer	f_{WDT} = 15 kHz	Grade-3, Grade-4: (TYP.) 0.3 µA	f_{WDT} = 15 kHz	L-grade, K-grade: (TYP.) 0.22 µA
A/D converter	During conversion	Grade-3, Grade-4: (TYP.) 1.3 mA, (MAX.) 1.6 mA	During conversion	L-grade, K-grade: (TYP.) 1.3 mA, (MAX.) 1.7 mA
	Added current Sample-and-hold circuit operation	Grade-3, Grade-4: (TYP.) 0.8 mA, (MAX.) 1.2 mA	–	–
LVD operation	–	Grade-3, Grade-4: (TYP.) 0.045 µA	–	L-grade, K-grade: (TYP.) 0.08 µA
BGO operation	–	Grade-3, Grade-4: (TYP.) 2.5 mA, (MAX.) 12.2 mA	–	L-grade, K-grade: (TYP.) 2.5 mA, (MAX.) 12.2 mA

Key Points for Porting:

- **Supply current characteristics**

  Please design the power supply of the target system according to the current specifications of the product to be used.

17.2 Pin Current Characteristics

Below is a comparison of pin current characteristics in each parameter of RL78/F22 and RL78/F12, F13.

Table 17-4. Pin Current Characteristics of RL78/F22, Compared with RL78/F13

Mode	RL78/F22		RL78/F13 (LIN)	
	Conditions	Pin Current Specifications	Conditions	Pin Current Specifications
Pin output current: High (IOH1)	4.0V ≤ EV_{DD} ≤ 5.5V	Grade-3: (MAX.) -5.0 mA / pin (MAX.) -50.0 mA / total of pins Grade-4: (MAX.) -5.0 mA / pin (MAX.) -42.0 mA / total of pins	4.0V ≤ EV_{DD} ≤ 5.5V	L-grade: (MAX.) -5.0 mA / pin (MAX.) -50.0 mA / total of pins K-grade: (MAX.) -5.0 mA / pin (MAX.) -42.0 mA / total of pins Y-grade: (MAX.) -5.0 mA / pin (MAX.) -32.0 mA / total of pins
	2.7V ≤ EV_{DD} < 4.0V	Grade-3, Grade-4: (MAX.) -3.0 mA / pin (MAX.) -29.0 mA / total of pins	2.7V ≤ EV_{DD} < 4.0V	L-grade, K-grade, Y-grade: (MAX.) -3.0 mA / pin (MAX.) -29.0 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) -0.5 mA / pin (MAX.) -15.0 mA / total of pins	–	–
Pin output current: Low (IOL1)	4.0V ≤ EV_{DD} ≤ 5.5V	Grade-3, Grade-4: (MAX.) 8.5 mA / pin (MAX.) 65.0 mA / total of pins	4.0V ≤ EV_{DD} ≤ 5.5V	L-grade, K-grade: (MAX.) 8.5 mA / pin (MAX.) 65.0 mA / total of pins Y-grade: (MAX.) 8.5 mA / pin (MAX.) 55.0 mA / total of pins
	2.7V ≤ EV_{DD} < 4.0V	Grade-3, Grade-4: (MAX.) 4.0 mA / pin (MAX.) 50.0 mA / total of pins	2.7V ≤ EV_{DD} < 4.0V	L-grade, K-grade: (MAX.) 4.0 mA / pin (MAX.) 50.0 mA / total of pins Y-grade: (MAX.) 4.0 mA / pin (MAX.) 45.0 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) 0.6 mA / pin (MAX.) 29.0 mA / total of pins	–	–
Pin output current: High (IOH2)	2.7V ≤ V_{DD} ≤ 5.5V	Grade-3, Grade-4: (MAX.) -0.1 mA / pin (MAX.) -2.0 mA / total of pins	2.7V ≤ V_{DD} ≤ 5.5V	L-grade, K-grade, Y-grade: (MAX.) -0.1 mA / pin (MAX.) -2.0 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) -0.1 mA / pin (MAX.) -2.0 mA / total of pins	–	–
Pin output current: Low (IOL2)	2.7V ≤ V_{DD} ≤ 5.5V	Grade-3, Grade-4: (MAX.) 0.4 mA / pin (MAX.) 5.0 mA / total of pins	2.7V ≤ V_{DD} ≤ 5.5V	L-grade, K-grade, Y-grade: (MAX.) 0.4 mA / pin (MAX.) 5.0 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) 0.4 mA / pin (MAX.) 5.0 mA / total of pins	–	–

Table 17-5. Pin Current Characteristics of RL78/F22, Compared with RL78/F12

Mode	RL78/F22		RL78/F12	
	Conditions	Pin Current Specifications	Conditions	Pin Current Specifications
Pin output current: High (IOH1)	4.0V ≤ EV_{DD} ≤ 5.5V	Grade-3: (MAX.) -5.0 mA / pin (MAX.) -50.0 mA / total of pins Grade-4: (MAX.) -5.0 mA / pin (MAX.) -42.0 mA / total of pins	4.0V ≤ EV_{DD} ≤ 5.5V	J-grade: (MAX.) -5.0 mA / pin (MAX.) -50.0 mA / total of pins K-grade: (MAX.) -5.0 mA / pin (MAX.) -42.0 mA / total of pins
	2.7V ≤ EV_{DD} < 4.0V	Grade-3, Grade-4: (MAX.) -3.0 mA / pin (MAX.) -29.0 mA / total of pins	2.7V ≤ EV_{DD} < 4.0V	J-grade, K-grade: (MAX.) -3.0 mA / pin (MAX.) -29.0 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) -0.5 mA / pin (MAX.) -15.0 mA / total of pins	1.8V ≤ EV_{DD} < 2.7V	J-grade: (MAX.) -0.5 mA / pin (MAX.) -15.0 mA / total of pins
Pin output current: Low (IOL1)	4.0V ≤ EV_{DD} ≤ 5.5V	Grade-3, Grade-4: (MAX.) 8.5 mA / pin (MAX.) 65.0 mA / total of pins	4.0V ≤ EV_{DD} ≤ 5.5V	J-grade, K-grade: (MAX.) 8.5 mA / pin (MAX.) 65.0 mA / total of pins
	2.7V ≤ EV_{DD} < 4.0V	Grade-3, Grade-4: (MAX.) 4.0 mA / pin (MAX.) 50.0 mA / total of pins	2.7V ≤ EV_{DD} < 4.0V	J-grade, K-grade: (MAX.) 4.0 mA / pin (MAX.) 50.0 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) 0.6 mA / pin (MAX.) 29.0 mA / total of pins	1.8V ≤ EV_{DD} < 2.7V	J-grade: (MAX.) 0.6 mA / pin (MAX.) 29.0 mA / total of pins
Pin output current: High (IOH2)	2.7V ≤ V_{DD} ≤ 5.5V	Grade-3, Grade-4: (MAX.) -0.1 mA / pin (MAX.) -2.0 mA / total of pins	2.7V ≤ V_{DD} ≤ 5.5V	J-grade, K-grade: (MAX.) -0.1 mA / pin (MAX.) -0.8 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) -0.1 mA / pin (MAX.) -2.0 mA / total of pins	1.8V ≤ EV_{DD} < 2.7V	J-grade: (MAX.) -0.1 mA / pin (MAX.) -0.8 mA / total of pins
Pin output current: Low (IOL2)	2.7V ≤ V_{DD} ≤ 5.5V	Grade-3, Grade-4: (MAX.) 0.4 mA / pin (MAX.) 5.0 mA / total of pins	2.7V ≤ V_{DD} ≤ 5.5V	J-grade, K-grade: (MAX.) 0.4 mA / pin (MAX.) 3.2 mA / total of pins
	1.8V ≤ EV_{DD} < 2.7V	Grade-3: (MAX.) 0.4 mA / pin (MAX.) 5.0 mA / total of pins	1.8V ≤ EV_{DD} < 2.7V	J-grade: (MAX.) 0.4 mA / pin (MAX.) 3.2 mA / total of pins

Key Points for Porting:

- **Pin current characteristics**

  Pin specifications vary depending on the pin block of the product. Please refer to the user's manual for details.

18. Appendix

18.1 RL78/F22 SFR (Special Function Register) Comparison

The SFR (Special Function Register) list for RL78/F22 product is shown below. Port-related registers, etc. vary depending on the product used. Please refer to the product manual for details.

Table 18-1. SFR List for RL78/F22 Product (1/5)

Address	Register							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
FFF00H	P0	P1	–	P3	P4	–	P6	P7
FFF08H	P8	P9	–	–	P12	P13	P14	–
FFF10H	SDR00		SDR01		–	–	–	–
FFF18H	TDR00		TDR01		–	–	–	–
FFF20H	PM0	PM1	–	PM3	PM4	–	PM6	PM7
FFF28H	PM8	PM9	–	–	PM12	–	PM14	–
FFF30H	ADWINR	–	AAUWINR	–	–	–	–	KRM
FFF38H	EGP0	EGN0	EGP1	EGN1	–	–	–	–
FFF40H	–	–	–	–	–	–	–	–
FFF48H	SDR10		SDR11		–	–	–	–
FFF50H	IICA0	IICS0	IICF0	–	SUBCUDW		–	–
FFF58H	TRDGRC0		TRDGRD0		TRDGRC1		TRDGRD1	
FFF60H	TRDCMPD0		TRDCMPC1		TRDCMPD1		TRDADTB0	
FFF68H	TRDADTB1		TRDRDT0	TRDRDT1	TRDDNR0	TRDGPR0	TRDDNR1	TRDGPR1
FFF70H	–	–	–	–	TDR02		TDR03	
FFF78H	TDR04		TDR05		TDR06		TDR07	
FFF80H	TDR10		TDR11		TDR12		TDR13	
FFF88H	–	–	–	–	–	–	–	–
FFF90H	–	–	SEC	MIN	HOUR	WEEK	DAY	MONTH
FFF98H	YEAR	SUBCUD	ALARMWM	ALARMWH	ALARMWW	RTCC0	RTCC1	–
FFFA0H	CMC	CSC	OSTC	OSTS	CKC	CKS0	–	–
FFFA8H	RESF	LVIM	LVIS	WDTE	CRCIN	–	–	–
FFFB0H	FLSEC		FLFSWS		FLFSWE		FSSET	FSSE
FFFB8H	–	–	–	–	–	–	–	–
FFFC0H	PFCMD	PFS	–	–	–	–	FLWE	–
FFFC8H	–	–	–	–	–	–	–	–
FFFD0H	IF2L	IF2H	–	–	MK2L	MK2H	–	–
FFFD8H	PR02L	PR02H	–	–	PR12L	PR12H	–	–
FFFE0H	IF0L	IF0H	IF1L	IF1H	MK0L	MK0H	MK1L	MK1H
FFFE8H	PR00L	PR00H	PR01L	PR01H	PR10L	PR10H	PR11L	PR11H
FFFF0H	MACRL		MACRH		–	–	–	–
FFFF8H	–	–	–	–	–	–	PMC	–

- P3, PM3: Delete the functions corresponding to P33 and P34.
- ADWINR: Access window selection for A/D converter related register.
- AAUWINR: Access window selection for AAU (Application Accelerator Unit) related register.
- FFF60H to FFF6FH: Added Timer RDe related registers.
- LVIM/LVIS: Set the detection level for LVD1 circuit.
- FFFB0H to FFFC6H: Added Flash memory control registers.
- IF2L (FFFD0H) to PR11H (FFFEFH): Change the interrupt-related flag to match the product specifications.

Table 18-1. SFR List for RL78/F22 Product (2/5)

Address	Register							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F0000H	–	–	–	–	–	–	–	–
F0008H	–	–	–	–	–	–	–	–
F0010H	–	–	–	–	–	–	PIOR0	PIOR1
F0018H	–	PIOR3	PIOR4	PIOR5	–	PIOR7	–	PIOR9
F0020H	–	PITHL1	–	PITHL3	PITHL4	–	PITHL6	PITHL7
F0028H	–	–	–	–	PITHL12	–	–	–
F0030H	PU0	PU1	–	PU3	PU4	–	PU6	PU7
F0038H	–	–	–	–	PU12	–	PU14	–
F0040H	–	PIM1	–	PIM3	–	–	PIM6	PIM7
F0048H	–	–	–	–	PIM12	–	–	–
F0050H	–	POM1	–	POM3	–	–	POM6	POM7
F0058H	–	–	–	–	POM12	–	–	–
F0060H	–	–	–	–	–	–	–	PMC7
F0068H	PMC8	PMC9	–	–	PMC12	–	–	–
F0070H	NFEN0	NFEN1	NFEN2	ISC	TIS0	TIS1	RAMSAR	PMS
F0078H	IAWCTL	INTFLG0	–	–	INTMSK	INTFLG1	–	–
F0080H	–	–	–	–	–	–	–	–
F0088H	–	–	–	–	–	–	–	–
F0090H	DFLCTL	–	–	–	–	–	–	–
F0098H	CFERRCTLR	CFERRSTR	–	–	ERRADRL		ERRADRH	–
F00A0H	HIOTRM	–	–	–	–	–	–	–
F00A8H	HOCODIV	–	–	–	–	–	–	–
F00B0H	–	–	–	–	–	–	–	–
F00B8H	CTSUTRIM0		CTSUTRIM1		CTSUTRIM2		CTSUTRIM3	
F00C0H	FLPMC	FLARS	FLAPL		FLAPH	FSSQ	FLSEDL	
F00C8H	FLSEDH	FLRST	FSASTL	FSASTH	FLWL		FLWH	
F00D0H	–	–	–	–	–	–	–	–
F00D8H	SPMCTRL	–	SPOFR		SPUFR		–	–
F00E0H	–	–	–	–	–	–	–	–
F00E8H	–	–	–	–	–	–	–	–
F00F0H	–	–	–	OSMC	–	–	–	–
F00F8H	–	PSMCR	LVDFCLR	–	–	–	BCDADJ	–

- PIOR9: Added pin assignment register for peripheral functions.
- PMC8, PMC9: Added analog/digital port selection register. (ADPC register has been deleted.)
- RAMSAR: Added RAM start addresses setting register.
- IAWCTL: The TSPMCm register has been added to the target registers for the GPORT bit, and the PSMCR register has been added to the target registers for the GCSC bit.
- INTFLG1: Added TAU0 interrupt determination flag.
- F0098H to F009EH: Added code flash memory ECC related register.
- HOCODIV: The specifications of HOCO frequency selection bit have been changed to match RL78/F22 product.
- CTSUTRIM0/1/2/3: Added capacitive sensing unit (CTSU2SLa) related register.
- F00C0H to F00CFH: Added Flash memory control registers.
- PSMCR: Added RAM shut down mode related register.
- LVDFCLR: Added LVD detection flag clear register.

Table 18-1. SFR List for RL78/F22 Product (3/5)

Address	Register							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F0100H	SSR00/SSR10		SSR01/SSR11		SIR00/SIR10		SIR01/SIR11	
F0108H	SMR00/SMR10		SMR01/SMR11		SCR00/SCR10		SCR01/SCR11	
F0110H	SE0/SE1		SS0/SS1		ST0/ST1		SPS0/SPS1	
F0118H	SO0/SO1		SOE0/SOE1		–	–	–	–
F0120H	SOL0/SOL1		SSE0/SSE1		–	–	–	–
F0128H	–	–	–	–	–	–	–	–
F0130H	–	–	–	–	–	–	–	–
F0138H	–	–	–	–	–	–	–	–
F0140H	TCR00/TCR10		TCR01/TCR11		TCR02/TCR12		TCR03/TCR13	
F0148H	TCR04		TCR05		TCR06		TCR07	
F0150H	TMR00/TMR10		TMR01/TMR11		TMR02/TMR12		TMR03/TMR13	
F0158H	TMR04		TMR05		TMR06		TMR07	
F0160H	TSR00/TSR10		TSR01/TSR11		TSR02/TSR12		TSR03/TSR13	
F0168H	TSR04		TSR05		TSR06		TSR07	
F0170H	TE0/TE1		TS0/TS1		TT0/TT1		TPS0/TPS1	
F0178H	TO0/TO1		TOE0/TOE1		TOL0/TOL1		TOM0/TOM1	
F0180H	CTSUCRAL		CTSUCRAH		CTSUCRBL		CTSUCRBH	
F0188H	CTSUMCHL		CTSUMCHH		CTSUCHACAL		CTSUCHACAH	
F0190H	–	–	–	–	CTSUCHTRCAL		CTSUCHTRCAH	
F0198H	–	–	–	–	CTSUSRL		–	–
F01A0H	CTSUSO0		CTSUSO1		CTSUSC		CTSUUC	
F01A8H	CTSUDBGR0		CTSUDBGR1		CTSUSUCLK0		CTSUSUCLK1	
F01B0H	CTSUSUCLK2		CTSUSUCLK3		–	–	–	–
F01B8H	–	–	–	–	–	–	–	–
F01C0H	CTSUOPTL		CTSUOPTH		CTSUSCTACTL		CTSUSCTACTH	
F01C8H	–	–	–	–	CTSUMCACT1L		CTSUMCACT1H	
F01D0H	CTSUMCACT2L		CTSUMCACT2H		CTSUMCACT3L		CTSUMCACT3H	
F01D8H	CTSUAJCRL		CTSUAJCRH		CTSUAJTHRL		CTSUAJTHRH	
F01E0H	CTSUAJMMARL		CTSUAJMMARH		CTSUAJBLACL		CTSUAJBLACH	
F01E8H	CTSUAJBLARL		CTSUAJBLARH		CTSUAJRRL		–	–
F01F0H	UTSEL	–	–	–	–	–	I2SER	–
F01F8H	CTSUTRG	–	–	–	–	–	–	–

- F0100H to F0123H: The SAU0/SAU1 related register is selected by UTSEL register.
- F0140H to F017FH: The TAU0/TAU1 related register is selected by UTSEL register.
- F0180H to F01EDH: Added capacitive sensing unit (CTSU2SLa) related register.
- UTSEL: Added register to select access to SAU0 or SAU1, and TAU0 or TAU1.
- I2SER: Added simplified-I^2S enable register.
- CTSUTRG: Added external trigger selection for capacitive sensing unit (CTSU2SLa).

Table 18-1. SFR List for RL78/F22 Product (4/5)

Address	Register							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F0200H	ERADR		ECCIER	ECCER	ECCTPR	ECCTMDR	ECCDWRVR	
F0208H	–	–	–	–	–	–	–	–
F0210H	–	TSPMC1	–	–	–	–	TSPMC6	TSPMC7
F0218H	–	–	–	–	–	–	–	–
F0220H	PSRSEL	–	PSNZCNT0	PSNZCNT1	PSNZCNT2	PSNZCNT3	–	–
F0228H	PWMDLY0		PWMDLY1		PWMDLY2		–	–
F0230H	IICCTL00	IICCTL01	IICWL0	IICWH0	SVA0	–	–	–
F0238H	–	–	–	–	–	–	–	–
F0240H	TRJCR0	TRJIOC0	TRJMR0	TRJISR0	–	–	–	–
F0248H	OPCTL0	OPDF0	OPDF1	OPEDGE	OPSR	–	TRDMBKCTL	TRDMBKCMP
F0250H	–	–	–	TRDSTR	TRDMR	TRDPMR	TRDFCR	TRDOER1
F0258H	TRDOER2	TRDOCR	TRDDF0	TRDDF1	–	–	–	–
F0260H	TRDCR0	TRDIORA0	TRDIORC0	TRDSR0	TRDIER0	TRDPOCR0	TRD0	
F0268H	TRDGRA0		TRDGRB0		–	–	–	–
F0270H	TRDCR1	TRDIORA1	TRDIORC1	TRDSR1	TRDIER1	TRDPOCR1	TRD1	
F0278H	TRDGRA1		TRDGRB1		–	–	–	–
F0280H	TRDCMPB0		–	–	TRDCMPA1		–	–
F0288H	TRDCMPB1		–	–	TRDADTC0		–	–
F0290H	TRDADTC1		–	–	–	–	TRDRSF0	TRDRSF1
F0298H	TRDADCR	–	TRDEMR0	TRDEMR1	–	–	–	–
F02A0H	–	–	–	–	–	–	–	–
F02A8H	–	–	–	–	–	–	–	–
F02B0H	AAU window registers							
F02B8H								
F02C0H	PER0	PER1	PER2	–	LINCKSEL	RTCCL	STPSTC	ADCKS
F02C8H	PLLCTL	PLLSTS	CKSEL	MDIV	POCRES	–	CLMTES	–
F02D0H	HDTCCR0	–	HDTCCT0	HDTRLD0	HDTSAR0		HDTDAR0	
F02D8H	HDTCCR1	–	HDTCCT1	HDTRLD1	HDTSAR1		HDTDAR1	
F02E0H	DTCBAR	SELHS0	SELHS1	–	–	–	–	–
F02E8H	DTCEN0	DTCEN1	DTCEN2	DTCEN3	DTCEN4	–	–	–
F02F0H	CRC0CTL	–	PGCRCL		–	–	–	–
F02F8H	–	CRCMD	CRCD		–	–	–	–

- TSPMCm: Added port setting for capacitive sensing unit (CTSU2SLa).
- F0248H to F024FH, F0280H to F029BH: Added timer RDe related register.
- F02B0H to F02BFH: Added AAU (Application Accelerator Unit) related register. For details, see Table 18-2.
- PER1: Added CTSUEN bit.
- ADCKS: Added A/D converter operation clock select register.
- PLLCTL: Changed the PLL oscillation stabilization time to 50 µs or more.
- CKSEL: Added PLL input clock select bit.

Table 18-1. SFR List for RL78/F22 Product (5/5)

Address	Register							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F0300H to F0698H	–	–	–	–	–	–	–	–
F06A0H	ADDR0M		ADDR1M		ADDR2M		ADDR3M	
F06A8H	ADDR4M		ADDR5M		ADDR6M		ADDR7M	
F06B0H	A/D converter window registers							
F06B8H								
F06C0H	–	LWBR0	LBRP0	LSTC0	LUSC0/	–	–	–
F06C8H	LMD0	LBFC0	LSC0	LWUP0	LIE0	LEDE0	LCUC0	–
F06D0H	LTRC0	LMST0	LST0	LEST0	LDFC0	LIDB0	LCBR0	LUDB00
F06D8H	LDB01	LDB02	LDB03	LDB04	LDB05	LDB06	LDB07	LDB08
F06E0H	LUOER0	LUOR01	–	–	LUTDR0		LURDR0	
F06E8H	LUWTDR0		–	–	LBSS0	–	LRSS0	–
F06F0H	TRJ0		–	–	–	–	–	–
F06F8H	–	–	–	–	–	–	–	–
F0700H to F07F8H	–	–	–	–	–	–	–	–

- F06A0H to F06AFH: Added A/D converter data register (mirror area).
- F06B0H to F06BFH: Added A/D converter related register. For details, see Table 18-3.
- LBSS0, LRSS0: Added LIN related register.

Table 18-2. AAU (Application Accelerator Unit) Window Register

Address	Register (Page.0)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F02B0H	ADTREG0		ADTREG1		ADTREG2		ADTREG3	
F02B8H	–	–	ACTREG	AKRAG/ ADUTYMX	AIDREF/AL1REF		AIQREF/AL2REF	

Address	Register (Page.1)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F02B0H	AKPD/AL3REF		AKID/AL1OFS		AKPQ/AL2OFS		AKIQ/AL3OFS	
F02B8H	–	–	–	–	AILIM/AKI1		APILIM/AKI2	

Address	Register (Page.2)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F02B0H	AIDBFL/ADUTYL1		AIDBFH/ADUTYL2		AIQBFL/ADUTYL3		AIQBFH/AIPL1	
F02B8H	ADOVER/AIPL2		AQOVER/AIPL3		–	–	–	–

Remark The window to be accessed is selected by the AAUWINR register.

Table 18-3. A/D Converter Window Register

Address	Register (Page.0)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	ADCSR		–	–	ADANSA0		ADANSA1	
F06B8H	ADADS0		ADADS1		ADADC	–	ADCER	

Address	Register (Page.1)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	ADSTRGR		ADEXICR		ADANSB0		ADANSB1	
F06B8H	–	–	–	–	ADOCDR		ADRD	

Address	Register (Page.2)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	ADDR0		ADDR1		ADDR2		ADDR3	
F06B8H	ADDR4		ADDR5		ADDR6		ADDR7	

Address	Register (Page.3)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	ADDR8		ADDR9		ADDR10		–	–
F06B8H	–	–	–	–	–	–	–	–

Address	Register (Page.4)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	–	–	–	–	–	–	–	–
F06B8H	–	–	–	–	ADDR22		ADDR23	

Address	Register (Page.5)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	ADDR24		ADDR25		ADDR26		ADDR27	
F06B8H	–	–	ADDR29		–	–	–	–

Address	Register (Page.6)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	–	–	–	–	–	–	ADSHCR	
F06B8H	–	–	–	–	–	–	–	–

Address	Register (Page.7)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	–	–	–	–	–	–	–	–
F06B8H	–	–	ADDISCR	–	–	–	–	–

Address	Register (Page.8)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	ADGSPCR		–	–	–	–	–	–
F06B8H	–	–	ADHVREFCNT	–	–	–	–	–

Address	Register (Page.13)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	–	–	–	–	–	–	–	–
F06B8H	–	–	–	–	–	ADSSTRL	–	ADSSTRO

Address	Register (Page.14)							
	Address + 0	Address + 1	Address + 2	Address + 3	Address + 4	Address + 5	Address + 6	Address + 7
F06B0H	ADSSTR0	ADSSTR1	ADSSTR2	ADSSTR3	ADSSTR4	ADSSTR5	ADSSTR6	ADSSTR7
F06B8H	ADSSTR8	ADSSTR9	ADSSTR10	–	–	–	–	–

Remark The window to be accessed is selected by the ADWINR register.

19. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/F22, F25 User's Manual: Hardware [R01UH1061EJ]
- RL78/F13, F14 User’s Manual: Hardware [R01UH0368EJ]
- RL78/F12 User’s Manual: Hardware [R01UH0231EJ]
- RL78 Family User's Manual: Software [R01US0015EJ]

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025.07.30	–	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 November 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.