DA913x PCB Layout Guidelines

This document contains the guidelines for creating a successful PCB layout containing the DA913x family of products

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1. Terms and Definitions

EMI	Electromagnetic interference
EVB	Evaluation board
PMIC	Power management integrated circuit

2. References

[1] DA9130 Datasheet, Renesas Electronics GmbH.
[2] DA9131 Datasheet, Renesas Electronics GmbH.
[3] DA9132 Datasheet, Renesas Electronics GmbH.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

PCB layout is a critical part of all switching power supply designs. As there are high switching currents, sensitive control signals in close proximity and a high power-density, control of the PCB layout is needed to ensure the correct electrical and thermal operation of the system.

It is important to use ground and power planes with high current power management devices. Renesas recommends that you use both a ground and main system voltage plane underneath the PMIC. The input decoupling can then decouple the planes. As both VDD and GND are planes, inductive cancellation will provide a very low impedance path to the IC.

It is not possible to produce a set of rigid rules for layer construction within a PCB because each design has its own requirements: it is not appropriate for Renesas to suggest which plane should be power and which should be ground. Instead, this application note uses examples from the Renesas PCB range to illustrate practices that have been found useful.

3.1 Design help and guidance

In most sales regions Renesas offers to review customer schematics and PCB layouts. Use of this design-in service is recommended to ensure power management solutions are optimized for reliability.

4. General PCB layout guidance

Sections 4.1 and 4.2 discuss general PCB layout rules that can be applied to the whole design. Section 4.3 onwards addresses guidelines for specific parts of a Renesas PMIC, for example buck converters and LDOs.

Key layout principles include:

- Current-carrying traces are as thick as possible
- The board has a low impedance ground
- Sensitive signals are shielded from interference by noisy traces

4.1 Ground impedance

The ground plane should have low impedance for all areas of the PCB. This will help with power control, will improve signal quality and reduce EMI.

The use of a ground layer and flooding of other layers with multiple vias are good methods to keep the impedance low.

4.2 Buck-specific layout guidelines

This section provides guidance for the layout of specific areas of a power supply.

Keep in mind that the top and bottom planes are also used for heat dissipation. It is good practice to place micro-vias and filled vias to keep the thermal resistance low. It is necessary to keep the vias around the pass devices (PVDD/Vsys, PGND and LX) to a reasonable amount and density by thinking about both the heat dissipation and the power planes impedance.

A thick through hole filled via is very good at conducting the heat from top to bottom planes, but can reduce the shielding effect and increase the impedance of power planes on internal layers.

The input capacitors should be places as close as possible to the chip, and the inductors should be placed close to the chip, but can be placed further away than the input caps depending on space constraints.

The differential feedback traces should be taken directly from the output at the capacitor pads and should be routed close to each other. It is also possible to take the feedback from the point of load, but this increases the risk of noise being introduced onto this trace because of the extra length it would run. Good power planes can avoid the need for such point of load feedback configuration.

The feedback traces must be shielded from all noise sources, especially the LX nodes of buck converters. Noise fed into a feedback pin often creates extra voltage ripple on the buck output. In the reference design example of section 4.4, the feedback traces are on the bottom layer and therefore away from the noisy LX nodes.

4.3 Non-power pins

4.3.1 AVDD

AVDD is used for the analog side of the sub-PMIC. It is sensitive to noise and must be decoupled from PVDD.

It is recommended to place a decoupling capacitor as close as possible to the chip's AVDD and AGND pads.

4.3.2 GPIOs

GPIO pins are usually unaffected by the layout and so can be given a low priority during layout.

4.4 Example of PCB layout used in Renesas reference boards

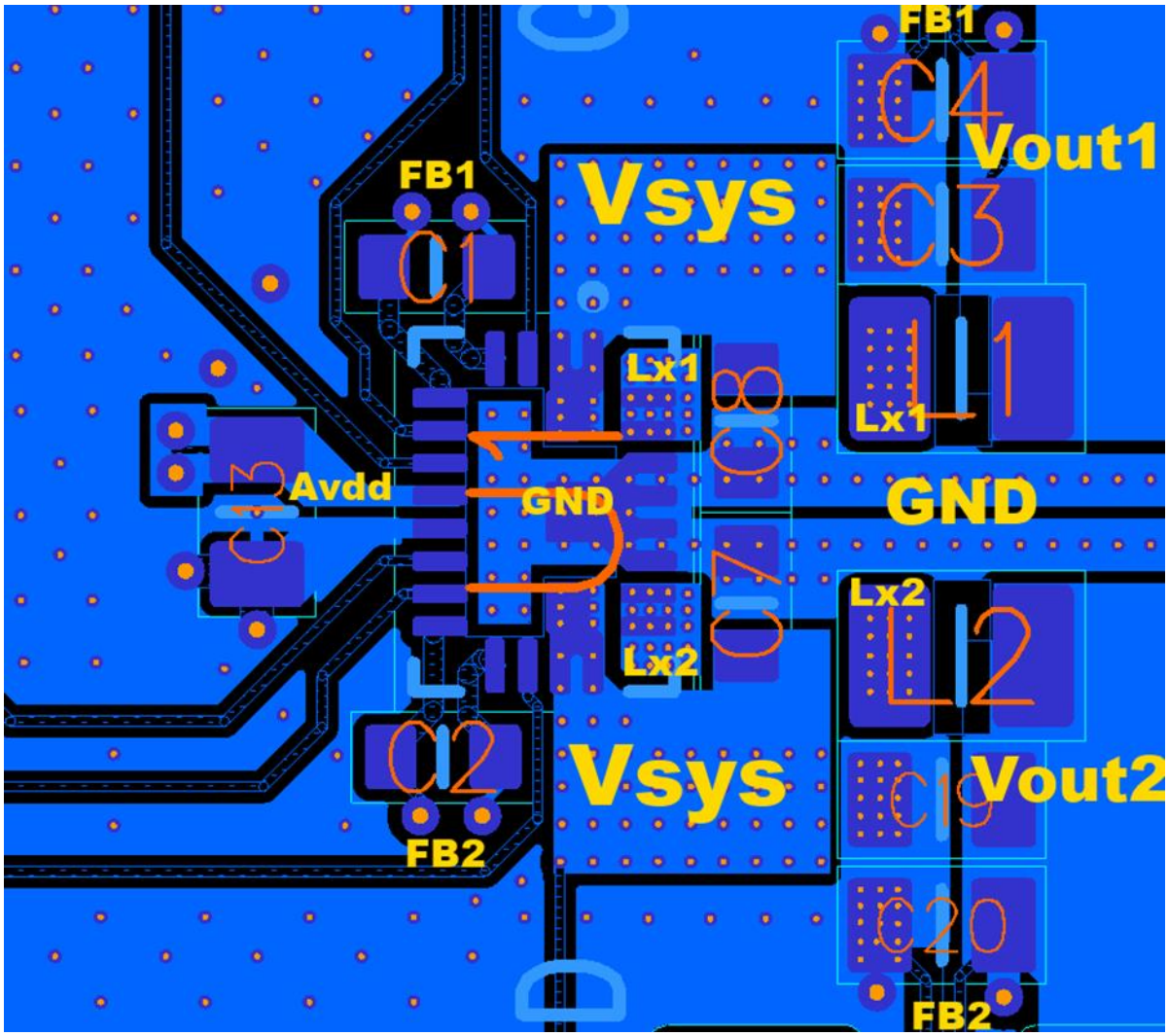

Figure 1. Layer 1 (top)

C13 is placed close to AVDD and AGND pads and connected to Vsys on layers 3-4 and to ground on layers 2-5-6.

The large copper area around Vsys is used as a heatsink and connected to a Vsys power plane on another layer through micro-vias.

The ground pad below the chip extends towards the input capacitors C7 and C8 and is connected to the ground plane on the top side of the board.

LX1 and LX2 pads are connected to the coils L1 and L2 through an internal plane. A choice has been made to prioritize the decoupling capacitors C7 and C8 and place them closer to the Vsys and GND pads.

FB1 and FB2 differential feedback lines are kept away from LX and go below the top layer.

Thin traces extending towards the left and top are GPIOs.

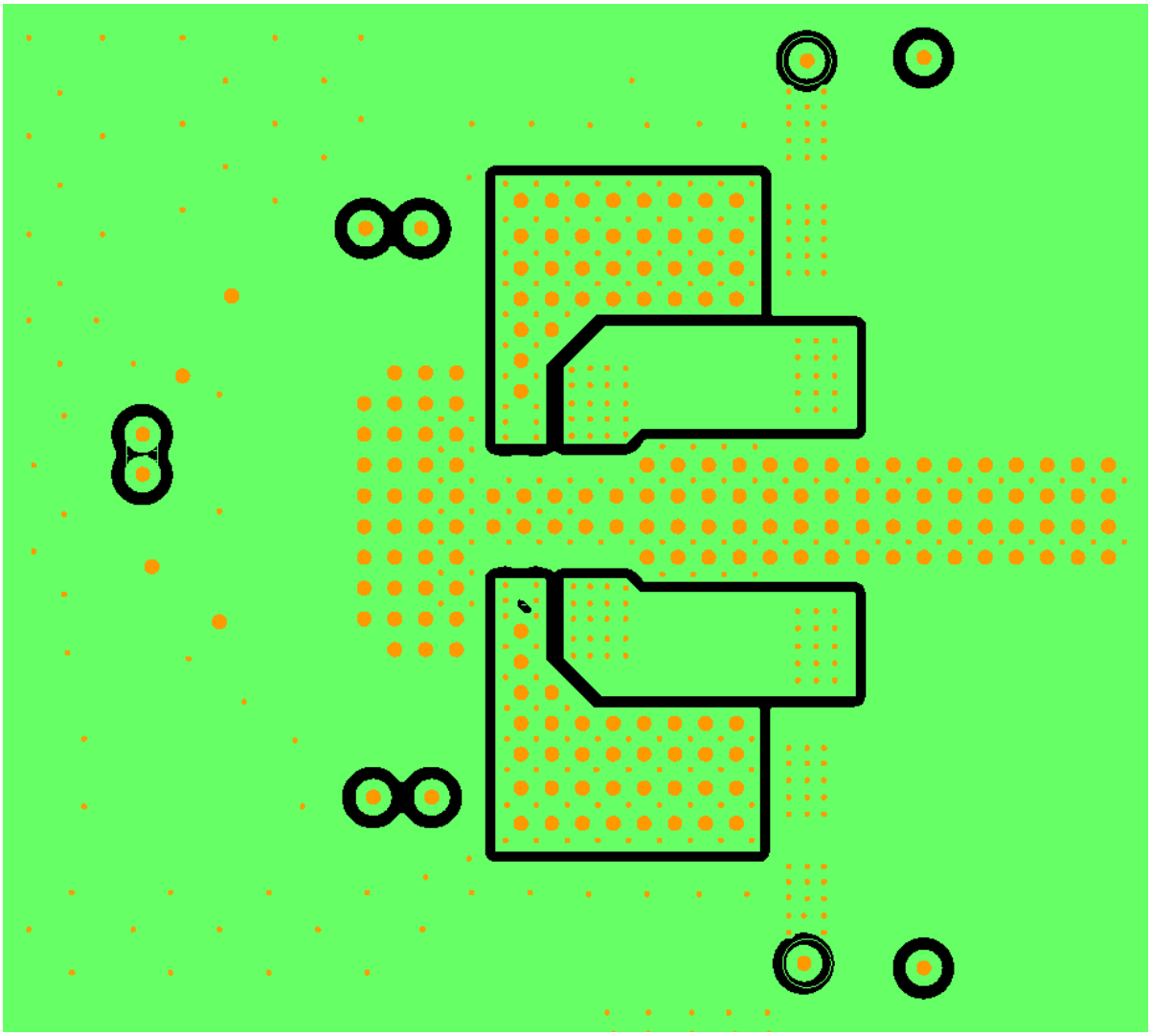

Figure 2. Layer 2 (internal)

This layer Is a ground plane with four polygons: Two LX traces going between the LX1 and LX2 pads on the chip and the coils L1 and L2. The other two polygons connect the Vsys trace to the PVDD pads.

Note the amount of layer 1-2 micro-vias to connect the planes together and the layer 2-4 micro-vias to transfer the heat.

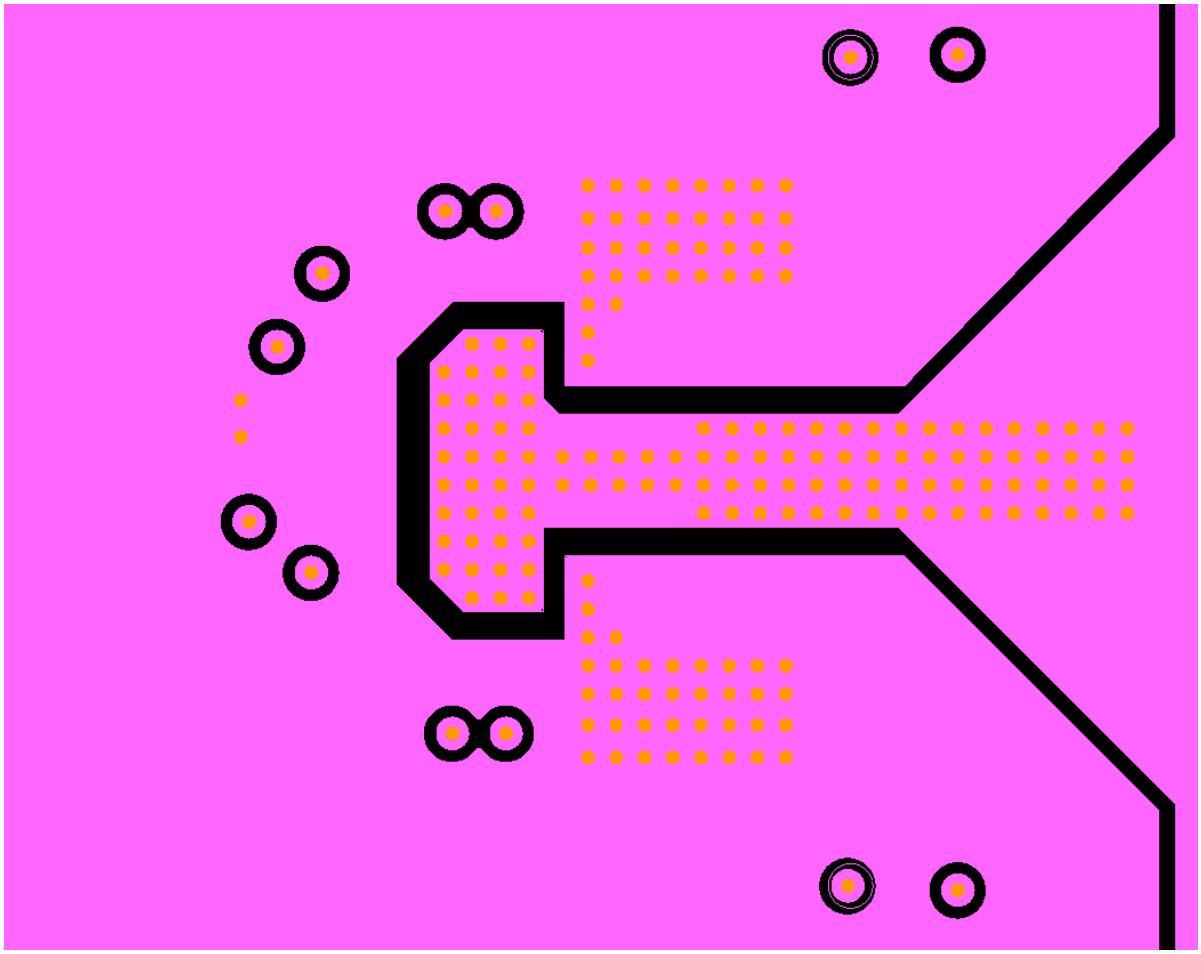

Figure 3. Layer 3 and 4 (internal)

These layers are shared between a ground plane under the chip and on the right side, and a Vsys plane left of the chip. Vias through layers 2, 3, 4 and 5 ensure a low thermal and electrical impedance between the layers.

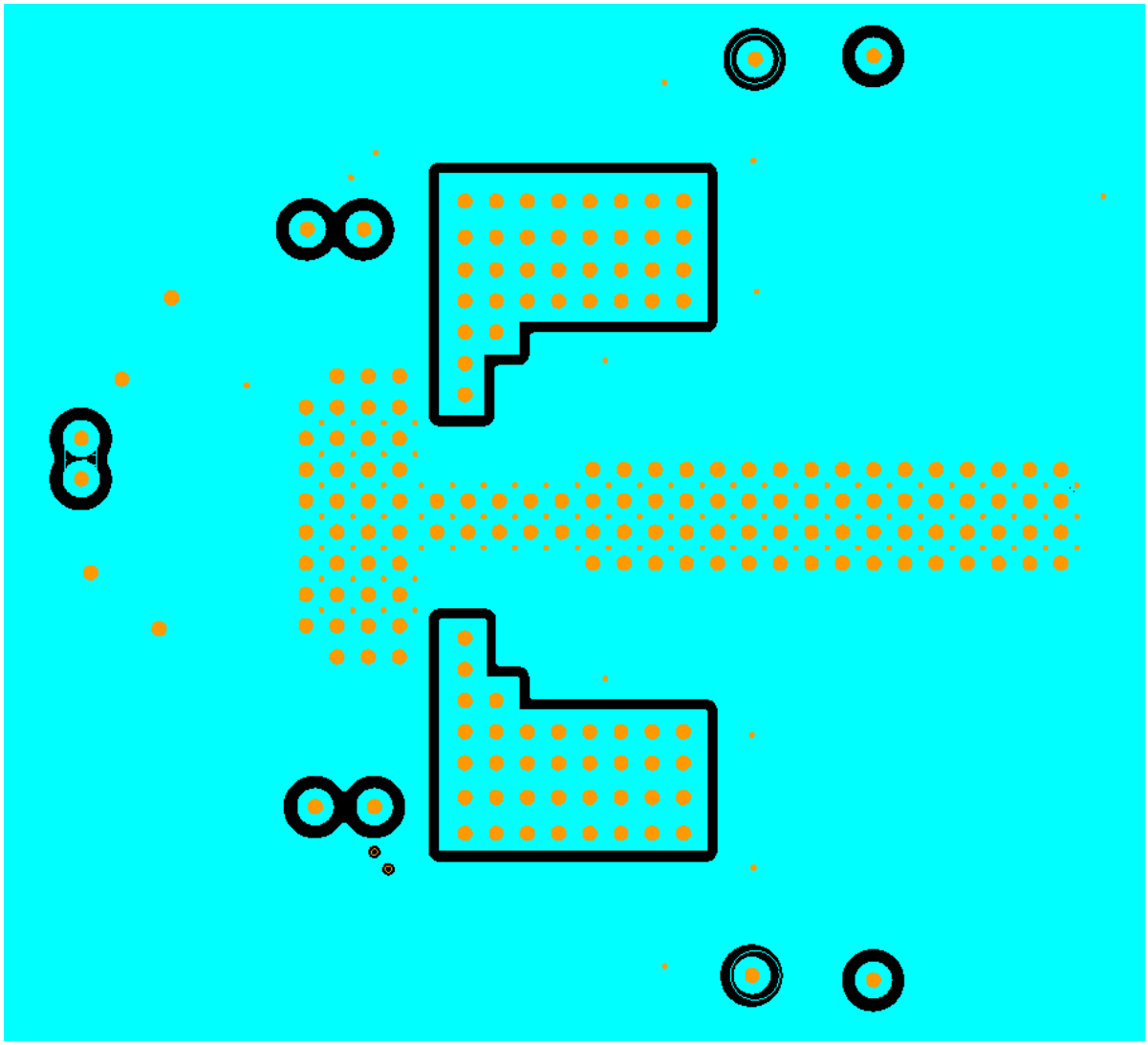

Figure 4. Layer 5 (internal)

This layer is a ground plane with a dissipation area for Vsys, connected to the top layer.

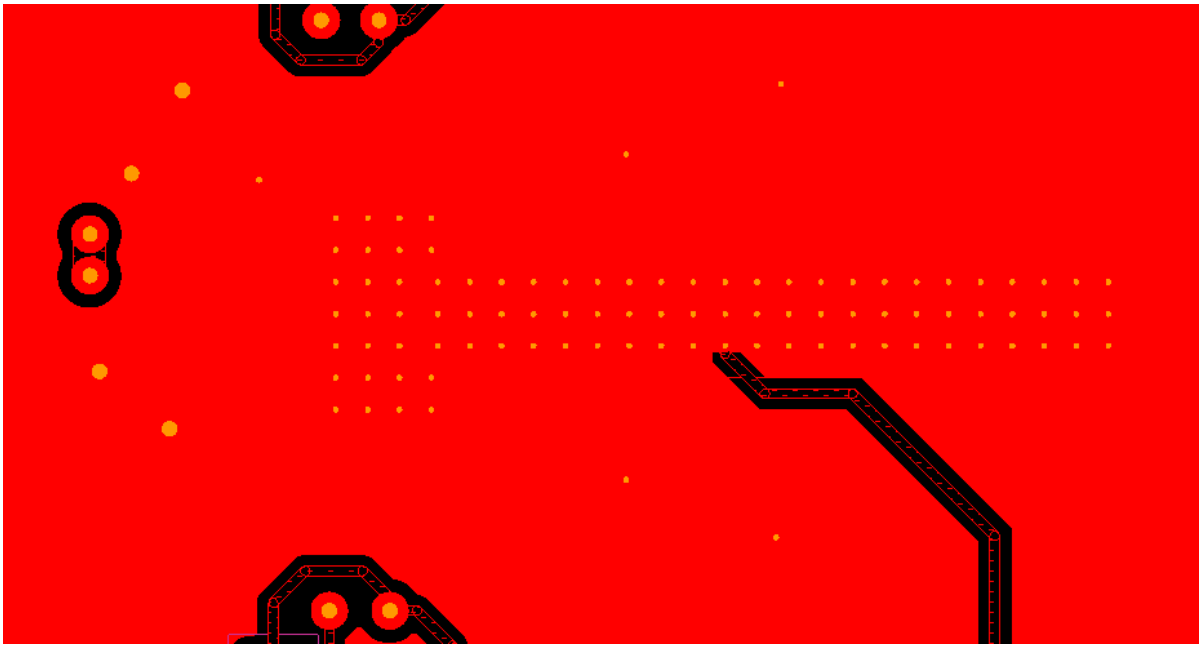

Figure 5. Layer 6 (bottom)

This layer is a ground plane used mostly for heat dissipation.

The trace on the right is used for probing the ground voltage close to the chip. This can be considered as a quiet ground.

The symmetrical vias on the top and bottom of the chip are the differential feedback lines and are shielded form the noisy power signals.

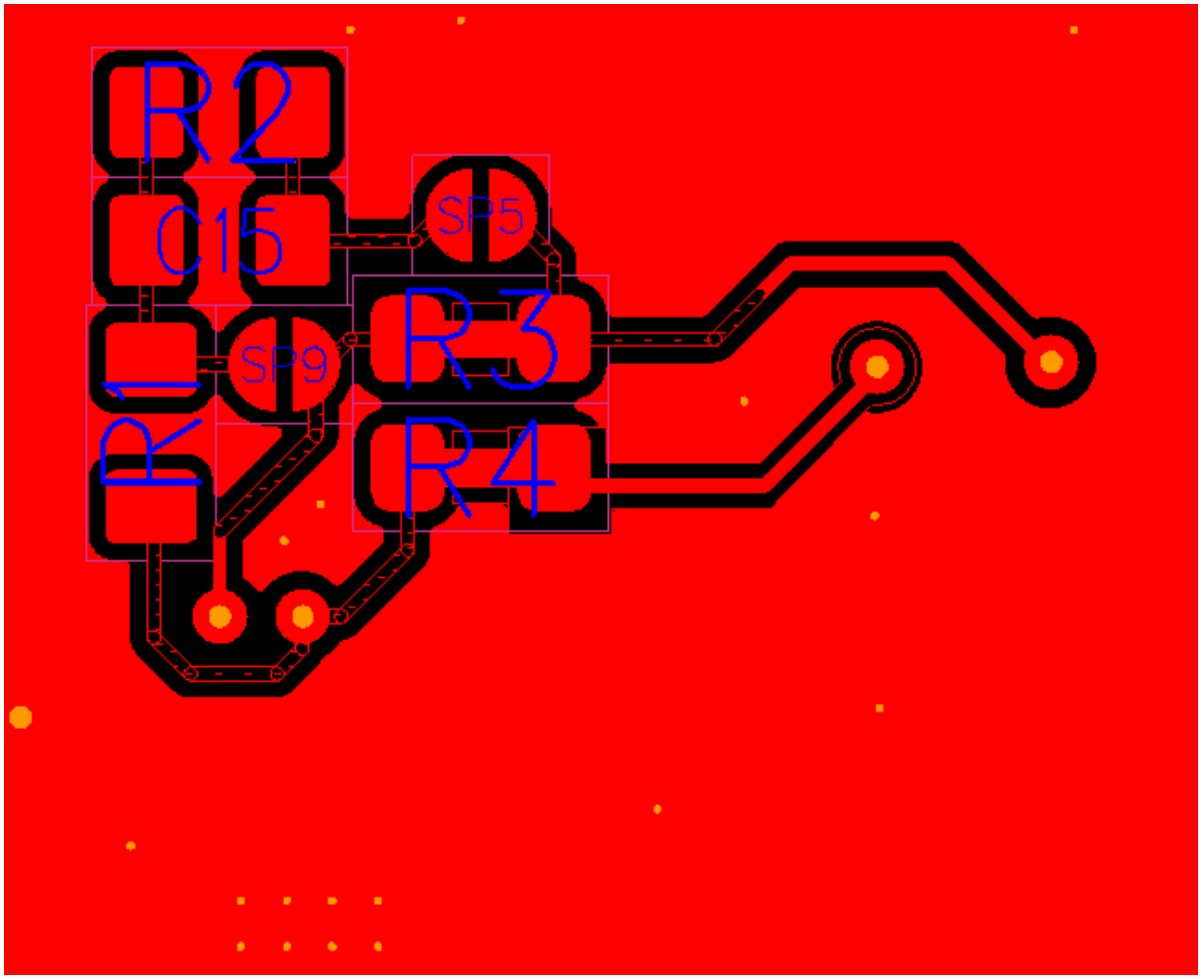

Figure 6. Differential feedback

Those two lines connect the ground through R4 and Vout through R3, extending from the output capacitor on the right to the chip's feedback pins on the left. Traces are kept close to each other to limit noise on a sensitive signal.

R3 and R4 are zero-ohm resistors used for measurements and can be removed and shorted on a customer design.

The RC network using the shorting points SP5 and SP9, R1-R2 and C15 is optional and is used as a voltage divider. The typical application is to output 3.3 V with Vsel set to 1.65 V.

5. Conclusions

The PCB layout for integrated power management ICs requires careful consideration if an optimised system is to be achieved. Practical guidelines have been presented together with example layouts of Renesas's own reference boards.

6. Revision History

Revision	Date	Description
01.01	July 14, 2025	
Modifications: ▪ Converted to new template		
01.00	Dec 10, 2021	First version.

STATUS DEFINITIONS

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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