Design Guide

PCB Design Guidelines for High Speed Signal Interfaces

RZ/G3S LFBGA 14.0/13.0sq

Renesas Electronics
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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

Introduction

This document describes a PCB design guideline for designing a board with the RZ/G3S.

The interfaces described in this document are listed below.

- USB 2.0
- PCI Express Gen 2.0

1. USB 2.0

In this section, the design guideline about USB 2.0 is described.

1.1 External Components Requirements

The following describes the external components requirements for the USB 2.0 interface.

1.1.1 Power Supply

Power rail noise filtering is necessary to guarantee the correct functioning of the USB 2.0 interface.
The RZ/G3S has three power rails for the USB 2.0 interface:

- USB_VDD33
- USB_VDD18
- USB_AVDD18

Figure 1.1 shows configurations of decoupling capacitors. The values of the capacitors and their configurations are examples of the recommended values. The inductance of the PCB should be as small as possible.

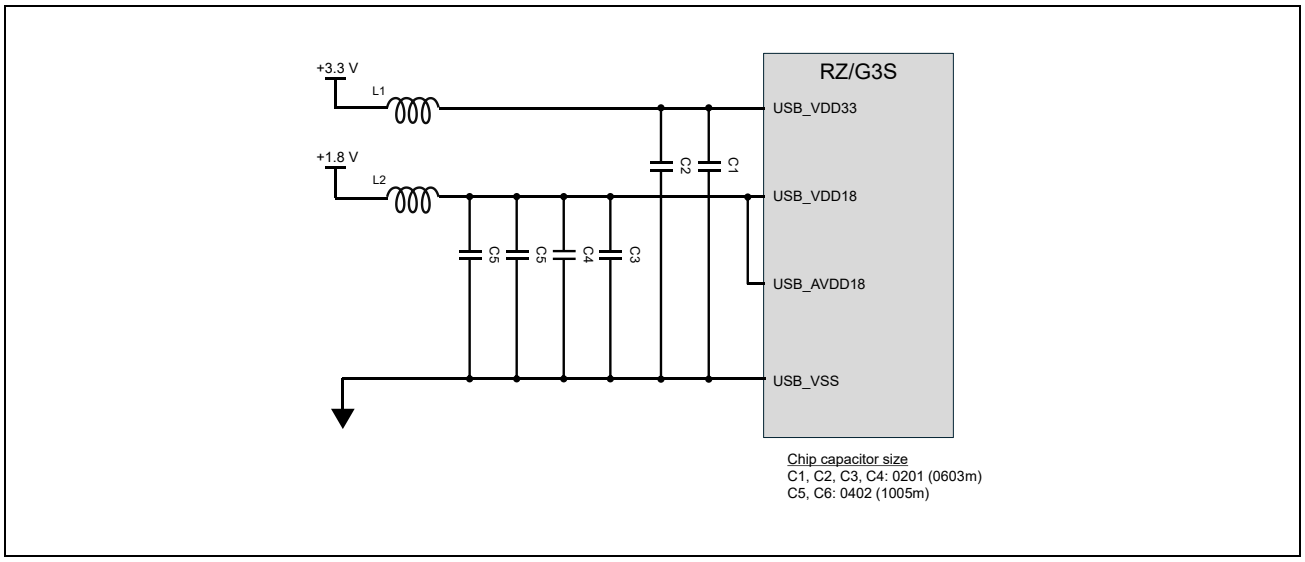

Figure 1.1 Decoupling Capacitors for USB 2.0

Table 1.1 lists the capacitor and inductor values for the respective parts shown in **Figure 1.1**.

Table 1.1 External Parts for PCB Power Lines of USB 2.0

Designator	Value	Tolerance	Voltage Rating*1	Size
C1, C2	0.1 µF	±10%	10 V	0201 (0603m)
C3, C4	0.1 µF	±10%	6.3 V	0201 (0603m)
C5	2.2 µF	±20%	6.3 V	0402 (1005m)
C6	10 µF	±20%	6.3 V	0402 (1005m)
L1*2	600Ω	±25%	—	0402 (1005m)
L2	1.0 µH	±20%	—	0603 (1608m)

Note 1. It is recommended that the voltage rating be no less than three times the value of the supply voltage.

Note 2. The ferrite bead is optional and can be placed further away from the power supply pin.

Critical PCB design considerations are outlined below.

Analog Power Supply

- USB_AVDD18 and USB_VDD18 need to be connected to a 1.8-V analog power supply pattern.
- The wiring impedance of the analog power supply needs to be as small as possible.
- An analog power supply should be isolated from a digital power supply by using either an inductor or ferrite bead, or by separating the power planes and placing additional ceramic capacitors. These components should be located close to the RZ/G3S.
- The analog power supply pattern must NOT be close to other signal wiring.

Digital Power Supply

- USB_VDD33 should be connected to a 3.3-V digital power supply plane.
- The wiring impedance of the digital power supply needs to be as small as possible.

GND Wiring

- USB_VSS should be connected to a USB GND or GND plane.
- The wiring impedance of GND needs to be as small as possible.
- The USB GND or GND plane must NOT be close to other signal wiring.

1.1.2 Reference Resistor

For calibration, the USB PHY requires a calibration resistor to be connected to the USB_RREF pin.

Figure 1.2 shows a configuration of this resistor.

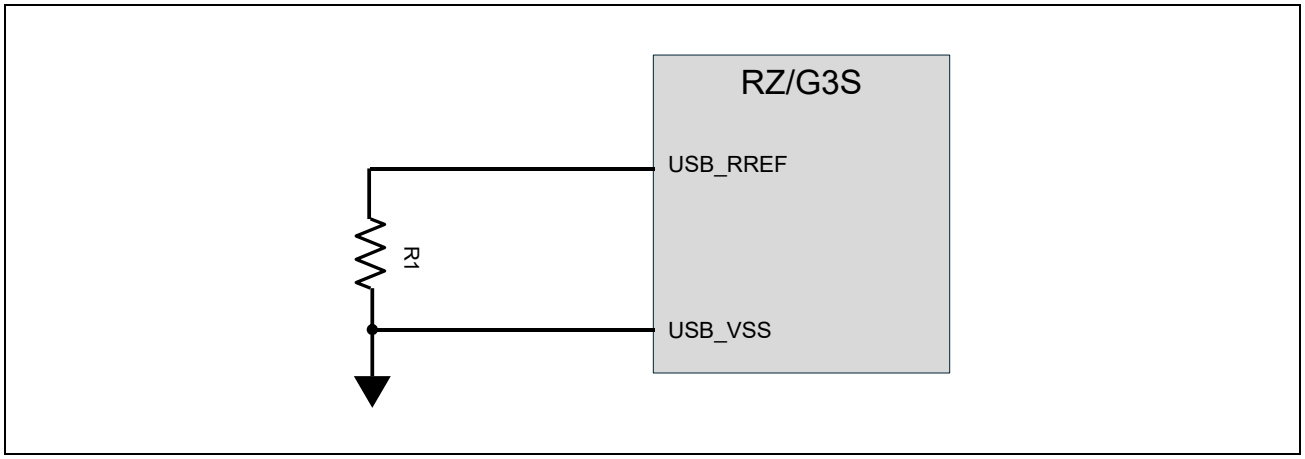

Figure 1.2 Reference Resistor for USB 2.0

Table 1.2 lists the resistor value for the part shown in **Figure 1.2**.

Table 1.2 External Parts for USB 2.0

Designator	Value	Tolerance	Size
R1	1.8kΩ	±1%	0201 (0603m)

Critical PCB design considerations are outlined below.

- A 1.8-kΩ reference resistor should be located between USB_RREF and USB_VSS.
- The reference resistor should be located close to the RZ/G3S, and the wiring should be designed with the resistance below 0.5Ω.
- The reference resistor should NOT be located in parallel with a capacitor to avoid affecting the calibration.
- The reference resistor and wiring must NOT be placed adjacent to or intersect with other signal wiring.
- To prevent noise contamination, the layer under the reference resistor and wiring should be GND plane.

1.1.3 External Components for USB0_VBUSIN

The RZ/G3S has a USB0_VBUSIN pin for peripheral VBUS input.

Figure 1.3 shows external components requirements for USB0_VBUSIN.

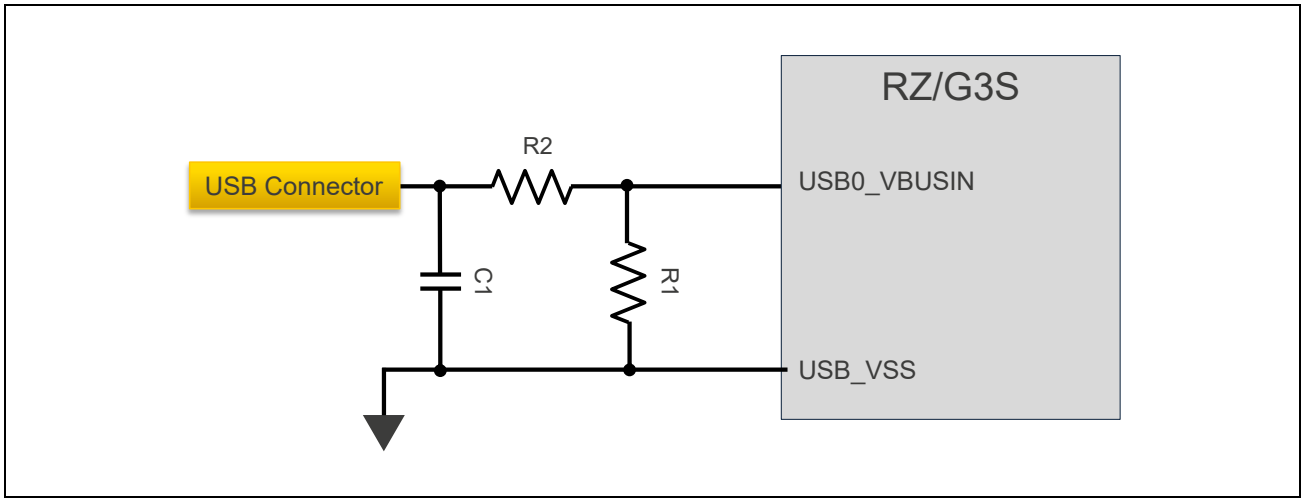

Figure 1.3 External Components for USB0_VBUSIN

Table 1.3 lists the resistor and capacitor values for the respective parts shown in **Figure 1.3**.

Table 1.3 External Parts for USB0_VBUSIN

Designator	Value	Tolerance	Voltage Rating*3	Size
R1*1	1.0kΩ	±1%	—	0402 (1005m)
R2*1	1.8kΩ	±1%	—	0402 (1005m)
C1*2	1.0 µF	±25%	10 V	0201 (0603m)

Note 1. The input voltage to USB0_VBUSIN should be supplied with 1.8 V by a resistor divider. When an external device is connected to the USB connector during power off, the voltage above the withstand voltage is applied between the gate and drain, which may damage the IO.

Note 2. It is recommended to connect a capacitor to prevent chattering on USB0_VBUSIN.

Note 3. It is recommended that the voltage rating be no less than three times the value of the supply voltage.

1.2 PCB Layout

This section describes layout considerations when designing for the USB 2.0 interface.

1.2.1 Transmission Line

Give design priority to the high priority items marked with a check mark.

Table 1.4 Guidelines for PCB Signal Lines of USB2.0

Items		Guidelines	Refer to
Line impedance		√: Differential 90Ω ± 10% Single-end 45Ω ± 10%	**Figure 1.4** (4)
Line length difference	Between each pos. and neg.	√: Same length as much as possible √: Line length is as short as possible	—
Line bending		Recommended : External angle 45° (Prohibited: >45°)	—
Line layer Number of vias	Between each pos. and neg.	Same layer Note: Recommended: Top layer without any vias Same via number (number is as few as possible)	—
Line width	Between each pos. and neg.	√: Same width as much as possible	**Figure 1.4** (1)
Return path		√: Place Continuous Ground Plane under Diff.	**Figure 1.4** (5)
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to Diff.	—

Note: Do not use SSC (Spread Spectrum Clock) as the reference clock.

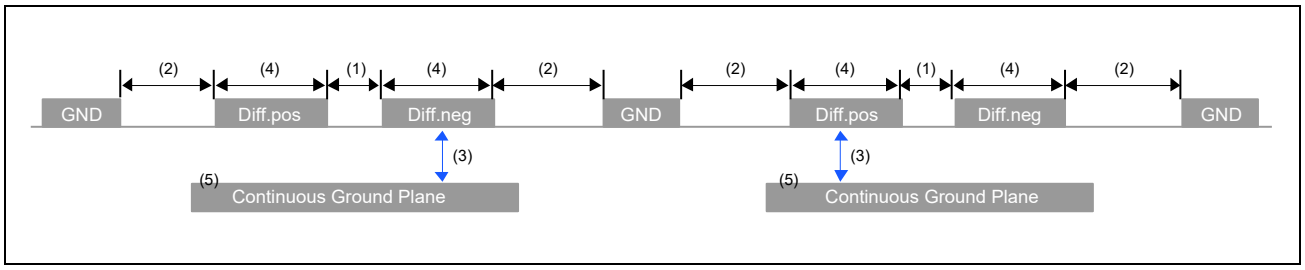

Figure 1.4 Signal Lines Example 1

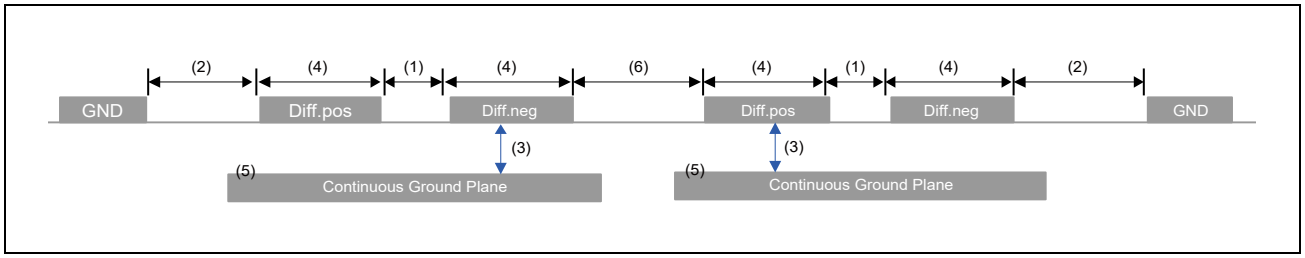

Figure 1.5 Signal Lines Example 2

Critical PCB design considerations are outlined below.

- The DP/DM wiring must not cross the power supply split or plane void.
- The DP/DM wiring must not intersect with other signal wiring. When placing them close to each other is unavoidable, a digital power plane or GND plane should be placed between the layers to isolate the signals.
- The number of bends in the DP/DM wiring should be minimized as much as possible. When bending is necessary, avoid right-angle bends and instead use two 45-degree bends.
- To prevent noise contamination, the layer under the DP/DM wiring should be GND plane.

1.2.2 Processing of Unused Terminals

- DP/DM should be connected to GND through a 10-kΩ resistor.
- USB_RREF should be left open.
- USB_VDD18 and USB_AVDD18 should be connected to a 1.8-V power supply.*1 However, it is not necessary to separate the digital power supply from the analog power supply.
- USB_VDD33 should be connected to GND.
- Assert the internal signal whose bit name is dirpd*2, and power down the core VDD via this internal signal.

Note 1. Do NOT connect USB_VDD18 and USB_AVDD18 to GND, as this means that the internal circuit is floating and through current may occur.

Note 2. Clamp the core VDD or GND when there is an internal input signal whose status is open except dirpd.

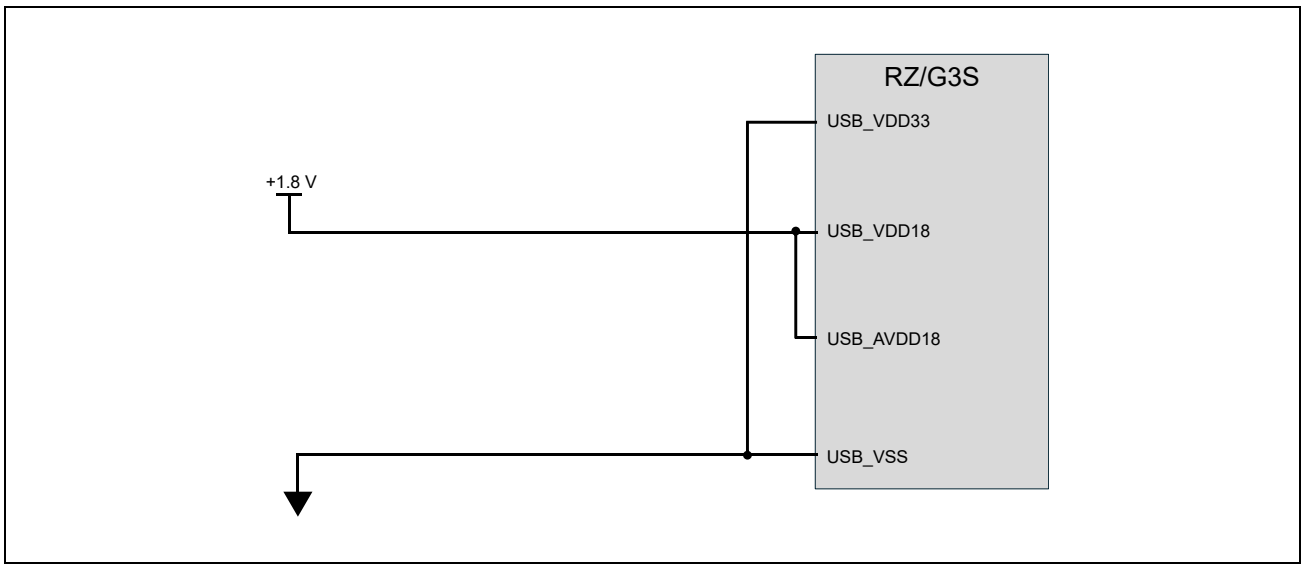

Figure 1.6 Configuration of External Parts (1/2)

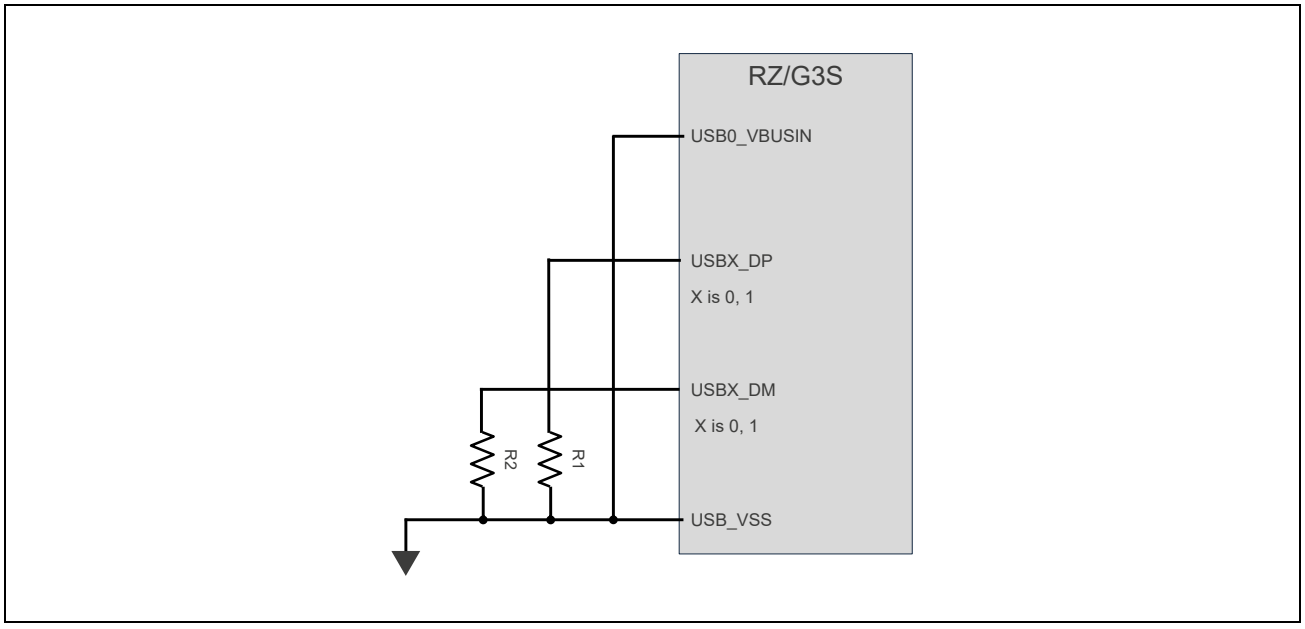

Figure 1.6 Configuration of External Parts (2/2)

1.2.3 EMI/ESD Protection

Notes on EMI/ESD protection are described below.

- When EMI/ESD protection components such as a coil and a diode are mounted on the USB transmission lines, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. The components should be carefully evaluated and selected to ensure USB 2.0 High-Speed compliance to avoid signal integrity issue.

Figure 1.7 shows an example connection when EMI/ESD protection components are used.

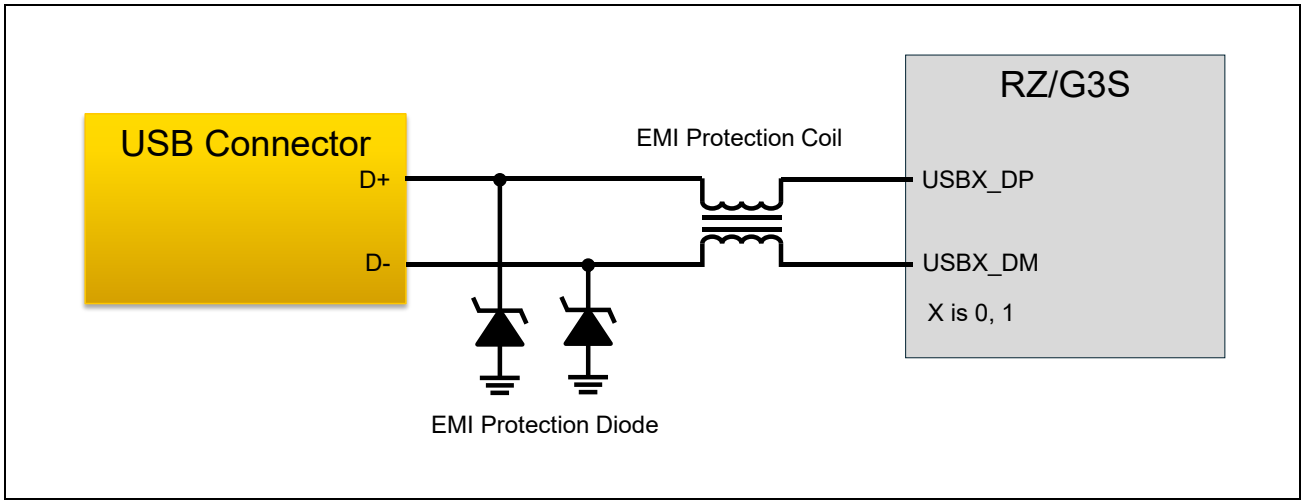

Figure 1.7 Connection Example when EMI/ESD Protection Components are Used

1.3 PCB Verification

This section describes Signal Integrity (SI) verification items when designing for the USB 2.0 interface.

1.3.1 Signal Integrity

This section focuses on the Signal Integrity (SI) side of design verification.

1.3.1.1 Differential Transmission Line Impedance

Renesas recommends doing a Time Domain Reflectometry (TDR) analysis to verify the differential impedance of the transmission line and optimize the design to reduce the impedance discontinuities.

The transmission line referred to above is the end to end (die to die) connection between the downstream facing port (DFP) and the upstream facing port (UFP). If a MUX, HUB, or other device exists in between, the end-point becomes this device.

Figure 1.8 illustrates a simulator circuit for TDR analysis.

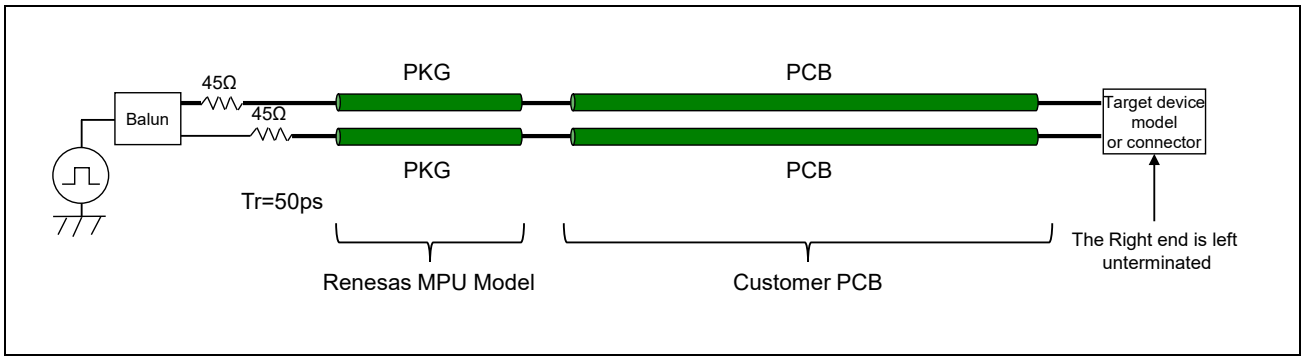

Figure 1.8 Simulator Circuit for TDR Analysis

2. PCI Express Gen 2.0

In this section, the design guideline about PCI Express 2.0 (hereinafter referred to as PCIe) is described.

Applicable Standard

For general information on electrical and transfer path characteristics and on connector specifications required in designing a PCB, refer to the specifications issued by the standards certification body listed in the table below.

Table 2.1 Standards Applicable to PCI Express

Standards Certification	Title of Specification
PCI-SIG	PCI Express® Base Specification Revision 4.0
	PCI Express Card Electromechanical Specification Revision 4.0

2.1 General Guidelines

For the basic design of differential wiring patterns, refer to the guidelines issued by the PCI-SIG as shown below. The information is relevant regardless of whether the standard being implemented is PCIe generation 1 or 2. The relevant descriptions are mainly given in the section “Layout considerations”.

Note that the differential impedance value of the transfer path (differential wiring pattern) differs with the module, that is, according to whether it is PCIe generation 1 or 2.

- Board Design Guidelines for PCI Express™ Architecture
  (Please download from https://members.pcisig.com/)

2.2 External Components Requirements

This section describes the external components requirements for the PCIe interface.

2.2.1 Power Supply

Power rail noise filtering is necessary to guarantee the correct functioning of the PCIe interface.

The RZ/G3S PCIe interface has two power rails:

- PCIE_VDD18
- PCIE_VDD09

Figure 2.1 shows configurations of decoupling capacitors. The values of the capacitors and their configurations are examples of the recommended values (see **section 2.7.3** for component placement recommendations).

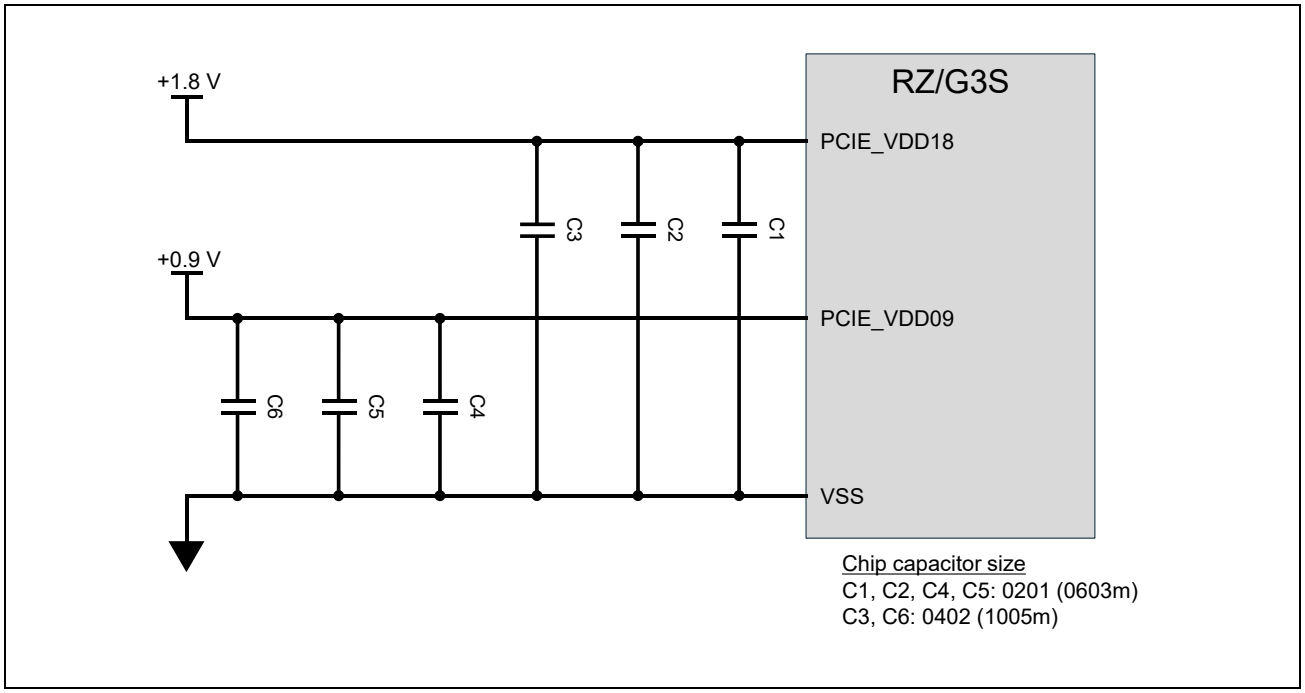

Figure 2.1 Decoupling Capacitors for PCIe

Table 2.2 lists the capacitor values for the respective parts shown in **Figure 2.1**.

Table 2.2 External Parts for PCB Power Lines of PCIe

Designator	Value	Tolerance	Voltage Rating*1	Size
C1, C4	1000 pF	±10%	6.3 V	0201 (0603m)
C2, C5	0.1 µF	±10%	6.3 V	0201 (0603m)
C3, C6	10 µF	±20%	6.3 V	0402 (1005m)

Note 1. It is recommended that the voltage rating be no less than three times the value of the supply voltage.

2.2.2 AC Coupling

All transmitters shall be AC coupled according to the PCI Express® Base Specification standard. **Figure 2.2** shows the AC coupling connection of the transmitter on the system PCB.

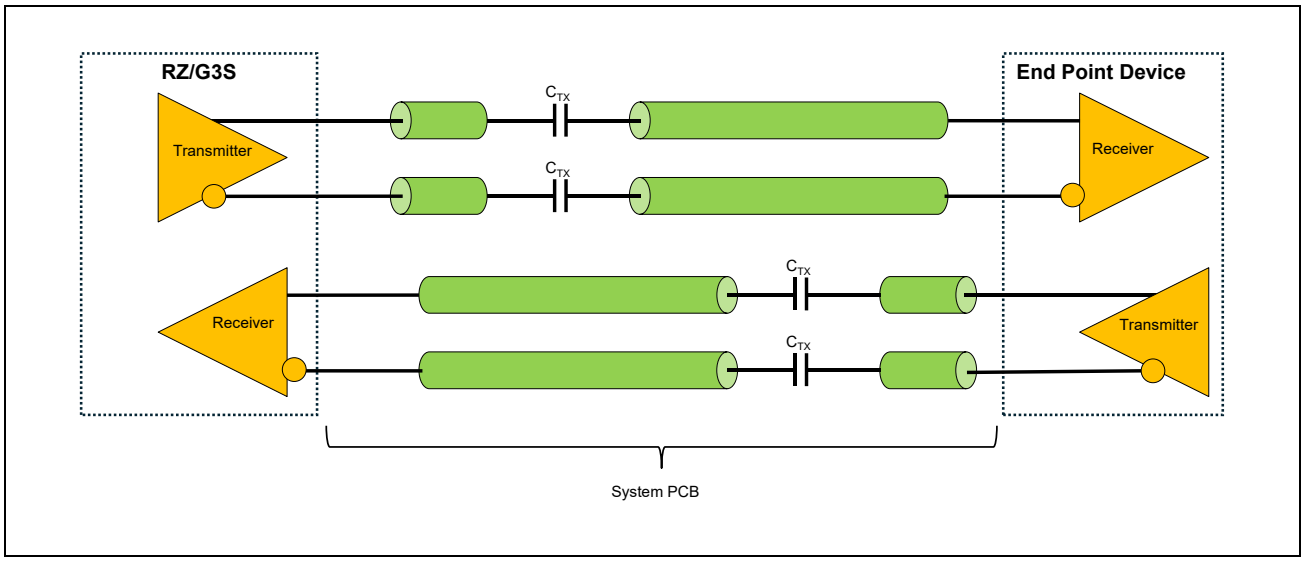

Figure 2.2 Transmitter AC Coupling Connection

Table 2.3 summarizes the allowed capacitor value range from the standard.

Table 2.3 AC Coupling Value Range for PCIe

Designator	Min	Max	Unit
C_{TX}	176	265	nF

2.3 Clock Requirements

This section describes the clocking requirements for the PCIe interface.

2.3.1 Clocking Architecture

In a PCIe system, both the transmitter and receiver devices are supplied with a reference clock, designated as PCIE_CLK in this document. For all PCIe generations, PCIE_CLK is a 100 MHz HCSL differential clock. The table below shows the maximum frequency stability requirements by generation for Common Clock architectures.

Table 2.4 PCIE_CLK DC Specifications

PCIe Generation	Frequency Stability (ppm)*1
PCIe 1.1	±300
PCIe 2.1	±300

Note 1. For all Separate Reference architectures, the frequency stability of the reference clock is ±100 ppm.

The RZ/G3S supports the following clocking architectures:

- Common Clock (CC)
- Common Clock with Spread (CCS)
- Separate Reference No Spread (SRNS)

The RZ/G3S does not support the following clocking architecture:

- Separate Reference Independent Spread (SRIS)

Common Clock Architecture

In Common Clock (CC) architectures, both the transmitter and receiver devices are clocked by the same PLL. **Figure 2.3** shows a block diagram of this architecture. Common clock is the most widely supported PCIe clocking architecture. This architecture easily supports SSC on both PCIe devices for EMI reduction, allowing for Common Clock with Spread (CCS).

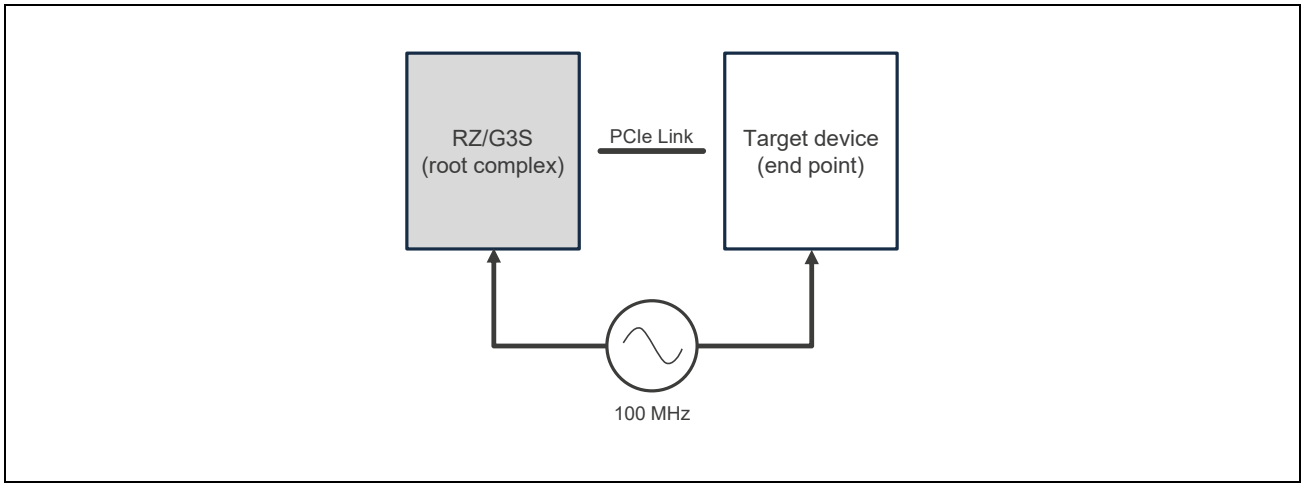

Figure 2.3 Common Clock Architecture

Separate Reference Architecture

In Separate Reference architectures, different clock sources are used for the transmitter and receiver devices. **Figure 2.4** shows a block diagram of this architecture. The elastic buffers automatically take care of the clock shift between TX and RX in an SRNS architecture.

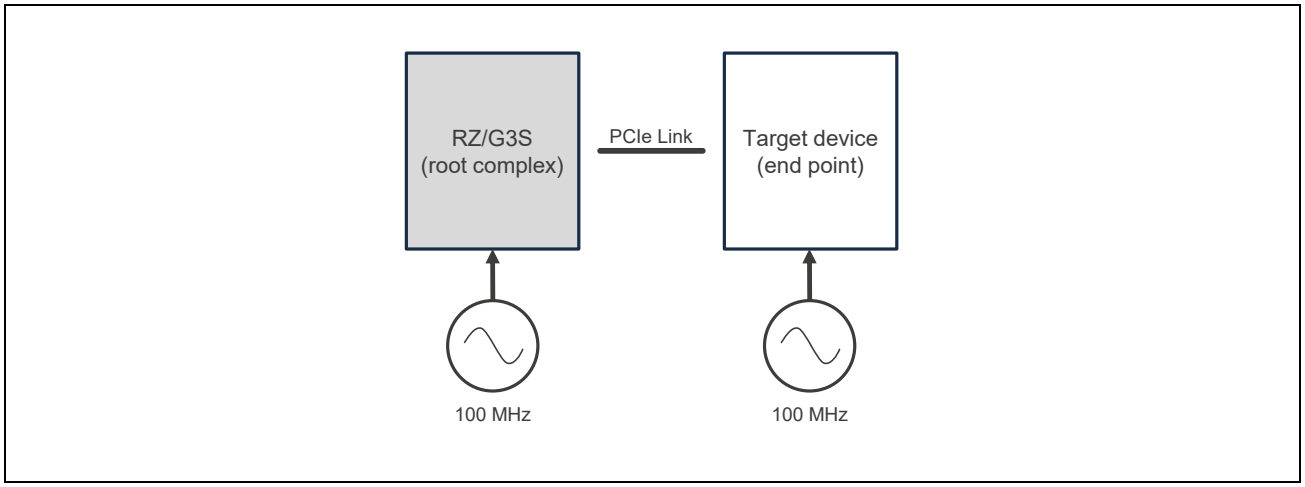

Figure 2.4 Separate Reference Architecture

2.3.2 Clocking Input Format

The PCIE_CLK is a differential High-Speed Current Steering Logic (HCSL) clock. HCSL drivers source current into an external 50-Ω load.

The RZ/G3S supports HCSL and Low-Power HCSL (LP-HCSL) input formats. **Figure 2.5** and **Figure 2.6** illustrate PCIE_CLK configuration when using HCSL and LP-HCSL input formats.

LP-HCSL reduces the power consumption of the driver, and integrates the termination resistors into the driver, removing the need for external components. LP-HCSL drivers use a Push-Pull architecture that allows for a longer clock track length between devices on the PCB. LP-HCSL drivers can also be AC-coupled without change to the termination or swing.

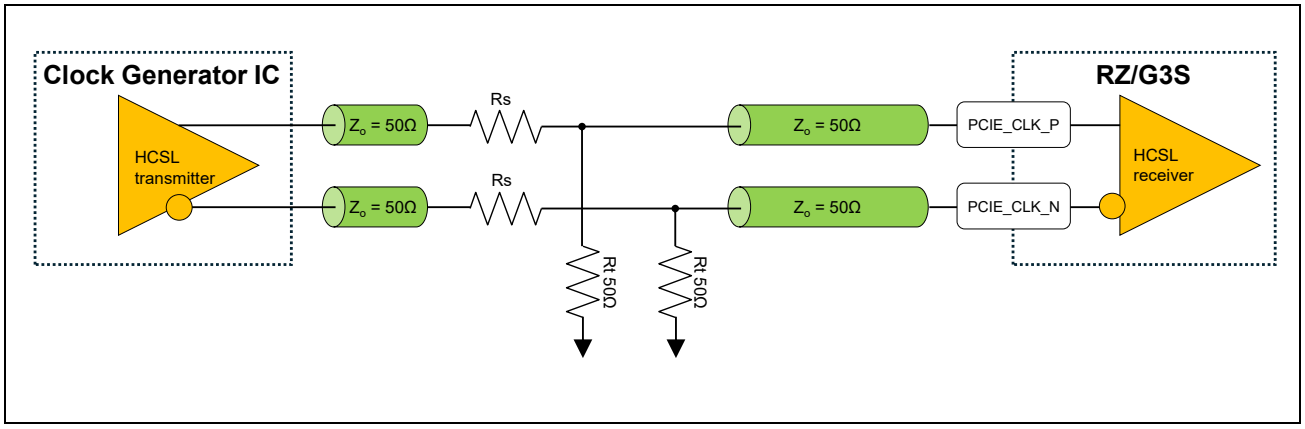

Figure 2.5 HCSL Input Format

Note

The series resistor (Rs) value depends on the clock generator IC. Refer to the part datasheet for the correct value.

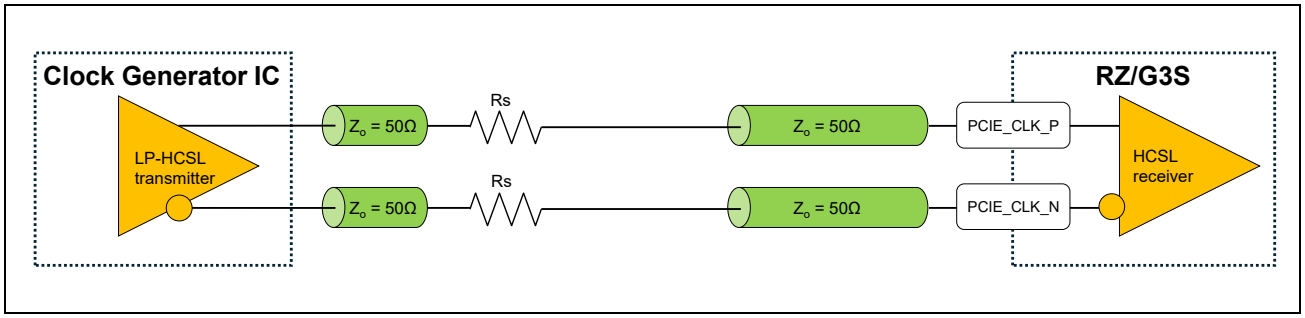

Figure 2.6 LP-HCSL Input Format

Note

The series resistor (Rs) value depends on the clock generator IC. Refer to the part datasheet for the correct value.

2.4 PCIE REFCLK DC Specifications and AC Timing Requirements

Table 2.5 lists the PCIE REFCLK DC specifications and AC timing requirements.

V_{CROSS}, V_{MAX}, and V_{MIM} are particularly important parameters to take into consideration when selecting a reference clock generator device.

Table 2.5 PCIE REFCLK DC Specifications and AC Timing Requirements

		100 MHz Input		
Parameter	Description	Min	Max	Unit
Rising edge rate	Rising edge rate	0.6	4.0	V/ns
Falling edge rate	Falling edge rate	0.6	4.0	V/ns
V_{IH}	Differential input high voltage	+150	—	mV
V_{IL}	Differential input low voltage	—	+150	mV
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} over all rising clock edges	—	+140	mV
V_{RB}	Ring-back voltage margin	-100	+100	mV
T_{STABLE}	Time before V_{RB} is allowed	500	—	ps
$T_{PERIOD\ AVG}$	Average clock period accuracy	-300	+2800	ppm
$T_{PERIOD\ ABS}$	Absolute period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns
$T_{CCJITTER}$	Cycle to cycle jitter	—	150	ps
V_{MAX}	Absolute Max input voltage	—	+1.15	V
V_{MIN}	Absolute Min input voltage	—	-0.3	V
Duty cycle	Duty cycle	40	60	%
Rise-Fall matching	Rising edge rate (PCIE_CLK_P) to falling edge rate (PCIE_CLK_N) matching	—	20	%
Z_{C-DC}	Clock source DC impedance	40	60	Ω

2.5 Recommended Clock Solution

Customers can choose any appropriate clock solution (HCSL or LP-HCSL type). Renesas provides an industry-leading PCI Express® clock solution.

Renesas' complete portfolio of PCI Express® clock products can be found at the static URL below:

https://www.renesas.com/en/products/clocks-timing/application-specific-clocks/pci-express-clocks

Renesas' portfolio also includes programmable crystal oscillators to use as part of a PCI Express® clock solution. Details can be found at the static URL below:

https://www.renesas.com/en/products/clocks-timing/crystal-oscillators

Refer to **section 2.6** for example clocking solutions.

2.6 Example of Implementation

The section below demonstrates two implementation examples used on Renesas design for the RZ/G3S.

2.6.1 HCSL Clock Buffer Common Clock Architecture Implementation

The schematic below is an implementation example using a Renesas 4-output PCIe Gen1/2/3 synthesizer IC (part number: 5V41236) and a Renesas XL family 1000fs quartz-based PLL oscillator (part number: XLH536025.000000I) to create a common clock architecture clocking solution.

The CLKD clock output is connected to the SoC PCIE_CLK pin, and the CLKA clock output is connected to the end-point device (in this case, PCIe slot connector).

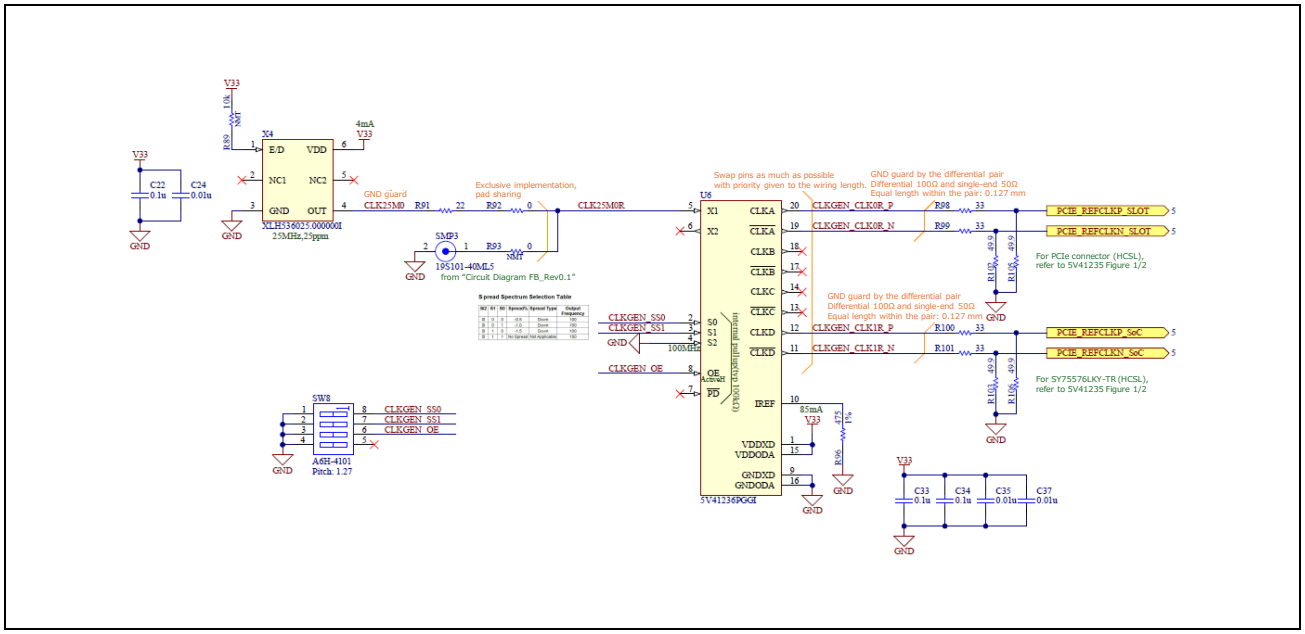

Figure 2.7 Example Common Clock Architecture Using HCSL Input Format

Below are links to the product pages for the devices mentioned above:

Part Number: 5V41236

Description: 4-output PCIe Gen1/2/3 (HCSL clock buffer)

Product page:

https://www.renesas.com/en/products/clocks-timing/application-specific-clocks/pci-express-clocks/5v41236-4-output-pcie-gen123-synthesizer

Part Number: XLH536025.000000I

Description: XL Family 1000fs Quartz-based PLL Oscillator

Product page:

https://www.renesas.com/en/products/clocks-timing/crystal-oscillators/xl-1000fs-quartz-based-pll-oscillator

2.6.2 LP-HCSL Clock Buffer Common Clock Architecture Implementation

The schematic below is an implementation example using a Renesas VersaClock 3S programmable clock generator (part number: 5L35023) to create a common clock architecture clocking solution.

The 5L35023 can store the configuration in an internal OTP memory, and the 5L35023B-615NLGI is used for the RZ/G3S-EVKIT. The DIFF2 clock output is connected to the SoC PCIE_CLK pin, and the DIFF1 clock output is connected to the end-point device (in this case, PCIe slot connector).

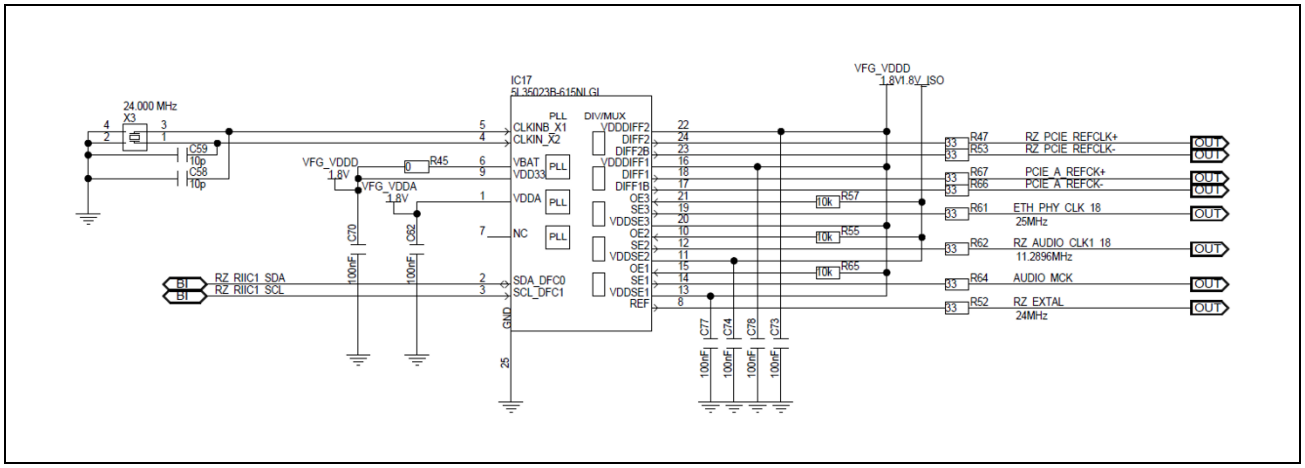

Figure 2.8 Example Common Clock Architecture Using LP-HCSL Input Format

Below is a link to the product page for the device mentioned above:

Part Number: 5L35023

Description: VersaClock 3S Programmable Clock Generator (LP-HCSL clock buffer)

Product page: https://www.renesas.com/en/products/5l35023

2.7 PCB Layout

This section describes layout considerations when designing for the PCIe interface.

2.7.1 Transmission Line

The PCIe interface employs full-duplex differential signaling, comprising transmit (TX) and receive (RX) pairs, to exchange data with other devices. Accurate wiring of these signal pairs and reference clocks is essential for maintaining the integrity of the PCIe link.

Critical PCB design considerations are outlined below.

Signal Routing

- TX, RX, and clock signals must be routed as matched differential pairs to minimize crosstalk and maintain signal integrity.
- To minimize EMI and maintain signal integrity, high-speed transmission lines should avoid sharp bends (90° and 45°). Arced traces reduce impedance discontinuities caused by etching variations, improving signal quality.

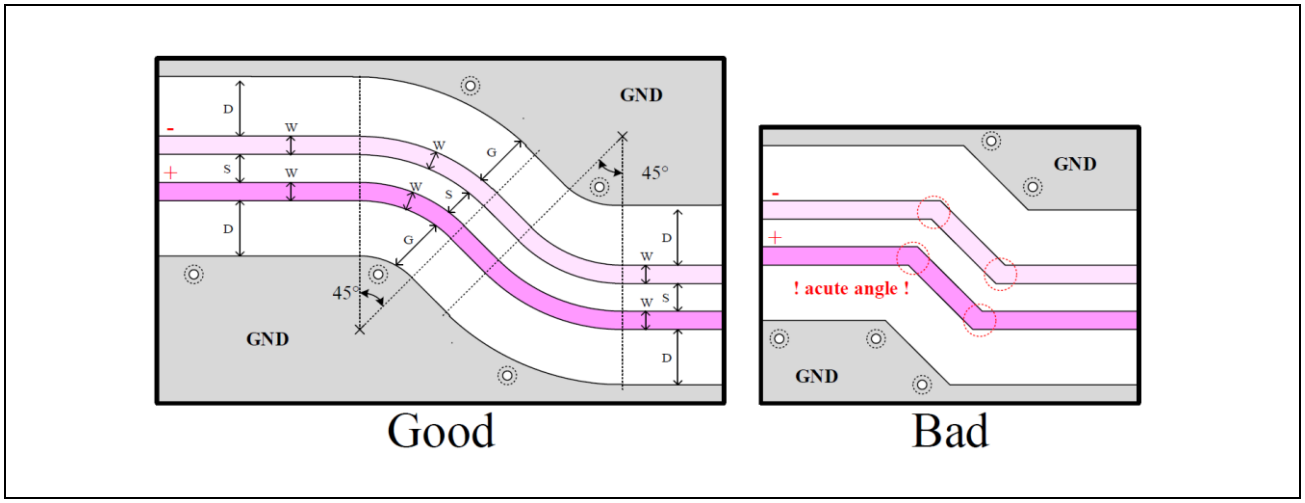

Figure 2.9 Example of Differential Pair Routing Using Arc Traces

- Refer to **Table 2.6** for specific routing impedance recommendation to ensure optimal signal integrity.

Table 2.6 Routing Impedance Recommendation for PCIe Interface

Signal Type	Min	Typ	Max
PCIE_CLK	90Ω	100Ω	110Ω
PCIE_RX	80.75Ω	85Ω	89.25Ω
PCIE_TX	80.75Ω	85Ω	89.25Ω

- Length matching: Signals should be intra-pair and inter-pair length matched and also phase matched.
- Intra-pair skew: Differential pairs (P and N) must be length-matched to within 0.125 mm to maintain signal integrity and reduce crosstalk. Length mismatches can lead to phase differences between P and N signals, which can degrade signal quality. To mitigate this effect, length mismatches should be corrected as close to their source as possible.
- Inter-pair skew: Since PCIe employs full-duplex differential signaling, independent timing clocks for TX and RX pairs mitigate the need for strict length-matching between them.

- To ensure optimal signal integrity, physical separation of high-speed signals from other signals is crucial. Routing crossing signals on distant layers and avoiding direct crossings beneath reference layers can significantly reduce crosstalk. In cases where crossings are necessary, consider the use of core dielectric to provide additional isolation.
- To ensure optimal signal integrity, route high-speed differential signals on solid ground planes. Avoid routing over different digital ground or analog ground planes to minimize crosstalk and maintain impedance. If ground plane splits are unavoidable, employ stitching capacitors technique to establish a low-impedance return path for high-frequency across the split.
- To preserve signal integrity, place symmetrical ground vias when transitioning high-speed differential signals between layers. This technique helps to minimize reflections and maintain impedance continuity.

Signal Shielding

- To mitigate crosstalk between differential pairs, it is recommended to shield them with ground planes. This helps to confine electromagnetic interference and improve signal integrity.
- To mitigate insertion loss of differential transmission lines (especially for longer channel), via stitching techniques are recommended. This technique helps to maintain signal integrity and ensure compliance with end-to-end insertion loss standards.

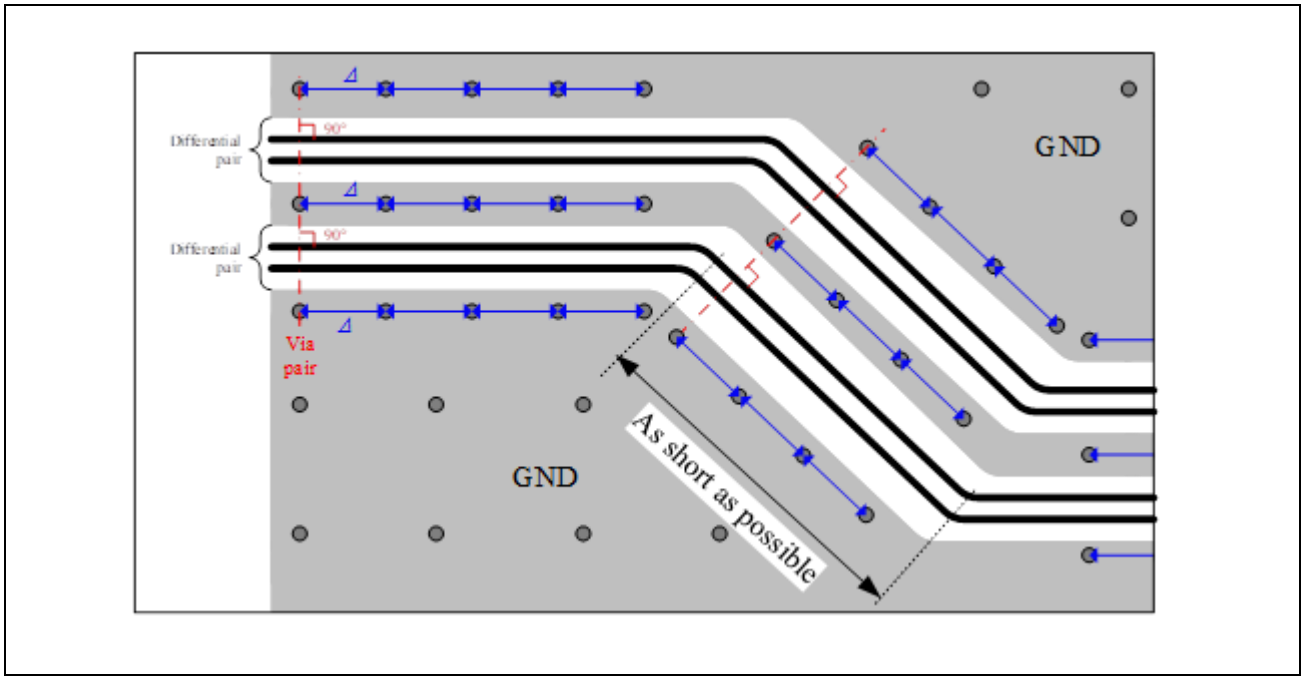

Figure 2.10 Example of Differential Pair Shielding Techniques

2.7.2 AC Coupling Capacitors

- To optimize the integrity of high-speed signals, place AC capacitors as close as possible to the root complex and end-point transmitter to reduce impedance and minimize signal degradation.
- To minimize impedance discontinuities and ensure optimal signal integrity, use a symmetrical layout for the connections to each polarity of the coupling capacitor. This helps to balance the impedance on both sides of the capacitor and reduce signal reflections.
- Reduce the length of stubs associated with AC coupling capacitors to minimize impedance discontinuities and signal reflections.
- If signal integrity simulations indicate signal slew rate issues, consider removing the ground plane under AC coupling capacitor pads. This can reduce parasitic capacitance and improve the signal rise/fall time.

Figure 2.11 shows a differential connection with 85-Ω impedance to an AC coupling capacitor, spaced 0.5 mm apart.

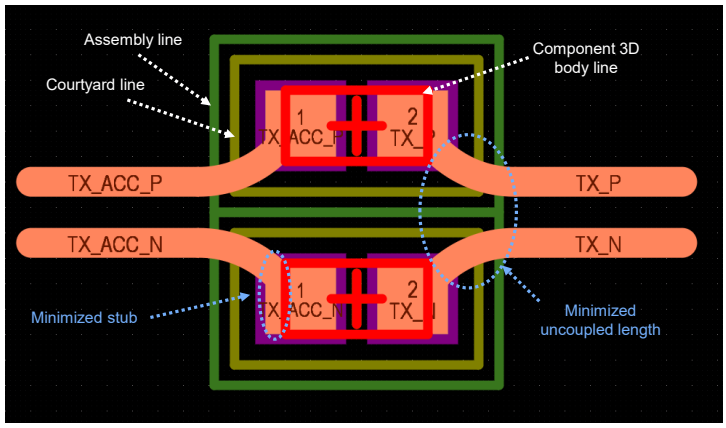

Figure 2.11 Differential Pair Routing to AC Coupling Capacitor Layout

2.7.3 Power Delivery Network (PDN)

Below are the layout recommendations to achieve optimal decoupling efficacy.

Decoupling Capacitor Placement

It is recommended to place 0201 (0603m) capacitors under the BGA power ball and 0402 (1005m) capacitors close to the MPU.

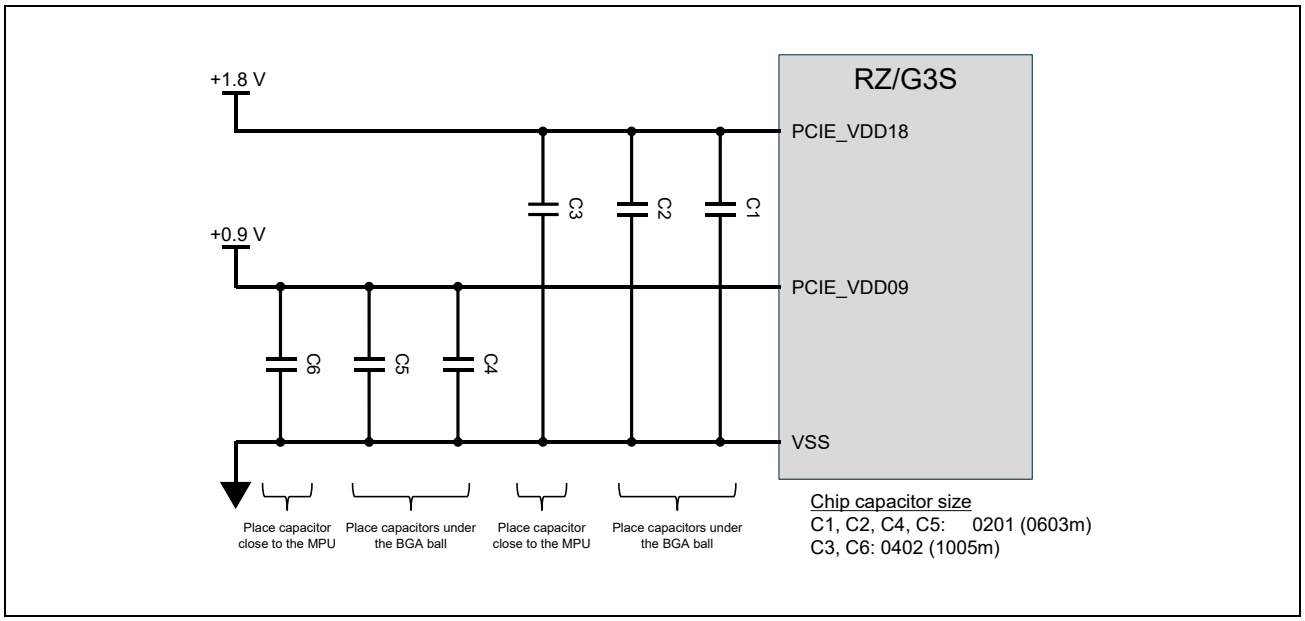

Figure 2.12 Decoupling Capacitors Placement for PCIe

Decoupling Capacitor Ground Return Path

It is recommended to use the ground balls listed in the table below as ground return path for decoupling capacitors.

Table 2.7 Decoupling Capacitors Ground Return Balls

Power Net	Return Ball (14x14mm package)	Return Ball (13x13mm package)
PCIE_VDD09	V12, AD16	Not applicable (No PCIe feature)
PCIE_VDD18	V12, AD16	Not applicable (No PCIe feature)

2.8 PCB Verification

This section describes Signal Integrity (SI) and Power Integrity (PI) verification items when designing for the PCIe interface.

2.8.1 Signal Integrity

This section focuses on the Signal Integrity (SI) side of design verification.

There are three type of verification items:

Normative: refer to verification items that the PCI Express® Base Specification standard specifies to achieve compliance.

Informative: refer to verification items that are useful to create the best layout possible to achieve compliance.

Recommended: refer to verification items that Renesas recommends doing a check to achieve compliance.

2.8.1.1 Insertion Loss

This verification is informative.

The differential insertion loss of the transmission line should be less than -2 dB up to 1.25 GHz (PCIe Gen1 Nyquist frequency) or up to 2.5 GHz (PCIe Gen2 Nyquist frequency). **Figure 2.13** illustrates the TX and RX differential insertion loss mask for PCIe Gen 2 (5-Gb/s bit rate).

The transmission line referred to above is the end to end (die to die) connection between the root-complex and the end-point. If a MUX or other device exists in between, the end-point becomes this device.

RZG3S PKG + PCB + (end-point device PKG) or (MUX or other device)

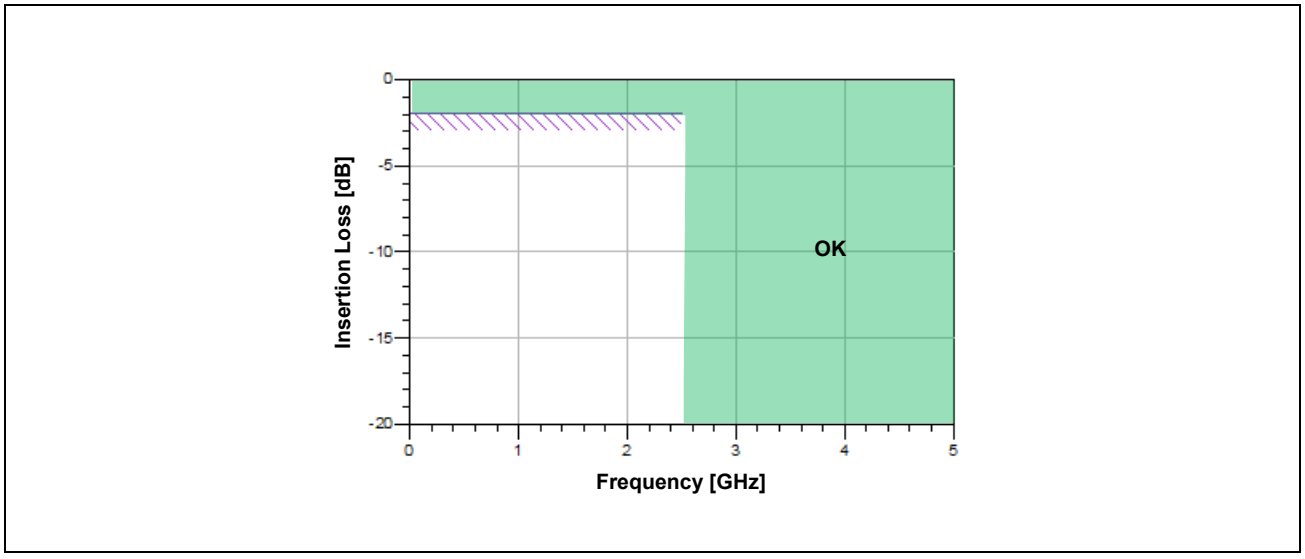

Figure 2.13 Tx & Rx Differential Insertion Loss Mask

Renesas recommends doing this verification to understand the end to end loss of the PCIe system.

2.8.1.2 Return Loss

This verification is normative.

The differential return loss of the transmission line should be more than -10 dB up to 1.25 GHz (PCIe Gen1 Nyquist frequency) and more than -8 dB up to 2.5 GHz (PCIe Gen2 Nyquist frequency). **Figure 2.14** illustrates the TX and RX differential return loss mask for PCIe Gen 2.

The common mode return loss of the transmission line should be more than -6 dB up to 1.25 GHz (PCIe Gen1 Nyquist frequency) and 2.5 GHz (PCIe Gen2 Nyquist frequency). **Figure 2.15** illustrates the TX and RX common mode return loss mask PCIe Gen 2.

The transmission line referred to above is the end to end (die to die) connection between the root-complex and the end-point. If a MUX or other device exists in between, the end-point becomes this device.

RZ/G3S PKG + PCB + (end-point device PKG) or (MUX or other device)

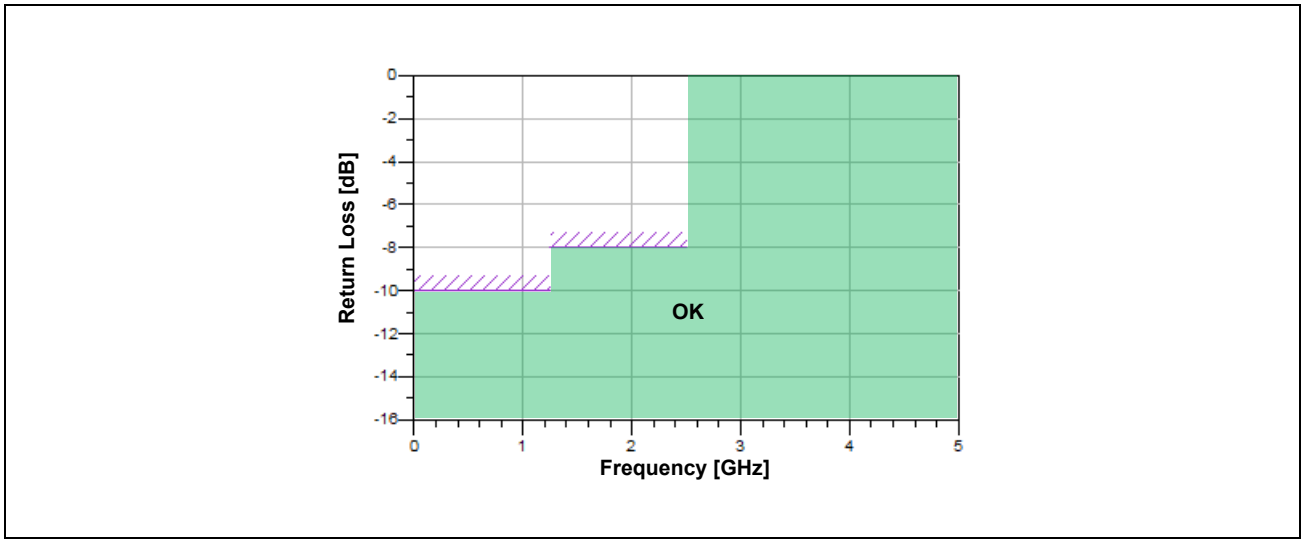

Figure 2.14 Tx & Rx Differential Return Loss Mask

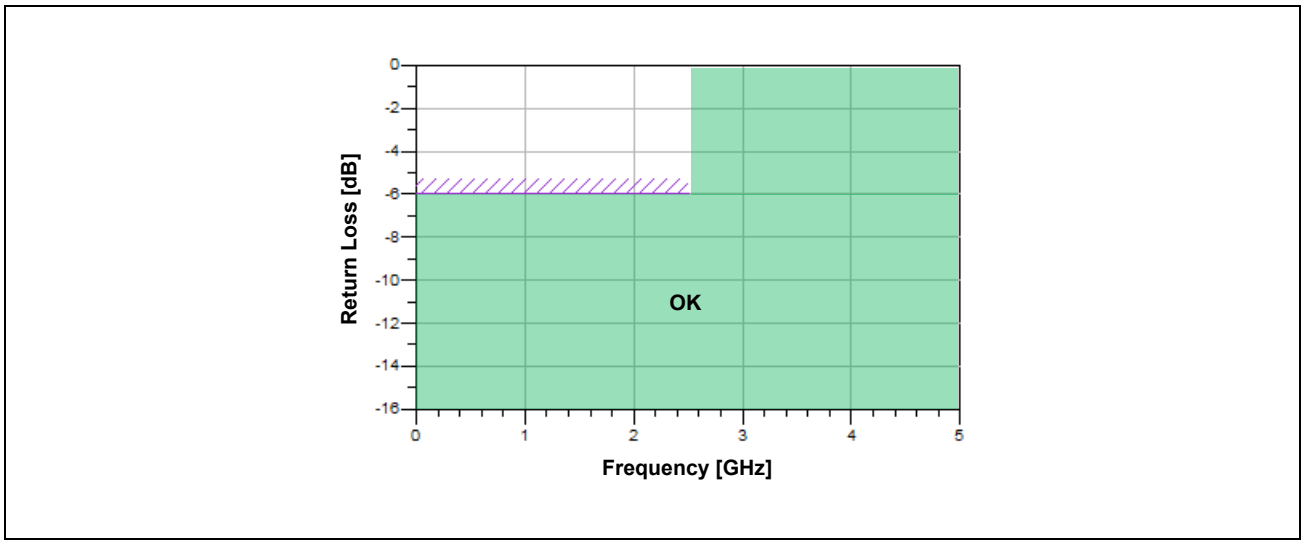

Figure 2.15 Tx & Rx Common Mode Return Loss Mask

Renesas recommends doing this verification to verify if the designed transmission line complies with the PCI Express® Base Specification.

2.8.1.3 Differential Transmission Line Impedance

Renesas recommends doing a Time Domain Reflectometry (TDR) analysis to verify the differential impedance of the transmission line and optimize the design to reduce the impedance discontinuities. The transmission line referred to above is the end to end (die to die) connection between the root-complex and the end-point. If a MUX or other device exists in between, the end-point becomes this device.

Figure 2.16 and **Figure 2.17** illustrate simulator circuits for single ended and differential TDR analysis.

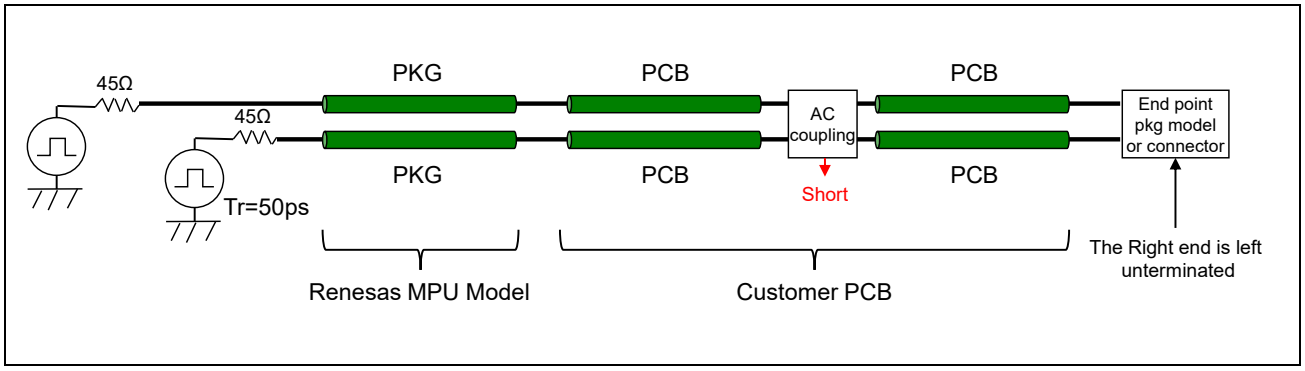

Figure 2.16 Simulator Circuit for Single Ended TDR Analysis

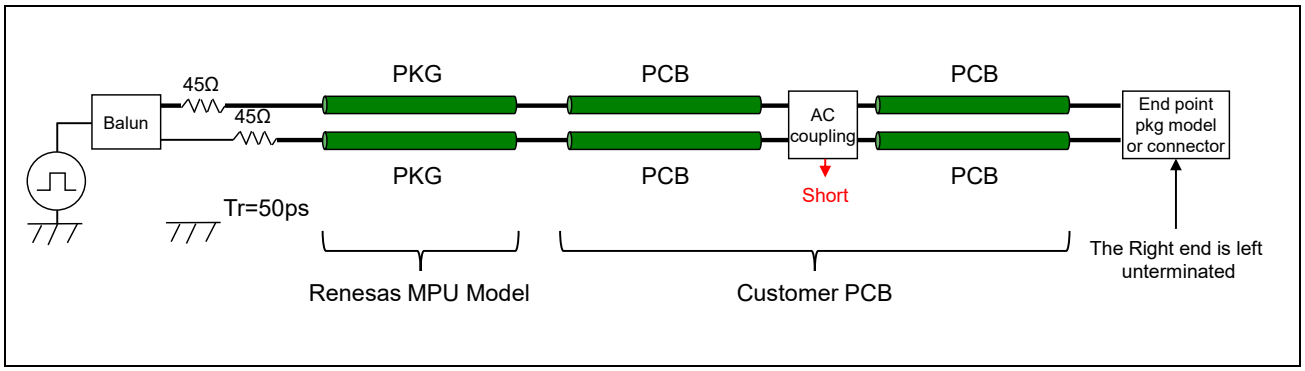

Figure 2.17 Simulator Circuit for Differential TDR Analysis

2.8.2 Power Integrity

This section focuses on the power integrity (PI) side of design verification. The simulations described here are recommendations.

2.8.2.1 Loop Inductance Requirements

Renesas strongly recommends performing loop inductance calculations to guarantee proper operation of the PCIe interface.

The loop inductance to the nearest decoupling capacitor on the PCB should be less than the value shown below:

PCIE_VDD09: **2.00 nH @100 MHz**.

PCIE_VDD18: **1.90 nH @100 MHz**.

The loop inductance can be calculated using the following formula:

$L_{loop} = L_{pwr} + L_{gnd}$

Figure 2.18 illustrates the loop formed by the PCB trace and the closest decoupling capacitor.

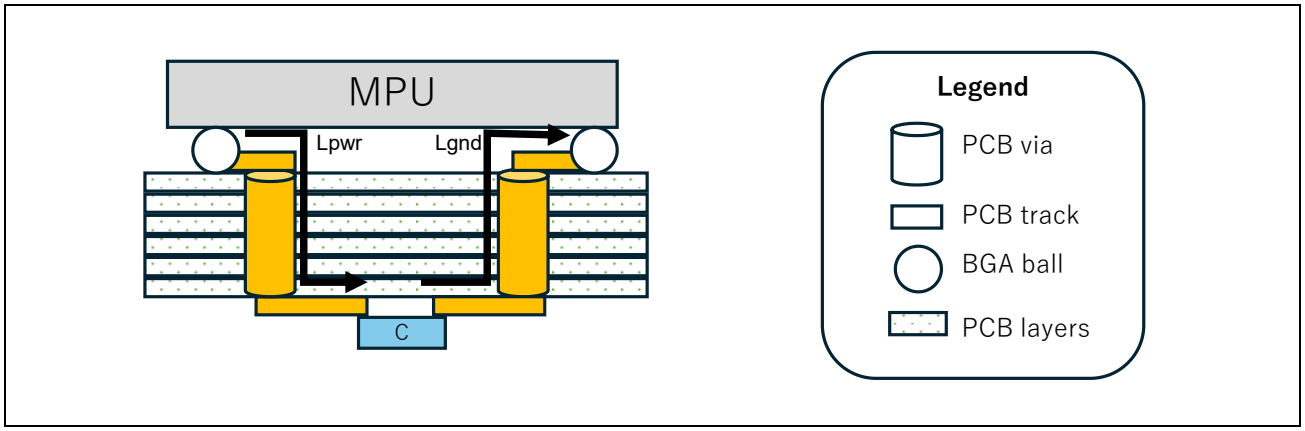

Figure 2.18 Concept for Loop Inductance

2.8.2.2 Loop Inductance Extraction Methodology

The inductance of the loop formed by the PCB traces to the closest decoupling capacitor can be modeled directly or indirectly. Refer to each section for details.

Direct Modeling

Direct modeling can be done with a parasitic extractor (e.g., Ansys Q3D).

Figure 2.19 illustrates direct modeling.

Designate the BGA ball as the source and the decoupling capacitor pad as the sink.

If there are multiple BGA balls for a specific power or ground net, merge them together in parallel to calculate a single equivalent source-to-sink inductance value.

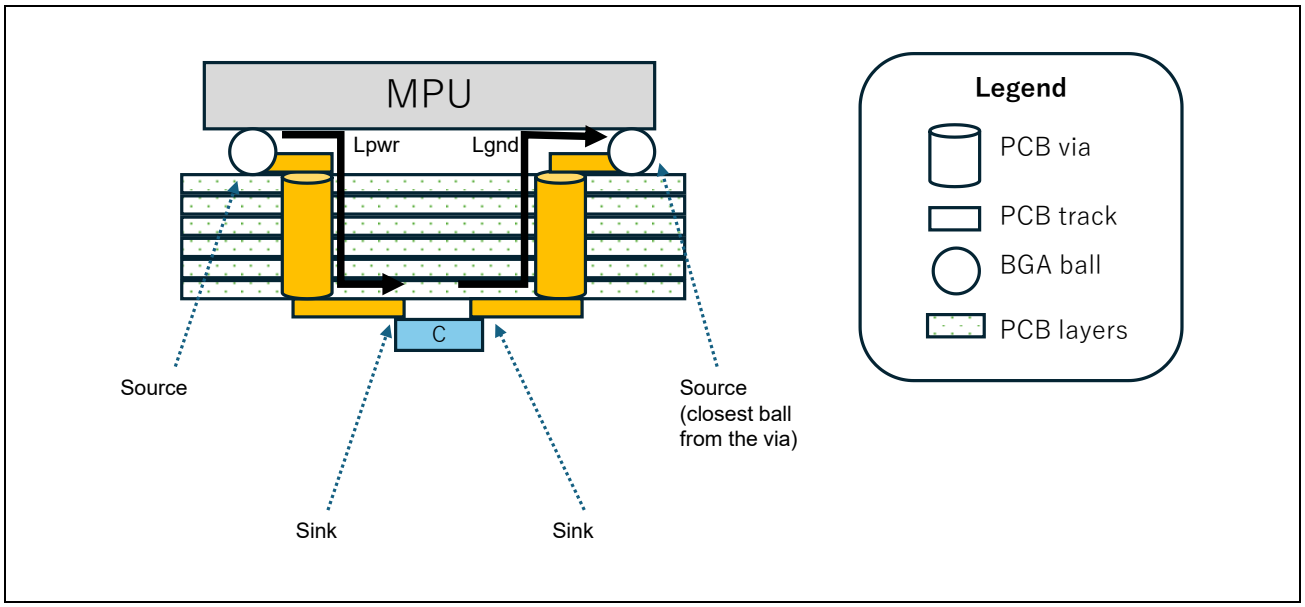

Figure 2.19 Concept for Direct Modeling

Indirect Modeling

Indirect modeling can be performed using 2.5D (e.g., Ansys SIwave) or 3D (e.g., Ansys HFSS) tools.

To achieve greater accuracy in modeling, it is recommended to use 3D simulation, as 2.5D simulation only considers the vertical dimension of vias, neglecting other 3D effects.

Figure 2.20 illustrates indirect modeling.

Create a 2-port S-parameter model representing the power and ground net.

Also, create an RL lumped model to approximate the net's impedance.

Excite both models with a current source and perform AC simulations and compare responses magnitudes.

Run AC simulation and probe the magnitude of the net connected to the current source.

Adjust the inductance and resistance values of the lumped model to align its frequency response with that of the S-parameter model.

Figure 2.21 shows the fitted lumped model response compared to the S-parameter model response.

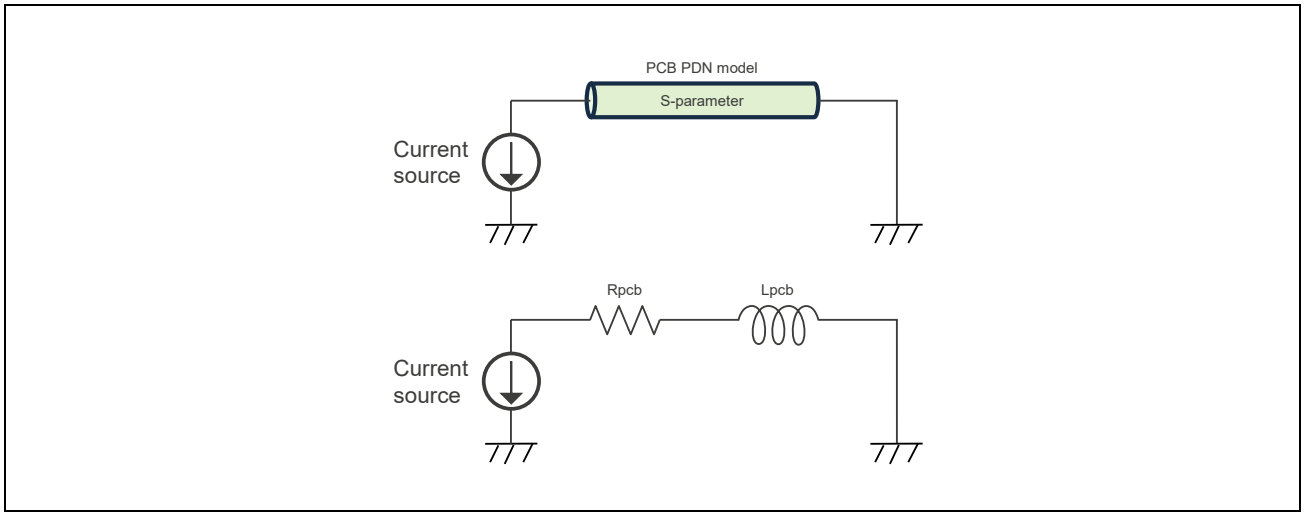

Figure 2.20 Simulator Circuit for Indirect Modeling

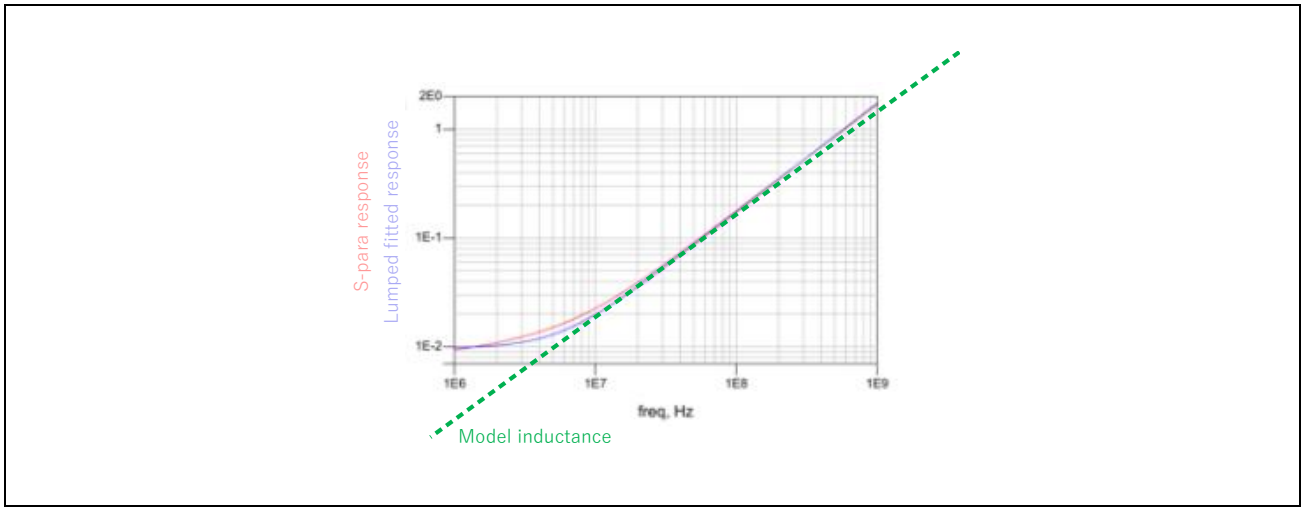

Figure 2.21 Fitted Lumped vs S-Parameter Model Response

REVISION HISTORY	RZ/G3S PCB Design Guidelines for High Speed Signal Interfaces

Rev.	Date	Description	
		Page	Summary
1.10	Nov. 10, 2023	—	First edition issued as R01AN5871EJ
2.00	Apr. 14, 2026	All	Restructured the sections of the document and reorganized some sentences, figures, and tables to make them easier to read. Basically, the content of the document remains unchanged.

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PCB Design Guidelines for High Speed Signal Interfaces

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RZ/G3S
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