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M16C/64 Group

Oscillation Stop/Reoscillation Detect Function Application Example

1. Abstract

This document describes an application example for the oscillation stop/reoscillation detect function of the microcomputer.

The oscillation stop/reoscillation detect function provides a means of detecting that the main clock oscillator circuit has stopped operating and that it restarted oscillating. When stoppage or restart of oscillation is detected, a reset or an oscillation stop/reoscillation detected interrupt is generated. Which of these is to be generated can be selected by the CM27 bit of the CM2 register. In the sample program, this register is chosen to generate only an oscillation stop/reoscillation detected interrupt.

Table 1 shows specifications of the oscillation stop/reoscillation detect function.

Table 1. Specifications of the Oscillation Stop/Reoscillation Detect Function

Item	Specification
Oscillation stoppage detectable clock and frequency range	Main clock frequency (fXIN) ≥ 2 MHz Note 1
Oscillation stop/reoscillation detect function enable condition	Set the CM20 bit to 1 (oscillation stop/reoscillation detect function enabled). Note 2
Operation when oscillation stop/reoscillation is detected	• When CM27 bit = 0: a reset is generated. • When CM27 bit = 1: an oscillation stop/reoscillation detected interrupt is generated.

Note 1: If the main clock frequency is 2 MHz or less, the oscillation stop/reoscillation detect function cannot be used.

Note 2: If the main clock frequency is 2 MHz or less, set the CM20 bit to 0 (oscillation stop/reoscillation detect function disabled).

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

- Microcomputers: M16C/64 group
- Main clock: 2 MHz or more

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Description of the Application Example

3.1 System Configuration

- Main clock: 6 MHz
- CPU clock source during normal oscillation: PLL clock (XIN multiplied by 4 [24 MHz])
- CPU clock source when oscillation stoppage is detected: 125 kHz on-chip oscillator clock
- Oscillation stop/reoscillation detected interrupt function: Enabled (CM20 bit = 1 (enabled))
- Operation when oscillation stop/reoscillation is detected: Oscillation stop/reoscillation detected interrupt is generated. (CM27 bit = 1)
  However, once an interrupt is generated, the oscillation stop/reoscillation detected interrupt is disabled. (CM22 bit not cleared to 0)
- Port P0: Output counter during normal oscillation (count-up cycle: 1 sec)
- Port P1_0: Oscillation stoppage detection output when oscillation has stopped (output cycle: 2 Hz)
- Timer A0 timer mode: 50-ms cycle timer produced
  The 50-ms timer is used for different purposes depending on the main clock oscillation state.
  - During normal oscillation
    - Purpose of use: Port P0 count-up 1-sec timer
    - Count source: f32TIMAB (PLL clock (24 MHz) divided by 32)
    - Timer A0 set value: 37,499 (50 ms × 24 MHz/f32TIMAB – 1)
  - When oscillation has stopped
    - Purpose of use: Port P1_0 output 2-Hz timer
    - Count source: f32TIMAB (125 kHz on-chip oscillator divided by 32)
    - Timer A0 set value: 194 (50 ms × 125 kHz/f32TIMAB – 1)

3.2 Description of Software Operation

1) When the main clock (6 MHz) is oscillating normally (during normal oscillation)
   1-1) Count down the 1-sec timer each time a timer A0 interrupt is generated (at 50-ms intervals).
   1-2) Count up port P0 each time the 1-sec timer underflows. When a count of 256 is reached, the count recycles to 0.
2) When the main clock (6 MHz) is detected to have stopped oscillating (when oscillation stoppage is detected)
   2-1) When oscillation stoppage is detected, the CM22 bit is set to 1 at the same time an oscillation stop/reoscillation detected interrupt is generated. [Note 1]
   2-2) When oscillation stoppage state is confirmed, switch the CPU clock source from the PLL clock to the 125 kHz on-chip oscillator. [Note 2]
   2-3) In an oscillation stop/reoscillation detected interrupt handler, check the CM23 bit (XIN monitor flag) to determine whether the oscillation remains stopped or not.
3) When the main clock (6 MHz) remains stopped oscillating (oscillation stopped)
   3-1) If the timer A0 interrupt request flag = 1 (when 50 ms underflowed), count down the 250-ms timer for port P1_0 output.
   3-2) Invert the port P1_0 output each time the 250-ms timer underflows.

Note 1: In the sample program, the CM22 bit remains set to 1. Therefore, once oscillation stoppage is detected, no more oscillation stop/reoscillation detected interrupts are generated.

Note 2: While the CPU clock source is the PLL clock, even if the main clock has stopped oscillating, the CM21 bit does not change state to 1 (125 kHz on-chip oscillator clock) and the PLL frequency synthesizer alone provides a clock. The oscillation stop/reoscillation detected interrupt handler is executed by this clock.

3.3 Description of the Oscillation Stop/Reoscillation Detected Interrupt Handling

(1) Since in the sample program the PLL clock is selected for the CPU clock source, the CM21 bit does not change state even when the main clock has stopped. Therefore, the CM21 bit is set to 1 (125 kHz on-chip oscillator) at the beginning of the interrupt handler to switch the CPU clock source to the 125 kHz on-chip oscillator.

(2) The main clock state is determined by reading the CM23 bit (XIN monitor flag) several times within the interrupt handler. In the sample program, the main clock is determined to have stopped oscillating when the CM23 bit is sampled as 1 in 8 consecutive reads. The method for checking the CM23 bit is described in Section 3.3.1, "CM23 Bit (XIN Monitor Flag) Check Example."

Figure 2 shows an oscillation stop/reoscillation detected interrupt handling flowchart.

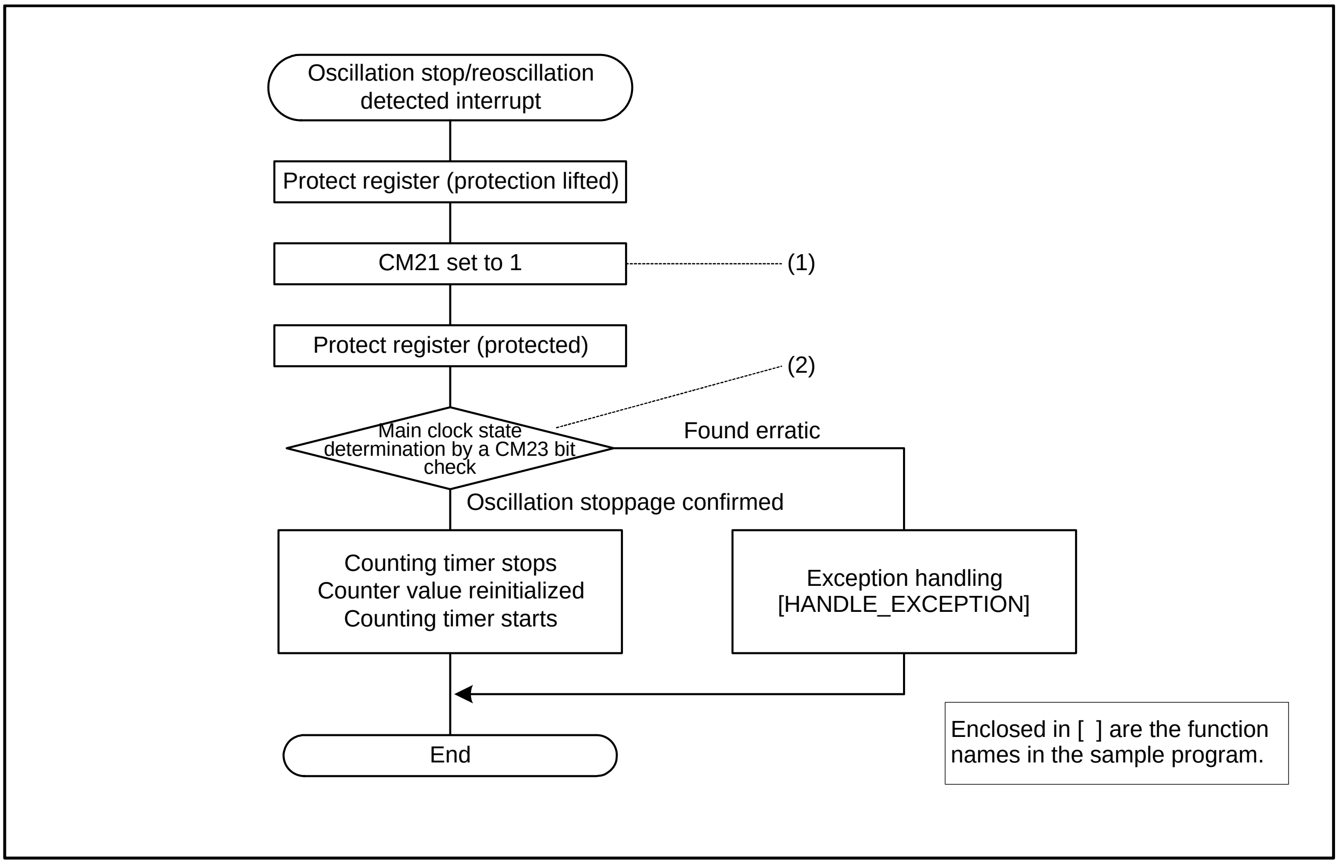

Figure 2. Oscillation Stop/Reoscillation Detected Interrupt Handling Flowchart

3.3.1 CM23 Bit (XIN Monitor Flag) Check Example

(1) The CM23 bit (XIN monitor flag) is checked at given intervals.
(This interval time is generated by a loop process.)

(2) The main clock is determined to have stopped oscillating when the CM23 bit is sampled as 1 in 8 consecutive reads.

(3) Occurrence of an exception is assumed if the number of times the CM23 bit is checked exceeds 16.

Figure 3 shows a CM23 bit (XIN monitor flag) check flowchart.

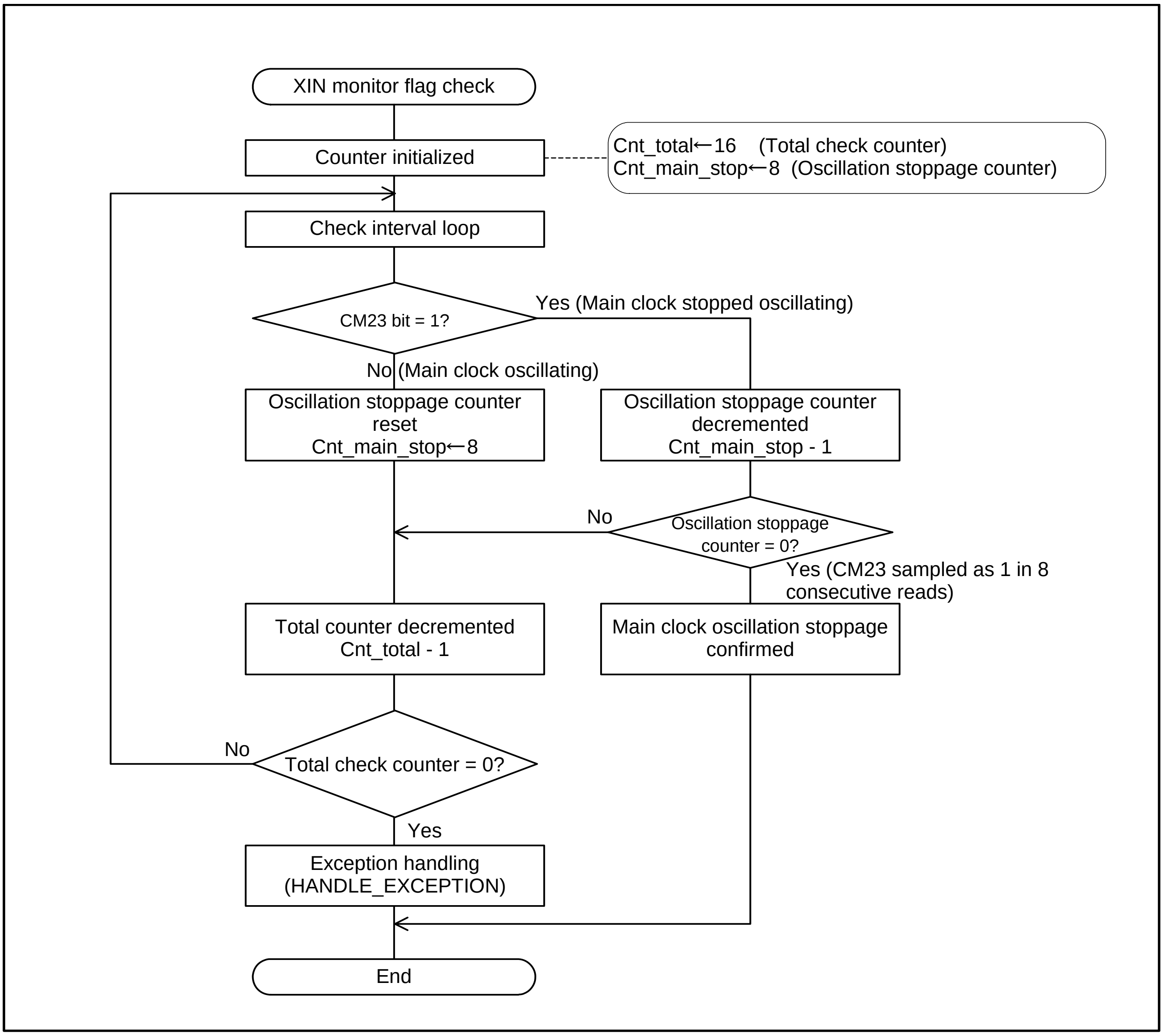

Figure 3. CM23 Bit (XIN Monitor Flag) Check Flowchart

3.3.2 Exception Handling (HANDLE_EXCEPTION)

In the sample program, unless the CM23 bit (XIN monitor flag) is sampled as 1 (main clock stopped oscillating) 8 times consecutively within a total check count of 16, an exception condition is assumed.

4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in Section 3.2, “Description of Software Operation.” For details about each register, see the hardware manual of the M16C/64 group.

(1) Set up the oscillation stop detection register (CM2), system clock control register 1 (CM1), and system clock control register 0 (CM0).

b7							b0
0		0	0			1	1

Protect register (PRCR)

- PRC0 CM0, CM1, CM2, PLC0, PCLKR register write enable
  1: Enables write
- PRC1 PM0, PM1, PM2, TB2SC, INVC0, INVC1 register write enable
  1: Enables write
- Reserved bits
  Set these bits to 0.

b7							b0
1	X	0	0			0	1

Oscillation stop detection register (CM2)

- CM20 Oscillation stop/reoscillation detection enable bit
  1: Enables oscillation stop/reoscillation detect function
- CM21 System clock select bit 2
  0: Main clock or PLL clock
- CM22 Oscillation stop/reoscillation detection flag
  0: Main clock stop/reoscillation not detected
  1: Main clock stop/reoscillation detected
- CM23 XIN monitor flag (read-only)
  0: Main clock oscillating
  1: Main clock stopped
- Reserved bits
  Set these bits to 0.
- CM27 Operation select bit when oscillation stop/reoscillation detected
  1: Oscillation stop/reoscillation detected interrupt

> When the CM20 bit = 1 and CM23 bit = 1 (main clock stopped), do not set the CM21 bit to 0.

> The CM22 bit is cleared to 0 by writing 0 in a program. Writing 1 to this bit has no effect. Nor is it cleared to 0 by acceptance of an oscillation stop/reoscillation detected interrupt.
> No oscillation stop/reoscillation detected interrupts are generated even if oscillation stoppage or reoscillation is detected when the CM22 bit = 1.

b7							b0
				0	0	0	

System clock control register 1 (CM1)

- CM11 System clock select bit 1
  0: Main clock
- Reserved bits
  Set these bits to 0.
- CM15 XIN-XOUT drive capability select bit
  0: Low
  1: High
- CM17, CM16 System clock divide ratio select bits 1
  00: Not divide mode
  01: Divide-by-2 mode
  10: Divide-by-4 mode
  11: Divide-by-16 mode

> The CM11 bit is usable when the CM07 bit = 0 and CM21 bit = 0.

b7							b0
0	0	0					

System clock control register 0 (CM0)

- CM05 Main clock stop bit
  0: Oscillating
- CM06 System clock divide ratio select bit 0
  0: CM16, CM17 bits enabled
- CM07 System clock select bit
  0: Main clock, PLL clock, or 125 kHz on-chip oscillator

(2) Set up the processor mode register 2 (PM2)

b7							b0
X	X	X		0	X		1

Processor mode register 2 (PM2)

- PM20 SFR access wait specification when PLL operating
  1: Specifies 1 wait cycle
- Reserved bit
  Set this bit to 0.

Figure 4. Procedure for Setting Up the Registers to Use the Oscillation Stop/Reoscillation Detect Function (1)

(3) Set PLC04 and PLC03 (reference frequency counter setting bits) and PLC02, PLC01 and PLC00 (PLL multiplication factor select bits).

b7 b0
0 X

PLL control register 0 (PLC0)

To set up the PLL control register (PLC0), write to it when the PLC07 bit = 0 (PLL turned off).

PLC02, PLC01, PLC00 PLL multiplication factor select bits
- 000: Setting prohibited
- 001: Multiply by 2
- 010: Multiply by 4
- 011: Multiply by 6
- 100: Multiply by 8
- 101:, 110:, 111: Setting prohibited

Reserved bit
When read, its value is indeterminate.

PLC04, PLC03 Reference frequency counter setting bits
- 00: Not divide
- 01: Divide by 2
- 10: Divide by 4
- 11: Setting prohibited

PLC07 Operation enable bit
0: Turns PLL off

(4) Set up PLL operation (PLC07 bit).

b7 b0
1 X

PLL control register 0 (PLC0)

PLC07 Operation enable bit
1: Runs PLL

Before setting the PLC07 bit to 1 (PLL operating), set the CM05 bit to 0 (main clock oscillating) first.

(5) Wait a while (t_{su}(PLL)) until the PLL oscillation stabilizes.

(6) Switch the system clock from the main clock to the PLL clock.

b7 b0
0 0 1

System clock control register 1 (CM1)

CM11 System clock select bit 1
1: PLL clock

(7) Set up the protect register (PRCR).

b7 b0
0 0 0 0 0

Protect register (PRCR)

PRC0 CM0, CM1, CM2, PLC0, PCLKR register write enable
0: Disables write

PRC1 PM0, PM1, PM2, TB2SC, INVC0, INVC1 register write enable
0: Disables write

Reserved bits
Set these bits to 0.

Figure 5. Procedure for Setting Up the Registers to Use the Oscillation Stop/Reoscillation Detect Function (2)

5. Sample Programs

Download a sample program from the Renesas Technology website. Click the screen menu "Application Note" on the left side of the M16C family's top web page.

6. Reference Documents

Hardware manual

M16C/64 Group Hardware Manual
(Get the latest version from the Renesas Technology website.)

Technical updates and technical news

(Get the latest information from the Renesas Technology website.)

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Inquiries

http://www.renesas.com/inquiry
mailto:csc@renesas.com

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